



PSMN1R5-25YL

N-channel TrenchMOS logic level FET

Rev. 01 — 16 June 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in industrial and communications applications.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- Class-D amplifiers
- Motor control
- DC-to-DC converters
- Server power supplies

1.4 Quick reference data

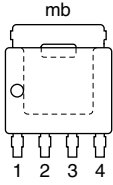
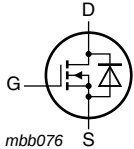
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	25	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ;	[1]	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	109	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 10\text{ A}$; $V_{DS} = 12\text{ V}$; see Figure 14 ; see Figure 15	-	9.2	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 10\text{ A}$; $V_{DS} = 12\text{ V}$; see Figure 14 ; see Figure 15	-	36	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$	-	1.13	1.5	mΩ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 SOT669 (LPAK)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN1R5-25YL	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	25	V	
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 150 °C; R _{GS} = 20 kΩ	-	25	V	
V _{GS}	gate-source voltage		-20	20	V	
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	[1]	-	100	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	[1]	-	100	A
I _{DM}	peak drain current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C; see Figure 3	-	815	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	109	W	
T _{stg}	storage temperature		-55	150	°C	
T _j	junction temperature		-55	150	°C	
Source-drain diode						
I _S	source current	T _{mb} = 25 °C;	[1]	-	100	A
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	815	A	
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 25 V; R _{GS} = 50 Ω; unclamped	-	290	mJ	

[1] Continuous current is limited by package.

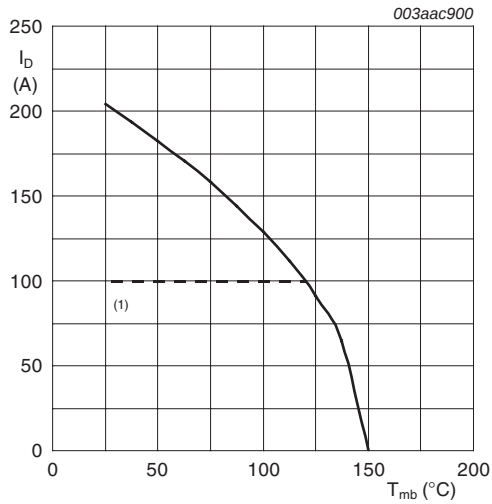


Fig 1. Continuous drain current as a function of mounting base temperature

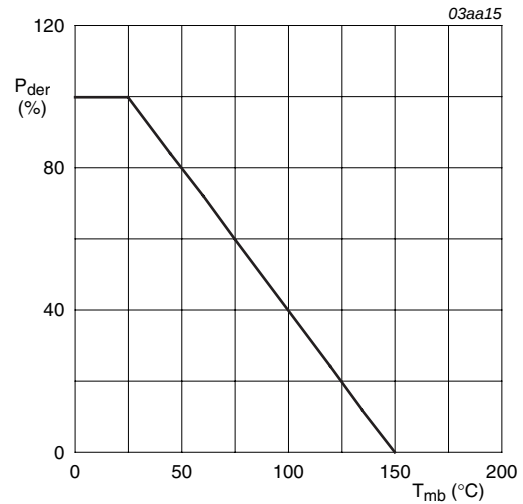
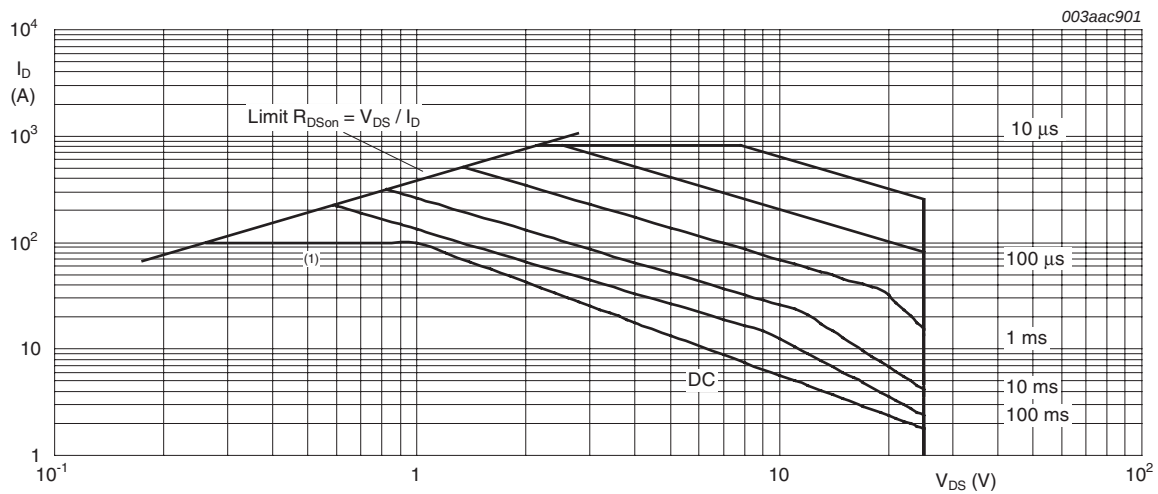


Fig 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$


$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse
(1) Capped at 100 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.5	1.1	K/W

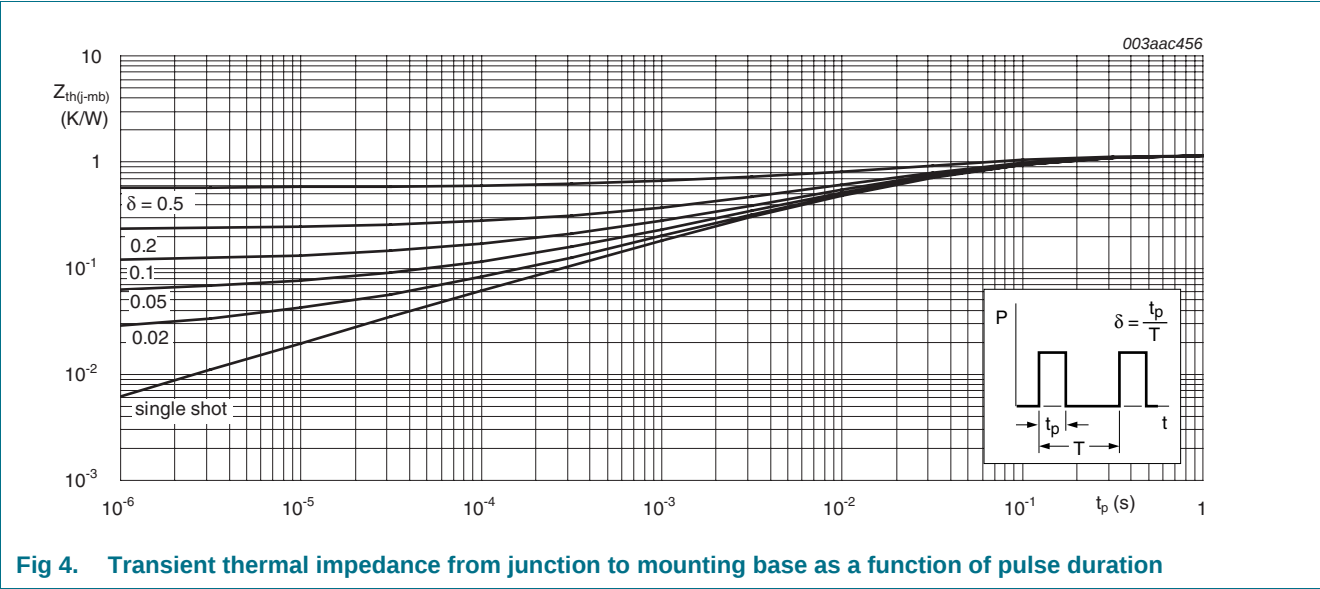


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

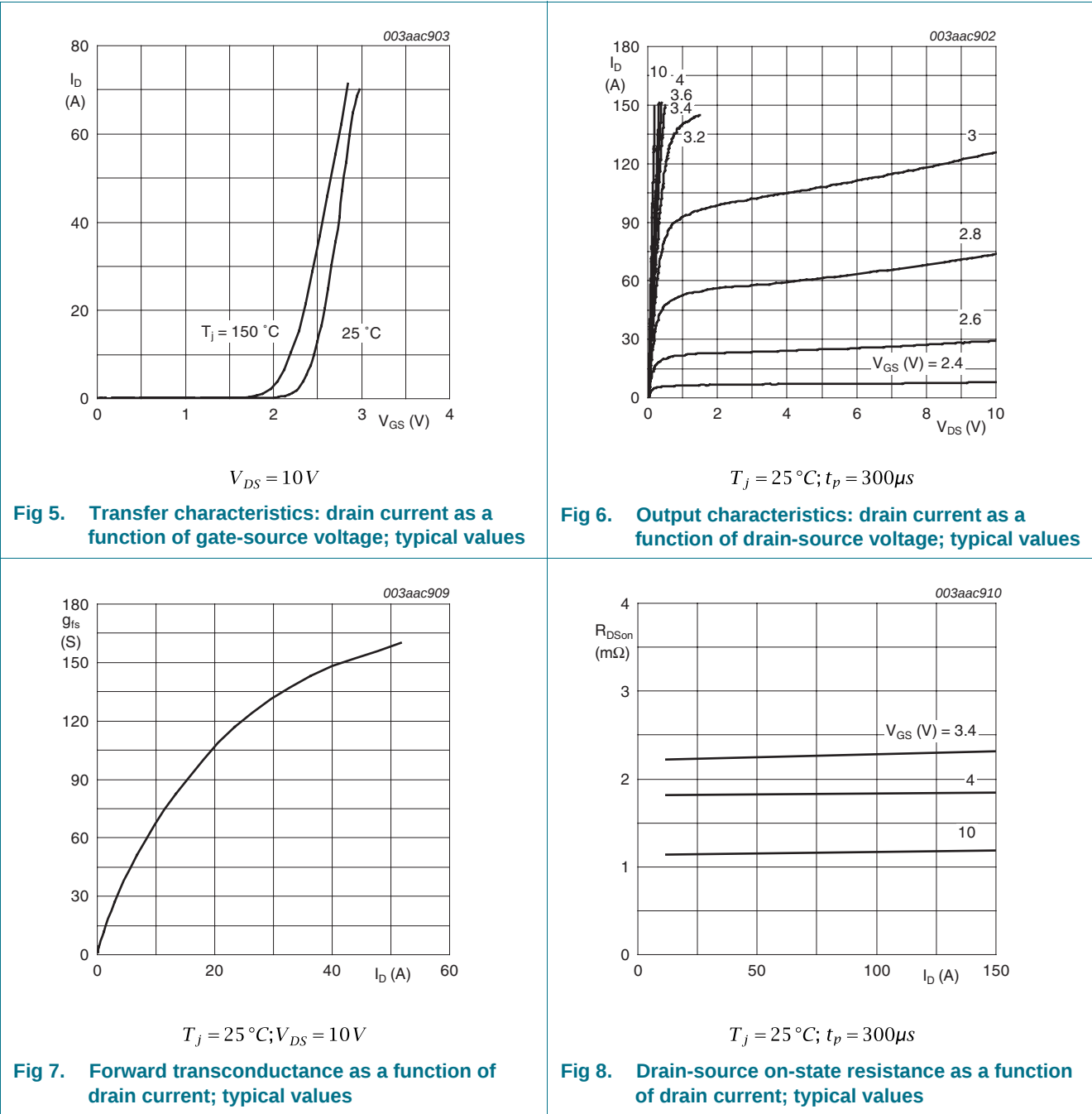
Table 6. Characteristics

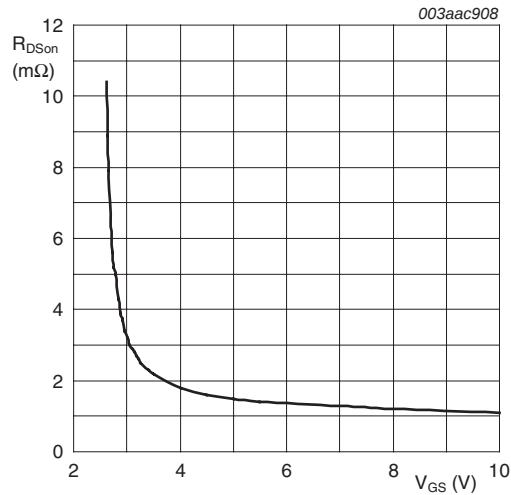
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	25	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$; see Figure 11 ; see Figure 12	1.3	1.7	2.15	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 150 ^\circ C$; see Figure 12	0.65	-	-	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = -55 ^\circ C$; see Figure 12	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 25 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	-	1	μA
		$V_{DS} = 25 V$; $V_{GS} = 0 V$; $T_j = 150 ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = -16 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V$; $I_D = 15 A$; $T_j = 25 ^\circ C$	-	1.61	2.2	m Ω
		$V_{GS} = 10 V$; $I_D = 15 A$; $T_j = 150 ^\circ C$; see Figure 13	-	-	2.6	m Ω
		$V_{GS} = 10 V$; $I_D = 15 A$; $T_j = 25 ^\circ C$	-	1.13	1.5	m Ω
R_G	gate resistance	$f = 1 MHz$	-	0.77	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10 A$; $V_{DS} = 12 V$; $V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	76	-	nC
		$I_D = 0 A$; $V_{DS} = 0 V$; $V_{GS} = 10 V$	-	71	-	nC
		$I_D = 10 A$; $V_{DS} = 12 V$; $V_{GS} = 4.5 V$; see Figure 14 ; see Figure 15	-	36	-	nC
Q_{GS}	gate-source charge	$I_D = 10 A$; $V_{DS} = 12 V$; $V_{GS} = 4.5 V$; see Figure 14 ; see Figure 15	-	12.3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	7.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.5	-	nC
Q_{GD}	gate-drain charge		-	9.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12 V$; see Figure 14	-	2.4	-	V
C_{iss}	input capacitance	$V_{DS} = 12 V$; $V_{GS} = 0 V$; $f = 1 MHz$;	-	4830	-	pF
C_{oss}	output capacitance	$T_j = 25 ^\circ C$; see Figure 16	-	1280	-	pF
C_{rss}	reverse transfer capacitance		-	465	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 V$; $R_L = 0.5 \Omega$; $V_{GS} = 4.5 V$;	-	50	-	ns
t_r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	97	-	ns
$t_{d(off)}$	turn-off delay time		-	72	-	ns
t_f	fall time		-	36	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 17	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	43	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	-	50	-	nC

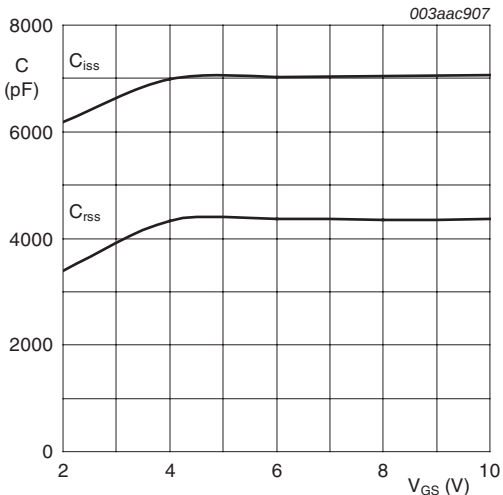
[1] Tested to JEDEC standards where applicable.





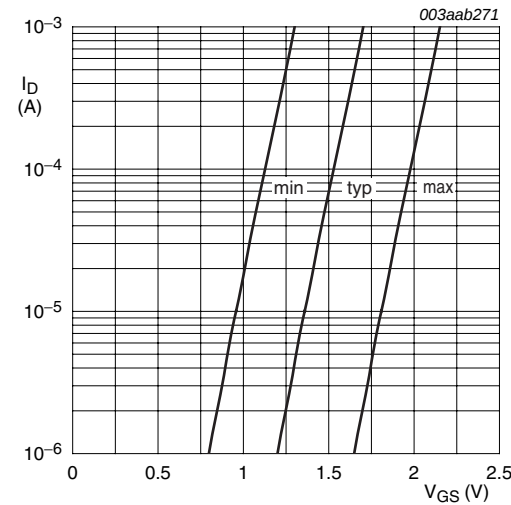
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 15\text{ A}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



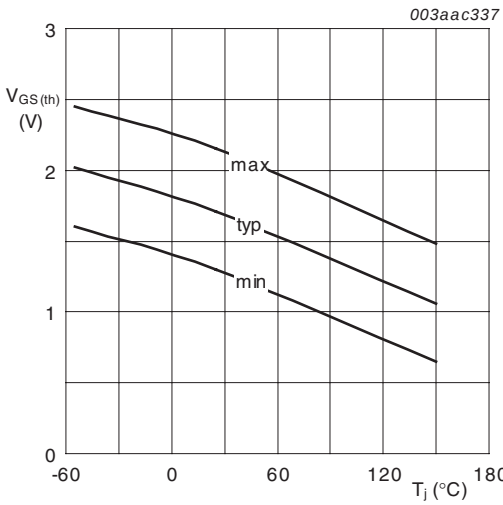
$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 10. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



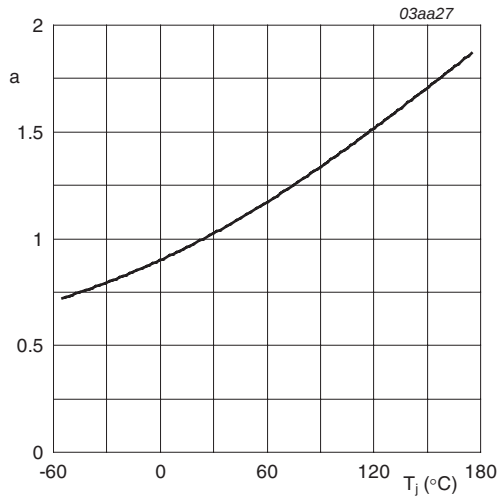
$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

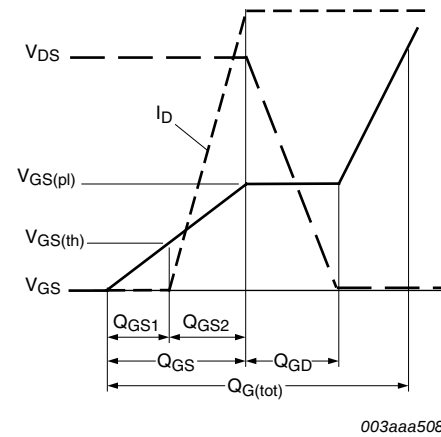
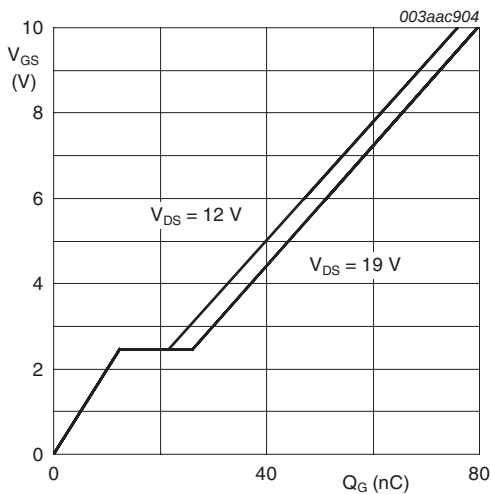
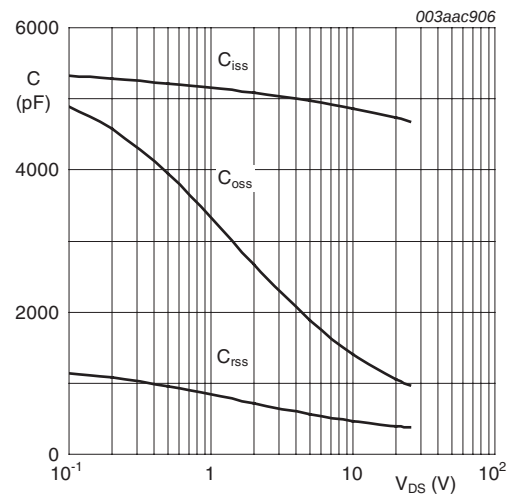


Fig 14. Gate charge waveform definitions



$$T_j = 25^{\circ}\text{C}; I_D = 15\text{ A}$$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

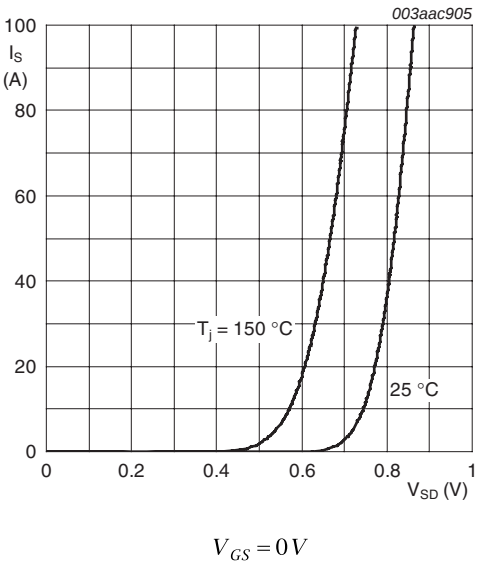


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

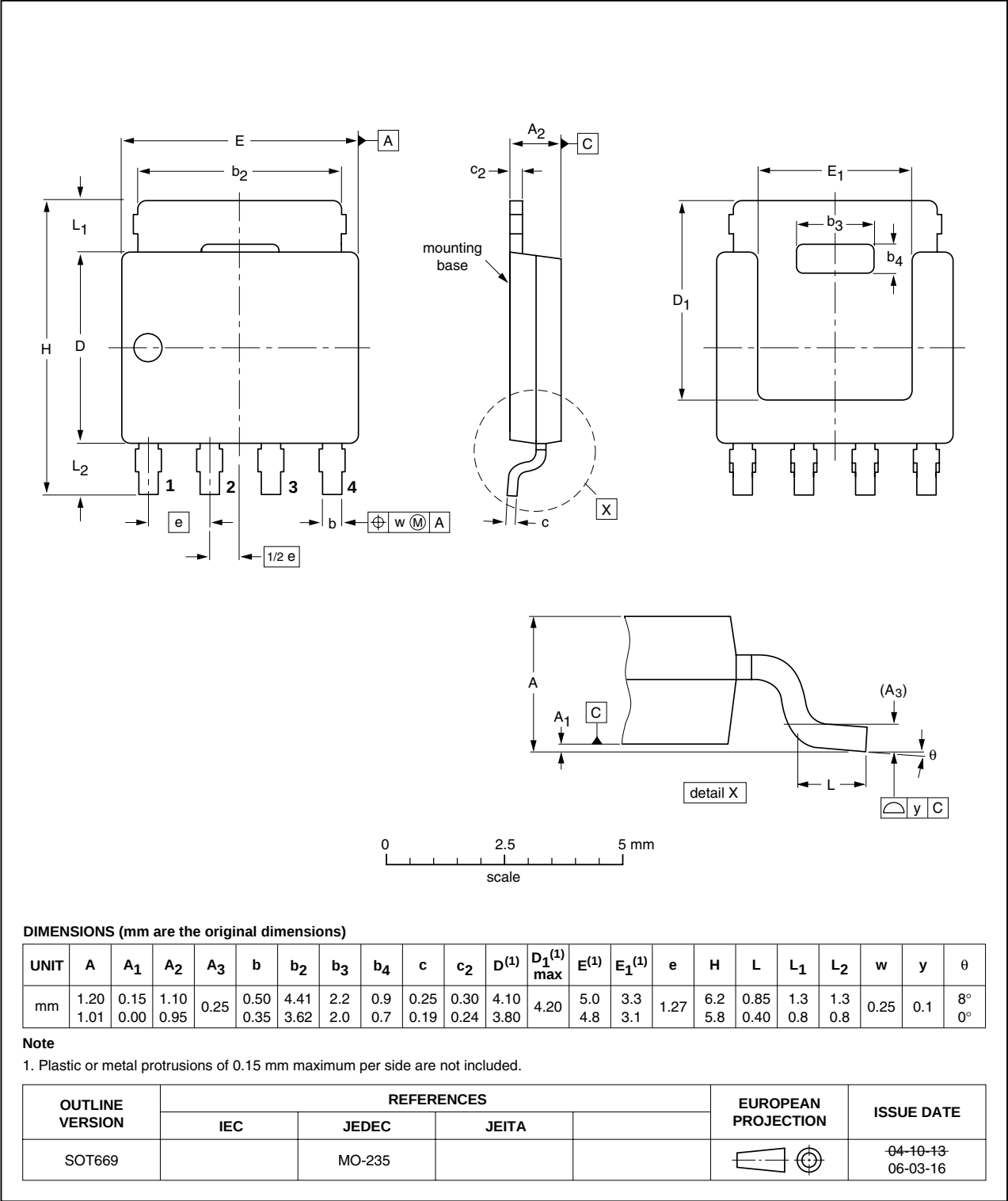


Fig 18. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R5-25YL_1	20090616	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

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