

NPIC6C596

Power logic 8-bit shift register; open-drain outputs

Rev. 2 — 4 July 2013

Product data sheet

1. General description

The NPIC6C596 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and open-drain outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset \overline{MR} input. A LOW on \overline{MR} resets both the shift register and storage register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register. To provide additional hold time in cascaded applications, the serial output QS7 is clocked out on the falling edge of SHCP. Data in the storage register drives the gate of the output extended-drain NMOS (EDNMOS) transistor whenever the output enable input (\overline{OE}) is LOW. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the registers.

The open-drain outputs are 33 V/100 mA continuous current extended-drain NMOS transistors designed for use in systems that require moderate load power such as LEDs. Integrated voltage clamps in the outputs provide protection against inductive transients making the device suitable for power driver applications such as relays, solenoids and other low-current or medium-voltage loads.

2. Features and benefits

- Specified from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Low R_{DSon}
- Eight Power EDNMOS transistor outputs of 100 mA continuous current
- 250 mA current limit capability
- Output clamping voltage 33 V
- 30 mJ avalanche energy capability
- Enhanced cascading for multiple stages
- All registers cleared with single input
- Low power consumption
- ESD protection:
 - ◆ HBM JDS-001 Class 2 exceeds 2500 V
 - ◆ CDM JESD22-C101E exceeds 1000 V

3. Applications

- LED sign
- Graphic status panel
- Fault status indicator

4. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| NPIC6C596D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| NPIC6C596PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| NPIC6C596BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

5. Functional diagram

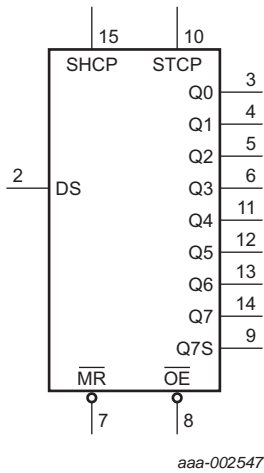


Fig 1. Logic symbol

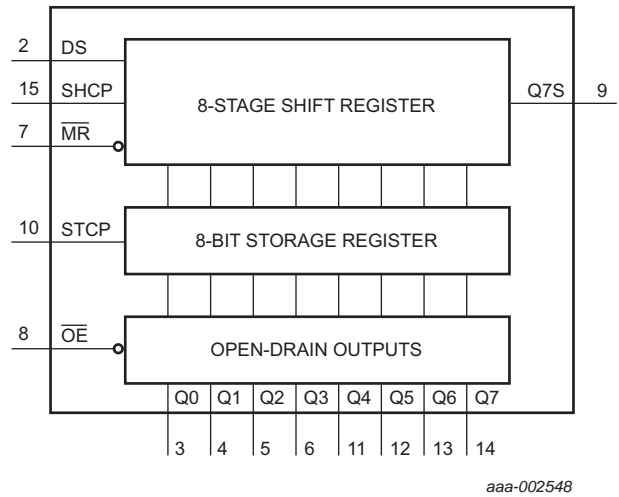


Fig 2. Functional diagram

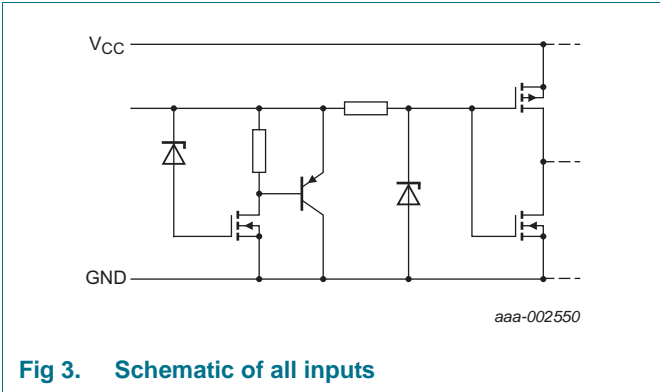


Fig 3. Schematic of all inputs

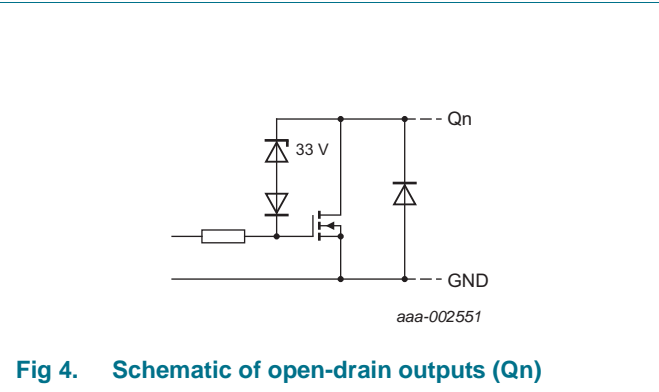


Fig 4. Schematic of open-drain outputs (Qn)

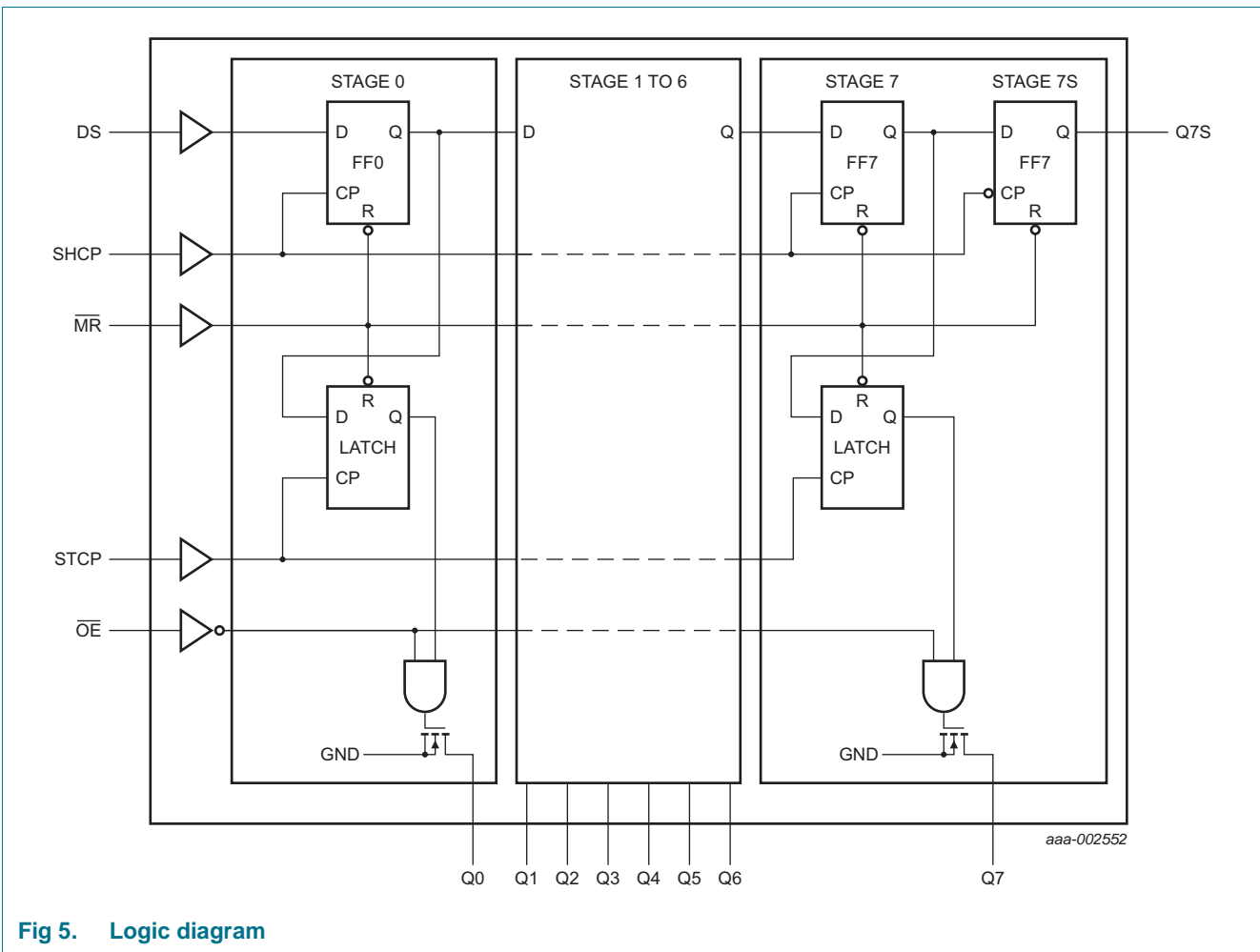


Fig 5. Logic diagram

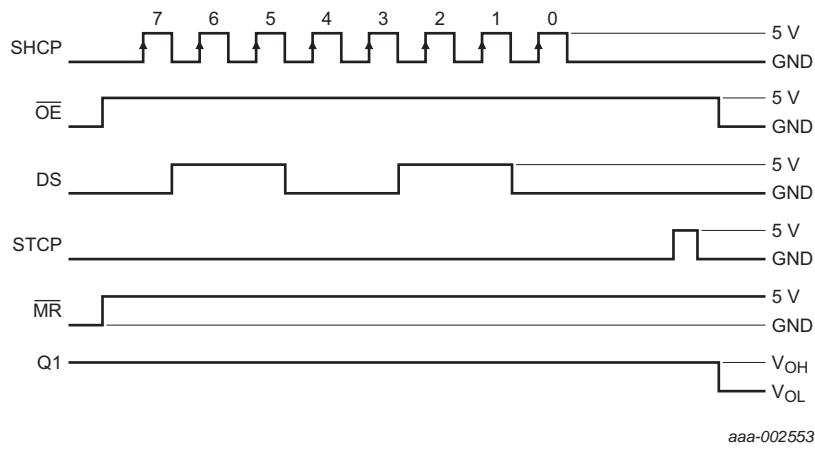


Fig 6. Timing diagram

6. Pinning information

6.1 Pinning

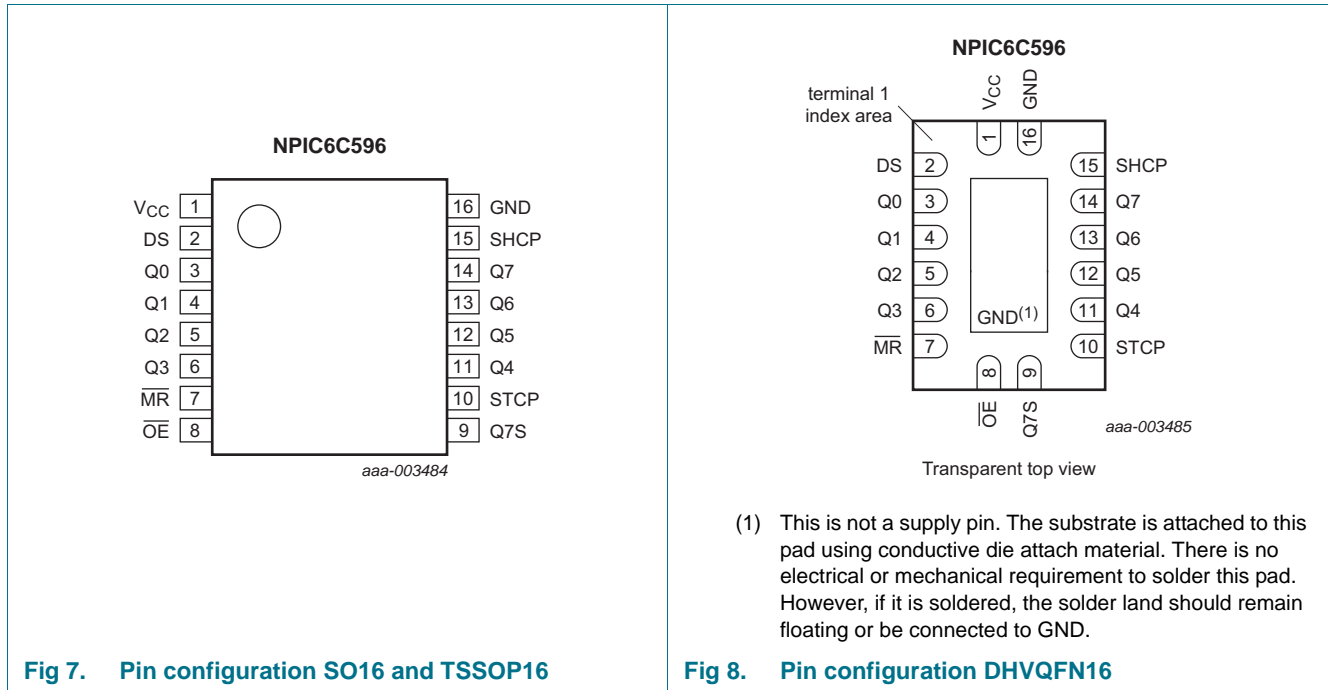


Fig 7. Pin configuration SO16 and TSSOP16

Fig 8. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------------|----------------------------|-----------------------------------|
| V _{CC} | 1 | supply voltage |
| DS | 2 | serial data input |
| Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | 3, 4, 5, 6, 11, 12, 13, 14 | parallel data output (open-drain) |
| $\overline{\text{MR}}$ | 7 | master reset (active LOW) |
| $\overline{\text{OE}}$ | 8 | output enable input (active LOW) |
| Q7S | 9 | serial data output |
| STCP | 10 | storage register clock input |
| SHCP | 15 | shift register clock input |
| GND | 16 | ground (0 V) |

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-------------|----------------------------|--|------|------|------|----|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V | |
| V_I | input voltage | | -0.3 | +7.0 | V | |
| V_{DS} | drain-source voltage | power EDNMOS drain-source voltage | [1] | - | +33 | V |
| $I_{d(SD)}$ | source-drain diode current | continuous | - | 250 | mA | |
| | | pulsed | [2] | - | 500 | mA |
| I_D | drain current | $T_{amb} = 25\text{ °C}$ | | | | |
| | | continuous; each output; all outputs on | - | 100 | mA | |
| | | pulsed; each output; all outputs on | [2] | - | 250 | mA |
| I_{DM} | peak drain current | single output; $T_{amb} = 25\text{ °C}$ | [2] | - | 250 | mA |
| E_{AS} | avalanche energy | single pulse; see Figure 9 | [3] | - | 30 | mJ |
| I_{AL} | avalanche current | see Figure 9 | [3] | - | 200 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C | |
| P_{tot} | total power dissipation | $T_{amb} = 25\text{ °C}$ | [4] | | | |
| | | SO16 | - | 800 | mW | |
| | | TSSOP16 | - | 725 | mW | |
| | | DHVQFN16 | - | 1825 | mW | |
| | | $T_{amb} = 125\text{ °C}$ | [4] | | | |
| | | SO16 | - | 160 | mW | |
| | | TSSOP16 | - | 145 | mW | |
| DHVQFN16 | - | 365 | mW | | | |

[1] Each power EDNMOS source is internally connected to GND.

[2] Pulse duration $\leq 100\ \mu\text{s}$ and duty cycle $\leq 2\%$.

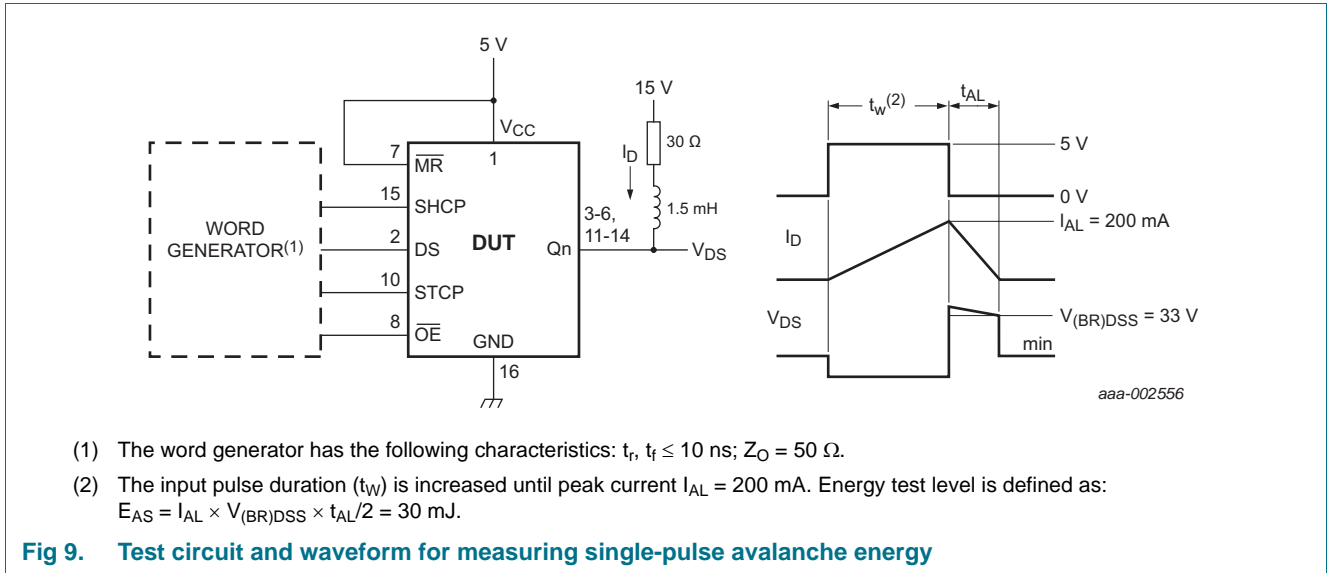
[3] $V_{DS} = 15\text{ V}$; starting junction temperature (T_j) = 25 °C ; $L = 1.5\text{ H}$; avalanche current (I_{AL}) = 200 mA .

[4] For SO16 packages: above 25 °C the value of P_{tot} derates linearly with 6.4 mW/°C .

For TSSOP16 packages: above 25 °C the value of P_{tot} derates linearly with 5.8 mW/°C .

For DHVQFN16 packages: above 25 °C the value of P_{tot} derates linearly with 14.6 mW/°C .

7.1 Test circuit and waveform



8. Recommended operating conditions

Table 4. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------|--|----------|-----|------|------|
| V_{CC} | supply voltage | | 4.5 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| I_D | drain current | pulsed drain output current; $V_{CC} = 5$ V; $T_{amb} = 25$ °C; all outputs on | [1][2] - | - | 250 | mA |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |

[1] Pulse duration $\leq 100 \mu s$ and duty cycle $\leq 2 \%$.

[2] Technique should limit $T_j - T_{amb}$ to 10 °C maximum.

9. Static characteristics

Table 5. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | $V_{CC} = 5.0$ V; $T_{amb} = 25$ °C | | | Unit |
|----------|---------------------------|--|-------------------------------------|------|--------------|------|
| | | | Min | Typ | Max | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 4.5$ V to 5.5 V | $0.85V_{CC}$ | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 4.5$ V to 5.5 V | - | - | $0.15V_{CC}$ | V |
| V_{OH} | HIGH-level output voltage | serial data output Q7S; $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = -20 \mu A$; $V_{CC} = 4.5$ V | 4.4 | 4.49 | - | V |
| | | $I_O = -4$ mA; $V_{CC} = 4.5$ V | 4.0 | 4.2 | - | V |

Table 5. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | V _{CC} = 5.0 V; T _{amb} = 25 °C | | | Unit |
|----------------------|----------------------------------|--|---|-------|-----|------|
| | | | Min | Typ | Max | |
| V _{OL} | LOW-level output voltage | serial data output Q7S; V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0.005 | 0.1 | V |
| | | I _O = 4 mA; V _{CC} = 4.5 V | - | 0.3 | 0.5 | V |
| I _{IH} | HIGH-level input current | V _{CC} = 5.5 V; V _I = V _{CC} | - | - | 1 | μA |
| I _{IL} | LOW-level input current | V _{CC} = 5.5 V; V _I = 0 V | -1 | - | - | μA |
| V _{(BR)DSS} | drain-source breakdown voltage | I _D = 1 mA | 33 | 37 | - | V |
| V _{SD} | source-drain voltage | diode forward voltage; I _F = 100 mA | - | 0.85 | 1.2 | V |
| I _{CC} | supply current | logic supply current; V _{CC} = 5.5 V; V _I = V _{CC} or GND | | | | |
| | | all outputs off | - | 0.004 | 200 | μA |
| | | all outputs on [1] | - | 0.006 | 500 | μA |
| | | all outputs off; SHCP = 5 MHz; C _L = 30 pF; see Figure 14 and Figure 16 | - | 0.75 | 5 | mA |
| I _{O(nom)} | nominal output current | V _{DS} = 0.5 V; T _{amb} = 85 °C; I _{out} = I _D [2][3][4] | - | 140 | - | mA |
| I _{DSX} | drain cut-off current | V _{CC} = 5.5 V; V _{DS} = 30 V | - | 0.002 | 0.2 | μA |
| | | V _{CC} = 5.5 V; V _{DS} = 30 V; T _{amb} = 125 °C | - | 0.15 | 0.3 | μA |
| R _{DSon} | drain-source on-state resistance | see Figure 17 and Figure 18 [2][3] | | | | |
| | | V _{CC} = 4.5 V; I _D = 50 mA | - | 3.0 | 9 | Ω |
| | | V _{CC} = 4.5 V; I _D = 50 mA; T _{amb} = 125 °C | | 5.4 | 12 | Ω |
| | | V _{CC} = 4.5 V; I _D = 100 mA | - | 3.1 | 10 | Ω |

[1] Output currents below 250 mA current limit.

[2] Technique should limit T_j - T_{amb} to 10 °C maximum.

[3] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

[4] Nominal output current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_{amb} = 85 °C.

10. Dynamic characteristics

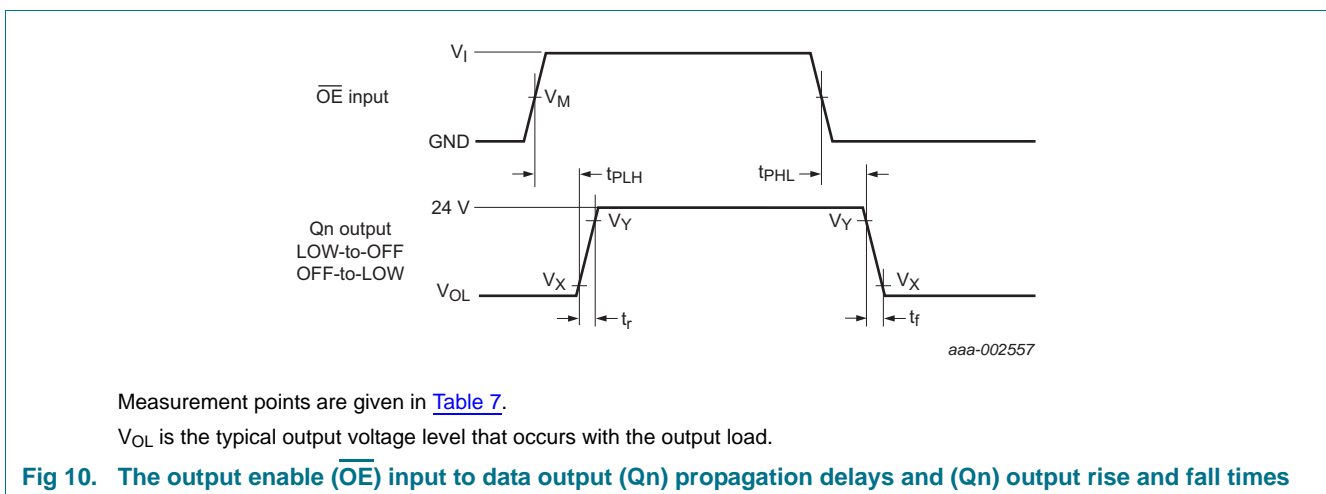
Table 6. Dynamic characteristics

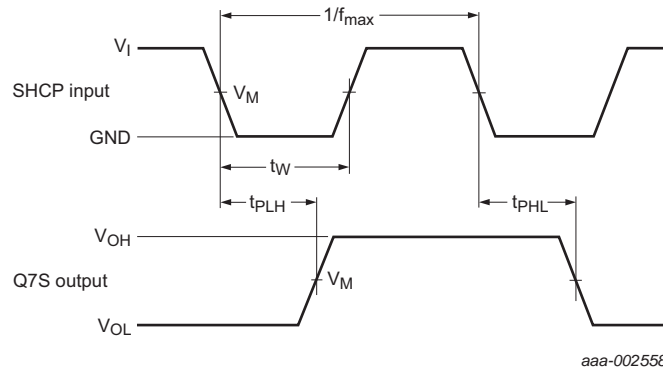
Voltages are referenced to GND (ground = 0 V); For test circuit see [Figure 14](#).

| Symbol | Parameter | Conditions | V _{CC} = 5.0 V; T _{amb} = 25 °C | | | Unit |
|------------------|------------------------------------|--|---|-----|-----|------|
| | | | Min | Typ | Max | |
| t _{PLH} | LOW to HIGH propagation delay | \overline{OE} to Qn; I _D = 75 mA; see Figure 10 and Figure 19 | - | 97 | - | ns |
| t _{PHL} | HIGH to LOW propagation delay | \overline{OE} to Qn; I _D = 75 mA; see Figure 10 and Figure 19 | - | 9 | - | ns |
| t _r | rise time | \overline{OE} to Qn; I _D = 75 mA; see Figure 10 and Figure 19 | - | 60 | - | ns |
| t _f | fall time | \overline{OE} to Qn; I _D = 75 mA; see Figure 10 and Figure 19 | - | 18 | - | ns |
| t _{pd} | propagation delay | SHCP to Q7S; I _D = 75 mA; see Figure 11 [1] | - | 5 | - | ns |
| f _{max} | maximum frequency | SHCP; I _D = 75 mA; see Figure 11 [2] | - | - | 10 | MHz |
| t _{rr} | reverse recovery time | I _F = 100 mA; dI/dt = 10 A/μs; see Figure 13 [3][4] | - | 120 | - | ns |
| t _a | reverse recovery current rise time | I _F = 100 mA; dI/dt = 10 A/μs; see Figure 13 [3][4] | - | 100 | - | ns |
| t _{su} | set-up time | DS to SHCP; see Figure 12 | 15 | - | - | ns |
| t _h | hold time | DS to SHCP; see Figure 12 | 15 | - | - | ns |
| t _W | pulse width | | 40 | - | - | ns |

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SHCP → Q7S propagation delay and setup time plus some timing margin.
- [3] Technique should limit T_j - T_{amb} to 10 °C maximum.
- [4] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

10.1 Test circuits and waveforms





aaa-002558

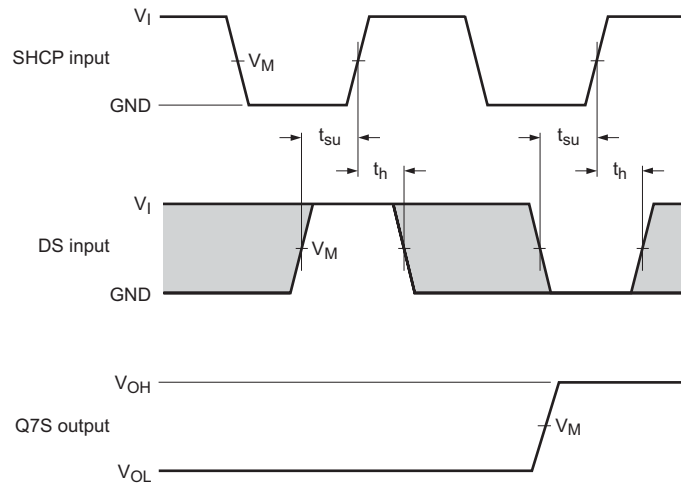
Measurement points are given in [Table 7](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 11. The shift clock (SHCP) to serial data output (Q7S) propagation delays with the minimum shift clock pulse width and maximum shift clock frequency

Table 7. Measurement points

| Supply voltage | Input | Output | | |
|----------------|-------------|-------------|-------------|-------------|
| V_{CC} | V_M | V_M | V_X | V_Y |
| 5 V | $0.5V_{CC}$ | $0.5V_{DS}$ | $0.1V_{DS}$ | $0.9V_{DS}$ |



aaa-002559

Measurement points are given in [Table 8](#).

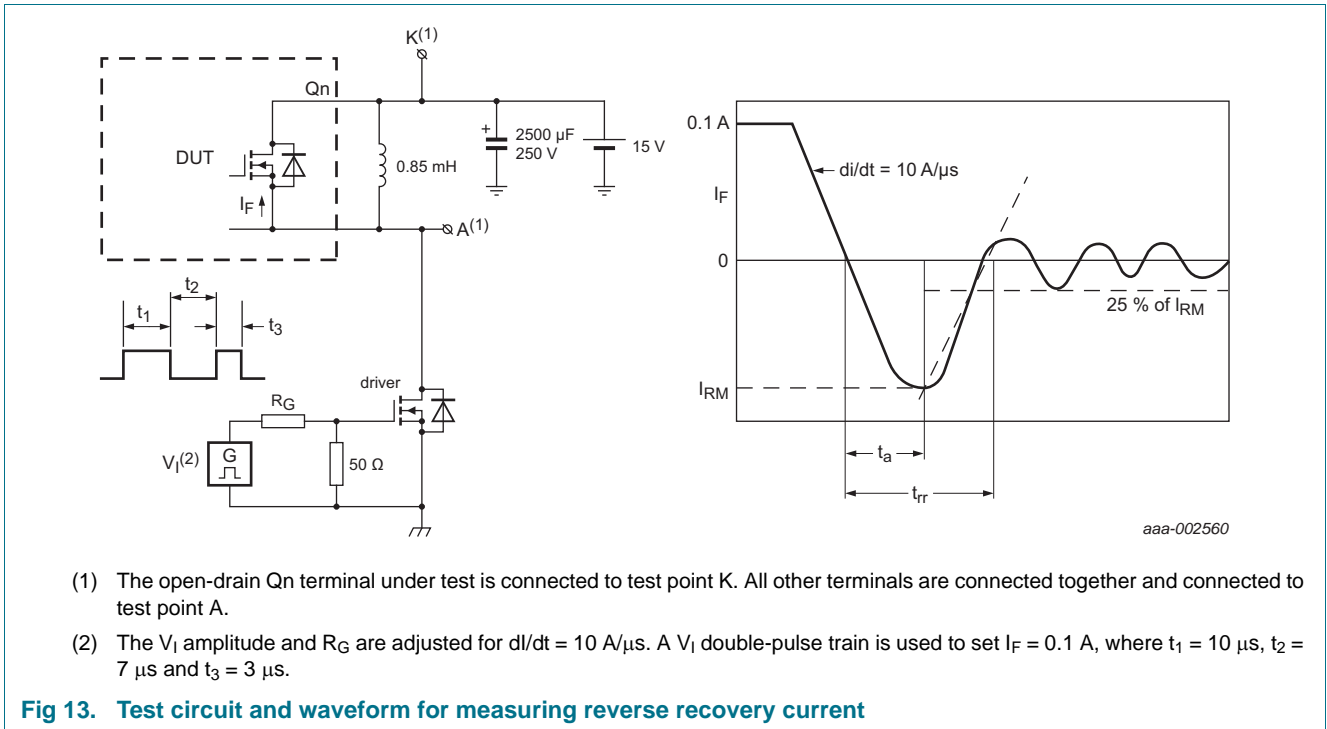
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 12. The data set-up and hold times for the serial data input (DS)

Table 8. Measurement points

| Supply voltage | Input | Output |
|----------------|-------------|-------------|
| V_{CC} | V_M | V_M |
| 5 V | $0.5V_{CC}$ | $0.5V_{CC}$ |



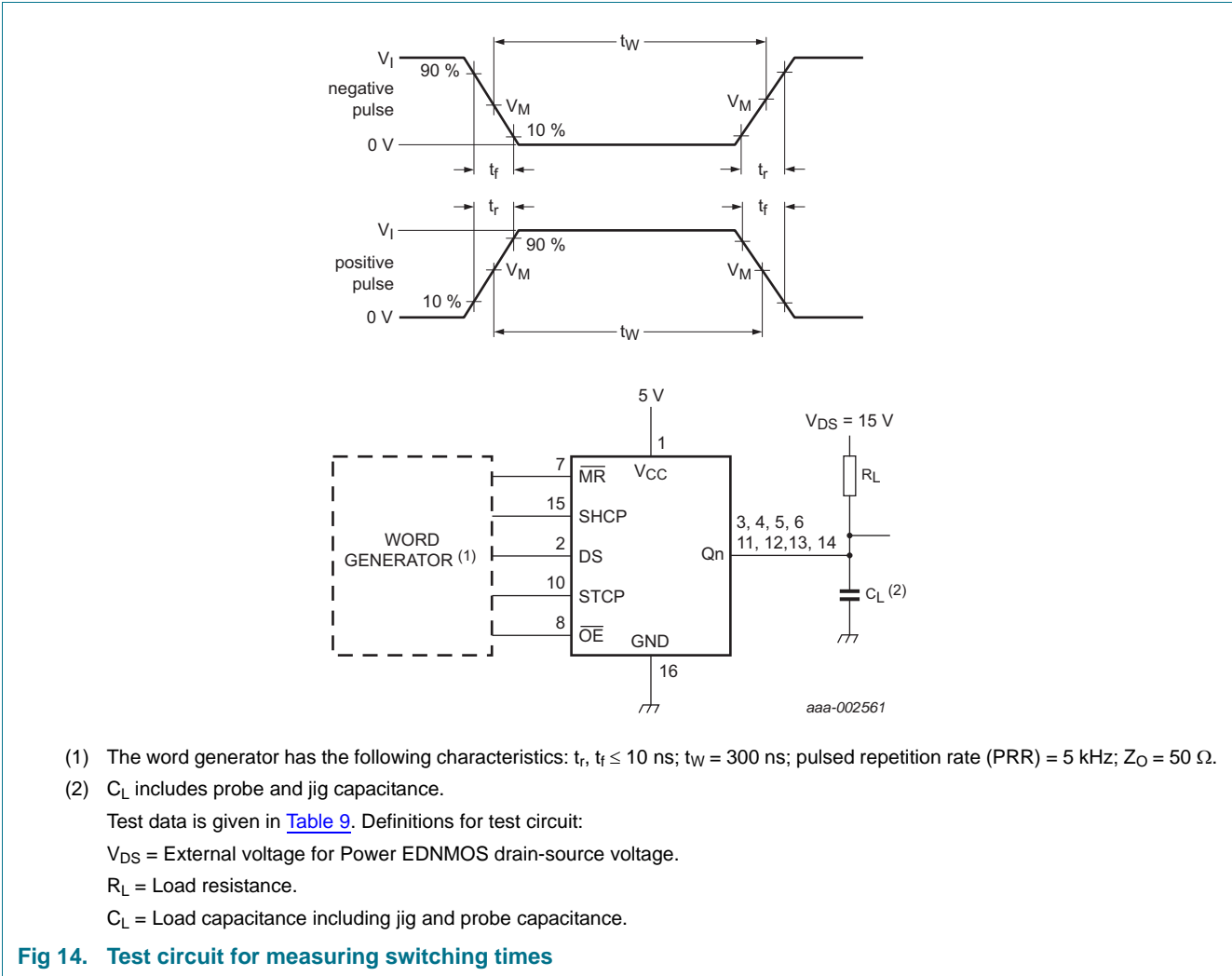
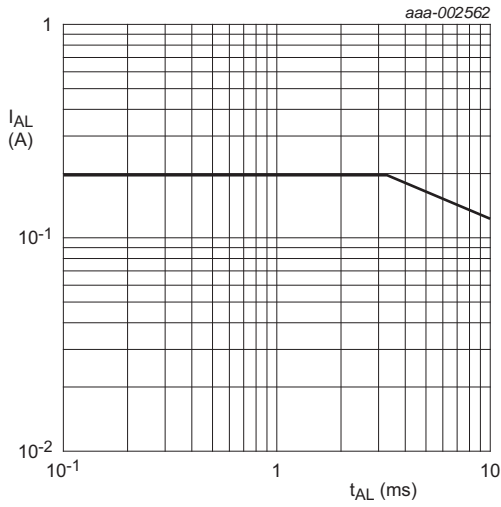


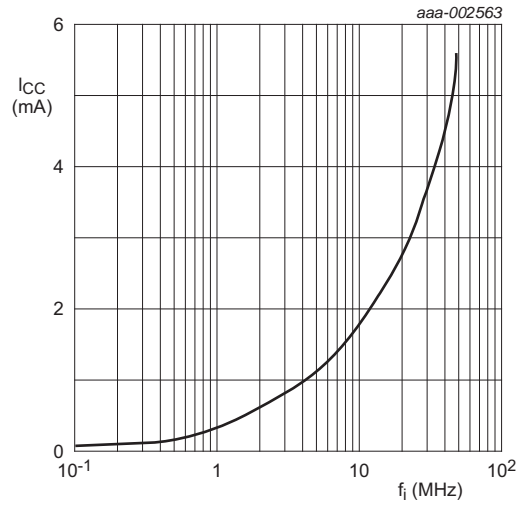
Table 9. Test data

| Supply voltage | Input | | | Load | |
|----------------|-------|--------------|-------|-------|--------------|
| | V_I | t_r, t_f | V_M | C_L | R_L |
| 5 V | 5 V | ≤ 10 ns | 50 % | 30 pF | 200 Ω |



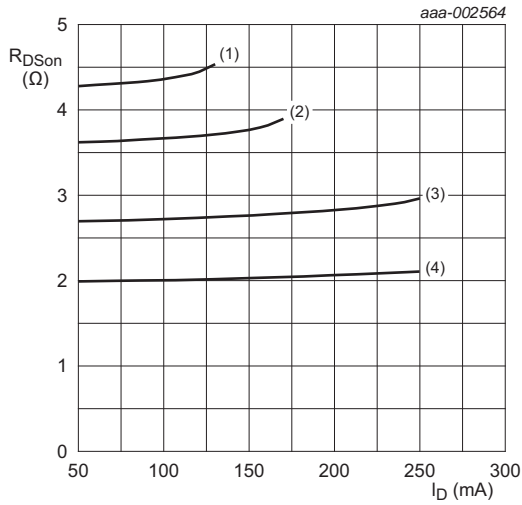
$T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig 15. Avalanche current (peak) versus time duration of avalanche



$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$.

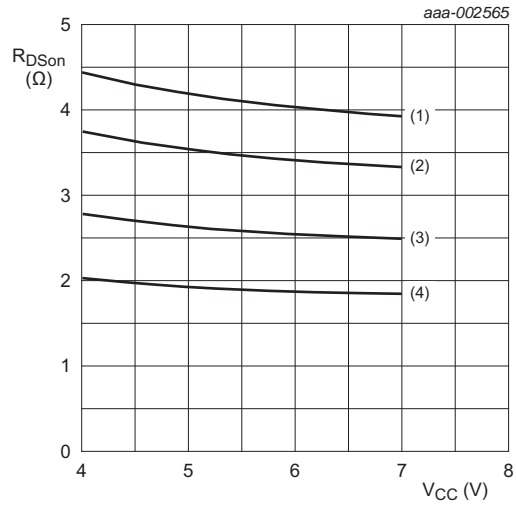
Fig 16. Supply current versus frequency



$V_I = V_{CC}$ or GND and $V_O = \text{GND}$ or V_{CC} .

- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$

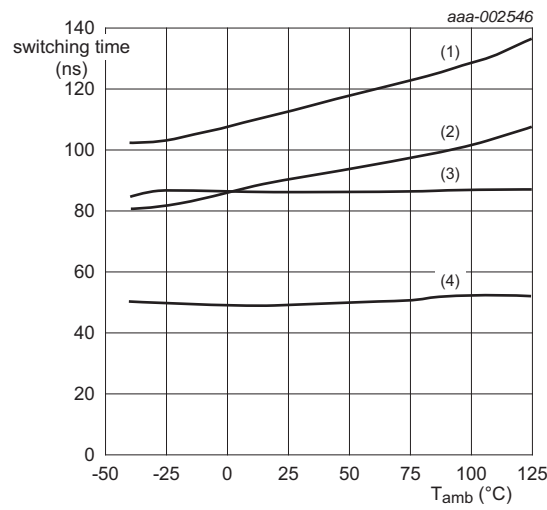
Fig 17. Drain-source on-state resistance versus drain current



$V_I = V_{CC}$ or GND and $V_O = \text{open circuit}$.

- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 18. Static drain-source on-state resistance versus supply voltage



Technique limit $T_J - T_C$ to 10 °C maximum.

- (1) t_{PLH} .
- (2) t_r .
- (3) t_f .
- (4) t_{PHL} .

Fig 19. Switching time versus case temperature

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

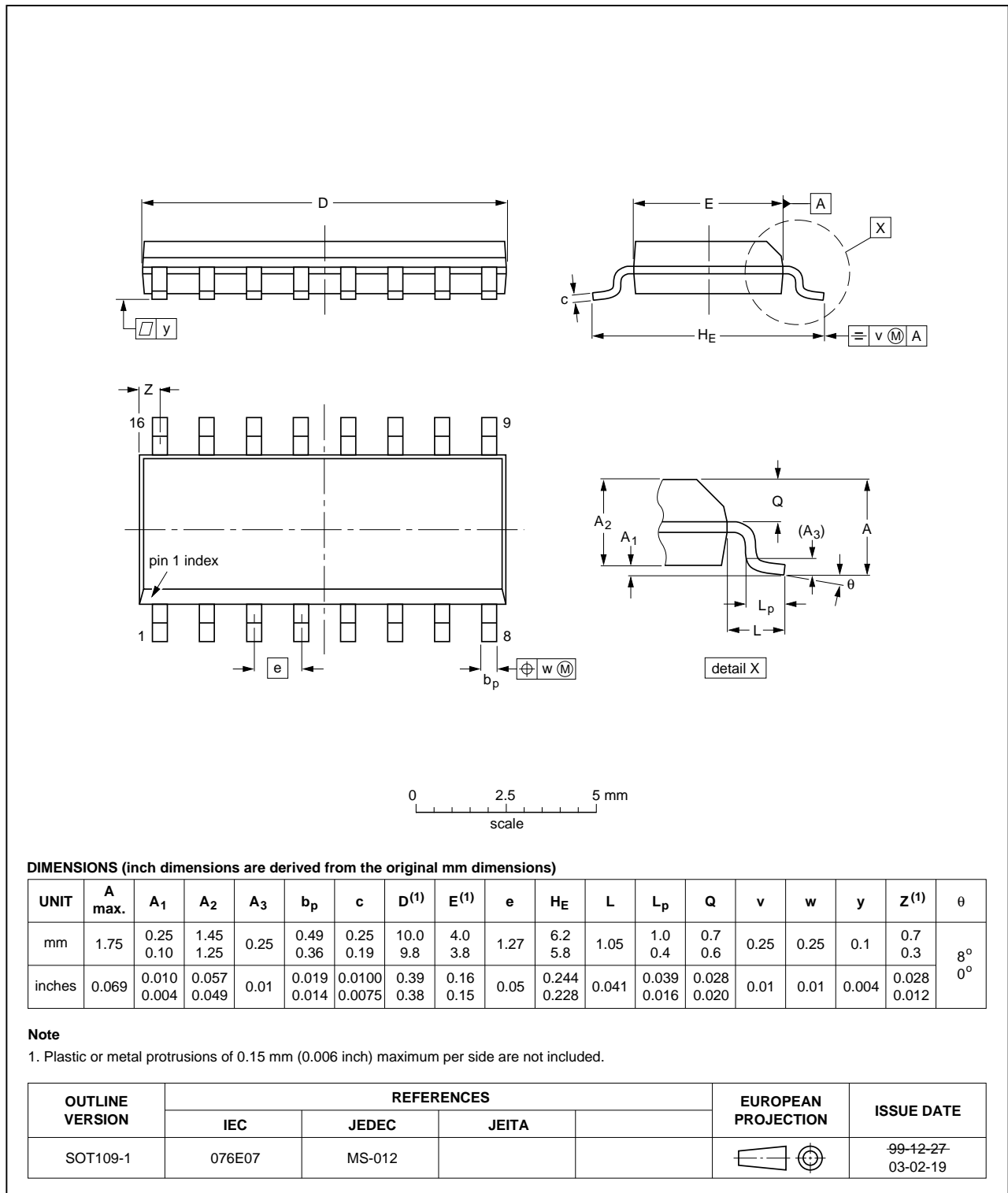


Fig 20. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

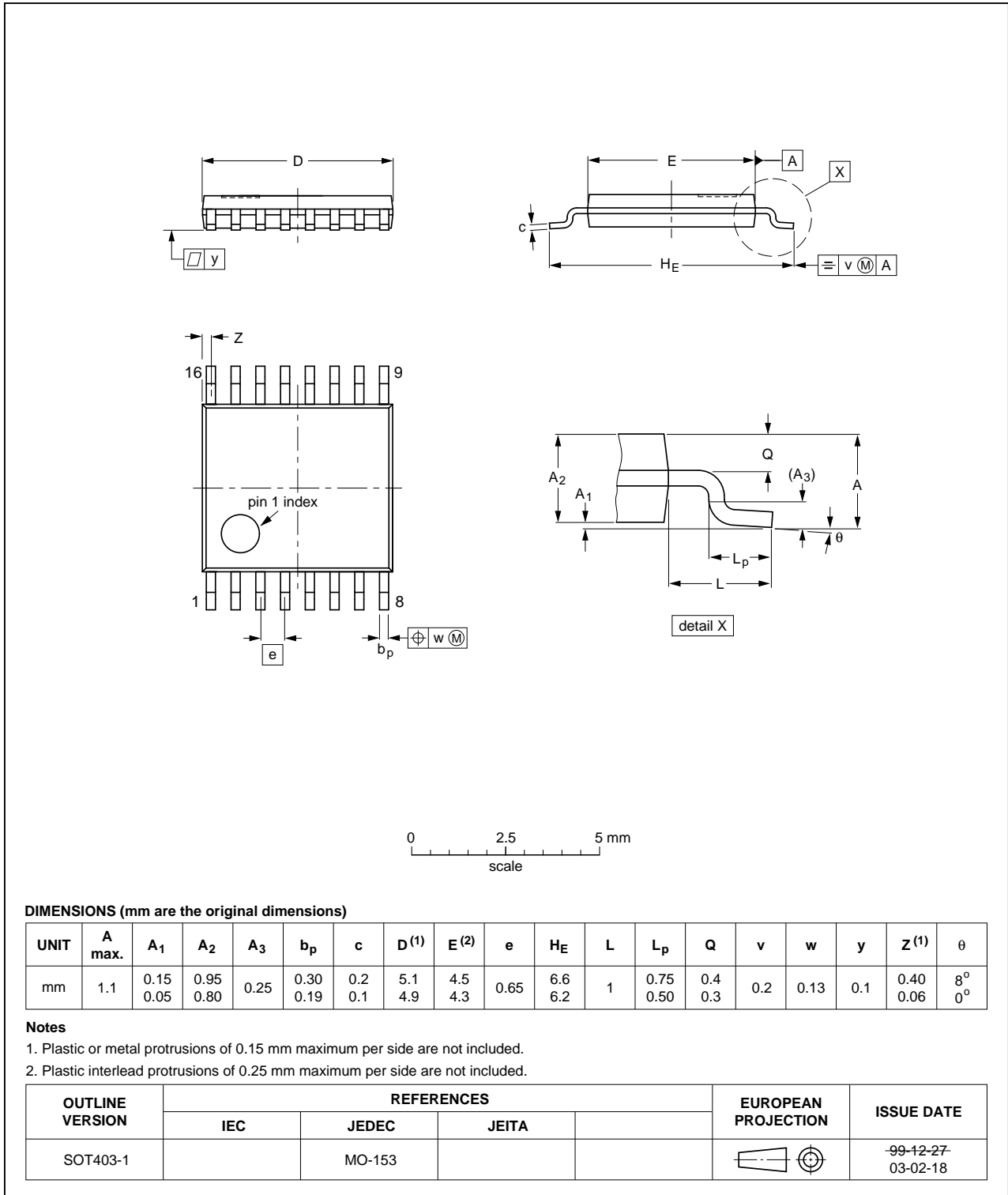


Fig 21. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

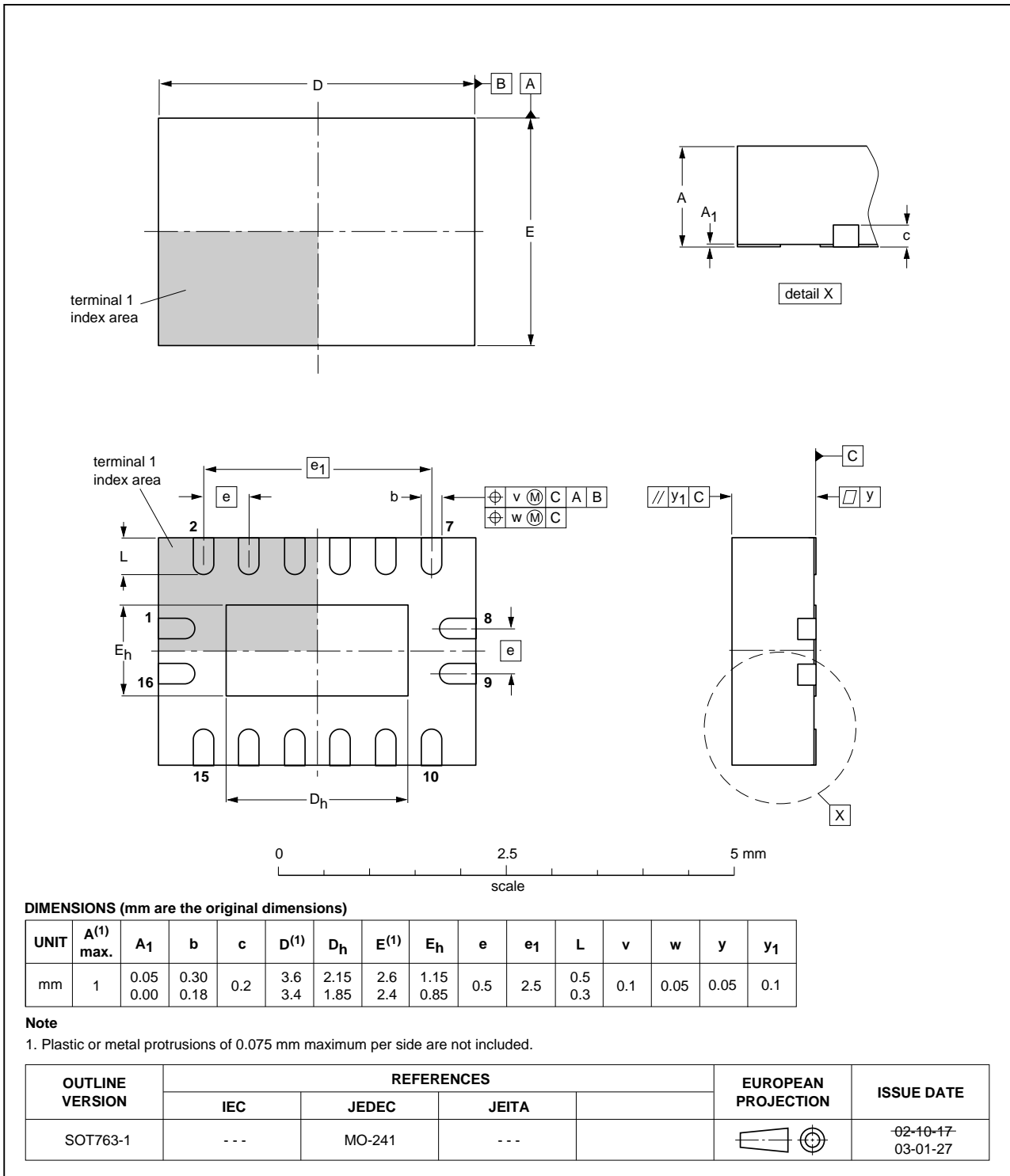


Fig 22. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| EDNMOS | Extended Drain Negative Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--------------------------------|--------------------|---------------|---------------|
| NPIC6C596 v.2 | 20130704 | Product data sheet | - | NPIC6C596 v.1 |
| Modifications: | • Figure 5 corrected (errata). | | | |
| NPIC6C596 v.1 | 20120821 | Product data sheet | - | - |

14. Legal information

14.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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