Click here for production status of specific part numbers.

MAX17673/MAX17673A Integrated 4.5V to 60V Synchronous 1.5A HV Buck and Dual 2.7V to 5.5V, 1A Buck Regulators

General Description

MAX17673/MAX17673A power management integrated circuits (PMIC) integrate a 60V high voltage (HV), high efficiency synchronous DC-DC buck regulator and two 5.5V high efficiency synchronous DC-DC buck regulators. All three regulators offer integrated power MOSFETs.

The HV regulator operates from a 4.5V to 60V input voltage range and the LV regulators operate from a 2.7V to 5.5V input voltage range. The HV regulator supports load currents up to 1.5A, and can regulate output voltages from 0.9V to 5.5V. The LV regulators support load currents up to 1A, and can regulate output voltages from 0.75V to 4.8V.

MAX17673/MAX17673A offer independent peak current mode control, hiccup mode overcurrent protection, ENABLE input and Power OK signal in the three regulators. The switching frequency is adjustable between 1MHz and 4MHz in the LV regulators, and the HV regulator can be programmed to run at a fractional switching frequency of the LV regulators. The HV regulator offers an adjustable soft-start function, while the LV regulators present internally fixed soft-start. Users can choose to operate the devices in either pulse frequency modulation (PFM) or forced pulse width modulation (PWM) scheme. The MAX17673A offers external clock synchronization.

The devices are available in a 28-pin, 5mm x 5mm TQFN package and operates over a -40°C to +125°C temperature range.

Applications

- Industrial Control Power Supplies
- FPGA/CPLD Power Supplies
- Distributed Supply Regulation
- Base Station Power Supplies
- High Voltage Single Board Systems

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Reduces External Components and Total Cost
  - Synchronous Operation for High Efficiency
  - Internal Compensation for a Wide Output Voltage Range
  - All-Ceramic Capacitors,Compact Layout
- Integrates Three DC-DC Regulators
  - Wide 4.5V to 60V Input Voltage Range for the HV Regulator. 2.7V to 5.5V Input Range for LV Regulators.
  - Adjustable 0.9V to 5.5V Output for the HV Regulator and 0.75V up to 4.8V Output for LV Regulators
  - Delivers up to 1.5A Load Current for the HV Regulator and 1A Load Current for LV Regulators
  - Adjustable Switching Frequency: 250KHz to 800KHz for HV Regulator and 1MHz to 4MHz for LV Regulators
  - Programmable LV / HV Switching Frequency Ratio (2, 3, 4, 5, 6, 7, 8)
  - EN/UVLO for HV buck and EN for LV regulators
- Reduces Power Dissipation
  - 550µA in PFM and 10.2mA in PWM Mode Quiescent Current
  - Peak Efficiency > 92%
  - Auxiliary Bootstrap LDO for Improved Efficiency
  - PFM Mode for High Light-Load Efficiency
  - 7.4µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Peak-Current Limit Protection
  - Hiccup Mode Overload Protection
  - Soft-Start Reduces Inrush Current During Startup (Adjustable for HV Regulator)
  - Built-In Output-Voltage Monitoring with POKH, POKA, and POKB
  - Monotonic Startup into Prebiased Load
  - Overtemperature Protection
  - Dynamic Mode Change for On-the-Fly Shift Between PFM and PWM Mode
  - -40°C to +125°C Operating Temperature Range
  - Complies with CISPR22(EN55022) Class B Conducted and Radiated Emissions

19-100403; Rev 2; 11/19

maxim integrated™

Absolute Maximum Ratings

INH to PGND ..... -0.3V to +65V
ENH to GND ..... -0.3V to +65V
BSTH to PGND ..... -0.3V to +70V
LXH to PGND ..... -0.3V to (V_{INH} + 0.3V)
BSTH to LXH ..... -0.3V to +6V
BSTH to V_{CC} ..... -0.3V to +65V
INA, INB to PGND ..... -0.3V to +6V
ENA, ENB to GND ..... -0.3V to +6V
LXA to PGND ..... -0.3V to (V_{INA} + 0.3V)
LXB to PGND ..... -0.3V to (V_{INB} + 0.3V)
EXTVCC, V_{CC} to GND ..... -0.3V to +6V
FBH, FBA, FBB, POKH, POKA, POKB, MODE/SYNC to GND ..... -0.3V to +6V
SSH, RT, FDIV to GND ..... -0.3V to (V_{CC} + 0.3V)
LXH Total RMS Current ..... ±1.6A
LXA, LXB Total RMS Current ..... ±1.1A
PGNDA, PGNDB, PGNDH to GND ..... -0.3V to 0.3V
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 34.5mW/°C above +70°C.) 2758.6mW
Operating Temperature Range (Note 1) ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 28 TQFN	
Package Code	T2855+6C
Outline Number	**21-0140**
Land Pattern Number	**90-0026**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	+29° C/W
Junction to Case (θ_{JC})	+2° C /W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{INH} = V_{ENH} = 24V, V_{EXTVCC} = V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, $V_{FB_}$ = 1V, C_{VCC} = 2.2µF, R_{FDIV} = 0Ω, RT = LX_ = SSH = POK_ = OPEN, V_{BST} to V_{LXH} = 5V, $V_{MODE/SYNC}$ = $V_{PGND_}$ = V_{GND} = V_{SGND} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range for HV Regulator	V_{INH}		4.5		60	V
Input Voltage Range for LV Regulator A-B	V_{INA}, V_{INB}		2.7		5.5	V
INH Shutdown Current	I_{IN_SH}	V_{ENH} = V_{ENA} = V_{ENB} = 0V (shutdown mode), V_{EXTVCC} = 0V)		7.3	15	µA
INA, INB Shutdown Current	I_{INL_SH}	V_{ENH} = V_{ENA} = V_{ENB} = 0V (shutdown mode)		0.25	1.5	µA
INH Quiescent Current	I_{INH_QPWM}	Normal switching, PWM mode, f_{SW_HV} = 400kHz, V_{FBH} = 0.9V, MODE = 0V, V_{EXTVCC} = 0V		10.2		mA
INA, INB Quiescent Current	I_{INL_QPWM}	Normal switching, PWM mode, f_{SW_LV} = 2MHz, V_{FBA} = V_{FBB} = 0.75V, MODE = 0V, V_{EXTVCC} = 0V		8.8		mA
ENABLE/UVLO (EN)						
Enable Threshold for HV Regulator	V_{ENH_R}	ENH rising	1.175	1.200	1.225	V
	V_{ENH_F}	ENH falling	1.055	1.080	1.105	
Enable Input Leakage Current for HV Regulator	I_{ENH_LKG}	V_{ENH} = 1.25V, T_A =25°C	-100		+100	nA
Enable threshold for LV Regulator A-B	V_{ENL_R}	ENA, ENB rising	1.2			V
	V_{ENL_F}	ENA, ENB falling			0.4	
Enable Hysteresis for LV Regulator A-B	V_{ENL_HYS}			150		mV
Enable Input Leakage Current for LV Regulator A-B	I_{ENL_LKG}	T_A = T_J = +25°C, V_{ENA}, V_{ENB} = 5.5V	-250		250	nA
V_{CC} LDO						
V_{CC} Output Voltage Range	V_{CC}	0mA ≤ I_{VCC} ≤ 15mA, V_{EXTVCC} = 0V, 6V < V_{INH} < 60V	4.75	5.00	5.25	V
V_{CC} Current Limit	I_{VCC_MAX}	V_{VCC} = 3.5V, V_{INH} = 4.5V	20	54	100	mA
V_{CC} Dropout	V_{CC_DO}	V_{INH} = 4.5V , I_{VCC} = 15mA			0.5	V
V_{CC} UVLO	V_{CC_UVR}	Undervoltage lockout rising	2.50	2.62	2.70	V
	V_{CC_UVF}	Undervoltage lockout falling	2.43	2.49	2.55	

Electrical Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{EXTVCC} = V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, $V_{FB_}$ = 1V, C_{VCC} = 2.2µF, R_{FDIV} = 0Ω, RT = LX_ = SSH = POK_ = OPEN, V_{BST} to V_{LXH} = 5V, $V_{MODE/SYNC}$ = $V_{PGND_}$ = V_{GND} = V_{SGND} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL POWER SUPPLY						
EXTVCC Switchover Voltage	V_{EXTVCC_R}	EXTVCC rising, V_{INH} > 4.5V	2.83	2.89	3.00	V
	V_{EXTVCC_F}	EXTVCC falling, V_{INH} > 4.5V	2.80	2.86	2.95	
EXTVCC Current Limit	I_{EXTVCC_MAX}	V_{EXTVCC} = 3.3V, V_{VCC} = 3V,	20	40	100	mA
EXTVCC Dropout	V_{EXTVCC_DO}	V_{EXTVCC} = 3.3V, I_{VCC} = 15mA			125	mV
HIGH-SIDE MOSFET & LOW SIDE MOSFET DRIVER						
High-Side MOSFET On-Resistance for HV Regulator	R_{HSH}	I_{LXH} = 0.1A, V_{EXTVCC} = 5V (Note 3)		290	600	mΩ
Low-Side MOSFET On-Resistance for HV Regulator	R_{LSH}	I_{LXH} = 0.1A, V_{EXTVCC} = 5V (Note 3)		170	350	mΩ
LX Leakage Current for HV Regulator	I_{LXH_LKG}	V_{LXH} = (V_{INH} - 1V) to (V_{PGNDH} +1 V); T_A = 25°C	-1		+1	µA
High-Side MOSFET On-Resistance for LV Regulator A-B	R_{HSL}	V_{INA}, V_{INB} = 5V, I_{LXA}, I_{LXB} = 190mA, V_{EXTVCC} = 3.6V (Note 3)		120	300	mΩ
Low-Side MOSFET On-Resistance for LV Regulator A-B	R_{LSL}	V_{INA}, V_{INB} = 5V, I_{LXA}, I_{LXB} = 190mA, V_{EXTVCC} = 3.6V (Note 3)		60	100	mΩ
LX Leakage Current for LV Regulator A-B	I_{LXL_LKG}	LXA, LXB = GND, or V_{INA}, V_{INB}. T_A = 25°C	-0.5		+0.5	µA
SOFT-START						
Soft-Start Current for HV Regulator	I_{SS_HV}	V_{SSH} = 0.5V	4.25	5.00	5.75	µA
Soft-Start Time for LV Regulators	t_{SS_LV}	Time duration of output voltage ramp up		4096		cycles
FEEDBACK (FBH, FBA, FBB)						
FBH Regulation Voltage for HV Regulator	V_{FBH}		0.888	0.900	0.912	V
FBA, FBB Regulation Voltage	V_{FBL_REG}		0.740	0.750	0.760	V
FBH Input Bias Current for HV Regulator	I_{FB_HV}	0 ≤ V_{FBH} ≤ 1V, T_A = 25°C. EXTVCC or INH valid	-150		+150	nA
FBA, FBB Input Bias Current for LV Regulator A-B	I_{FB_LKG}	0 < V_{FBA}, V_{FBB} < 1V, T_A = 25°C. EXTVCC or INH valid	-150		+150	nA

Electrical Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{EXTVCC} = V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, $V_{FB_}$ = 1V, C_{VCC} = 2.2µF, R_{FDIV} = 0Ω, RT = LX_ = SSH = POK_ = OPEN, V_{BST} to V_{LXH} = 5V, $V_{MODE/SYNC}$ = $V_{PGND_}$ = V_{GND} = V_{SGND} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PFM/HIBERNATE MODE						
FBH PFM Skip Threshold	V_{FBH_PFMR}	V_{FBH} rising	102	102.75	103.7	%
FBH PFM Resume Threshold	V_{FBH_PFMF}	V_{FBH} falling	100.4	101	101.8	%
FBA, FBB PFM Skip Threshold	V_{FBL_PFMR}	V_{FBA}, V_{FBB} rising	101.2	102.5	103.6	%
FBA, FBB PFM Resume Threshold	V_{FBL_PFMF}	V_{FBA}, V_{FBB} falling	100.5	101.7	102.8	%
CURRENT LIMIT						
Peak Current Limit Threshold for HV Regulator	I_{LXH_PKLMT}		2.3	2.7	3.1	A
Negative Current Limit Threshold for HV Regulator	$I_{LIM_NEG_HV}$	Current entering into LXH pin		1.1		A
PFM Current Limit for HV Regulator	I_{LXH_PFM}			0.82		A
Peak Current Limit Threshold for LV Regulator A-B	$I_{LX_PKLMT_LV}$		1.40	1.70	2.05	A
Negative Current Limit Threshold for LV Regulator A-B	$I_{LIM_NEG_LV}$	Current entering into the LXA, LXB pin		0.75		A
PFM Current Limit for LV Regulators A-B	I_{LXL_PFM}			0.54		A
RT/FDIV AND TIMINGS						
Switching Frequency for LV Regulator A-B	f_{SW_LV}	R_{FDIV} = 0Ω	1.78	2.00	2.22	MHz
		R_{RT} = 29.93kΩ, R_{FDIV} > 1.35kΩ (Note 3)	3.36	4.00	4.64	
		R_{RT} = 229.4kΩ, R_{FDIV} > 1.35kΩ	0.80	1.00	1.21	
Switching Frequency for HV Regulator	f_{SW_HV}	R_{FDIV} = 0Ω	356	400	444	kHz
		R_{RT} = 29.93kΩ, R_{FDIV} = 15kΩ	672	800	928	
		R_{RT} = 90kΩ, R_{FDIV} > 89kΩ	220	250	298	
$V_{FB_}$ Undervoltage Trip Level to Cause HICCUP	V_{OUT_HICF}	In percentage of $V_{FB_}$	60	64	70	%
HICCUP Timeout				32768		Cycles

Electrical Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{EXTVCC} = V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, $V_{FB_}$ = 1V, C_{VCC} = 2.2µF, R_{FDIV} = 0Ω, RT = LX_ = SSH = POK_ = OPEN, V_{BST} to V_{LXH} = 5V, $V_{MODE/SYNC}$ = $V_{PGND_}$ = V_{GND} = V_{SGND} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum On-Time for HV Regulator	$t_{ON_MIN_HV}$	V_{EXTVCC} = 5V, V_{INH} = 24V		73	105	ns
MAX Duty Cycle for HV Regulator	D_{MAX_HV}			93.2		%
Minimum On-Time for LV Regulator A-B	$t_{ON_MIN_LV}$	V_{EXTVCC} = 5V, V_{INA} = V_{INB} = 5V		38	55	ns
Minimum OFF time for LV regulator A-B	$t_{OFF_MIN_LV}$	V_{EXTVCC} = 5V, V_{INA} = V_{INB} = 3.6V		15		ns
MODE Threshold (MAX17673) MODE/SYNC Threshold (MAX17673A)	V_{IH}		1.4			V
	V_{IL}				0.4	
Sync Frequency Capture Range	f_{SYNC}	f_{SW_LV} = 1MHz and f_{SW_LV} = 4MHz MAX17673A Only	0.9 x f_{SW_LV}		1.1 x f_{SW_LV}	MHz
Sync Pulse High Time	t_{SYNC_HIGH}		25			ns
Sync Pulse Low Time	t_{SYNC_LOW}		25			ns
POKH, POKA, POKB (POK_)						
POK_ Output Level Low		I_{POK} = 10mA			250	mV
POK_ Output Leakage Current		T_A = T_J = 25°C	-0.25		+0.25	µA
V_{OUT} Threshold for POK_ Assertion	V_{OUT_OKF}	$V_{FB_}$ falling	89.0	92.0	95.5	%
V_{OUT} Threshold for POK_ Deassertion	V_{OUT_OKR}	$V_{FB_}$ rising	92	95.0	98.5	%
POK_ delay after FB reaches rising threshold				2048		Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDNR}	Temp rising		165		°C
Thermal Shutdown Hysteresis	T_{SHDNHY}			20		°C

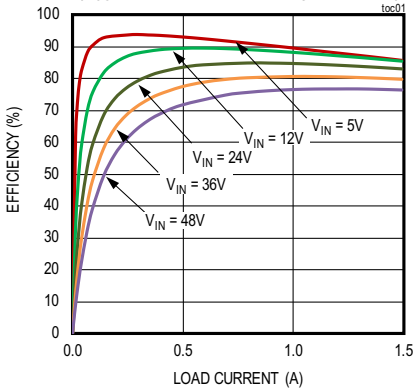
Note 2: All limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 3: Not production tested. Guaranteed by design.

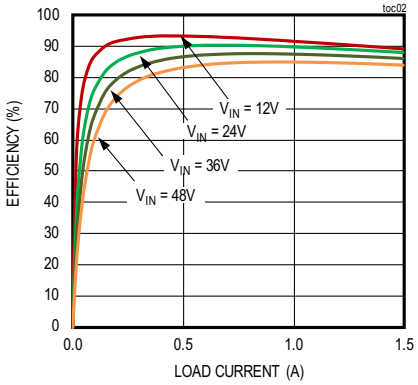
Typical Operating Characteristics

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

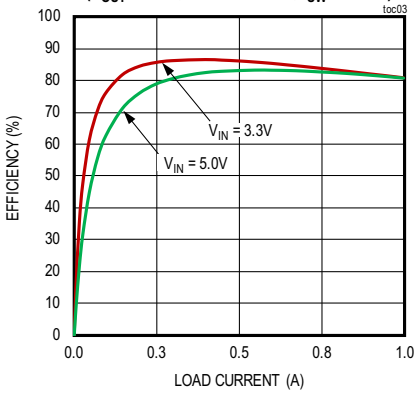
HV BUCK EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V, MODE = PWM, f_{SW} = 400kHz)



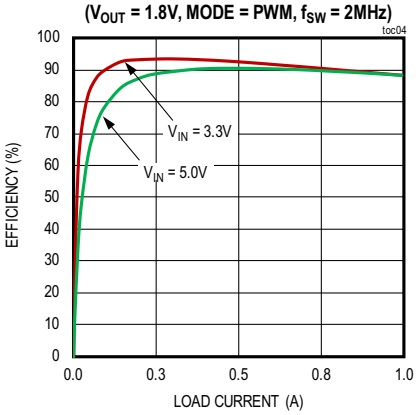
HV BUCK EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 5.0V, MODE = PWM, f_{SW} = 400kHz)



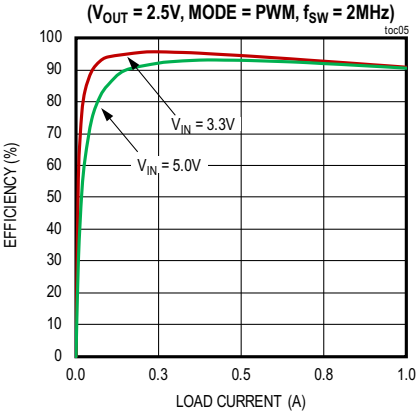
LV BUCK EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 1.0V, MODE = PWM, f_{SW} = 2MHz)



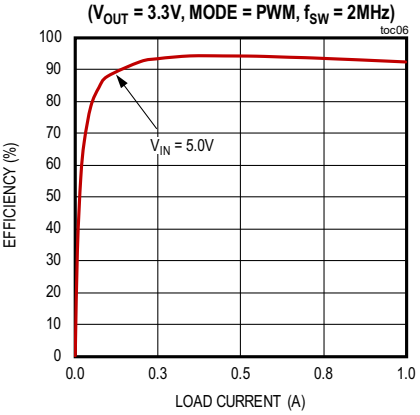
LV BUCK EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 1.8V, MODE = PWM, f_{SW} = 2MHz)



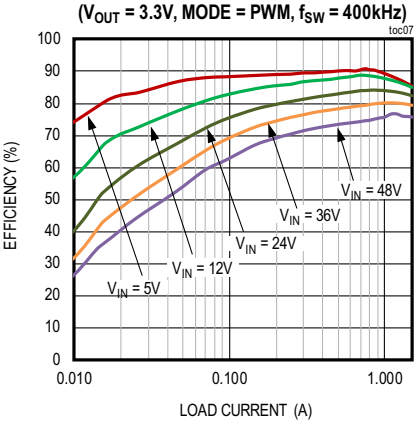
LV BUCK EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 2.5V, MODE = PWM, f_{SW} = 2MHz)



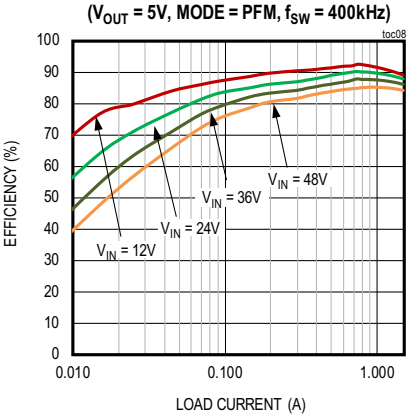
LV BUCK EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V, MODE = PWM, f_{SW} = 2MHz)



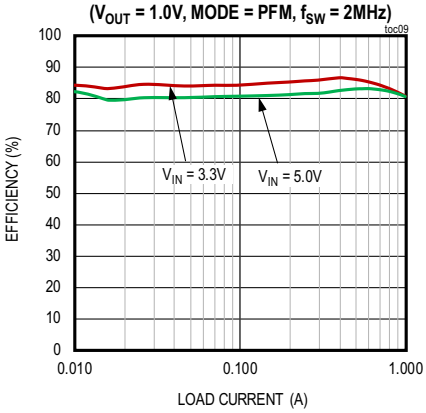
HV BUCK EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V, MODE = PWM, f_{SW} = 400kHz)



HV BUCK EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 5V, MODE = PFM, f_{SW} = 400kHz)



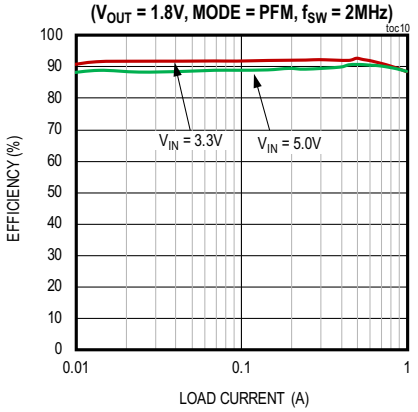
LV BUCK EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 1.0V, MODE = PFM, f_{SW} = 2MHz)



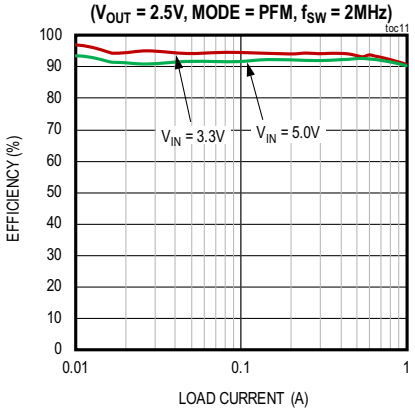
Typical Operating Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

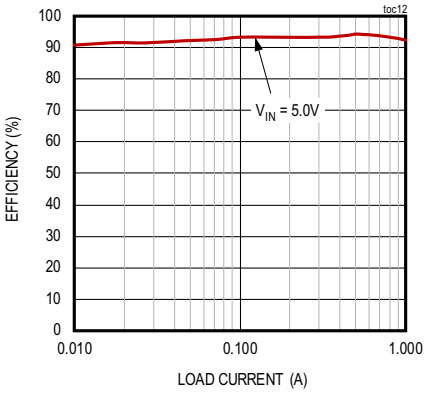
LV BUCK EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.8V, MODE = PFM, f_{SW} = 2MHz)



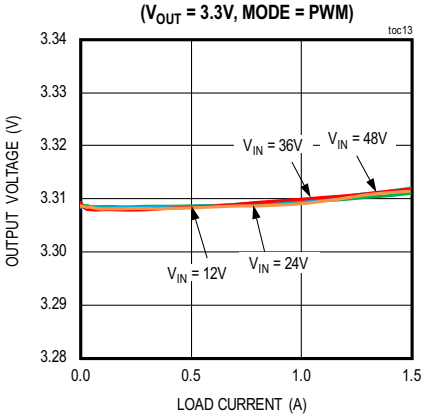
LV BUCK EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 2.5V, MODE = PFM, f_{SW} = 2MHz)



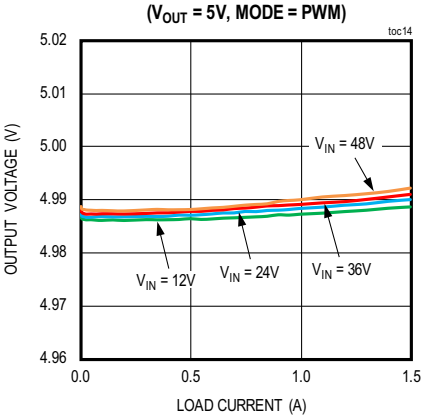
LV BUCK EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 3.3V, MODE = PFM, f_{SW} = 2MHz)



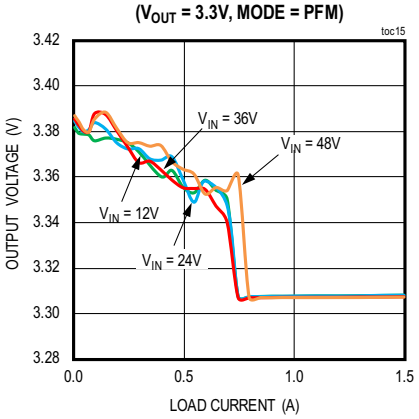
HV BUCK OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 3.3V, MODE = PWM)



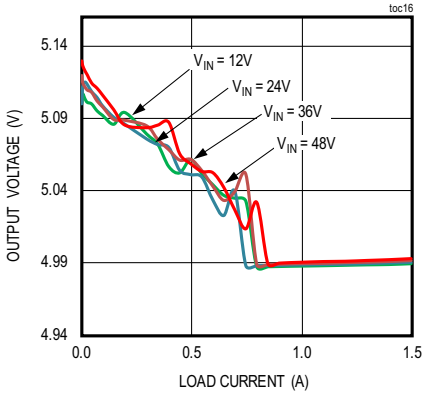
HV BUCK OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 5V, MODE = PWM)



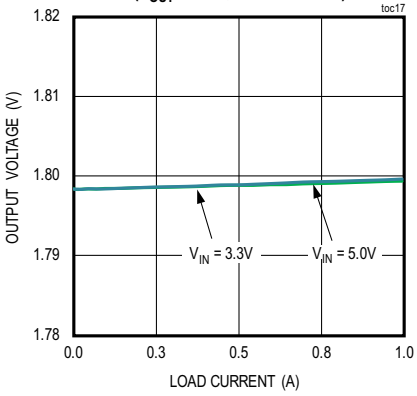
HV BUCK OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 3.3V, MODE = PFM)



HV BUCK OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 5V, MODE = PFM)



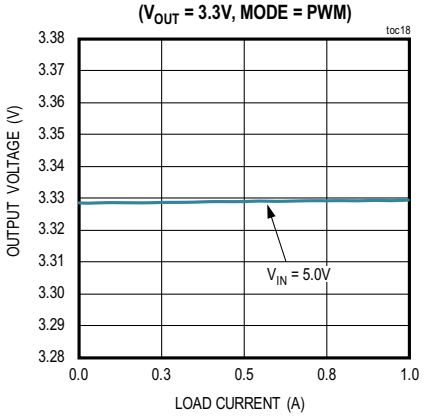
LV BUCK OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.8V, MODE = PWM)



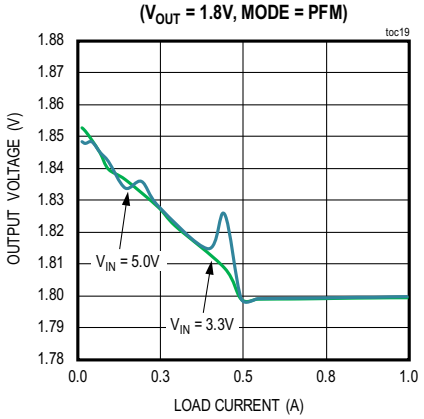
Typical Operating Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

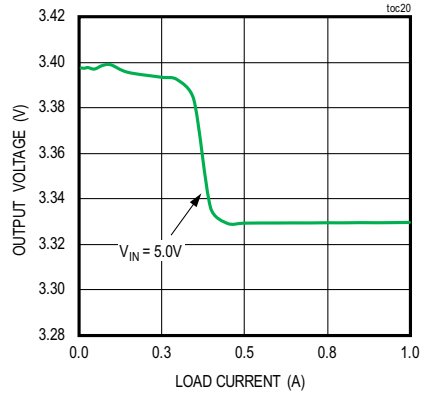
LV BUCK OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 3.3V, MODE = PWM)



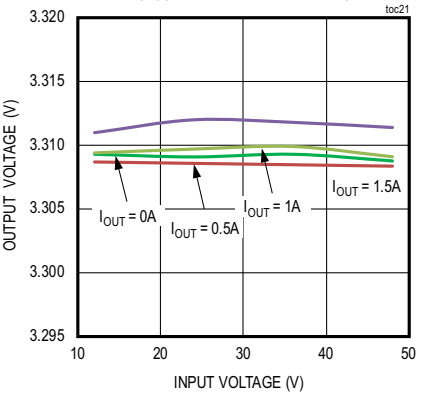
LV BUCK OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.8V, MODE = PFM)



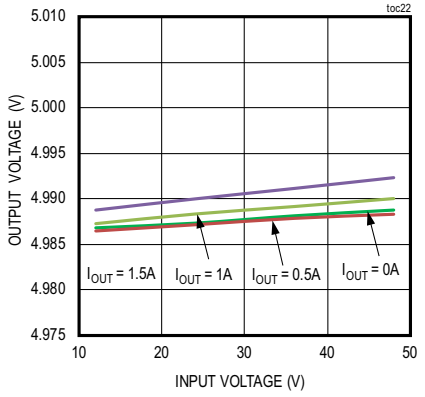
LV BUCK OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 3.3V, MODE = PFM)



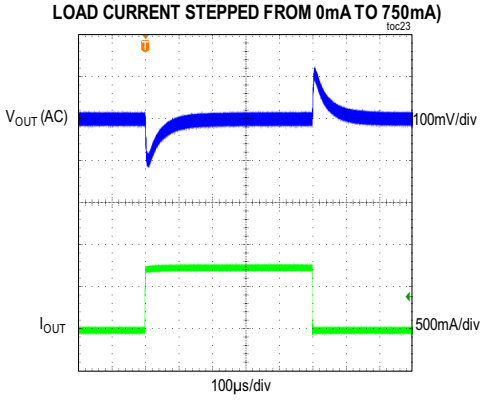
HV BUCK OUTPUT VOLTAGE vs. INPUT VOLTAGE (V_{OUT} = 3.3V, MODE = PWM)



HV BUCK OUTPUT VOLTAGE vs. INPUT VOLTAGE (V_{OUT} = 5.0V, MODE = PWM)



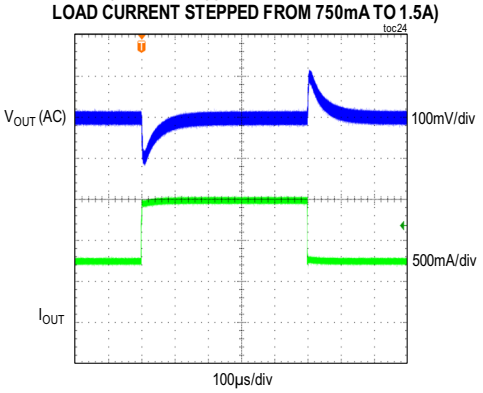
HV BUCK LOAD TRANSIENT RESPONSE (V_{IN} = 24V, V_{OUT} = 5V, MODE = PWM LOAD CURRENT STEPPED FROM 0mA TO 750mA)



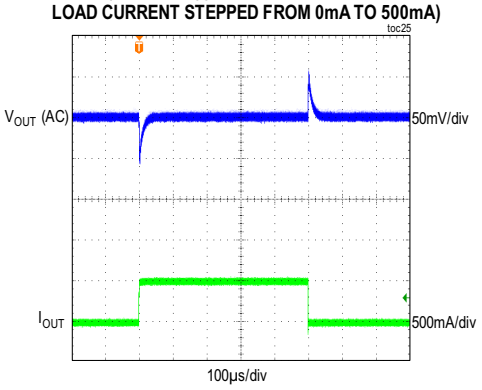
Typical Operating Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

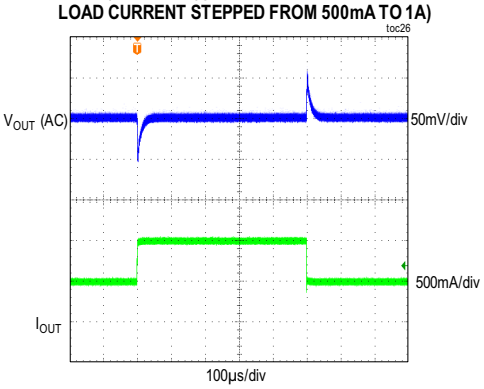
HV BUCK LOAD TRANSIENT RESPONSE
(V_{IN} = 24V, V_{OUT} = 5V, MODE = PWM
LOAD CURRENT STEPPED FROM 750mA TO 1.5A)



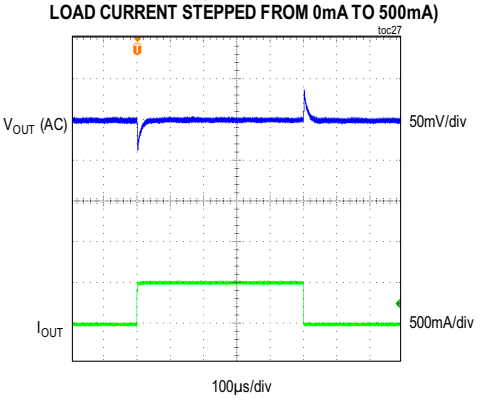
LV BUCK LOAD TRANSIENT RESPONSE
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PWM
LOAD CURRENT STEPPED FROM 0mA TO 500mA)



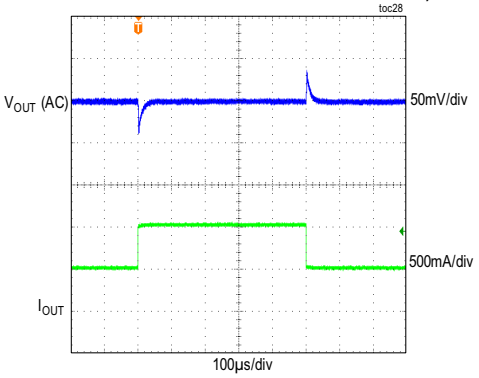
LV BUCK LOAD TRANSIENT RESPONSE
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PWM
LOAD CURRENT STEPPED FROM 500mA TO 1A)



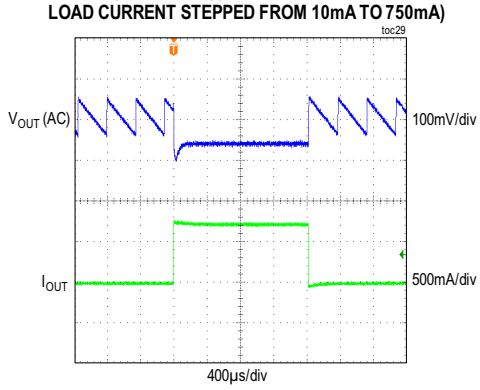
LV BUCK LOAD TRANSIENT RESPONSE
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PWM
LOAD CURRENT STEPPED FROM 0mA TO 500mA)



LV BUCK LOAD TRANSIENT RESPONSE
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PWM
LOAD CURRENT STEPPED FROM 500mA TO 1A)



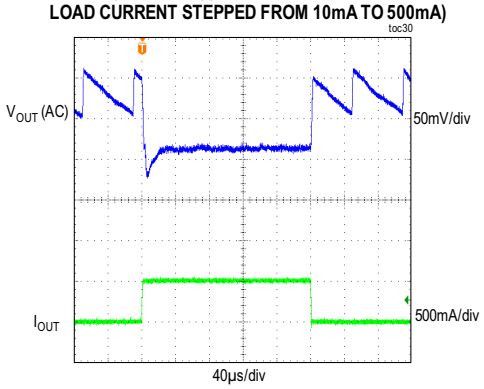
HV BUCK LOAD TRANSIENT RESPONSE
(V_{IN} = 24V, V_{OUT} = 5V, MODE = PFM
LOAD CURRENT STEPPED FROM 10mA TO 750mA)



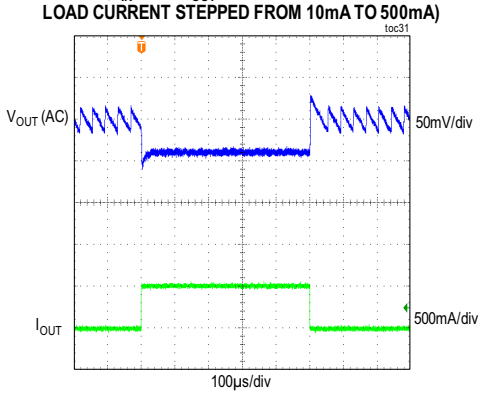
Typical Operating Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

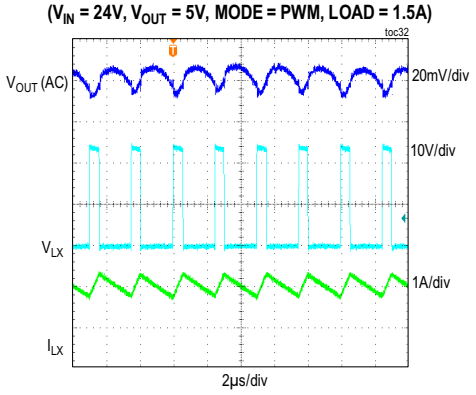
LV BUCK LOAD TRANSIENT RESPONSE
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PFM
LOAD CURRENT STEPPED FROM 10mA TO 500mA)



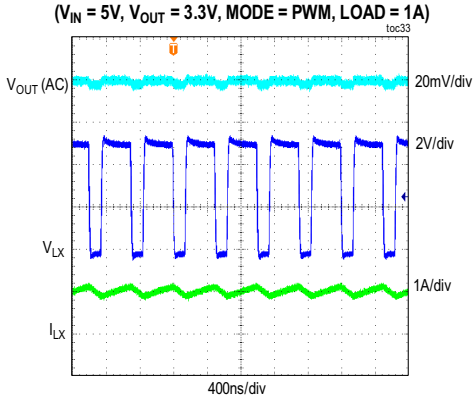
LV BUCK LOAD TRANSIENT RESPONSE
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PFM
LOAD CURRENT STEPPED FROM 10mA TO 500mA)



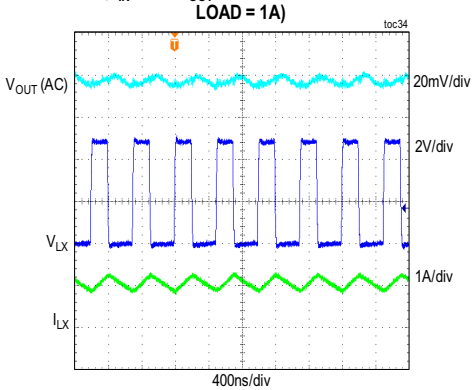
HV BUCK STEADY-STATE SWITCHING WAVEFORMS
(V_{IN} = 24V, V_{OUT} = 5V, MODE = PWM, LOAD = 1.5A)



LV BUCK STEADY-STATE SWITCHING WAVEFORMS
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PWM, LOAD = 1A)



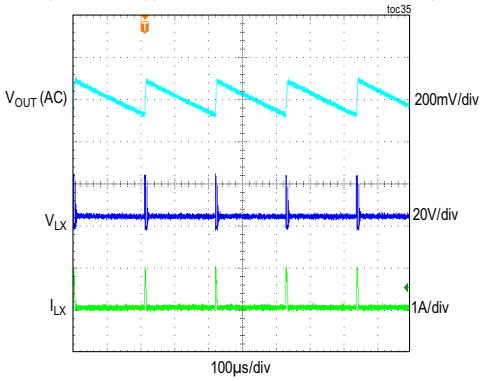
LV BUCK STEADY-STATE SWITCHING WAVEFORMS
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PWM
LOAD = 1A)



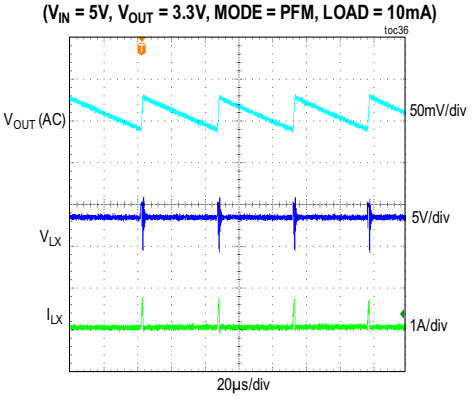
Typical Operating Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

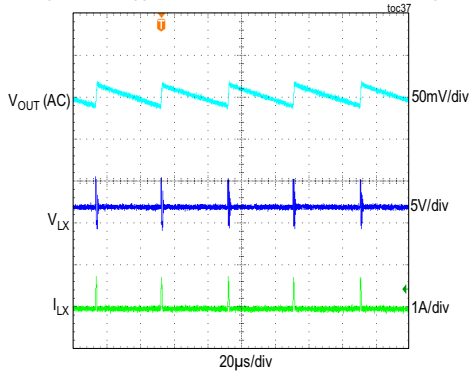
HV BUCK STEADY-STATE SWITCHING WAVEFORMS
(V_{IN} = 24V, V_{OUT} = 5V, MODE = PFM, LOAD = 15mA)



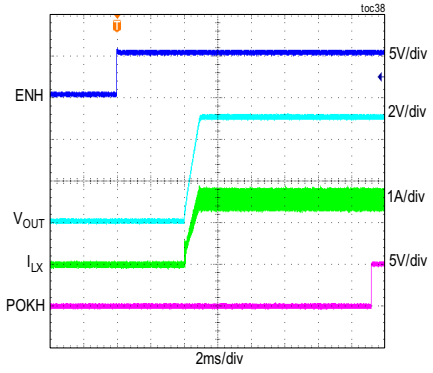
LV BUCK STEADY-STATE SWITCHING WAVEFORMS
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PFM, LOAD = 10mA)



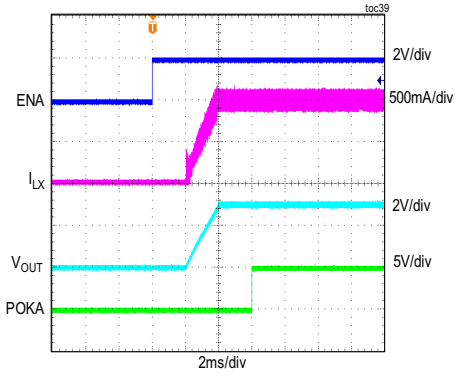
LV BUCK STEADY-STATE SWITCHING WAVEFORMS
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PFM, LOAD = 10mA)



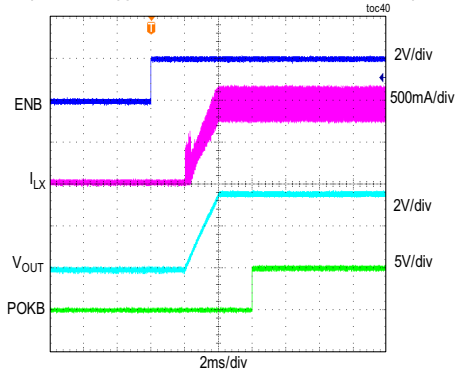
HV BUCK STARTUP THROUGH ENABLE
(V_{IN} = 24V, V_{OUT} = 5V, MODE = PWM, LOAD = 1.5A)



LV BUCK STARTUP THROUGH ENABLE
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PWM, LOAD = 1.0A)



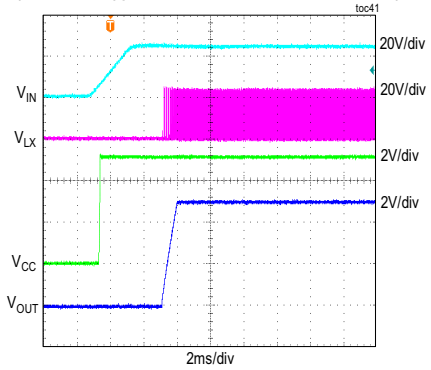
LV BUCK STARTUP THROUGH ENABLE
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PWM, LOAD = 1.0A)



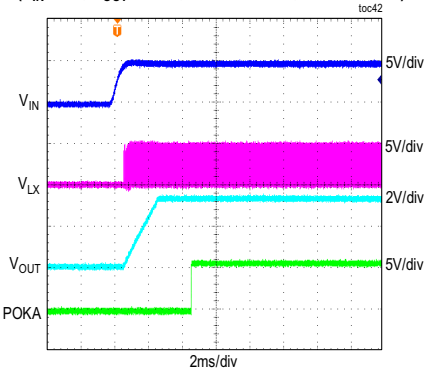
Typical Operating Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

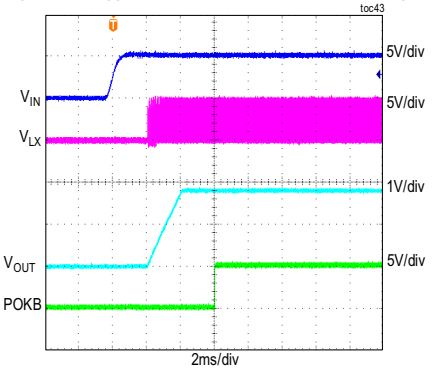
HV BUCK STARTUP FROM INPUT
(V_{IN} = 24V, V_{OUT} = 5V, MODE = PWM, LOAD = 1.5A)



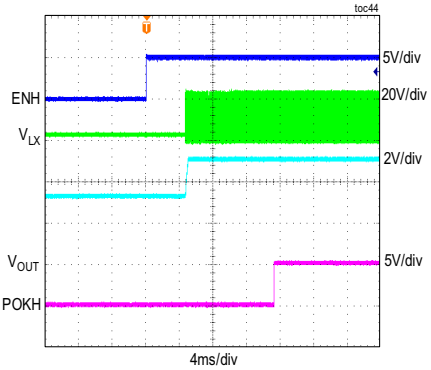
LV BUCK STARTUP FROM INPUT
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PWM, LOAD = 1.0A)



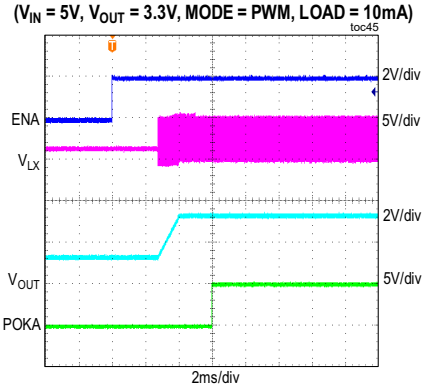
LV BUCK STARTUP FROM INPUT
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PWM, LOAD = 1.0A)



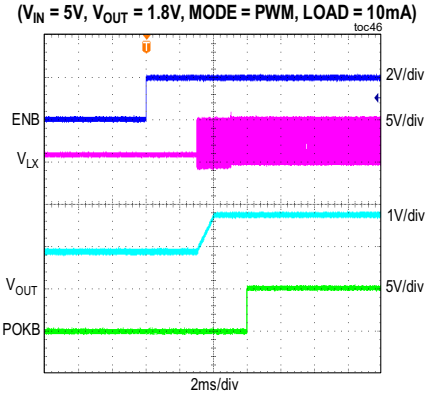
HV STARTUP THROUGH ENABLE, 3.3V PREBIAS
(V_{IN} = 24V, V_{OUT} = 5V, MODE = PWM, LOAD = 10mA)



LV STARTUP THROUGH ENABLE, 1.5V PREBIAS
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PWM, LOAD = 10mA)



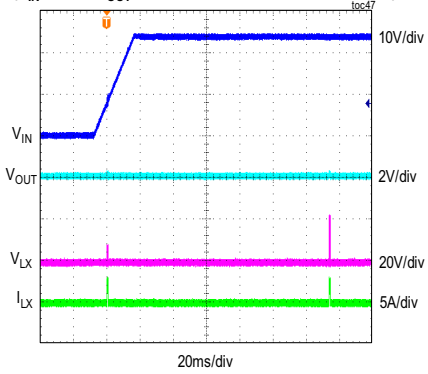
LV STARTUP THROUGH ENABLE, 0.8V PREBIAS
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PWM, LOAD = 10mA)



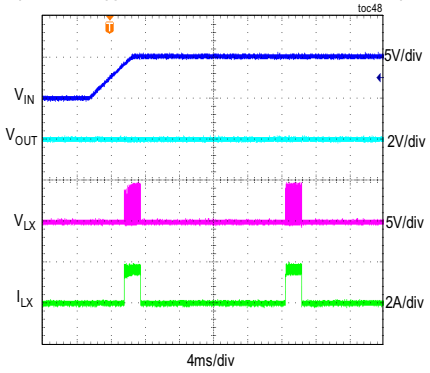
Typical Operating Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

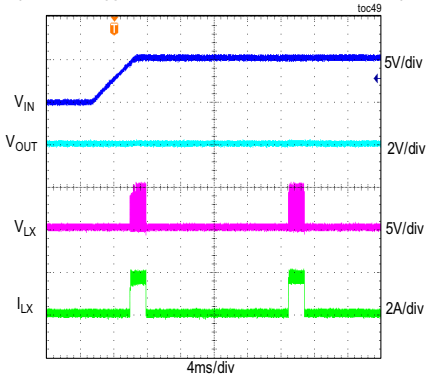
HV BUCK STARTUP WITH OUTPUT SHORT-CIRCUIT
(V_{IN} = 24V, V_{OUT} = 5V, MODE = PWM, LOAD = 1.5A)



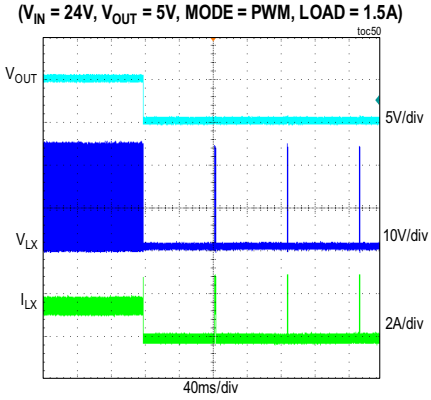
LV BUCK STARTUP WITH OUTPUT SHORT-CIRCUIT
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PWM, LOAD = 1.0A)



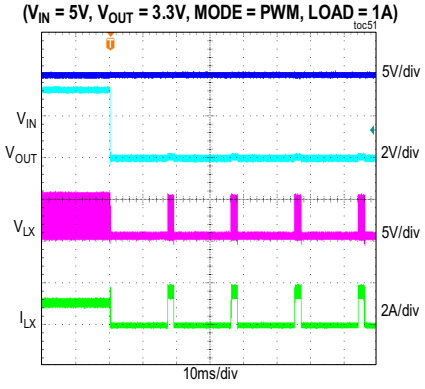
LV BUCK STARTUP WITH OUTPUT SHORT-CIRCUIT
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PWM, LOAD = 1.0A)



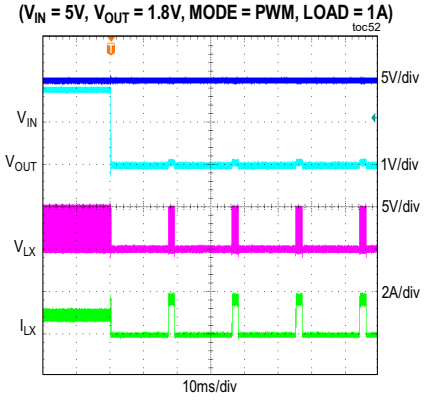
HV OUTPUT SHORT-CIRCUIT DURING STEADY-STATE
(V_{IN} = 24V, V_{OUT} = 5V, MODE = PWM, LOAD = 1.5A)



LV OUTPUT SHORT-CIRCUIT DURING STEADY-STATE
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PWM, LOAD = 1A)



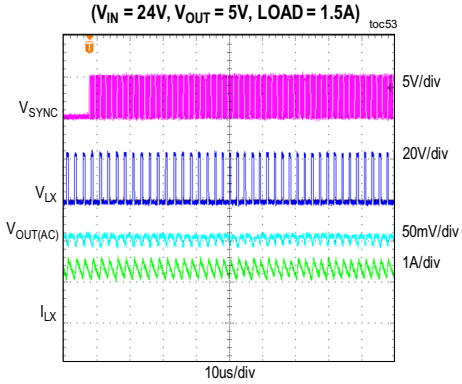
OUTPUT SHORT-CIRCUIT DURING STEADY-STATE
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PWM, LOAD = 1A)



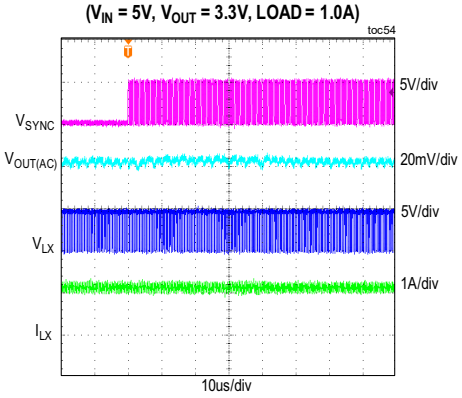
Typical Operating Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

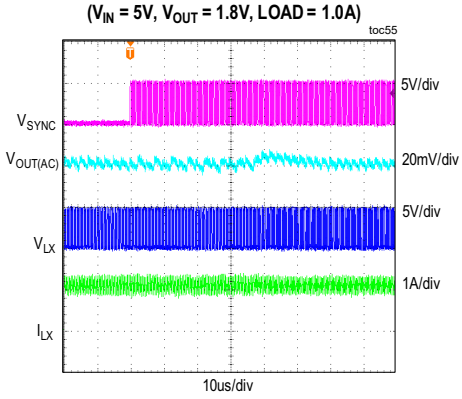
EXTERNAL CLOCK SYNCHRONIZATION
(V_{IN} = 24V, V_{OUT} = 5V, LOAD = 1.5A)



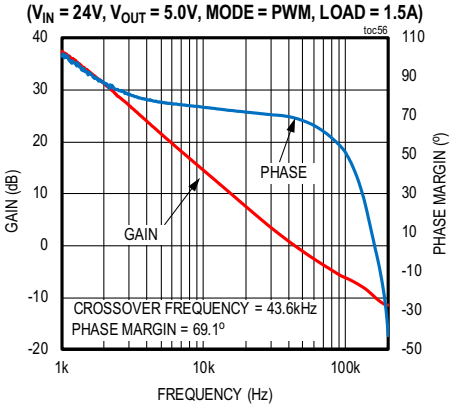
EXTERNAL CLOCK SYNCHRONIZATION
(V_{IN} = 5V, V_{OUT} = 3.3V, LOAD = 1.0A)



EXTERNAL CLOCK SYNCHRONIZATION
(V_{IN} = 5V, V_{OUT} = 1.8V, LOAD = 1.0A)



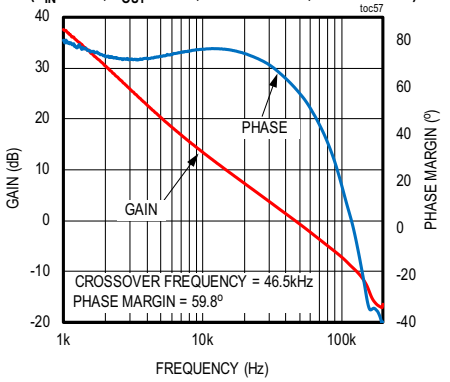
HV BUCK BODE PLOT
(V_{IN} = 24V, V_{OUT} = 5.0V, MODE = PWM, LOAD = 1.5A)



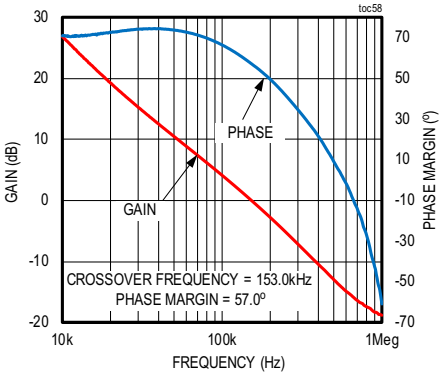
Typical Operating Characteristics (continued)

(V_{INH} = V_{ENH} = 24V, V_{GND} = V_{PGNDH} = V_{PGNDA} = V_{PGNDB} = FDIV = 0V, V_{INA} = V_{INB} = V_{ENA} = V_{ENB} = 5V, R_{RT} = OPEN, C_{VCC} = 2.2µF, C_{BSTH} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

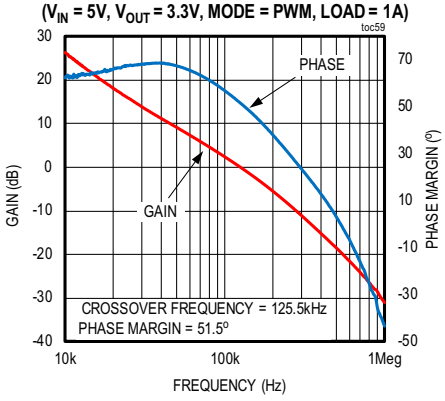
HV BUCK BODE PLOT
(V_{IN} = 24V, V_{OUT} = 3.3V, MODE = PWM, LOAD = 1.5A)



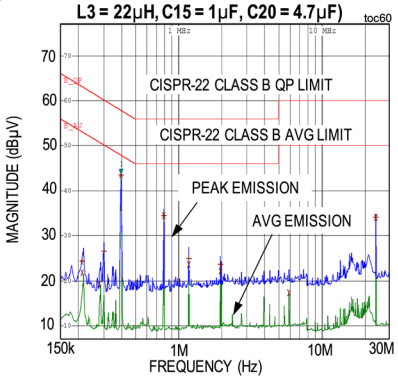
LV BUCK BODE PLOT
(V_{IN} = 5V, V_{OUT} = 1.8V, MODE = PWM, LOAD = 1A)



LV BUCK BODE PLOT
(V_{IN} = 5V, V_{OUT} = 3.3V, MODE = PWM, LOAD = 1A)

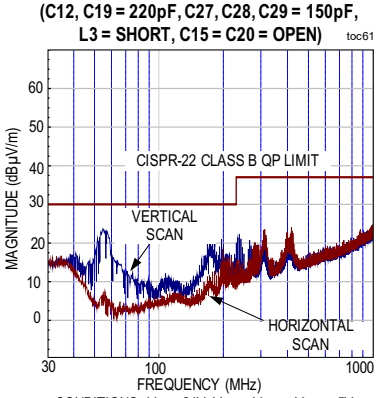


CONDUCTED EMISSION PLOT
(WITH FILTER: C12, C19 = 220pF, C27, C28, C29 = 150pF
L3 = 22µH, C15 = 1µF, C20 = 4.7µF)



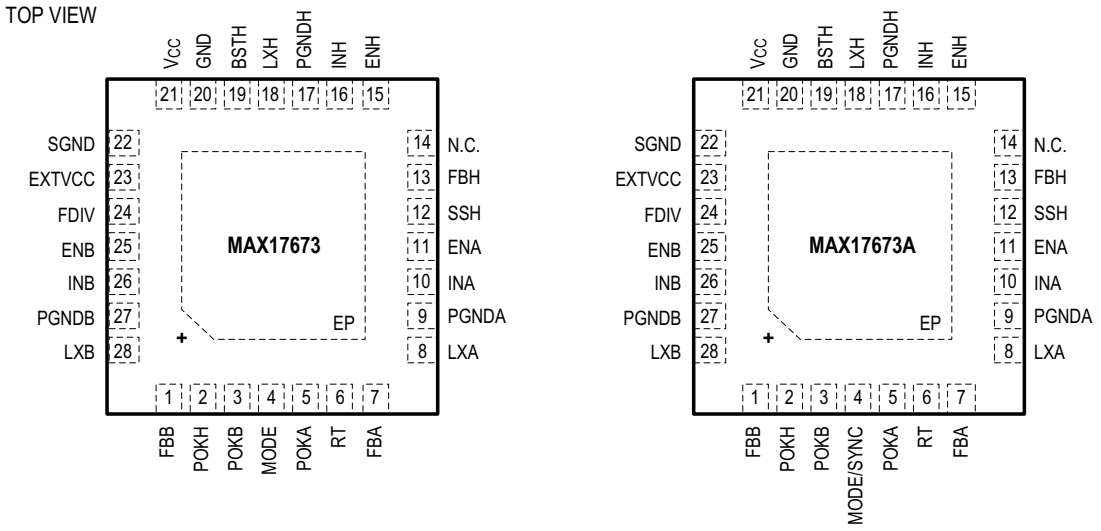
CONDITIONS: V_{IN} = 24V, V_{OH} = V_{INA} = V_{INB} = 5V, I_{OH} = 0.37A, I_{OA} = I_{OB} = 1A; FROM MAX17673AEVKIT#

RADIATED EMISSION PLOT
(C12, C19 = 220pF, C27, C28, C29 = 150pF,
L3 = SHORT, C15 = C20 = OPEN)



CONDITIONS: V_{IN} = 24V, V_{OH} = V_{INA} = V_{INB} = 5V, I_{OH} = 0.37A, I_{OA} = I_{OB} = 1A; FROM MAX17673AEVKIT#

Pin Configuration



TQFN
5mm x 5mm

TQFN
5mm x 5mm

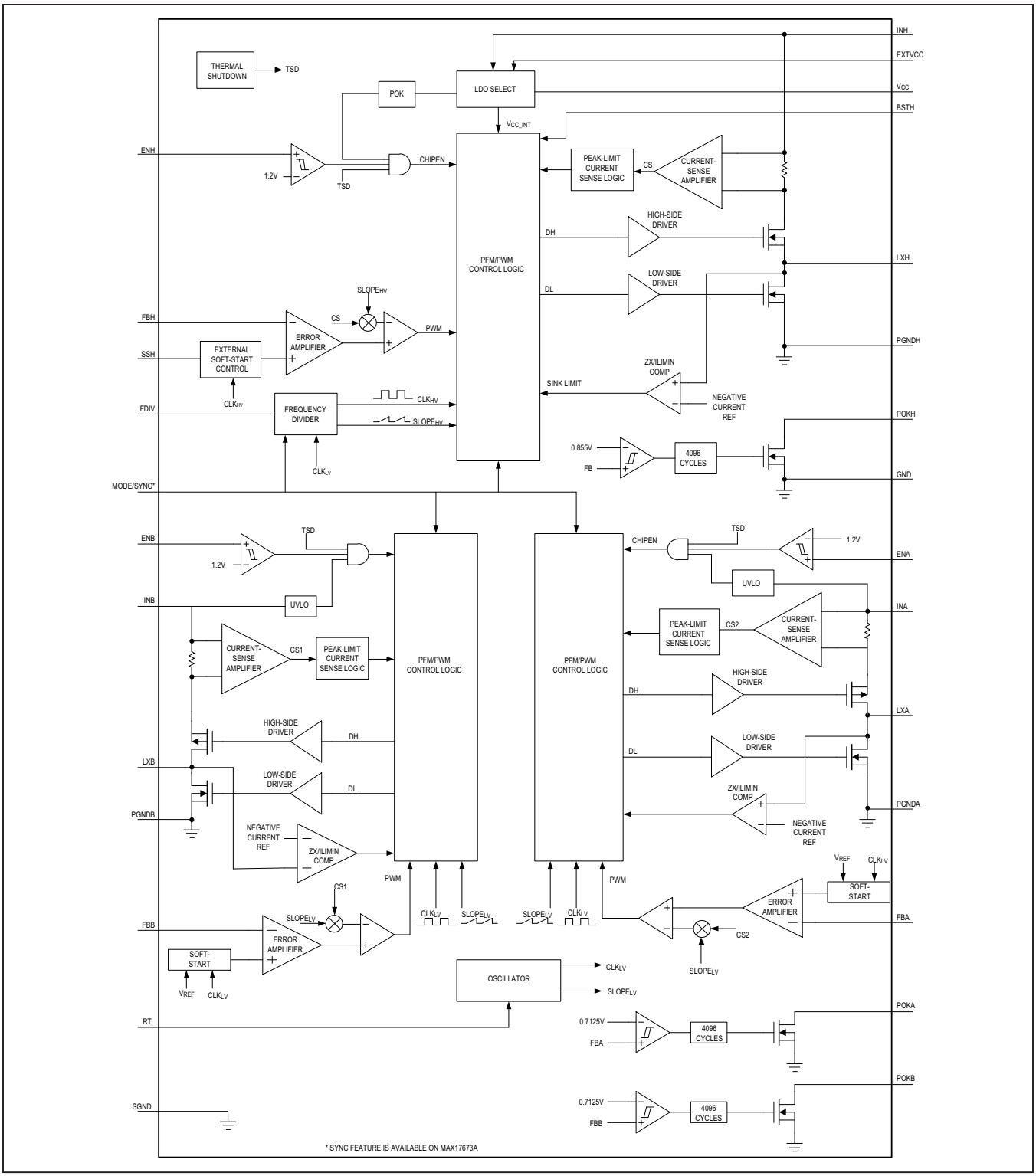
Pin Description

PIN	NAME	FUNCTION
1, 7	FBB, FBA	Feedback Inputs for LV Regulators. Connect FBA/FBB to the center of the external resistor-divider from the output of LV regulators to GND to set the output voltage.
2	POKH	Open-Drain Power Good to Monitor the Output of the HV Regulator. The POKH output is driven low if FBH drops below 92% of its set value. POKH goes high 2048 clock cycles after FBH rises above 95% of its set value. POKH is valid only if INH or EXTVCC is present.
3, 5	POKB, POKA	Open-Drain Power Good to Monitor the Output of the LV Regulators. The POKA/POKB output is driven low if FBA/FBB drops below 92% of its set value. POKA/POKB goes high 2048 clock cycles after FBA/FBB rises above 95% of its set value. POKA/POKB is valid only if INH or EXTVCC is present.
4	MODE /SYNC	Mode Selection Pin. The MODE/SYNC pin configures the devices to operate in PWM and PFM modes of operation. Leave the MODE/SYNC pin unconnected or connected to V_{CC} for PFM operation. Connect MODE/SYNC to SGND for constant-frequency PWM operation at all loads. MAX17673A can be synchronized to an external clock using this pin. See the *MODE Selection and External Clock Synchronization* section for more details.
6	RT	LV Regulator Switching Frequency Selection Input. Connect a resistor from RT to GND to program the LV regulator switching frequency from 1MHz to 4MHz.
8, 28	LXA, LXB	Switching Node of LV Regulators. Connect LXA and LXB pins to the switching node of the inductors. LXA and LXB are high impedance when the devices are in shutdown mode.
9, 27	PGNDA, PGNDB	Power Grounds for LV Regulators.
10, 26	INA, INB	Power Supply Input for LV Regulators. The input supply range is 2.7V to 5.5V.

Pin Description (continued)

PIN	NAME	FUNCTION
11, 25	ENA, ENB	LV Regulator Enable Input. Drive ENA/ENB high to enable the LV regulators output voltage.
12	SSH	Soft-Start Input for HV regulator. Connect a capacitor from SSH to GND to set the soft-start time.
13	FBH	Feedback Input for HV Regulator. Connect FBH to the center of the resistive divider between the HV regulator output voltage and GND.
14	N.C.	No Connection.
15	ENH	Enable Input. Drive ENH high to enable the HV regulator output voltage. Connect ENH to the center of a resistive divider between INH and GND to set the input voltage (undervoltage threshold) at which the devices turn on. Pull up to INH for always on operation.
16	INH	Power-Supply Input for the HV Regulator. The input supply range is from 4.5V to 60V.
17	PGNDH	Power Ground for the HV Regulator. Connect PGNDH externally to the power ground plane. Connect all GND and PGND pins together at one single point.
18	LXH	Switching Node of the HV Regulator. Connect LXH to the switching side of the inductor. LXH is high impedance when the devices are in shutdown mode.
19	BSTH	Bootstrap Capacitor for the HV Regulator. Connect a 0.1µF ceramic capacitor between BSTH and LXH.
20	GND	Analog Ground.
21	V_{CC}	Internal LDO Output. Bypass V_{CC} with 2.2µF ceramic capacitance to GND to enable proper operation. The internal regulator is turned on if ENH, ENA, or ENB is high.
22	SGND	Substrate Ground. Connect to GND.
23	EXTVCC	External Power Supply Input for the Internal LDO. Applying a voltage between 2.7V and 5.5V at the EXTVCC pin bypasses the internal LDO. If INH is present, EXTVCC is used only if it is above 3V (typ).
24	FDIV	HV Regulator Frequency Selection. Connect a resistor from FDIV to GND to select an LV/HV regulator frequency ratio (2, 3, 4, 5, 6, 7, 8). Pin read only at startup (first rise of ENH, ENA, or ENB).
—	EP	Exposed pad. Connect to the GND pin. Connect a large copper plane below the IC to improve heat dissipation capability. Add thermal vias below the exposed pad. Refer to the MAX17673/MAX17673A EV kit data sheet for a layout example.

Functional Diagram



Detailed Description

MAX17673/MAX17673A power management integrated circuits (PMIC) integrate a 60V high voltage (HV), high efficiency synchronous DC-DC buck regulator and two 5.5V Low Voltage (LV) high efficiency synchronous DC-DC buck regulators. All three regulators offer integrated MOSFETs.

The HV regulator and LV regulators are offered with independent input pins (INH, INA, and INB), ENABLE input pins (ENH, ENA, and ENB), switching nodes (LXH, LXA, and LXB pins), power ground pins (PGNDH, PGNDA, and PGNDB), and Power OK pins (POKH, POKA, and POKB). The controllers inside the devices are powered by linear regulators that generate the V_{CC} supply from the INH input or from the EXTVCC input. A valid INH or EXTVCC is required for operation of all the regulators.

The devices feature a peak current-mode control architecture. Output voltage regulation is achieved by sensing the output voltage through independent feedback pins (FBH, FBA, and FBB), comparing them against internal references, and setting the peak-current references for the independent peak current-mode control logic blocks. Stable operation is guaranteed by three independent internal error amplifiers with their compensation networks, and appropriate slope compensation in the peak current-mode controllers.

The RT pin offers adjustable switching frequency of the LV regulators. The FDIV pin allows selection of HV regulator switching frequency as a fraction of the LV regulators switching frequency. The MODE and MODE/SYNC pins allow selection of operating mode of the three regulators, between pulse width modulation (PWM) and pulse frequency modulation (PFM) modes. The MODE/SYNC pin on the MAX17673A can be used to synchronize the internal oscillator to an external system clock. The HV regulator offers a programmable soft-start function through the SSH pin, while the LV regulators offer an internally clocked soft-start function.

Linear Regulator and External Supply Input (EXTVCC)

The devices offer an internal low dropout (LDO) linear regulator, to power the internal functions by generating the V_{CC} Supply. The V_{CC} can be generated either from the INH supply, with an internal LDO or from the EXTVCC pin. The LDO are enabled only when at least one of the ENABLE inputs (ENH, ENA, or ENB) are asserted. The internal LDO uses INH when INH is above EXTVCC and EXTVCC is below the switchover threshold (3V). If INH is below EXTVCC, the LDO is disabled and EXTVCC is used to generate V_{CC}. A 2.2µF capacitor must be connected from the V_{CC} pin to GND for proper operation of the linear regulators. The linear regulators offer a current limit feature on the V_{CC} pin, and can handle a typical 54mA load current.

The output of the HV regulator may be applied to the EXTVCC pin, if it is above the switchover threshold. Powering the quiescent current through the EXTVCC input reduces the current drawn from the high voltage input INH, and hence reduces the losses in the INH LDO. When not used, the EXTVCC pin must be connected to GND.

Enabling the Regulators

The devices offer independent ENABLE pins for the three internal regulators. The HV regulator enable input (ENH) offers a programmable UVLO threshold. The LV ENABLE inputs (ENA and ENB) offer a digital logic threshold to enable or disable the regulators.

Switching Frequency Selection

The switching frequency of the LV regulators is set by the internal clock of the devices and can be set between 1MHz to 4MHz by connecting a resistor (R_{RT}) between the RT pin and GND. The switching frequency (f_{SW}) is related to the R_{RT} resistor by the following equation:

$$R_{RT} = (266/f_{SW_LV}) - 36.58$$

Where f_{SW_LV} is in MHz, and R_{RT} is in kΩ. The LV regulators are internally clocked 180° apart to minimize the ripple current drawn from the low voltage input source.

The switching frequency of the HV regulator is derived by dividing the LV regulator switching frequency by a programmable factor. The HV regulator switching frequency can be programmed by connecting a resistor (R_{FDIV}) between the FDIV pin and GND. This resistor is read only at startup. The following table lists the value of R_{FDIV} for different frequency division factors.

Table 1. Switching Frequency Selection for HV Regulator

FDIV RESISTOR (kΩ)	HV DIVIDING FACTOR (f_{SW_LV} / f_{SW_HV})
< 1.35	Internal RT (f_{SW_LV} = 2MHz, f_{SW_HV} = 400kHz
2.40	2
4.70	3
8.2	4
15	5
33	6
56	7
> 89	8

Operating Input Voltage

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_O + I_{OUT(MAX)}(R_{DCR} + R_{LS})}{D_{MAX}} + I_{OUT(MAX)}(R_{HS} - R_{LS})$$

$$V_{IN(MAX)} = \frac{V_O}{f_{SW(MAX)} \times t_{ON(MIN)}}$$

where,

V_O = Steady-state output voltage

$I_{OUT(MAX)}$ = Maximum load current

R_{DCR} = DC resistance of the inductor

$f_{SW(MAX)}$ = Maximum switching frequency

$t_{ON(MIN)}$ = Minimum switch on-time.

MODE Selection and External Clock Synchronization

The devices offer programmable PWM and PFM modes of operation. Connecting the MODE pin of MAX17673 or the MODE/SYNC pin of MAX17673A to GND operates the part in PWM operation. Connecting the MODE pin of MAX17673 or the MODE/SYNC pin of MAX17673A to V_{CC}, or leaving the pin open, enables the part to operate in PFM mode. The chosen operating mode applies to all the three regulators.

The MAX17673A offers external clock synchronization. The internal oscillator of the device can be synchronized to an external clock signal applied on the MODE/SYNC pin. The external synchronization frequency must be between 0.9 x f_{SW_LV} and 1.1 x f_{SW_LV}. Where f_{SW_LV} is the LV buck frequency programmed by the RT resistor. The MAX17673A operates in PWM mode when synchronized to an external clock.

The MAX17673A highlights a phase-locked-loop (PLL) clock generator that allows seamless on-the-fly synchronization to external clocks. The user must apply a valid clock frequency for at least "t_{min_sync}" time:

$$t_{min_sync} = 1024/f_{sw_LV} + 90us$$

Where, f_{SW_LV} = LV buck frequency in Hz.

PWM

Pulse width modulation (PWM) mode operation provides constant switching frequency at all load conditions, and is useful in frequency sensitive applications. In PWM mode, the inductor current is allowed to go negative, and hence remains continuous. PWM mode results in lower efficiency at light loads, compared to PFM mode.

PFM

Pulse frequency modulation (PFM) mode operation disables the negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 820mA for HV buck and 540mA for LV bucks, every clock cycle until the output rises to the PFM skip threshold (i.e., 102.75% typ for HV buck and 102.5% typ for LV bucks) of the nominal voltage. Once the output reaches the PFM skip threshold of the nominal voltage, both the high-side and low-side FETs are turned off and the devices enter hibernate operation until the load current discharges the output voltage to the PFM resume threshold (i.e., 101% typ for HV buck and 101.7% typ for LV Buck) of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the outputs fall below the PFM resume threshold of the nominal voltage, the devices come out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches the PFM skip threshold of the nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The disadvantage is that the output-voltage ripple is higher compared to PWM modes of operation and switching frequency is not constant at light loads.

Power Good Signal (POK)

The devices offer individual power good signals (POKH, POKA, and POKB) for the three internal regulators. The POK_ pins are open-drain output pins. The POK_ pins must be pulled up to the desired logic level voltages externally. The power good signals are driven high when the output voltage of the regulators reach 95% (typ) of the set values after soft-start is completed. The power good signals are pulled low during the soft-start period, and under fault conditions (thermal shutdown, or any of the corresponding ENABLE inputs are held low).

Overcurrent and Hiccup Mode

The devices are provided with a robust overcurrent protection scheme that protects the devices during overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 2.7A (typ) for HV buck and 1.7A (typ) for LV bucks. In addition, if due to a fault condition, feedback voltage (at FBH, FBA, or FBB pins) drops to 64% of the typical feedback voltage of the regulated value any time after soft-start is complete, hiccup mode is triggered. In hiccup mode, the converters are protected by suspending switching for a hiccup timeout period of 32,768 switching cycles. Once the hiccup timeout period expires, soft-start is attempted again. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions. The overcurrent and hiccup mode operation for the HV regulator and LV regulators work independent of each other.

Prebiased Output

When the devices start into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the devices. When the junction temperature of the devices exceeds +165°C, an on-chip thermal sensor shuts down the devices, allowing the devices to cool. The thermal sensor is common to all three regulators. The thermal sensor turns the devices on again after the junction temperature cools by 20°C. All three regulator soft-start cycle resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown during normal operation.

Applications Information

Input Capacitor Selection

The devices offer independent input terminals for the three internal regulators. Input capacitors must be placed near each of these input terminals (INH, INA, and INB) to reduce the peak currents drawn from the input power source, and to reduce the noise and voltage ripple on the input terminals. The input capacitor RMS current requirement (I_{RMS}) is calculated using following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{(V_{IN} - V_{OUT}) \times V_{OUT}}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with

high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where,

$D = V_{OUT}/V_{IN}$ is the duty ratio of the controller

f_{SW} = Switching frequency

ΔV_{IN} = Allowable input voltage ripple

η = efficiency

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

The inductors for the three regulators must be specified for operation with the MAX17673/MAX17673A. The switching frequency and output voltage determine the inductance value as follows

$$L = \frac{1.5 \times V_{OUT}}{f_{SW}}$$

where f_{SW} is in Hertz. Select low DC resistance (DCR) inductors close to the calculated values. The saturation current rating (I_{SAT}) of the inductor must be above the peak current limit of the regulator.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are typically sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to 3% of the output voltage setpoint. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$t_{RESPONSE} = \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where,

C_{OUT} is in Farad

I_{STEP} = Load current step

$t_{RESPONSE}$ = Response time of the controller

ΔV_{OUT} = Allowable output voltage deviation

f_C = Target closed-loop crossover frequency in Hz

f_{SW} = Switching frequency in Hz

Select f_C to be 1/10th of the switching frequency.

DC and AC bias derating characteristics of ceramic capacitors must be considered while selecting output capacitors. Derating curves are available from all major ceramic capacitor manufacturers.

Soft-Start Capacitor Selection

The devices implement adjustable soft-start operation for the HV regulator and fixed soft-start time for the LV regulators to reduce inrush current. A capacitor connected from the SSH pin to GND programs the soft-start time for the HV regulator. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 56 \times 10^{-06} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-06}}$$

For example, to program a 2ms soft-start time, a 12nF capacitor should be connected from the SSH pin to GND.

Setting the Input Undervoltage Lockout Level of the HV Regulator

The devices offer an adjustable input undervoltage lockout level for the HV regulator. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{INH} to GND (Figure 1). Connect the center node of the divider to the ENH pin.

Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.2}{(V_{INU} - 1.2)}$$

where, V_{INU} is the voltage at which the device must turns on. Ensure that V_{INU} is higher than 0.8 x V_{OUT}.

To reduce voltage ringing, a minimum damping resistance of 1kΩ should be placed in series with the ENH pin, when driven from an external signal source.

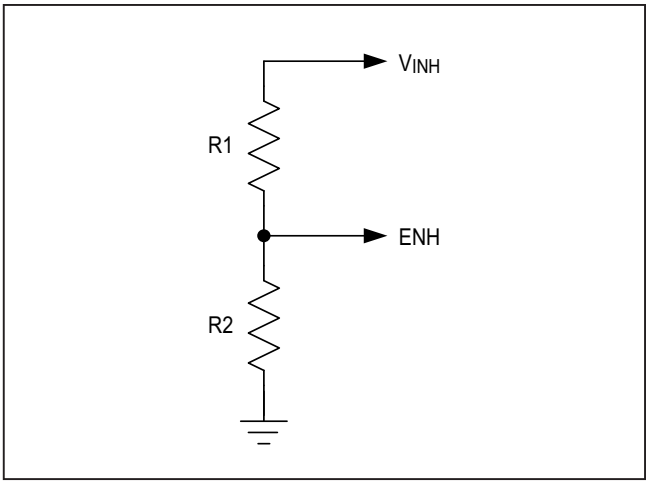


Figure 1. Setting the Input Undervoltage Lockout Level for the HV Regulator

Adjusting Output Voltage

The devices offer independent control of output voltages, by allowing individual sense and feedback inputs. Set the output voltage of the three regulators by using a resistive divider from the output voltages to the respective feedback (FB_) pins (Figure 2). Use the following expressions to choose the resistive divider values.

For the HV regulator:

$$R_U = 2165/(C_{OUT} \times f_{SW_HV})$$

$$R_B = \frac{R_U \times 0.9}{(V_{OUT} - 0.9)}$$

For LV regulators:

$$R_U = (721.5/(f_{SW_LV} \times C_{OUT})) - (8.7 \times V_{OUT})$$

$$R_B = \frac{R_U \times 0.75}{(V_{OUT} - 0.75)}$$

where V_{OUT} is in V, R_U and R_B are in kΩ, C_{OUT} is in µF, f_{SW_HV} and f_{SW_LV} are in MHz.

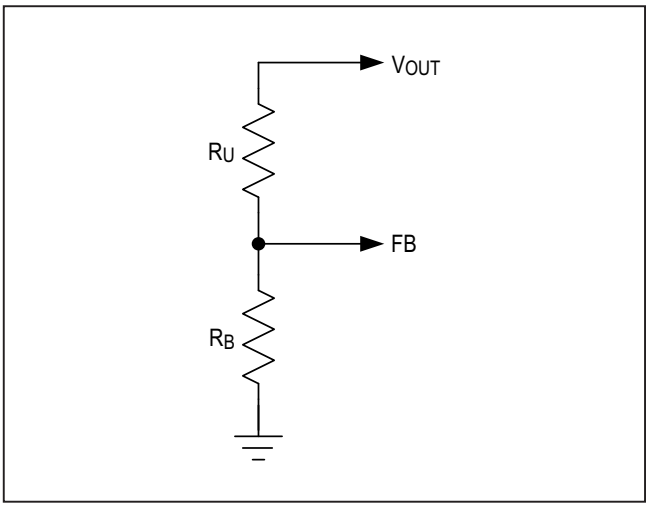


Figure 2. Setting the Output Voltage

Power Dissipation

The power dissipation inside the chip leads to an increase in the junction temperature of the MAX17673/MAX17673A. At a given operating condition, ensure that the junction temperature of the devices do not exceed +125°C. The power loss from the IC at full load can be calculated as follows:

$$P_{ICLOSS} = I^2_{OH} \quad [[D \times 120m] + 170m]$$

$$+f_{SW_HV}\left[28.515n + \left[V_{INH} \times I_{OH} \times 9n\right]\right]$$

$$+60m\left(I^2_{OA} \times D_A + I^2_{OB} \times D_B\right) + 60m\left(I^2_{OA} + I^2_{OB}\right)$$

$$+f_{SW_LV}\left[24.41n + 4n\left[V_{INA} \times I_{OA} + V_{INB} \times I_{OB}\right]\right]$$

where,

D, D_A, and D_B = Duty cycle of the HV, LVA, and LVB regulators, respectively

f_{SW_HV} and f_{SW_LV} = HV buck and LV buck switching frequencies

I_{OH}, I_{OA}, and I_{OB} = Output currents of the HV buck, LVA, and LVB buck converter.

For more information regarding power losses at different load current, switching frequency, output voltage, and input voltage refer to EE-sim model of the MAX17673/MAX17673A.

For a typical multilayer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 29°C/W$$

$$\theta_{JC} = 2°C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + \left(\theta_{JA} \times P_{ICLOSS}\right)$$

If the application has a thermal-management system that ensures that the exposed pad of the devices are maintained at a given temperature (T_{EP}) by using proper heat sinks, the junction temperature of the device can be estimated as:

$$T_{J(MAX)} = T_{EP} + \left(\theta_{JC} \times P_{ICLOSS}\right)$$

Junction temperatures greater than +125°C degrade operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

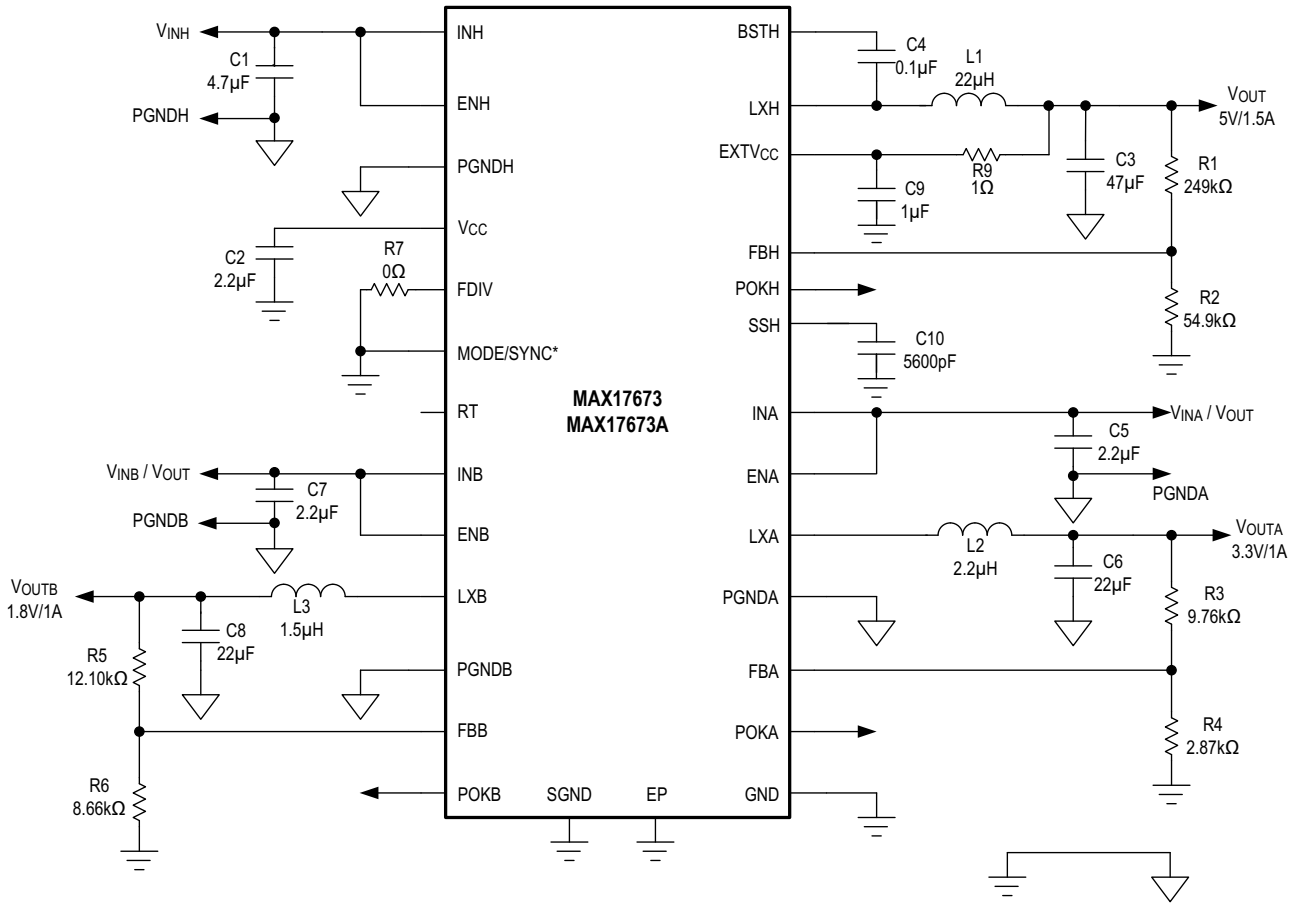
A ceramic input filter capacitor should be placed close to the IN_ pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum, typically the return terminal of the V_{CC} bypass capacitor. This helps to keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17673/MAX17673A evaluation kits layout available at **www.maximintegrated.com**.

Typical Application Circuit



* THE SYNC FEATURE IS AVAILABLE ON MAX17673A

f_{SW_HV} = 400kHz, f_{SW_LV} = 2MHz
L1: XAL6060 223ME
C3: GRM32ER71A476KE15
L2: IHHP1008ABER2R2M01
C6,C8: GRM21BZ70J226ME44
L3: IHHP1008ABER1R5M01

Ordering Information

PART	PIN-PACKAGE	PACKAGE SIZE	FUNCTIONALITY
MAX17673ATI+	28 TQFN	5mm x 5mm	—
MAX17673AATI+	28 TQFN	5mm x 5mm	SYNC Feature

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/18	Initial release	—
1	10/19	Updated the title, and the *General Description, Benefits and Features, Electrial Characteristics, Typical Operating Characteristics, Pin Configuration* and *Pin Description, Functional Diagram, Detailed Description, Operating Input Voltage, PFM, Power Dissipation, Typical Application Circuit* section, and added MAX17673AATI+ to the *Ordering Information*	1–22
2	11/19	Updated TOC60 and TOC61, *MODE Selection and External Clock Synchronization* section, and *Typical Application Circuit*; corrected typo	16, 21, 26

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