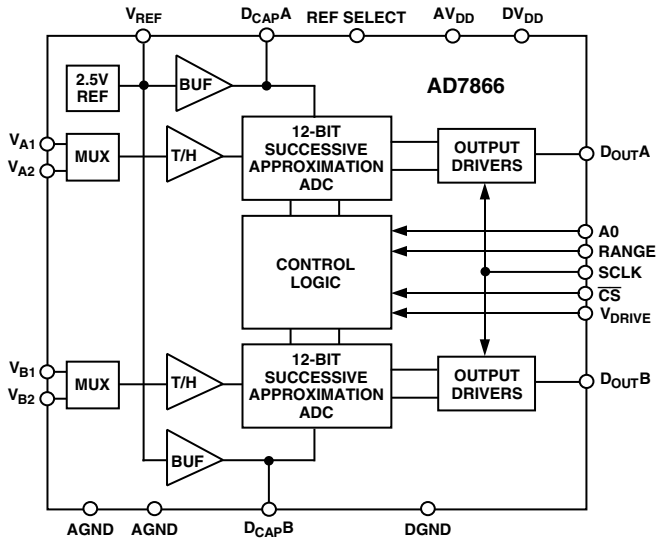
Dual 1 MSPS, 12-Bit, 2-Channel SAR ADC with Serial Interface

AD7866

FEATURES

Dual 12-Bit, 2-Channel ADC
Fast Throughput Rate: 1 MSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low Power
11.4 mW Max at 1 MSPS with 3 V Supplies
24 mW Max at 1 MSPS with 5 V Supplies
Wide Input Bandwidth
70 dB SNR at 300 kHz Input Frequency
On-Board Reference 2.5 V
–40°C to +125°C Operation
Flexible Power/Throughput Rate Management
Simultaneous Conversion/Read
No Pipeline Delays
High Speed Serial Interface SPI™/QSPI™/ MICROWIRE™/DSP Compatible
Shutdown Mode: 1 μA Max
20-Lead TSSOP Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7866 is a dual 12-bit high speed, low power, successive approximation ADC. The part operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 1 MSPS. The device contains two ADCs, each preceded by a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 10 MHz.

The conversion process and data acquisition are controlled using standard control inputs, allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$; conversion is also initiated at this point. The conversion time is determined by the SCLK frequency. There are no pipelined delays associated with the part.

The AD7866 uses advanced design techniques to achieve very low power dissipation at high throughput rates. With 3 V supplies and 1 MSPS throughput rate, the part consumes a maximum of 3.8 mA. With 5 V supplies and 1 MSPS, the current consumption is a maximum of 4.8 mA. The part also offers flexible power/throughput rate management when operating in sleep mode.

The analog input range for the part can be selected to be a 0 V to V_{REF} range or a 2 × V_{REF} range with either straight binary or twos complement output coding. The AD7866 has an on-chip 2.5 V reference that can be overdriven if an external reference is preferred. Each on-board ADC can also be supplied with a separate individual external reference.

The AD7866 is available in a 20-lead thin shrink small outline (TSSOP) package.

PRODUCT HIGHLIGHTS

1. The AD7866 features two complete ADC functions, allowing simultaneous sampling and conversion of two channels. Each ADC has a 2-channel input multiplexer. The conversion result of both channels is available simultaneously on separate data lines, or may be taken on one data line if only one serial port is available.
2. High Throughput with Low Power Consumption—The AD7866 offers a 1 MSPS throughput rate with 11.4 mW maximum power consumption when operating at 3 V.
3. Flexible Power/Throughput Rate Management—The conversion rate is determined by the serial clock, allowing the power consumption to be reduced as the conversion time is reduced through a SCLK frequency increase. Power efficiency can be maximized at lower throughput rates if the part enters sleep during conversions.
4. No Pipeline Delay—The part features two standard successive approximation ADCs with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

REV. A

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AD7866–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, Reference = 2.5 V External on $D_{CAP}A$ and $D_{CAP}B$, f_{SCLK} = 20 MHz, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion (SINAD)[2]	68	68	dB min	f_{IN} = 300 kHz Sine Wave, f_S = 1 MSPS
Total Harmonic Distortion (THD)[2]	–75	–75	dB max	f_{IN} = 300 kHz Sine Wave, f_S = 1 MSPS
Peak Harmonic or Spurious Noise (SFDR)[2]	–76	–76	dB max	f_{IN} = 300 kHz Sine Wave, f_S = 1 MSPS
Intermodulation Distortion (IMD)[2]				
Second Order Terms	–88	–88	dB typ	
Third Order Terms	–88	–88	dB typ	
Channel-to-Channel Isolation	–88	–88	dB typ	
SAMPLE AND HOLD				
Aperture Delay[3]	10	10	ns max	
Aperture Jitter[3]	50	50	ps typ	
Aperture Delay Matching[3]	200	200	ps max	
Full Power Bandwidth	12	12	MHz typ	@ 3 dB
	2	2	MHz typ	@ 0.1 dB
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±1.5	±1	LSB max	B Grade, 0 V to V_{REF} Range Only; ±0.5 LSB typ
		±1.5	LSB max	0 V to 2 × V_{REF} Range; ±0.5 LSB typ
Differential Nonlinearity	–0.95/+1.25	–0.95/+1.25	LSB max	Guaranteed No Missed Codes to 12 Bits
0 V to V_{REF} Input Range				Straight Binary Output Coding
Offset Error	±8	±8	LSB max	
Offset Error Match	±1.2	±1.2	LSB typ	
Gain Error	±2.5	±2.5	LSB max	
Gain Error Match	±0.2	±0.2	LSB typ	
2 × V_{REF} Input Range				–V_{REF} to +V_{REF} Biased about V_{REF} with
Positive Gain Error	±2.5	±2.5	LSB max	Twos Complement Output Coding
Zero Code Error	±8	±8	LSB max	
Zero Code Error Match	±0.2	±0.2	LSB typ	
Negative Gain Error	±2.5	±2.5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	V	RANGE Pin Low upon $\overline{CS}$ Falling Edge
	0 to 2 × V_{REF}	0 to 2 × V_{REF}	V	RANGE Pin High upon $\overline{CS}$ Falling Edge
DC Leakage Current	±500	±500	nA max	T_A = –40°C to +85°C
	1	1	µA max	85°C < T_A ≤ 125°C
Input Capacitance	30	30	pF typ	When in Track
	10	10	pF typ	When in Hold
REFERENCE INPUT/OUTPUT				
Reference Input Voltage	2.5	2.5	V	±1% for Specified Performance
Reference Input Voltage Range[4]	2/3	2/3	V min/V max	REF SELECT Pin Tied High
DC Leakage Current	±30	±30	µA max	V_{REF} Pin
	±160	±160	µA max	$D_{CAP}A$, $D_{CAP}B$ Pins
Input Capacitance	20	20	pF typ	
Reference Output Voltage[5]	2.45/2.55	2.45/2.55	V min/V max	
V_{REF} Output Impedance[6]	25	25	Ω typ	V_{DD} = 5 V
	45	45	Ω typ	V_{DD} = 3 V
Reference Temperature Coefficient	50	50	ppm/°C typ	
REF OUT Error (T_{MIN} to T_{MAX})	±15	±15	mV typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	0.7 V_{DRIVE}	0.7 V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 V_{DRIVE}	0.3 V_{DRIVE}	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 15 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V_{DRIVE} – 0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	±1	µA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance[3]	10	10	pF max	
Output Coding	Straight (Natural) Binary Twos Complement			Selectable with Either Input Range

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
CONVERSION RATE				
Conversion Time	16	16	SCLK cycles	800 ns with SCLK = 20 MHz
Track/Hold Acquisition Time[3]	300	300	ns max	
Throughput Rate	1	1	MSPS max	See Serial Interface Section
POWER REQUIREMENTS				
V_{DD}	2.7/5.25	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	2.7/5.25	V min/max	
I_{DD}[7]				Digital I/Ps = 0 V or V_{DRIVE}
Normal Mode (Static)	3.1	3.1	mA max	V_{DD} = 4.75 V to 5.25 V. Add 0.5 mA Typical if Using Internal Reference.
	2.8	2.8	mA max	V_{DD} = 2.7 V to 3.6 V. Add 0.35 mA Typical if Using Internal Reference.
Operational, f_S = 1 MSPS	4.8	4.8	mA max	V_{DD} = 4.75 V to 5.25 V. Add 0.5 mA Typical if Using Internal Reference.
	3.8	3.8	mA max	V_{DD} = 2.7 V to 3.6 V. Add 0.5 mA Typical if Using Internal Reference.
Partial Power-Down Mode	1.6	1.6	mA max	f_S = 100 kSPS, f_{SCLK} = 20 MHz Add 0.2 mA Typ if Using Internal Reference.
Partial Power-Down Mode	560	560	μA max	(Static) Add 100 μA Typical if Using Internal Reference.
Full Power-Down Mode	1	1	μA max	SCLK On or Off. T_A = –40°C to +85°C
	2	2	μA max	SCLK On or Off. 85°C < T_A ≤ 125°C
Power Dissipation[7]				
Normal Mode (Operational)	24	24	mW max	V_{DD} = 5 V
	11.4	11.4	mW max	V_{DD} = 3 V
Partial Power-Down (Static)	2.8	2.8	mW max	V_{DD} = 5 V. SCLK On or Off.
	1.68	1.68	mW max	V_{DD} = 3 V. SCLK On or Off.
Full Power-Down (Static)	5	5	μW max	V_{DD} = 5 V. SCLK On or Off.
	3	3	μW max	V_{DD} = 3 V. SCLK On or Off.

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +125°C.
[2]See Terminology section.
[3]Sample tested @ 25°C to ensure compliance.
[4]External reference range that may be applied at V_{REF}, $D_{CAP}A$, or $D_{CAP}B$.
[5]Relates to pins V_{REF}, $D_{CAP}A$, or $D_{CAP}B$.
[6]See Reference section for $D_{CAP}A$, $D_{CAP}B$ output impedances.
[7]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, V_{REF} = 2.5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK} [2]	10	kHz min	
	20	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	ns max	t_{SCLK} = 1/f_{SCLK}
	800	ns max	f_{SCLK} = 20 MHz
t_{QUIET}	50	ns max	Minimum Time between End of Serial Read and Next Falling Edge of $\overline{CS}$
t_2	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3[3]	25	ns max	Delay from $\overline{CS}$ until $D_{OUT}A$ and $D_{OUT}B$ Three-State Disabled
t_4[3]	40	ns max	Data Access Time after SCLK Falling Edge. $V_{DRIVE} \geq 3$ V, C_L = 50 pF; $V_{DRIVE} < 3$ V, C_L = 25 pF
t_5	0.4 t_{SCLK}	ns min	SCLK Low Pulsewidth
t_6	0.4 t_{SCLK}	ns min	SCLK High Pulsewidth
t_7	10	ns min	SCLK to Data Valid Hold Time
t_8[4]	25	ns max	$\overline{CS}$ Rising Edge to $D_{OUT}A$, $D_{OUT}B$, High Impedance
t_9[4]	10	ns min	SCLK Falling Edge to $D_{OUT}A$, $D_{OUT}B$, High Impedance
	50	ns max	SCLK Falling Edge to $D_{OUT}A$, $D_{OUT}B$, High Impedance

NOTES

[1]Sample tested at 25°C to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V.

[2]Mark/Space ratio for the CLK input is 40/60 to 60/40.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[4]$t_{8,}$ t_9 are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times t_8 and t_9 quoted in the timing characteristics are the true bus relinquish times of the part and are independent of the bus loading.

Specifications subject to change without notice.

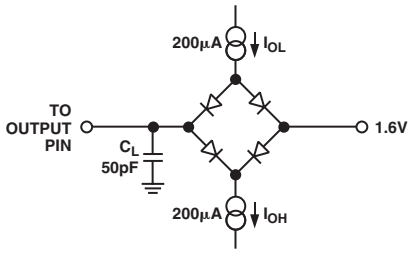


Figure 1. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

AV_{DD} to AGND . . . . . –0.3 V to +7 V
DV_{DD} to DGND . . . . . –0.3 V to +7 V
V_{DRIVE} to DGND . . . . . –0.3 V to DV_{DD} + 0.3 V
V_{DRIVE} to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
AV_{DD} to DV_{DD} . . . . . –0.3 V to +0.3 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Analog Input Voltage to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V to +7 V
V_{REF} to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND . . . –0.3 V to V_{DRIVE} + 0.3 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
Commercial (A, B Versions) . . . . . –40°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
TSSOP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance (TSSOP) . . . . . 143°C/W
θ_{JC} Thermal Impedance (TSSOP) . . . . . 45°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C
ESD . . . . . 1.5 kV

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Temperature Range	Resolution (Bits)	Package Description	Package Option
AD7866ARU	–40°C to +125°C	12	Thin Shrink SOC (TSSOP)	RU-20
AD7866BRU	–40°C to +125°C	12	Thin Shrink SOC (TSSOP)	RU-20
EVAL-AD7866CB[1]			Evaluation Board	
EVAL-CONTROL BRD2[2]			Controller Board	

NOTES

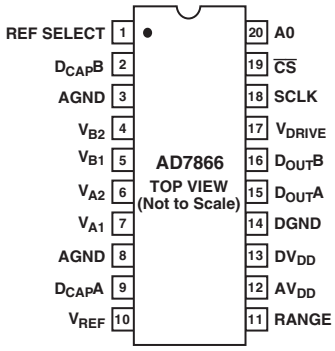
[1]This can be used as a standalone evaluation board or in conjunction with the evaluation board controller for evaluation/demonstration purposes.

[2]This evaluation board controller is a complete unit, allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB design ators. To order a complete evaluation kit, the particular ADC evaluation board, e.g., EVAL-AD7866CB, the EVAL-CONTROL BRD2, and a 12 V transformer must be ordered. See relevant Evaluation Board Technical note for more information.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7866 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	REF SELECT	Internal/External Reference Selection. Logic input. If this pin is tied to GND, the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. In addition, pins V_{REF}, $D_{CAP}A$, and $D_{CAP}B$ must be tied to decoupling capacitors. If the REF SELECT pin is tied to a logic high, an external reference can be supplied to the AD7866 through the V_{REF} pin, in which case decoupling capacitors are required on $D_{CAP}A$ and $D_{CAP}B$. However, if the V_{REF} pin is tied to AGND while REF SELECT is tied to a logic low, an individual external reference can be applied to both ADC A and ADC B through pins $D_{CAP}A$ and $D_{CAP}B$, respectively. See the Reference Configuration Options section.
2, 9	$D_{CAP}B$, $D_{CAP}A$	Decoupling capacitors are connected to these pins to decouple the reference buffer for each respective ADC. The on-chip reference can be taken from these pins and applied externally to the rest of a system. Depending on the polarity of the REF SELECT pin and the configuration of the V_{REF} pin, these pins can also be used to input a separate external reference to each ADC. The range of the external reference is dependent on the analog input range selected. See the Reference Configuration Options section.
3, 8	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7866. All analog input signals and any external reference signal should be referred to this AGND voltage. Both of these pins should connect to the AGND plane of a system. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
4, 5	V_{B2}, V_{B1}	Analog Inputs of ADC B. Single-ended analog input channels. The input range on each channel is 0 V to V_{REF} or a 2 × V_{REF} range depending on the polarity of the RANGE pin upon the falling edge of $\overline{CS}$.
6, 7	V_{A2}, V_{A1}	Analog Inputs of ADC A. Single-ended analog input channels. The input range on each channel is 0 V to V_{REF} or a 2 × V_{REF} range depending on the polarity of the RANGE pin upon the falling edge of $\overline{CS}$.
10	V_{REF}	Reference Decoupling and External Reference Selection. This pin is connected to the internal reference and requires a decoupling capacitor. The nominal reference voltage is 2.5 V, which appears at the pin; however, if the internal reference is to be used externally in a system, it must be taken from either the $D_{CAP}A$ or $D_{CAP}B$ pins. This pin is also used in conjunction with the REF SELECT pin when applying an external reference to the AD7866. See the REF SELECT pin description.

PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Function
11	RANGE	Analog Input Range and Output Coding Selection. Logic input. The polarity on this pin will determine what input range the analog input channels on the AD7866 will have, and will also select the type of output coding the ADC will use for the conversion result. On the falling edge of $\overline{CS}$, the polarity of this pin is checked to determine the analog input range of the next conversion. If this pin is tied to a logic low, the analog input range is 0 V to V_{REF} and the output coding from the part will be straight binary (for the next conversion). If this pin is tied to a logic high when $\overline{CS}$ goes low, the analog input range is $2 \times V_{REF}$ and the output coding for the part will be twos complement. However, if after the falling edge of $\overline{CS}$ the logic level of the RANGE pin has changed upon the eighth SCLK falling edge, the output coding will change to the other option without any change in the analog input range. (See the Analog Input and ADC Transfer Function sections.)
12	AV_{DD}	Analog Supply Voltage, 2.7 V to 5.25 V. This is the only supply voltage for all analog circuitry on the AD7866. The AV_{DD} and DV_{DD} voltages ideally should be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to AGND.
13	DV_{DD}	Digital Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD7866. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND.
14	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7866. The DGND and AGND voltages ideally should be at the same potential and must not be more than 0.3 V apart even on a transient basis.
15, 16	$D_{OUT}A$, $D_{OUT}B$	Serial Data Outputs. The data output is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data appears on both pins simultaneously from the simultaneous conversions of both ADCs. The data stream consists of one leading zero followed by three STATUS bits, followed by the 12 bits of conversion data. The data is provided MSB first. If $\overline{CS}$ is held low for another 16 SCLK cycles after the conversion data has been output on either $D_{OUT}A$ or $D_{OUT}B$, the data from the other ADC follows on the D_{OUT} pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either $D_{OUT}A$ or $D_{OUT}B$ alone using only one serial port. See the Serial Interface section.
17	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface will operate. This pin should be decoupled to DGND.
18	SCLK	Serial Clock. Logic Input. A serial clock input provides the SCLK for accessing the data from the AD7866. This clock is also used as the clock source for the conversion process.
19	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7866 and frames the serial data transfer.
20	A0	Multiplexer Select. Logic input. This input is used to select the pair of channels to be converted simultaneously, i.e., Channel 1 of both ADC A and ADC B, or Channel 2 of both ADC A and ADC B. The logic state of this pin is checked upon the falling edge of $\overline{CS}$, and the multiplexer is set up for the *next* conversion. If it is low, the following conversion will be performed on Channel 1 of each ADC; if it is high, the following conversion will be performed on Channel 2 of each ADC.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This applies to Straight Binary output coding. It is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Offset Error Match
This is the difference in Offset Error between the two channels.

Gain Error
This applies to Straight Binary output coding. It is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in Gain Error between the two channels.

Zero Code Error
This applies when using the twos complement output coding option, in particular with the 2 × V_{REF} input range as –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, i.e., V_{REF} – 1 LSB.

Zero Code Error Match
This refers to the difference in Zero Code Error between the two channels.

Positive Gain Error
This applies when using the twos complement output coding option, in particular with the 2 × V_{REF} input range as –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the last code transition (011 . . . 110) to (011 . . . 111) from the ideal (i.e., +V_{REF} – 1 LSB) after the Zero Code Error has been adjusted out.

Negative Gain Error
This applies when using the twos complement output coding option, in particular with the 2 × V_{REF} input range as –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the first code transition (100 . . . 000) to (100 . . . 001) from the ideal (i.e., –V_{REF} + 1 LSB) after the Zero Code Error has been adjusted out.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns into track mode after the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal-to-(Noise + Distortion) Ratio (SNDR)
This is the measured ratio of signal-to-(noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7866, it is defined as:

$$THD(db) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic, or spurious noise, is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum. But for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb).

The AD7866 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale (2 × V_{REF}), 455 kHz sine wave signal to all unselected input channels and determining how much that signal is attenuated in the selected channel with a 10 kHz signal (0 V to V_{REF}). The figure given is the worst-case across all four channels for the AD7866.

PSR (Power Supply Rejection)
See the Performance Curves section.

PERFORMANCE CURVES

TPC 1 shows a typical FFT plot for the AD7866 at 1 MHz sample rate and 300 kHz input frequency. TPC 2 shows the signal-to-(noise + distortion) ratio performance versus input frequency for various supply voltages while sampling at 1 MSPS with an SCLK of 20 MHz.

TPCs 3a to 4b show the power supply rejection ratio versus AV_{DD} supply ripple frequency for the AD7866 under different conditions. The power supply rejection ratio (PSRR) is defined as the ratio of the power in the ADC output at full-scale frequency f, to the power of a 100 mV sine wave applied to the ADC AV_{DD} supply of frequency f_S:

$$PSRR\,(dB) = 10 \log\left(Pf/Pf_S\right)$$

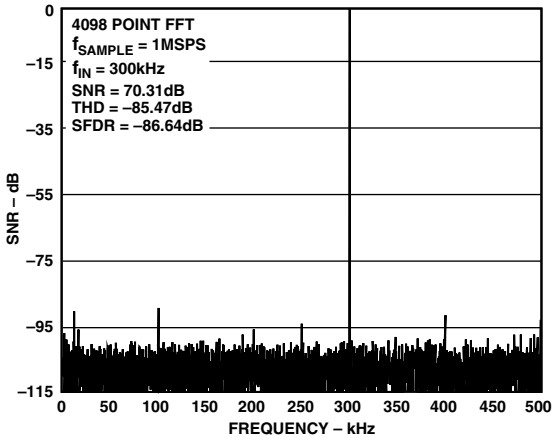
Pf = power at frequency f in ADC output, and Pf_S = power at frequency f_S coupled onto the ADC AV_{DD} supply. Here, a 100 mV peak-to-peak sine wave is coupled onto the AV_{DD} supply while the digital supply is left unaltered. TPCs 3a and 3b show the PSRR of the AD7866 when there is no decoupling on the supply, while TPCs 4a and 4b show the PSRR with decoupling capacitors of 10 µF and 0.1 µF on the supply.

TPCs 5 and 6 show typical DNL and INL plots for the AD7866.

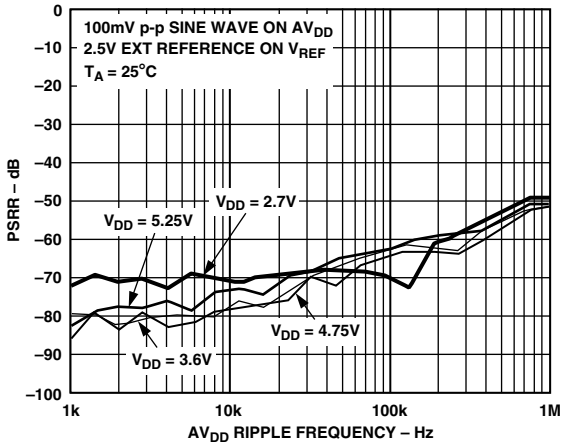
TPC 7 shows a graph of the total harmonic distortion versus analog input frequency for various source impedances.

TPC 8 shows a graph of total harmonic distortion versus analog input frequency for various supply voltages. See the Analog Input section.

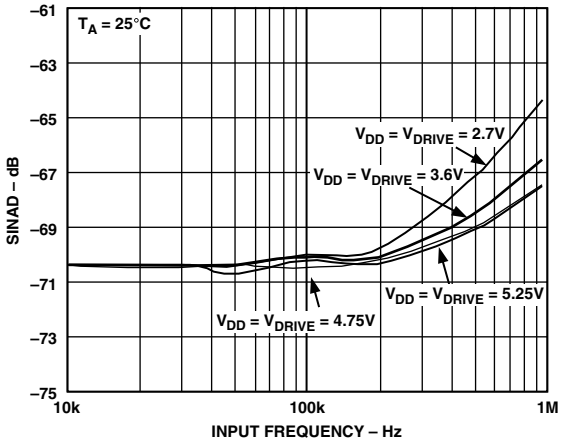
Typical Performance Characteristics



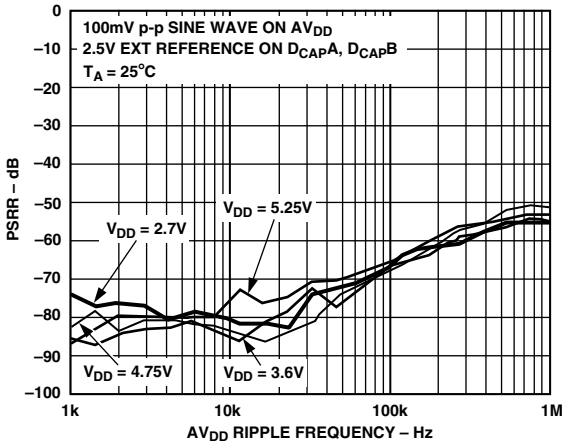
TPC 1. Dynamic Performance



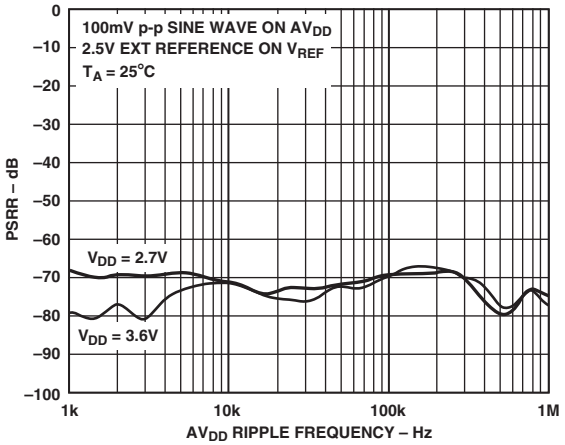
TPC 3a. PSRR vs. Supply Ripple Frequency, without Supply Decoupling



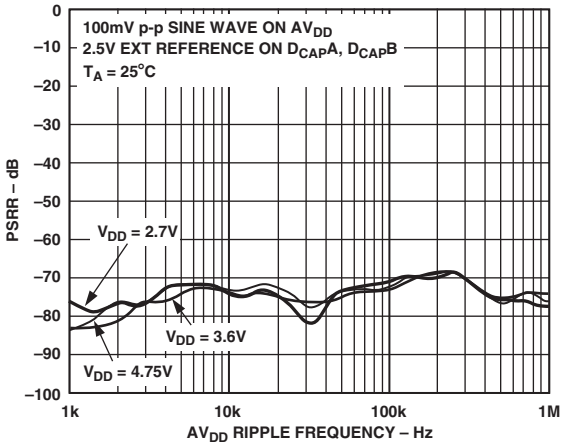
TPC 2. SINAD vs. Input Frequency



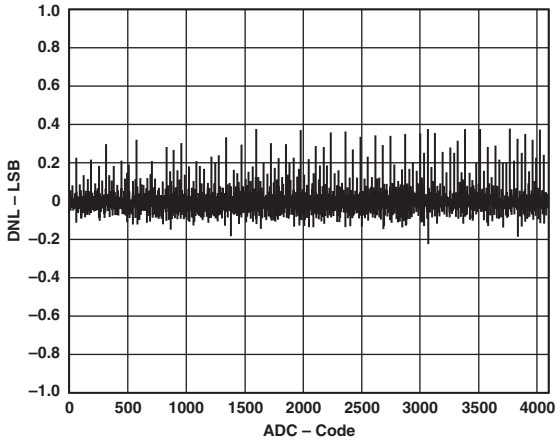
TPC 3b. PSRR vs. Supply Ripple Frequency, without Supply Decoupling



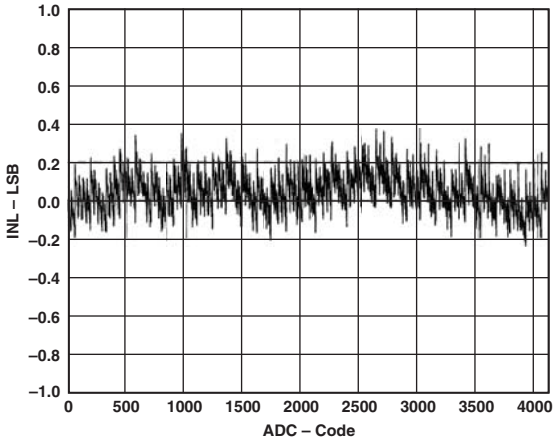
TPC 4a. PSRR vs. Supply Ripple Frequency, with Supply Decoupling



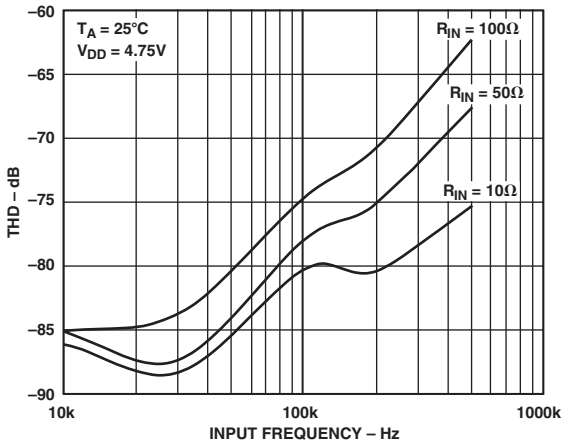
TPC 4b. PSRR vs. Supply Ripple Frequency, with Supply Decoupling



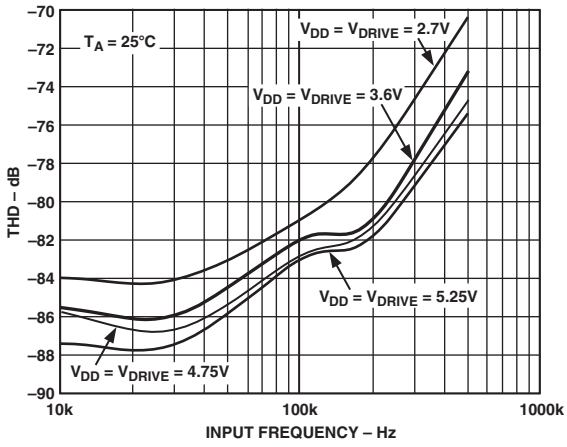
TPC 5. DC DNL Plot



TPC 6. DC INL Plot



TPC 7. THD vs. Analog Input Frequency for Various Source Impedances



TPC 8. THD vs. Analog Input Frequency for Various Supply Voltages

CIRCUIT INFORMATION

The AD7866 is a fast, micropower, dual 12-bit, single supply, A/D converter that operates from a 2.7 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7866 is capable of throughput rates of 1 MSPS when provided with a 20 MHz clock.

The AD7866 contains two on-chip track-and-hold amplifiers, two successive approximation A/D converters, and a serial interface with two separate data output pins, and is housed in a 20-lead TSSOP package, which offers the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part but also provides the clock source for each successive approximation ADC. The analog input range for the part can be selected to be a 0 V to V_{REF} input or a $2 \times V_{REF}$ input with either straight binary or twos complement output coding. The AD7866 has an on-chip 2.5 V reference that can be overdriven if an external reference is preferred. In addition, each ADC can be supplied with an individual separate external reference.

The AD7866 also features power-down options to allow power saving between conversions. The power-down feature is implemented across the standard serial interface, as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7866 has two successive approximation analog-to-digital converters, each based around a capacitive DAC. Figures 2 and 3 show simplified schematics of one of these ADCs. The ADC is comprised of control logic, a SAR, and a capacitive DAC, all of which are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 2 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{A1}, for example.

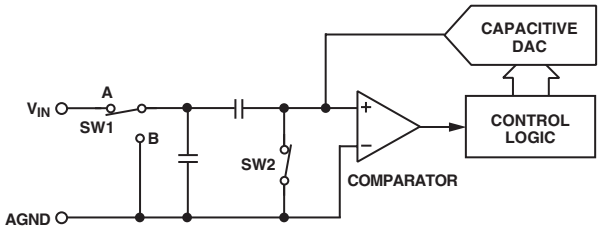


Figure 2. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 3), SW2 will open and SW1 will move to position B, causing the comparator to become unbalanced. The Control Logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The Control Logic generates the ADC output code. Figures 10 and 11 show the ADC transfer functions.

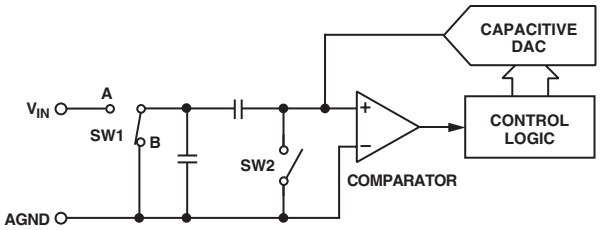


Figure 3. ADC Conversion Phase

ANALOG INPUT

Figure 4 shows an equivalent circuit of the analog input structure of the AD7866. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. This will cause these diodes to become forward-biased and start conducting current into the substrate. 10 mA is the maximum current these diodes can conduct without causing irreversible damage to the part. The capacitor C1 in Figure 4 is typically about 10 pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100 Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 20 pF typically. For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

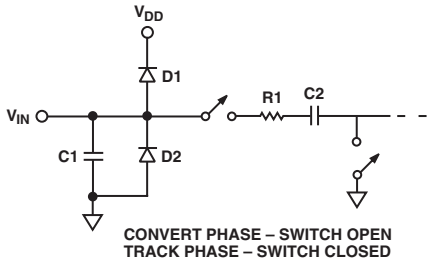


Figure 4. Equivalent Analog Input Circuit

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases, and performance will degrade (see TPC 7).

Analog Input Ranges

The analog input range for the AD7866 can be selected to be 0 V to V_{REF} or 2 × V_{REF} with either straight binary or twos complement output coding. The RANGE pin is used to select both the analog input range and the output coding, as shown in Figures 5 to 8. On the falling edge of $\overline{CS}$, point A, the logic level of the RANGE pin is checked to determine the analog input range of the next conversion. If this pin is tied to a logic low, the analog input range will be 0 V to V_{REF} and the output coding from the part will be straight binary (for the next conversion). If this pin is at a logic high when $\overline{CS}$ goes low, the analog input range will be 2 × V_{REF} and the output coding for the part will be twos complement. However, if after the falling edge of $\overline{CS}$, the logic level of the RANGE pin has changed upon the eighth falling SCLK edge, point B, the output coding will change to the other option without any change in the analog input range. So for the next conversion, twos complement output coding could be selected with a 0 V to V_{REF} input range, for example, if the RANGE pin is low upon the falling edge of $\overline{CS}$ and high upon the eighth falling SCLK edge, as shown in Figure 7. Figures 5 to 8 show examples of timing diagrams for selections of different analog input ranges with various output coding formats. Table I summarizes the required logic level of the RANGE pin for each selection. Note that the analog input range selected must not exceed V_{DD}. The logic input A0 is used to select the pair of channels to be converted simultaneously. The logic state of this pin is also checked upon the falling edge of $\overline{CS}$, and the multiplexers are set up for the next conversion. If it is low, the following conversion will be performed on Channel 1 of each ADC; if it is high, the following conversion will be performed on Channel 2 of each ADC.

Handling Bipolar Input Signals

Figure 9 shows how useful the combination of the 2 × V_{REF} input range and the twos complement output coding scheme is for handling bipolar input signals. If the bipolar input signal is biased about V_{REF} and twos complement output coding is selected, then V_{REF} becomes the zero code point, –V_{REF} is negative full-scale, and +V_{REF} becomes positive full-scale with a dynamic range of 2 × V_{REF}.

Transfer Functions

The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size is V_{REF}/4096. The ideal transfer characteristic for the AD7866 when straight binary coding is selected is shown in Figure 10, and the ideal transfer characteristic for the AD7866 when twos complement coding is selected is shown in Figure 11.

Table I. Analog Input and Output Coding Selection

Range Level @ Point A[1]	Range Level @ Point B[2]	Input Range[3]	Output Coding[3]
Low	Low	0 V to V_{REF}	Straight Binary
High	High	V_{REF} ± V_{REF}	Twos Complement
Low	High	V_{REF}/2 ± V_{REF}/2	Twos Complement
High	Low	0 V to 2 × V_{REF}	Straight Binary

NOTES
[1]Point A = Falling edge of $\overline{CS}$.
[2]Point B = Eighth falling edge of SCLK.
[3]Selected for next conversion.

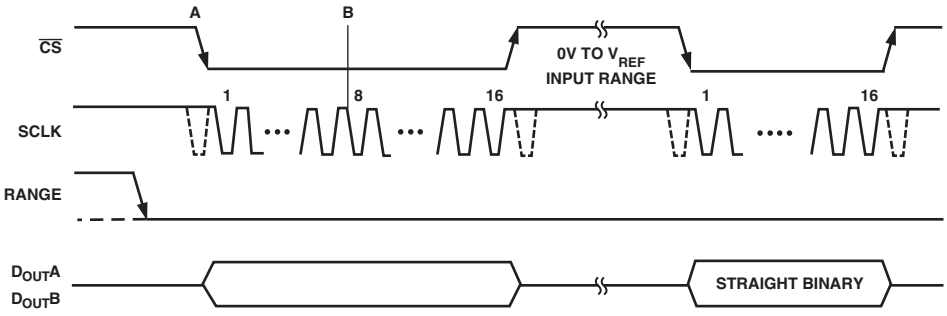


Figure 5. Selecting 0 V to V_{REF} Input Range with Straight Binary Output Coding

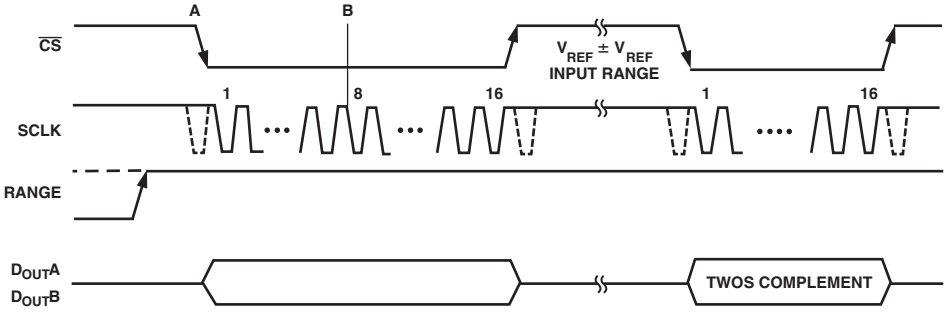


Figure 6. Selecting V_{REF} ± V_{REF} Input Range with Twos Complement Output Coding

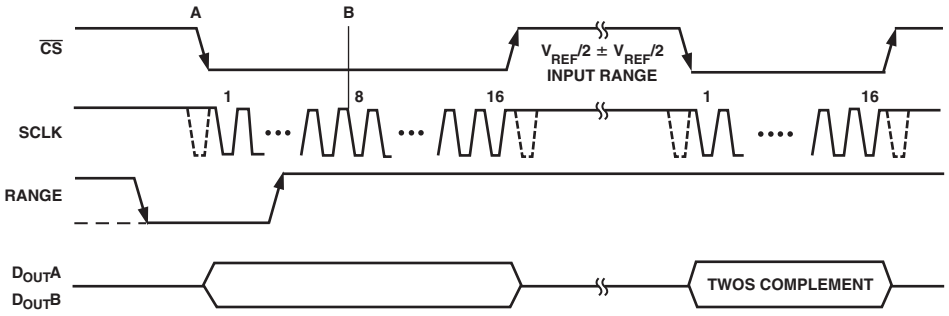


Figure 7. Selecting $V_{REF}/2 \pm V_{REF}/2$ Input Range with Twos Complement Output Coding

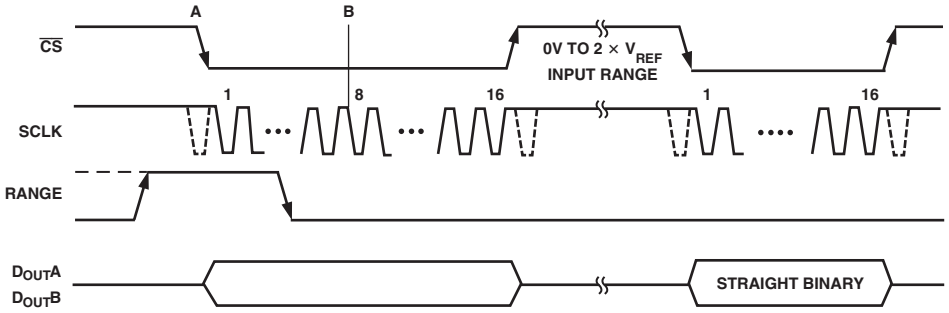


Figure 8. Selecting 0 V to 2 × V_{REF} Input Range with Straight Binary Output Coding

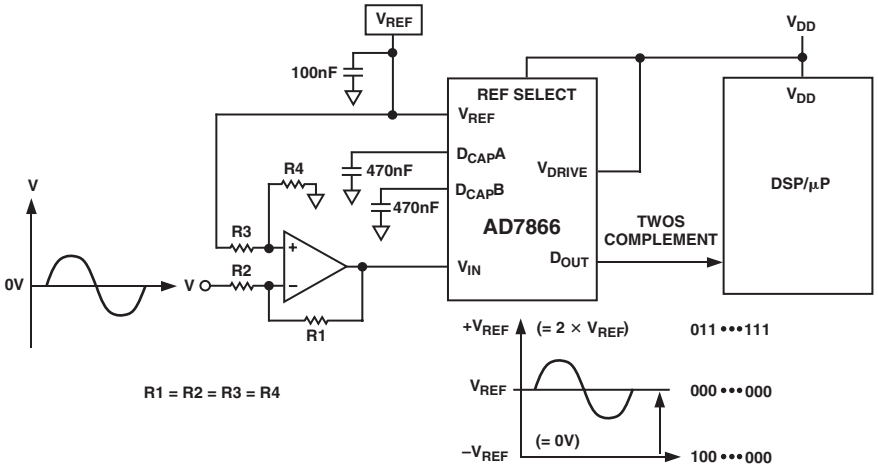


Figure 9. Handling Bipolar Signals with the AD7866

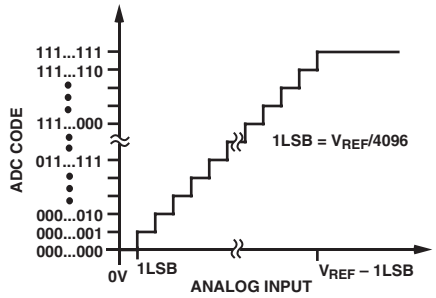


Figure 10. Straight Binary Transfer Characteristic with 0 V to V_{REF} Input Range

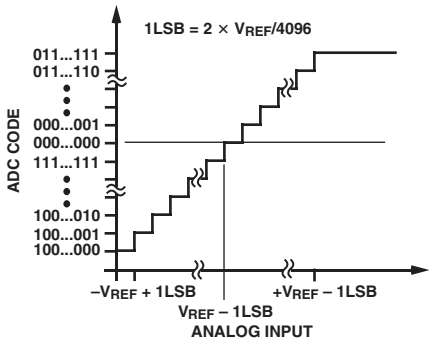


Figure 11. Twos Complement Transfer Characteristic with $V_{REF} \pm V_{REF}$ Input Range

Digital Inputs

The digital inputs applied to the AD7866 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the V_{DD} + 0.3 V limit as on the analog inputs. See maximum ratings.

Another advantage of SCLK, RANGE, REF SELECT, A0, and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. If one of these digital inputs is applied before V_{DD}, there is no risk of latch-up, as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to V_{DD}.

V_{DRIVE}

The AD7866 also has the V_{DRIVE} feature, which controls the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7866 was operated with a V_{DD} of 5 V, the V_{DRIVE} pin could be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors. For example, the AD7866 could be used with the 2 × V_{REF} input range, with a V_{DD} of 5 V while still being able to interface to 3 V digital parts.

REFERENCE CONFIGURATION OPTIONS

The AD7866 has various reference configuration options. The REF SELECT pin allows the choice of using an internal 2.5 V reference or applying an external reference, or even an individual external reference for each on-chip ADC if desired. If the REF SELECT pin is tied to AGND, then the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. In addition, pins V_{REF}, $D_{CAP}A$, and $D_{CAP}B$ must be tied to decoupling capacitors (100 nF, 470 nF, and 470 nF recommended, respectively). If the REF SELECT pin is tied to a logic high, an external reference can be supplied to the AD7866 through the V_{REF} pin to overdrive the on-chip reference, in which case decoupling capacitors are required on $D_{CAP}A$ and $D_{CAP}B$ again. However, if the V_{REF} pin is tied to AGND while REF SELECT is tied to a logic low, an individual external reference can be applied to both ADC A and ADC B through pins $D_{CAP}A$ and $D_{CAP}B$, respectively. Table II summarizes these reference options.

For specified performance, the last configuration was used with the same reference voltage applied to both $D_{CAP}A$ and $D_{CAP}B$. The connections for the relevant reference pins are shown in the typical connection diagrams. If the internal reference is being used, the V_{REF} pin should have a 100 nF capacitor connected to AGND very close to the V_{REF} pin. These connections are shown in Figure 12.

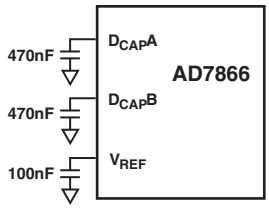


Figure 12. Relevant Connections when Using an Internal Reference

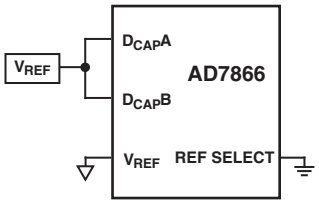


Figure 13. Relevant Connections when Applying an External Reference at $D_{CAP}A$ and/or $D_{CAP}B$

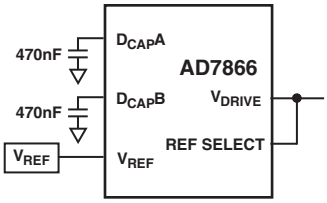


Figure 14. Relevant Connections when Applying an External Reference at V_{REF}

Figure 13 shows the connections required when an external reference is applied to $D_{CAP}A$ and $D_{CAP}B$. In this example, the same reference voltage is applied at each pin; however, a different voltage may be applied at each of these pins for each on-chip ADC. An external reference applied at these pins may have a range from 2 V to 3 V, but for specified performance it must be within ±1% of 2.5 V. Figure 14 shows the third option, which is to overdrive the internal reference through the V_{REF} pin. This is possible due to the series resistance from the V_{REF} pin to the internal reference. This external reference can have a range from 2 V to 3 V; but again, to get as close as possible to the specified performance, a 2.5 V reference is desirable. $D_{CAP}A$ and $D_{CAP}B$ decouple each on-chip reference buffer, as shown in Figure 15.

Table II. Reference Selection

Reference Option	REF SELECT	V_{REF}[1]	$D_{CAP}A$ and $D_{CAP}B$[2]
Internal	Low	Decoupling Capacitor	Decoupling Capacitor
Externally through V_{REF}	High	External Reference	Decoupling Capacitor
Externally through $D_{CAP}A$ and/or $D_{CAP}B$	Low	AGND	External Reference A and/or Reference B

NOTES
[1]Recommended value of decoupling capacitor = 100 nF.
[2]Recommended value of decoupling capacitor = 470 nF.

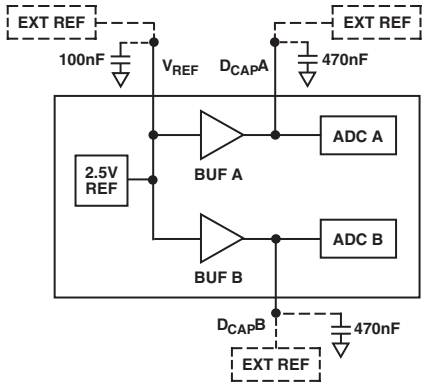


Figure 15. Reference Circuit

If the on-chip 2.5 V reference is being used, and is to be applied externally to the rest of the system, it may be taken from either the V_{REF} pin or one of the $D_{CAP}A$ or $D_{CAP}B$ pins. If it is taken from the V_{REF} pin, it must be buffered before being applied elsewhere as it will not be capable of sourcing more than a few microamps. If the reference voltage is taken from either the $D_{CAP}A$ pin or $D_{CAP}B$ pin, a buffer is not strictly necessary. Either pin is capable of sourcing current in the region of 100 μA; however, the larger the source current requirement, the greater the voltage drop seen at the pin. The output impedance of each of these pins is typically 50 Ω. In addition, this point represents the actual voltage applied to the ADC internally so any voltage drop due to the current load or disturbance due to a dynamic load will directly affect the ADC conversion. For this reason, if a large current source is necessary or a dynamic load is present, it is recommended to use a buffer on the output to drive a device.

Examples of suitable external reference devices that may be applied at pins V_{REF}, $D_{CAP}A$, or $D_{CAP}B$ are the AD780, REF192, REF43, and AD1582.

MODES OF OPERATION

The mode of operation of the AD7866 is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine which power-down mode, if any, the device will enter. Similarly, if already in a power-down mode, $\overline{CS}$ can control whether the device will return to normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance since the user does not have to worry about any power-up times with the AD7866 remaining fully powered all the time. Figure 16 shows the general diagram of the operation of the AD7866 in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$, as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge, but before the 16th SCLK falling edge, the part will remain powered up but the conversion will be terminated and $D_{OUT}A$ and $D_{OUT}B$ will go back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. The D_{OUT} line will not return to three-state after 16 SCLK cycles have elapsed, but instead when $\overline{CS}$ is brought high again. If $\overline{CS}$ is left low for another 16 SCLK cycles, the result from the other ADC on board will also be accessed on the same D_{OUT} line, as shown in Figure 22 (see also the Serial Interface section). The STATUS bits provided prior to each conversion result will identify which ADC the following result will be from. Once 32 SCLK cycles have elapsed, the D_{OUT} line will return to three-state on the 32nd SCLK falling edge. If $\overline{CS}$ is brought high prior to this, the D_{OUT} line will return to three-state at that point. Thus, $\overline{CS}$ may idle low after 32 SCLK cycles, until it is brought high again sometime prior to the next conversion (effectively idling $\overline{CS}$ low), if so desired, since the bus will still return to three-state upon completion of the dual result read.

Once a data transfer is complete and $D_{OUT}A$ and $D_{OUT}B$ have returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

Partial Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7866 is in partial power-down, all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter partial power-down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK as shown in Figure 17. Once $\overline{CS}$ has been brought high in this window of SCLKs, the part will enter partial power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ will be

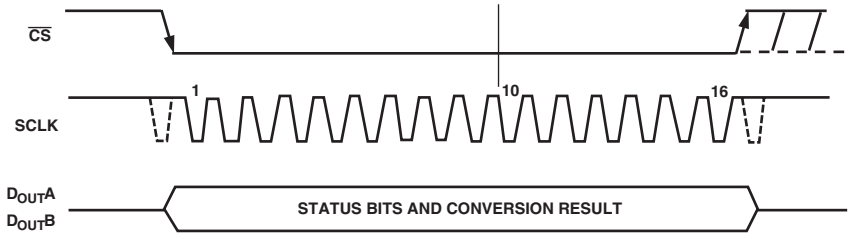


Figure 16. Normal Mode Operation

terminated, and $D_{OUT}A$ and $D_{OUT}B$ will go back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part will remain in normal mode and will not power down. This will avoid accidental power-down due to glitches on the $\overline{CS}$ line.

To exit this mode of operation and power up the AD7866 again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. In the case of an external reference, the device will be fully powered up once 16 SCLKs have elapsed, and valid data will result from the next conversion, as shown in Figure 18. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the AD7866 will again go into partial power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line; although the device may begin to power up on the falling edge of $\overline{CS}$, it will power down again on the rising edge of $\overline{CS}$. If the AD7866 is already in partial power-down mode and $\overline{CS}$ is brought high between the second and tenth falling edges of SCLK, the device will enter full power-down mode. For more information on the power-up times associated with partial power-down in various configurations, see the Power-Up Times section.

Full Power-Down Mode

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required, as power-up from a full power-down takes substantially longer than that from partial power-down. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate would be followed by a long period of inactivity and thus power-down. When the AD7866 is in full power-down, all analog circuitry is powered down. Full power-down is entered in a similar way as partial power-down, except the timing sequence shown in Figure 17 must be executed twice. The conversion process must be interrupted in a similar fashion by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK. The device will enter partial power-down at this point. To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure 19. Once $\overline{CS}$ has been brought high in this window of SCLKs, the part will power down completely.

Note that it is not necessary to complete the 16 SCLKs once $\overline{CS}$ has been brought high to enter a power-down mode.

To exit full power-down and power the AD7866 up again, a dummy conversion is performed, as when powering up from partial power-down. On the falling edge of $\overline{CS}$, the device will begin to power up and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The power-up time required must elapse before a conversion can be initiated, as shown in Figure 20. See the Power-Up Times section for the power-up times associated with the AD7866.

POWER-UP TIMES

The AD7866 has two power-down modes, partial power-down and full power-down, which are described in detail in the Modes of Operation section. This section deals with the power-up time required when coming out of either of these modes. It should be noted that the power-up times quoted apply with the recommended capacitors on the V_{REF}, $D_{CAP}A$, and $D_{CAP}B$ pins in place.

To power up from full power-down, approximately 4 ms should be allowed from the falling edge of $\overline{CS}$, shown in Figure 20 as $t_{POWER\ UP}$. Powering up from partial power-down requires much less time. If the internal reference is being used, the power-up time is typically 4 µs; but if an external reference is being used, the power-up time is typically 1 µs. This means that with any frequency of SCLK up to 20 MHz, one dummy cycle will always be sufficient to allow the device to power up from partial power-down when using an external reference (see Figure 18). Once the dummy cycle is complete, the ADC will be fully powered up and the input signal will be acquired properly. A dummy cycle may well be sufficient to power up the part when using an internal reference also, provided the SCLK is slow enough to allow the required power-up time to elapse before a valid conversion is requested. In addition, it should be ensured that the quiet time, t_{QUIET}, has still been allowed from the point where the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{CS}$. Alternatively, instead of slowing the SCLK to make the dummy cycle long enough, the $\overline{CS}$ high time could just be extended to include the required power-up time (as in Figure 20) when powering up from full power-down.

Different power-up time is needed when coming out of partial power-down for two cases where an internal or external reference is being used, primarily because of the on-chip reference buffers. They power down in partial power-down mode and must be powered up again if the internal reference is being used, but they do not need to be powered up again if an external reference is being used. The time needed to power up these buffers is not just their own power-up time but also the time required to charge up the decoupling capacitors present on pins V_{REF}, $D_{CAP}A$, and $D_{CAP}B$.

It should also be noted that during power-up from partial power-down, the track-and-hold, which was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as point A in Figure 18.

When power supplies are first applied to the AD7866, the ADC may power up in either of the power-down modes or the normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure that the part is fully powered up before attempting a valid conversion. Likewise, if the part is to be kept in the partial power-down mode immediately after the supplies are applied, two dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the tenth SCLK falling edge (see Figure 16); in the second cycle, $\overline{CS}$ must be brought high before the tenth SCLK edge but after the second SCLK falling edge (see Figure 17). Alternatively, if the part is to be placed in full power-down mode when the supplies have been applied, three dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the tenth SCLK falling edge (see Figure 16); the second and third dummy cycles place the part in full power-down (see Figure 19). See also the Modes of Operation section.

Once supplies are applied to the AD7866, enough time must be allowed for any external reference to power up and charge any reference capacitor to its final value, or enough time must be allowed for the internal reference buffer to charge the various reference buffer decoupling capacitors to their final values.

Then, to place the AD7866 in normal mode, a dummy cycle (1 μs to 4 μs approximately) should be initiated. If the first valid conversion is performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed. As mentioned earlier, when powering up from the power-down mode, the part will return to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However when the ADC initially powers up after supplies are applied, the track-and-hold will already be in track. This means that (assuming one has the facility to monitor the ADC supply current and thus determine which mode the AD7866 is in) if the ADC powers up in the desired mode of operation and thus a dummy cycle is not required to change mode, then neither is a dummy cycle required to place the track-and-hold into track. If no current monitoring facility is available, the relevant dummy cycle(s) should be performed to ensure the part is in the required mode.

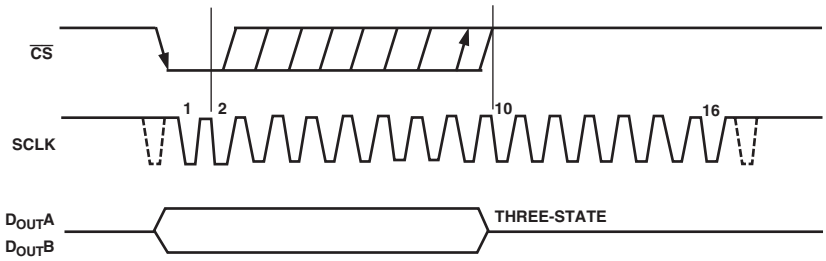


Figure 17. Entering Partial Power-Down Mode

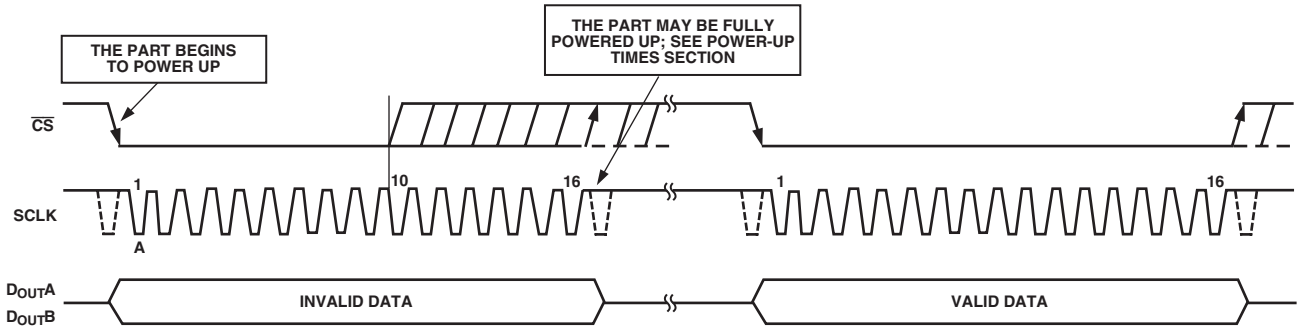


Figure 18. Exiting Partial Power-Down Mode

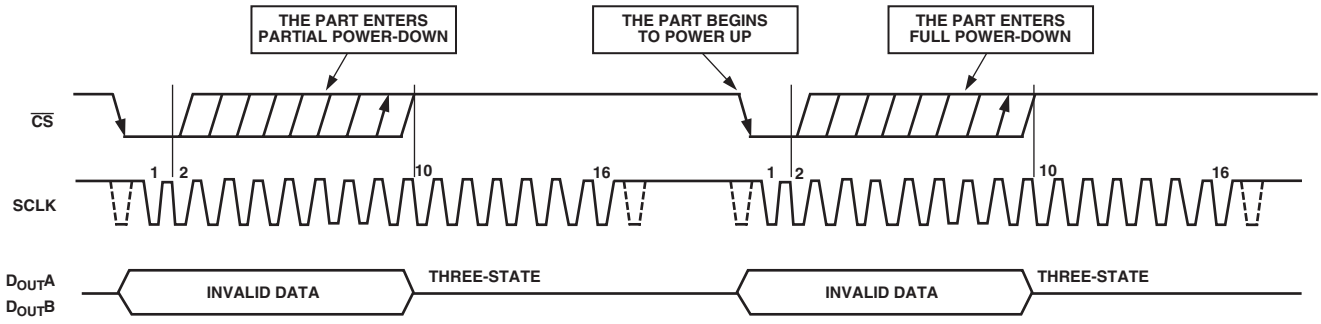


Figure 19. Entering Full Power-Down Mode

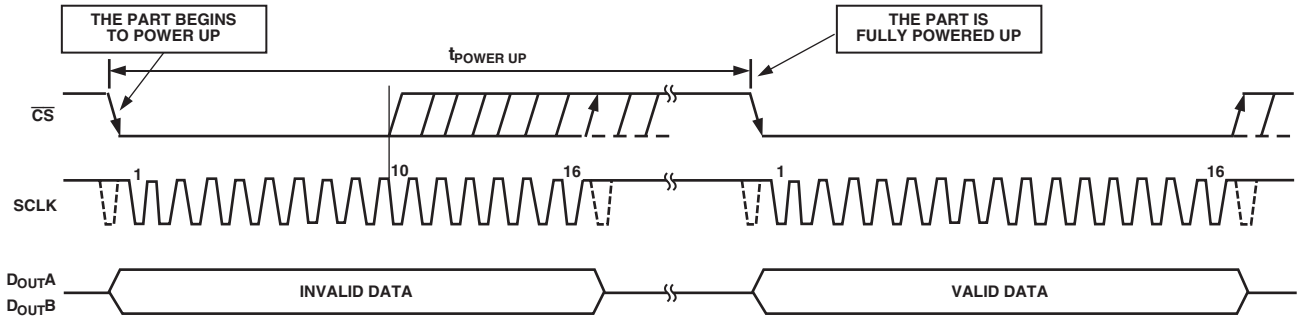


Figure 20. Exiting Full Power-Down Mode

POWER VS. THROUGHPUT RATE

When the AD7866 is in partial power-down mode and not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 21 shows that as the throughput rate is reduced, the part remains in its partial power-down state longer, and the average power consumption over time drops accordingly.

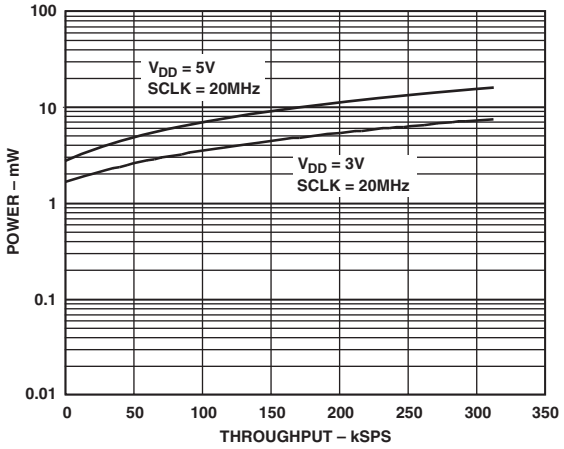


Figure 21. Power vs. Throughput for Partial Power-Down

For example, if the AD7866 is operated in a continuous sampling mode with a throughput rate of 100 kSPS and an SCLK of 20 MHz (V_{DD} = 5 V), and the device is placed in partial power-down mode between conversions, the power consumption is calculated as follows. The maximum power dissipation during normal operation is 24 mW (V_{DD} = 5 V). If the power-up time allowed from partial power-down is one dummy cycle, i.e., 1 µs, (assuming use of an external reference) and the remaining conversion time is another cycle, i.e., 1 µs, then the AD7866 can be said to dissipate 24 mW for 2 µs during each conversion cycle. For the remainder of the conversion cycle, 8 µs, the part remains in partial power-down mode. The AD7866 can be said to dissipate 2.8 mW for the remaining 8 µs of the conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is (2/10) × (24 mW) + (8/10) × (2.8 mW) = 7.04 mW. If V_{DD} = 3 V, SCLK = 20 MHz, and the device is again in partial power-down mode between conversions, the power dissipated during normal operation is 11.4 mW. The AD7866 can be said to dissipate 11.4 mW for 2 µs during each conversion cycle and 1.68 mW for the remaining 8 µs when the part is in partial power-down. With a throughput rate of 100 kSPS, the average power dissipated during each conversion cycle is (2/10) × (11.4 mW) + (8/10) × (1.68 mW) = 3.624 mW. Figure 21 shows the maximum power versus throughput rate when using the partial power-down mode between conversions with both 5 V and 3 V supplies for the AD7866.

SERIAL INTERFACE

Figure 22 shows the detailed timing diagram for serial interfacing to the AD7866. The serial clock provides the conversion clock and controls the transfer of information from the AD7866 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state; the analog input is sampled at this point. The conversion is also initiated at this point and requires 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold will go back into track on the next SCLK rising edge, as shown in Figure 22 at point B. On the rising edge of $\overline{CS}$, the conversion will be terminated and $D_{OUT}A$ and $D_{OUT}B$ will go back into three-state. If $\overline{CS}$ is not brought high but is instead held low for a further 16 SCLK cycles on $D_{OUT}A$, the data from conversion B will be output on

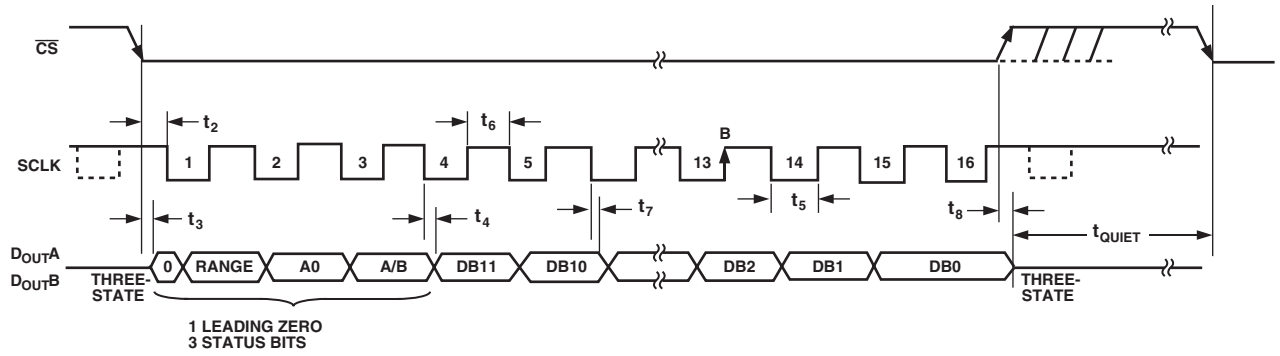


Figure 22. Serial Interface Timing Diagram

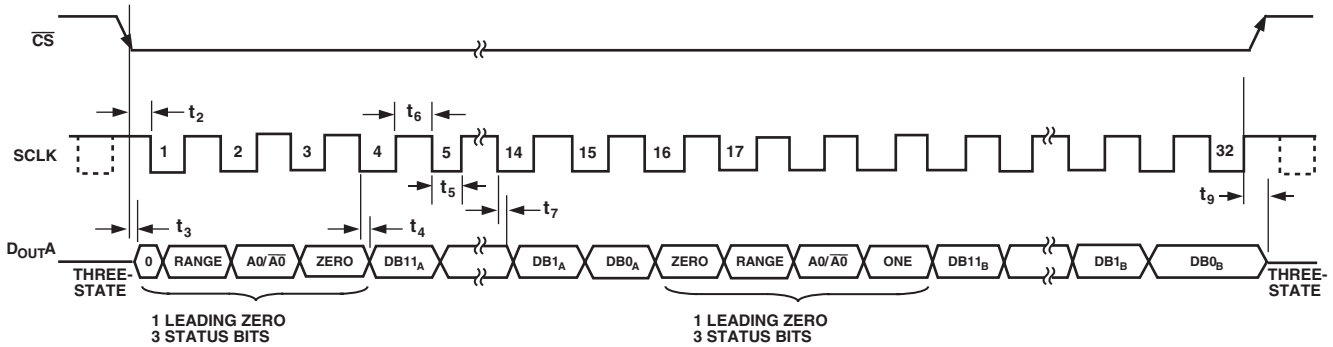


Figure 23. Reading Data from Both ADCs on One D_{OUT} Line

Table III. STATUS Bit Description

Bit	Bit Name	Comment
15	ZERO	Leading Zero. This bit will always be a zero output.
14	RANGE	The polarity of this bit reflects the analog input range that has been selected with the RANGE pin. If it is a 0, it means that in the previous transfer upon the falling edge of the $\overline{CS}$, the range pin was at a logic low, providing an analog input range from 0 V to V_{REF} for this conversion. If it is a 1, it means that in the previous transfer upon the falling edge of $\overline{CS}$, the RANGE pin was at a logic high, resulting in an analog input range of $2 \times V_{REF}$ selected for this conversion. See Analog Input section.
13	A0	This bit indicates on which channel the conversion is being performed, Channel 1 or Channel 2 of the ADC in question. If this bit is a 0, the conversion result will be from Channel 1 of the ADC; if it is a 1, the result will be from Channel 2 of the ADC in question.
12	A/B	This bit indicates from which ADC the conversion result comes. If this bit is a 0, the result is from ADC A; if it is a 1, the result is from ADC B. This is especially useful if only one serial port is available for use and one D_{OUT} line is used, as shown in Figure 23.

D_{OUT}A. Likewise, if $\overline{CS}$ is held low for a further 16 SCLK cycles on D_{OUT}B, the data from conversion A will be output on D_{OUT}B. This is illustrated in Figure 23 where the case for D_{OUT}A is shown. Note that in this case, the D_{OUT} line in use will go back into three-state on the 32nd SCLK rising edge or the rising edge of $\overline{CS}$, whichever occurs first.

Sixteen serial clock cycles are required to perform the conversion process and to access data from one conversion on either data line of the AD7866. $\overline{CS}$ going low provides the leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the first of three data STATUS bits. Thus the first falling clock edge on the serial clock has the leading zero provided and also clocks out the first of three STATUS bits. The final bit in the data transfer is valid on the sixteenth falling edge, having being clocked out on the previous (fifteenth) falling edge. In applications with a slower SCLK, it is possible to read in data on each SCLK rising edge, i.e., the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the leading zero provided and the fifteenth rising SCLK edge would have DB0 provided. The three STATUS bits that follow the leading zero provide information with respect to the conversion result that follows them on the D_{OUT} line in use. Table III shows how these identification bits can be interpreted.

MICROPROCESSOR INTERFACING

The serial interface on the AD7866 allows the parts to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7866 with some of the more common microcontroller and DSP serial interface protocols.

AD7866 to ADSP-218x

The ADSP-218x family of DSPs is directly interfaced to the AD7866 without any glue logic required. The V_{DRIVE} pin of the AD7866 takes the same supply voltage as that of the ADSP-218x. This allows the ADC to operate at a higher supply voltage than the serial interface, i.e., ADSP-218x, if necessary. This example shows both D_{OUT}A and D_{OUT}B of the AD7866 connected to both serial ports of the ADSP-218x.

The SPORT0 control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data-Words
ISCLK = 1, Internal Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0
ITFS = 1

The SPORT1 control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data-Words
ISCLK = 0, External Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0
ITFS = 1

To implement the power-down modes on the AD7866, SLEN should be set to 1001 to issue an 8-bit SCLK burst. The connection diagram is shown in Figure 24. The ADSP-218x has the TFS0 and RFS0 of the SPORT0 and the RFS1 of SPORT1 tied together, with TFS0 set as an output and both RFS0 and RFS1 set as inputs. The DSP operates in alternate framing mode and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and, as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and under certain conditions, equidistant sampling may not be achieved.

The timer and other registers are loaded with a value that will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and therefore the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (i.e., AX0 = TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone high, low, and high before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

For example, if the ADSP-2189 had a 20 MHz crystal such that it had a master clock frequency of 40 MHz, then the master cycle time would be 25 ns. If the SCLKDIV register is loaded with the value 3, an SCLK of 5 MHz is obtained and eight master clock periods will elapse for every 1 SCLK period. Depending on the throughput rate selected, if the timer register were loaded with the value, 803, (803 + 1 = 804), for example, 100.5 SCLKs would occur between interrupts and subsequently between transmit instructions. This situation would result in nonequidistant sampling as the transmit instruction is occurring on an SCLK edge. If the number of SCLKs between interrupts were a whole integer figure of N, equidistant sampling would be implemented by the DSP.

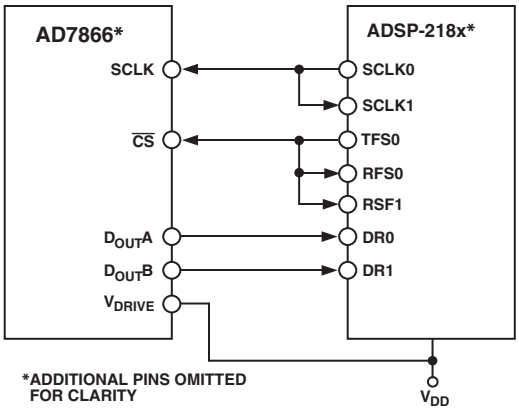


Figure 24. Interfacing the AD7866 to the ADSP-218x

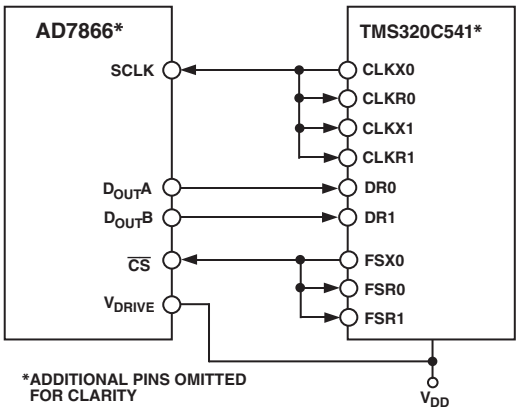


Figure 25. Interfacing the AD7866 to the TMS320C541

AD7866 to TMS320C541

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7866. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7866 with no glue logic required. The serial ports of the TMS320C541 are set up to operate in burst mode with internal CLKX (Tx serial clock on serial port 0) and FSX0 (Tx frame sync from serial port 0). The serial port control (SPC) registers must have the following setup:

SPC0: FO = 0, FSM = 1, MCM = 1 and TxM = 1
SPC1: FO = 0, FSM = 1, MCM = 0 and TxM = 0

The format bit, FO, may be set to 1 to set the word length to eight bits, in order to implement the power-down modes on the AD7866.

The connection diagram is shown in Figure 25. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C541 will provide equidistant sampling. The V_{DRIVE} pin of the AD7866 takes the same supply voltage as that of the TMS320C541. This allows the ADC to operate at a higher voltage than the serial interface, i.e., TMS320C541, if necessary.

AD7866 to DSP-563xx

The connection diagram in Figure 26 shows how the AD7866 can be connected to the ESSI (synchronous serial interface) of the DSP-563xx family of DSPs from Motorola. Each ESSI (there are two on-board) is operated in synchronous mode (bit SYN = 1 in CRB register) with internally generated word length frame sync for both Tx and Rx (bits FSL1 = 0 and FSL0 = 0 in CRB). Normal operation of the ESSI is selected by making MOD = 0 in the CRB. Set the word length to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA. To implement the power-down modes on the AD7866, the word length can be changed to eight bits by setting bits WL1 = 0 and WL0 = 0 in CRA. The FSP bit in the CRB should be set to 1 to make the frame sync negative. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the DSP-563xx provide equidistant sampling.

In the example shown in Figure 26, the serial clock is taken from the ESSI0, so the SCK0 pin must be set as an output, SCKD = 1, while the SCK1 pin is set up as an input, SCKD = 0. The frame sync signal is taken from SC02 on ESSI0, so SCD2 = 1, while on ESSI1, SCD2 = 0, so SC12 is configured as an input. The V_{DRIVE} pin of the AD7866 takes the same supply voltage as that of the DSP-563xx. This allows the ADC to operate at a higher voltage than the serial interface, i.e., DSP-563xx, if necessary.

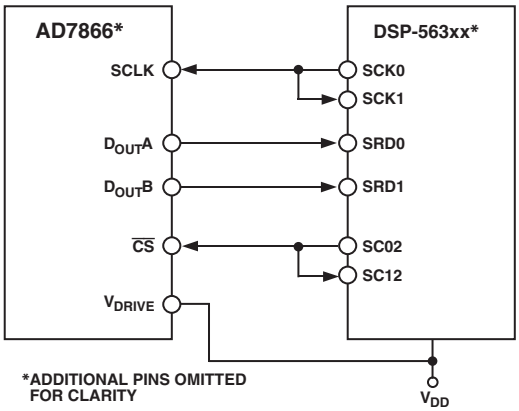


Figure 26. Interfacing to the DSP-563xx

APPLICATION HINTS

Grounding and Layout

The analog and digital supplies to the AD7866 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The AD7866 has very good immunity to noise on the power supplies as can be shown by the PSRR vs. Supply Ripple Frequency plots, TPC 3a to TPC 4b. However, care should be taken with regard to grounding and layout.

The printed circuit board that houses the AD7866 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum

etch technique is generally best for ground planes because it gives the best shielding. Both AGND pins of the AD7866 should be sunk in the AGND plane. Digital and analog ground planes should be joined at only one place. If the AD7866 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7866.

Avoid running digital lines under the device since these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7866 to avoid noise coupling. The power supply lines to the AD7866 should use the largest trace possible to provide low impedance paths and to reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. For this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. All digital supplies should have at least a 0.1 µF disk ceramic capacitor to DGND. V_{DRIVE} should have a 0.1 µF ceramic capacitor to DGND. To achieve the best results from these decoupling components, place them as close as possible to the device, ideally right up against it. The 0.1 µF capacitors should be common ceramic or surface-mount types, which have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), and provide a low impedance path to ground at high frequencies for handling transient currents due to internal logic switching. Figure 27 shows the recommended supply decoupling scheme. For information on the decoupling requirements of each reference configuration, see the Reference Configuration Options section.

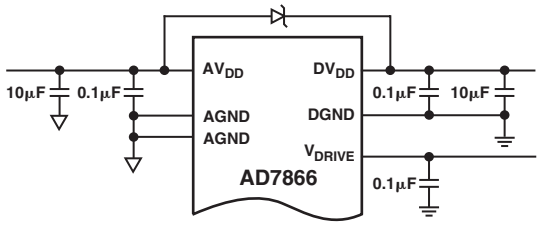


Figure 27. Recommended Supply Decoupling Scheme

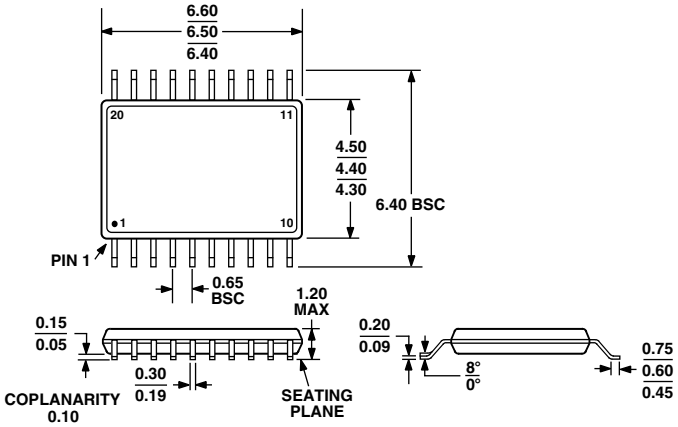
Evaluating the AD7866 Performance

The recommended layout for the AD7866 is outlined in the evaluation board for the AD7866. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the eval-controller board. The eval-controller board can be used in conjunction with the AD7866 evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7866.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7866.

OUTLINE DIMENSIONS

20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AC

Revision History

Location	Page
2/03—Data Sheet changed from REV. 0 to REV. A.	
Addition to FEATURES	1
Addition to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	5
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Added text to Analog Input Ranges section	12
Changes to Figure 9	13
Changes to POWER VS. THROUGHPUT RATE section	18
Replaced Figure 21	18
Updated OUTLINE DIMENSIONS	22

C02672–0–2/03(A)

PRINTED IN U.S.A.

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
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Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

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http://moschip.ru/get-element

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В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

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