

32K x 8 HIGH-SPEED CMOS STATIC RAM

MAY 2012

FEATURES

- High-speed access time: 10, 12 ns
- CMOS Low Power Operation
 - 1 mW (typical) CMOS standby
 - 125 mW (typical) operating
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V power supply
- Lead-free available

DESCRIPTION

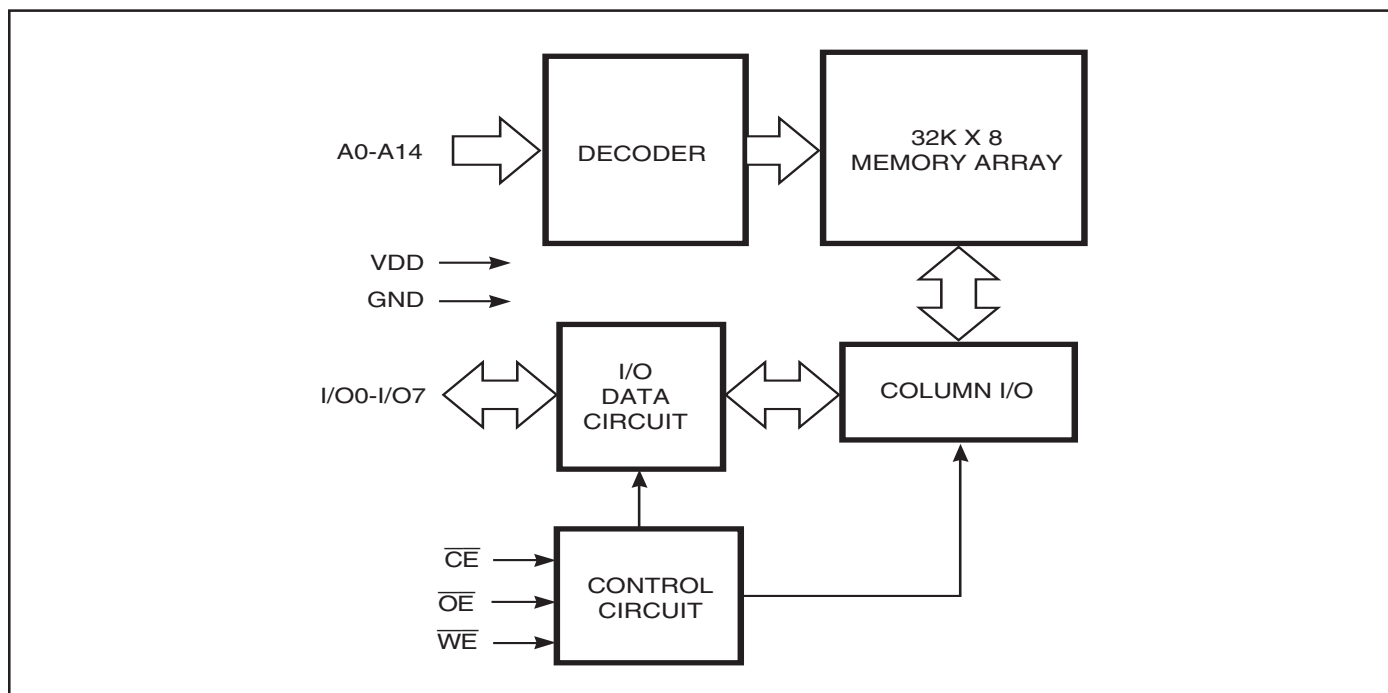
The ISSI IS61C256AL is a very high-speed, low power, 32,768 word by 8-bit static RAMs. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 10 ns maximum.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 150 μ W (typical) with CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Enable (\overline{CE}) input and an active LOW Output Enable (\overline{OE}) input. The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS61C256AL is pin compatible with other 32Kx8 SRAMs and are available in 28-pin SOJ and TSOP (Type I) packages.

FUNCTIONAL BLOCK DIAGRAM



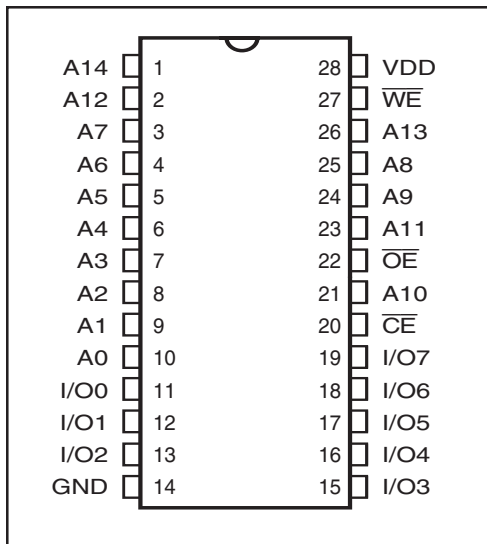
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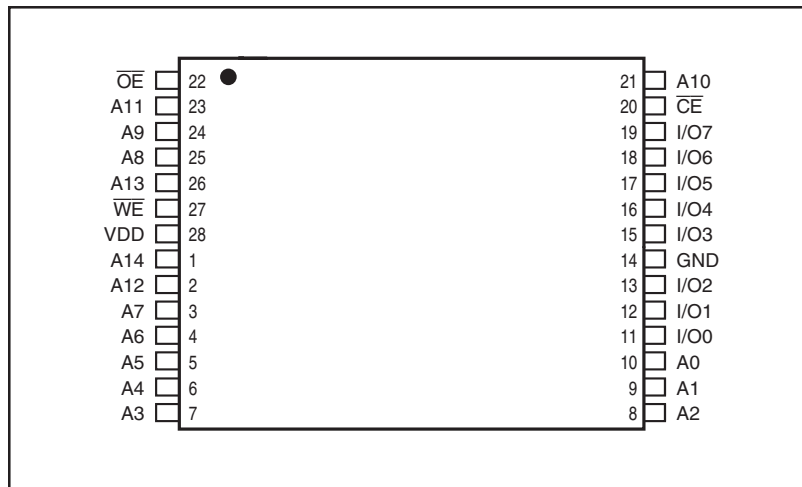
PIN CONFIGURATION

28-Pin SOJ



PIN CONFIGURATION

28-Pin TSOP



PIN DESCRIPTIONS

| | |
|-----------------|---------------------|
| A0-A14 | Address Inputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O0-I/O7 | Bidirectional Ports |
| VDD | Power |
| GND | Ground |

TRUTH TABLE

| Mode | \overline{WE} | \overline{CE} | \overline{OE} | I/O Operation | VDD Current |
|------------------------------|-----------------|-----------------|-----------------|---------------|-------------|
| Not Selected (Power-down) | X | H | X | High-Z | IsB1, IsB2 |
| Output Disabled | H | L | H | High-Z | Icc |
| Read | H | L | L | DOUT | Icc |
| Write | L | L | X | DIN | Icc |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|--------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.5 | W |
| I _{OUT} | DC Output Current (LOW) | 20 | mA |

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

| Range | Ambient Temperature | Speed (ns) | V _{DD} (V) |
|------------|---------------------|------------|---------------------|
| Commercial | 0°C to +70°C | -10 | 5V ± 5% |
| Commercial | 0°C to +70°C | -12 | 5V ± 10% |
| Industrial | -40°C to +85°C | -12 | 5V ± 10% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit | |
|-----------------|----------------------------------|----------------------------------------------------------------|--------------|-----------------------|--------|----|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -4.0 mA | 2.4 | — | V | |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 8.0 mA | — | 0.4 | V | |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{DD} + 0.5 | V | |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V | |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | Com. Ind. | -1 -2 | 1 2 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | Com. Ind. | -1 -2 | 1 2 | μA |

Note: 1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -10 | | -12 | | Unit |
|------------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------|------|------|------|------|
| | | | | Min. | Max. | Min. | Max. | |
| I _{CC1} | V _{DD} Operating Supply Current | V _{DD} = Max., \overline{CE} = V _{IL} I _{OUT} = 0 mA, f = 0 | Com. | — | 20 | — | 20 | mA |
| | | | Ind. | — | — | — | 25 | |
| I _{CC2} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., \overline{CE} = V _{IL} I _{OUT} = 0 mA, f = f _{MAX} | Com. | — | 45 | — | 35 | mA |
| | | | Ind. | — | — | — | 40 | |
| | | | typ. ⁽²⁾ | | | 25 | | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} \overline{CE} ≥ V _{IH} , f = 0 | Com. | — | 1 | — | 1 | mA |
| | | | Ind. | — | — | — | 2 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., \overline{CE} ≥ V _{DD} - 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 350 | — | 350 | μA |
| | | | Ind. | — | — | — | 450 | |
| | | | typ. ⁽²⁾ | | | 200 | | |

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 8 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 10 | pF |

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

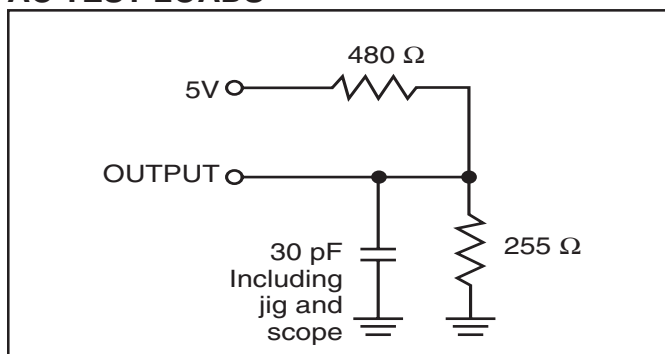
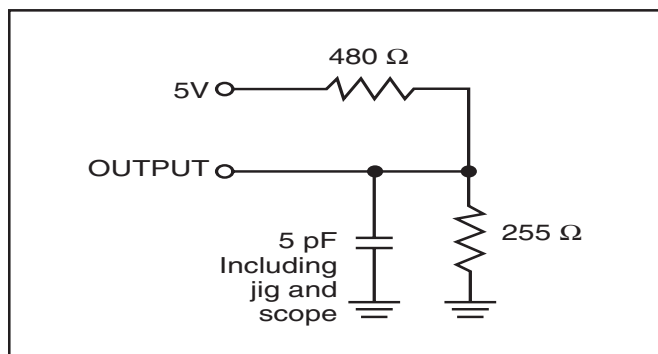
| Symbol | Parameter | -10 ns | | -12 ns | | Unit |
|------------------|----------------------------------|--------|-----|--------|------|------|
| | | Min. | Max | Min. | Max. | |
| t_{RC} | Read Cycle Time | 10 | — | 12 | — | ns |
| t_{AA} | Address Access Time | — | 10 | — | 12 | ns |
| t_{OHA} | Output Hold Time | 2 | — | 2 | — | ns |
| t_{ACS} | \overline{CE} Access Time | — | 10 | — | 12 | ns |
| t_{DOE} | \overline{OE} Access Time | — | 6 | — | 6 | ns |
| $t_{LZOE}^{(2)}$ | \overline{OE} to Low-Z Output | 0 | — | 0 | — | ns |
| $t_{HZOE}^{(2)}$ | \overline{OE} to High-Z Output | — | 5 | — | 6 | ns |
| $t_{LZCS}^{(2)}$ | \overline{CE} to Low-Z Output | 2 | — | 3 | — | ns |
| $t_{HZCS}^{(2)}$ | \overline{CE} to High-Z Output | — | 5 | — | 7 | ns |
| $t_{PU}^{(3)}$ | \overline{CE} to Power-Up | 0 | — | 0 | — | ns |
| $t_{PD}^{(3)}$ | \overline{CE} to Power-Down | — | 10 | — | 12 | ns |

Notes:

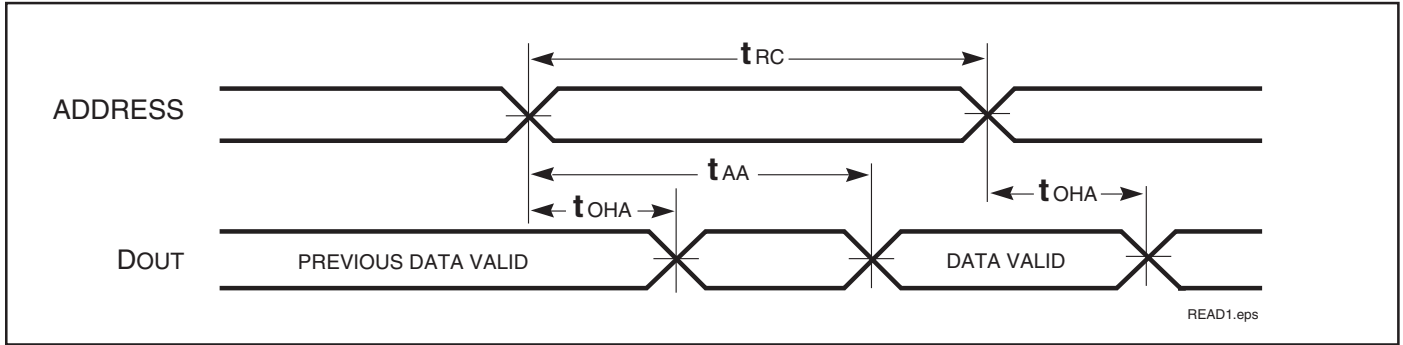
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

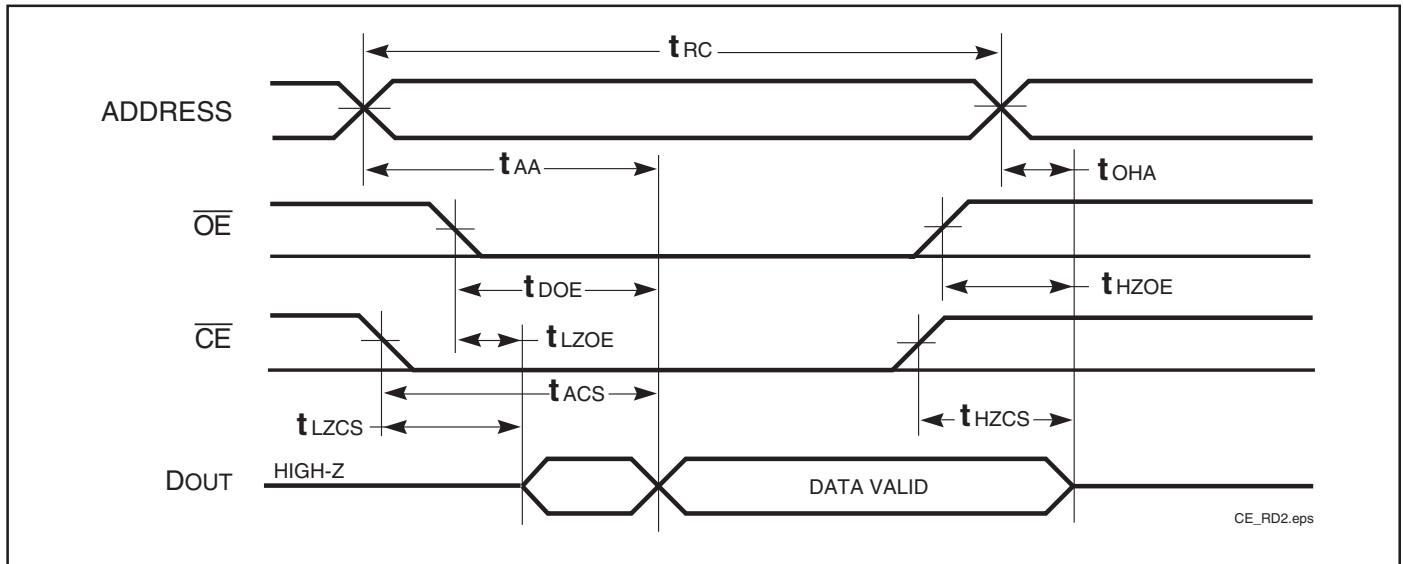
| Parameter | Unit |
|----------------------------------------------|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing and Reference Levels | 1.5V |
| Output Load | See Figures 1 and 2 |

AC TEST LOADS

Figure 1

Figure 2

AC WAVEFORMS
READ CYCLE NO. 1^(1,2)



READ CYCLE NO. 2^(1,3)



Notes:

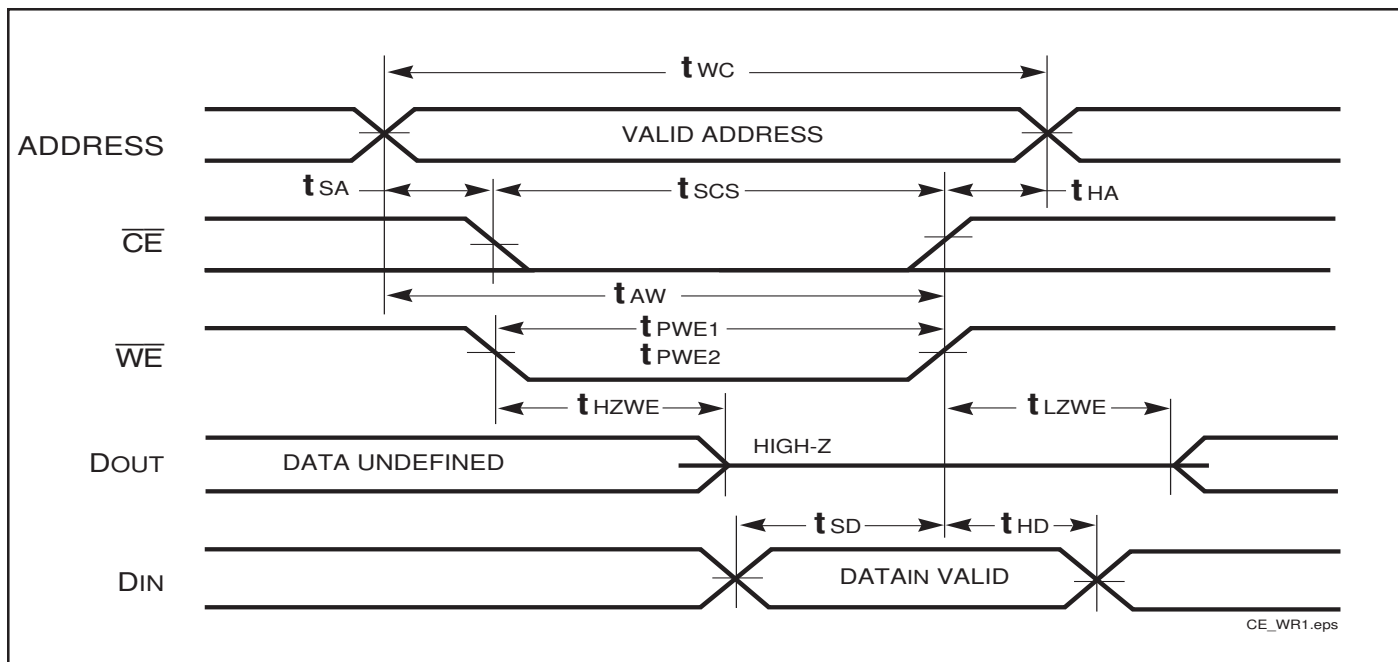
1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

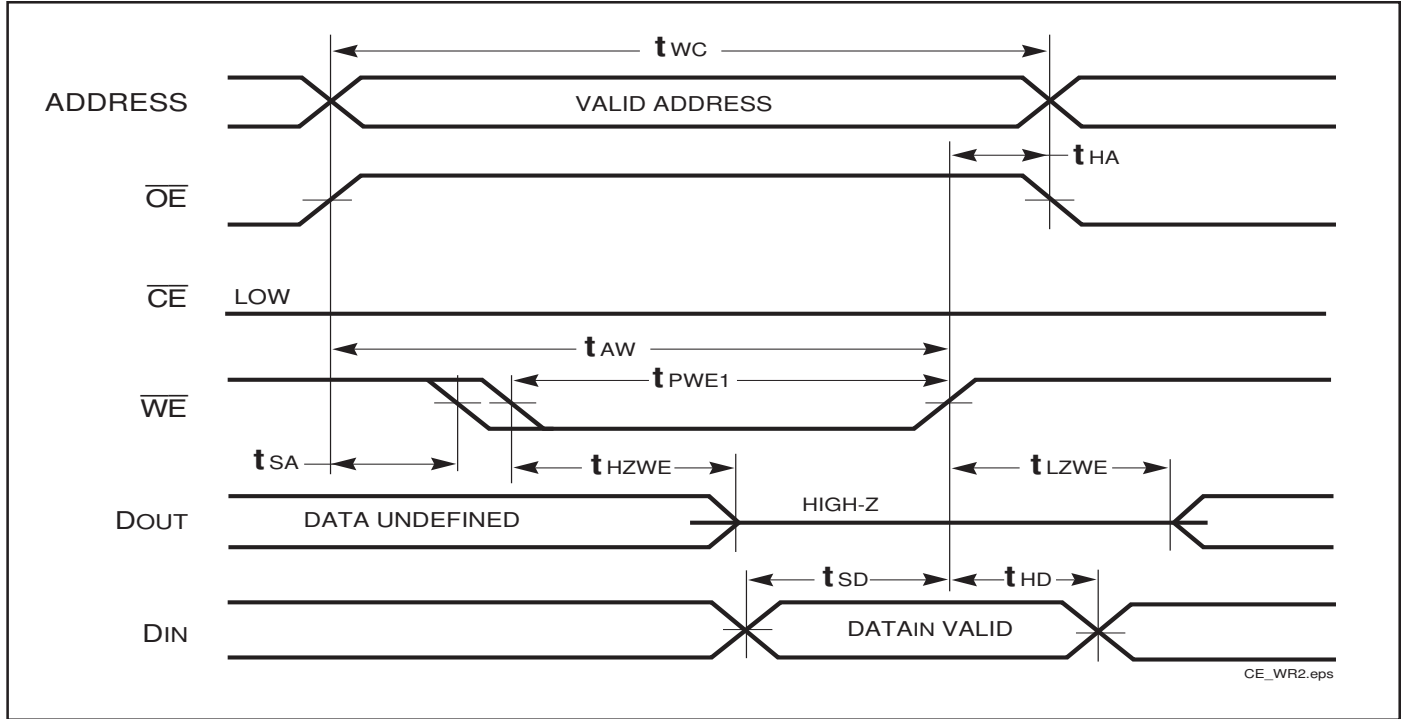
| Symbol | Parameter | -10 ns | | -12 ns | | Unit |
|------------------|-----------------------------------------------------|--------|-----|--------|------|------|
| | | Min. | Max | Min. | Max. | |
| t_{WC} | Write Cycle Time | 10 | — | 12 | — | ns |
| t_{SCS} | \overline{CE} to Write End | 9 | — | 10 | — | ns |
| t_{AW} | Address Setup Time to Write End | 9 | — | 10 | — | ns |
| t_{HA} | Address Hold from Write End | 0 | — | 0 | — | ns |
| t_{SA} | Address Setup Time | 0 | — | 0 | — | ns |
| t_{PWE1} | \overline{WE} Pulse Width (\overline{OE} LOW) | 9 | — | 9 | — | ns |
| t_{PWE2} | \overline{WE} Pulse Width (\overline{OE} HIGH) | 8 | — | 8 | — | ns |
| t_{SD} | Data Setup to Write End | 7 | — | 7 | — | ns |
| t_{HD} | Data Hold from Write End | 0 | — | 0 | — | ns |
| $t_{HZWE}^{(2)}$ | \overline{WE} LOW to High-Z Output | — | 6 | — | 6 | ns |
| $t_{LZWE}^{(2)}$ | \overline{WE} HIGH to Low-Z Output | 0 | — | 0 | — | ns |

Notes:

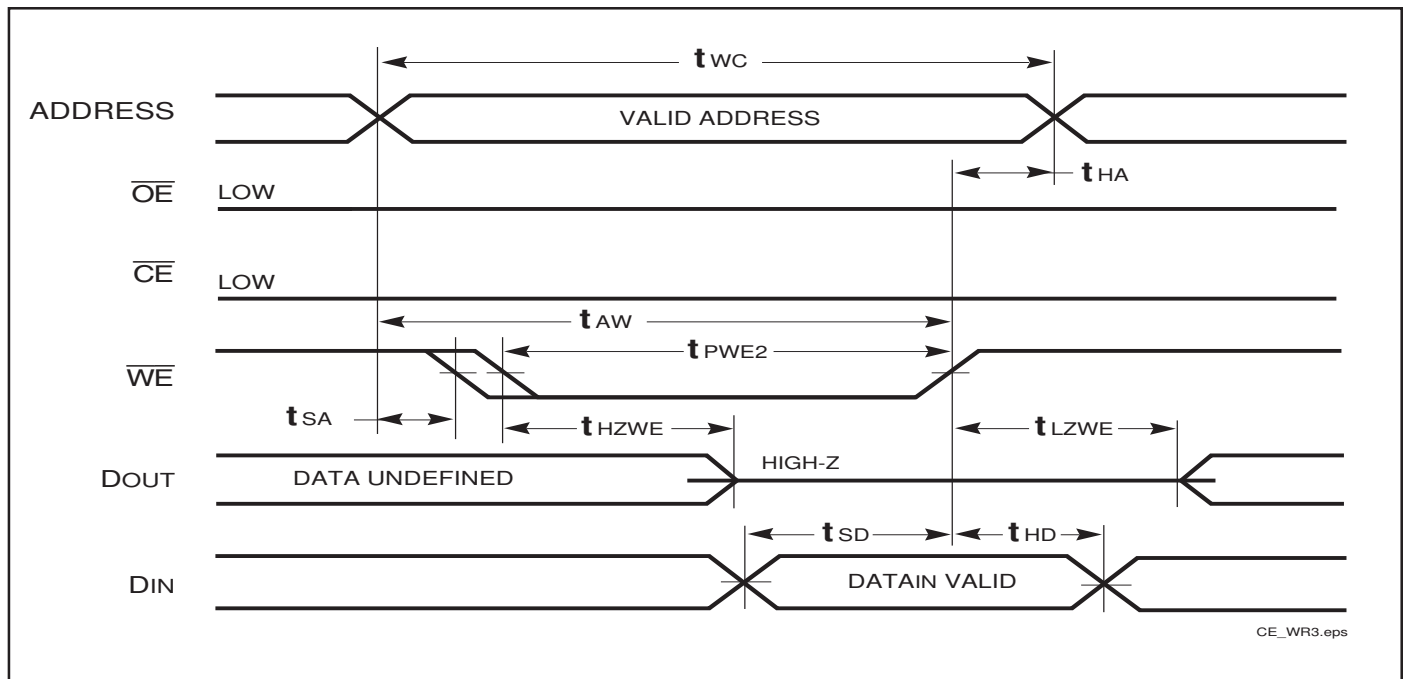
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS
WRITE CYCLE NO. 1 (\overline{WE} Controlled)^(1,2)


WRITE CYCLE NO. 2 (\overline{OE} is HIGH During Write Cycle) ^(1,2)



WRITE CYCLE NO. 3 (\overline{OE} is LOW During Write Cycle) ⁽¹⁾



Notes:

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $OE \geq V_{IH}$.

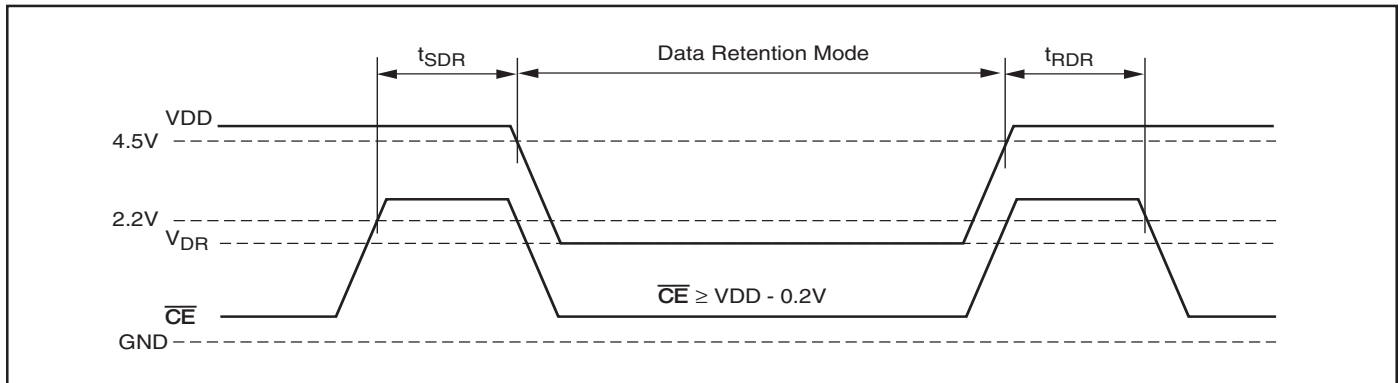
DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|------------------|------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------|------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | 2.0 | | 5.5 | V |
| I _{DR} | Data Retention Current | V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ V _{SS} + 0.2V | — | 50 | 90 | μA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | 0 | | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | t _{RC} | | — | ns |

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)

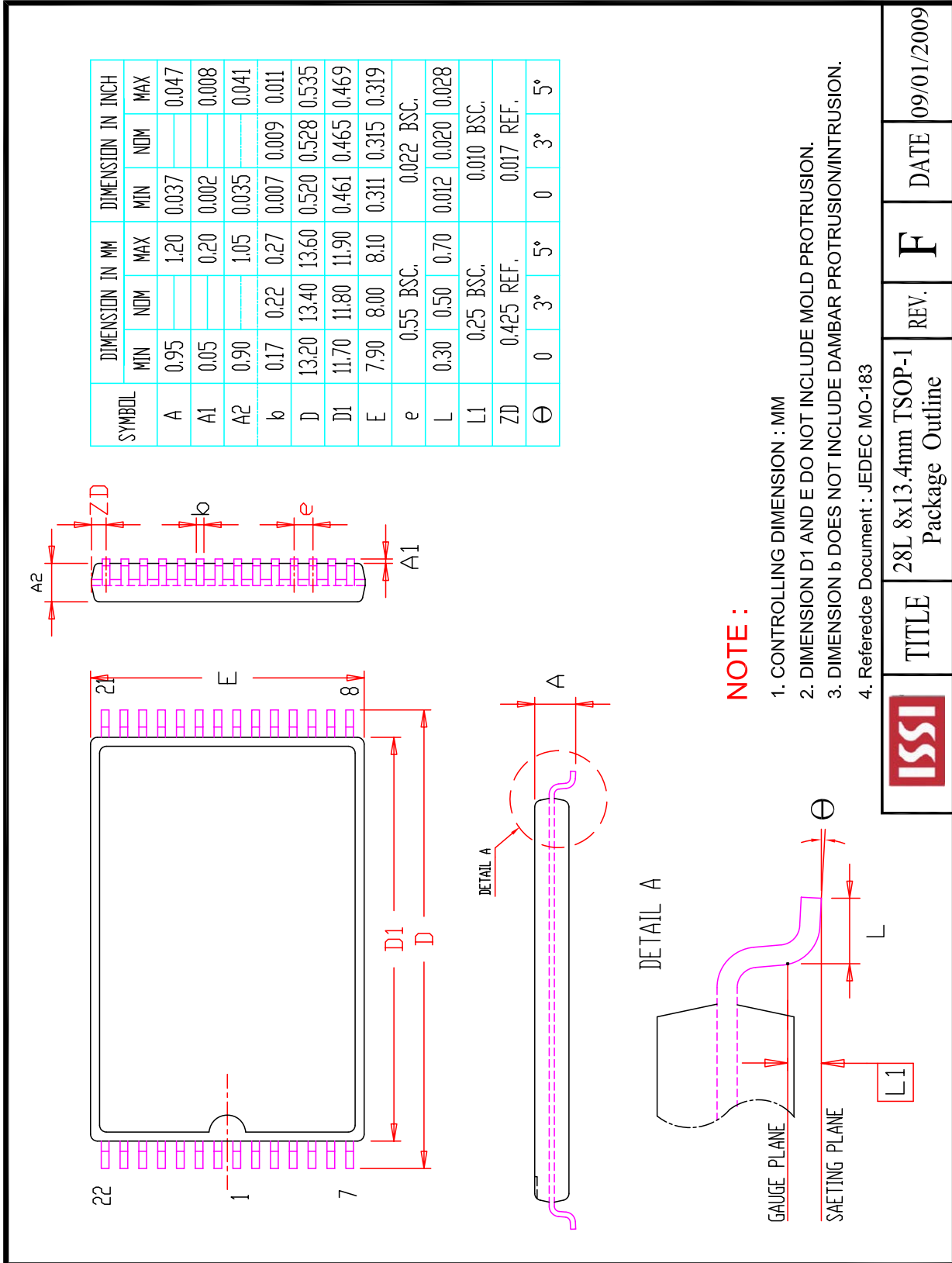


ORDERING INFORMATION: IS61C256AL**Commercial Range: 0 °C to +70 °C**

| Speed (ns) | Order Part Number | Package |
|-------------------|--------------------------|--------------------------------|
| 10 | IS61C256AL-10JL | 300-mil Plastic SOJ, Lead-free |
| | IS61C256AL-10T | TSOP (Type 1) |
| | IS61C256AL-10TL | TSOP (Type 1), Lead-free |
| 12 | IS61C256AL-12JL | 300-mil Plastic SOJ, Lead-free |
| | IS61C256AL-12T | TSOP (Type 1) |
| | IS61C256AL-12TL | TSOP (Type 1), Lead-free |

Industrial Range: -40 °C to +85 °C

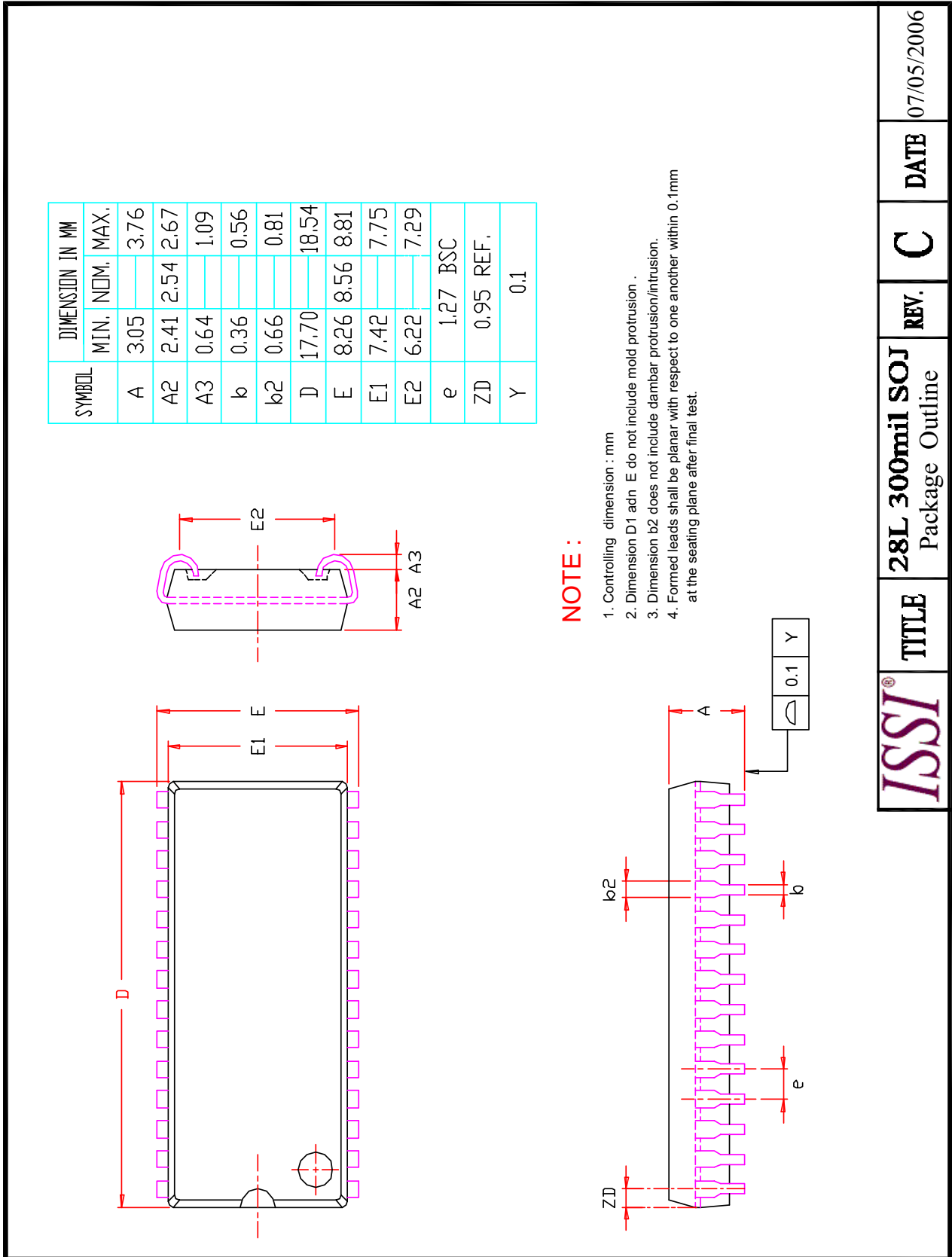
| Speed (ns) | Order Part Number | Package |
|-------------------|--------------------------|--------------------------------|
| 12 | IS61C256AL-12JLI | 300-mil Plastic SOJ, Lead-free |
| | IS61C256AL-12TI | TSOP (Type 1) |
| | IS61C256AL-12TLI | TSOP (Type 1), Lead-free |



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

| | | | |
|--|-------------------------------------|------|------------|
| | TITLE | REV. | DATE |
| | 28L 8x13.4mm TSOP-1 Package Outline | F | 09/01/2009 |



| SYMBOL | DIMENSION IN MM | |
|--------|-----------------|-----------|
| | MIN. | NOM. MAX. |
| A | 3.05 | 3.76 |
| A2 | 2.41 | 2.54 2.67 |
| A3 | 0.64 | 1.09 |
| k | 0.36 | 0.56 |
| k2 | 0.66 | 0.81 |
| D | 17.70 | 18.54 |
| E | 8.26 | 8.56 8.81 |
| E1 | 7.42 | 7.75 |
| E2 | 6.22 | 7.29 |
| e | 1.27 BSC | |
| ZD | 0.95 REF. | |
| Y | 0.1 | |

NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

ISSI

TITLE

28L 300mil SOJ
Package Outline

REV. C

DATE

07/05/2006

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