Micropower, Single- and Dual-Supply, Rail-to-Rail Instrumentation Amplifier

AD627

FEATURES

- Micropower, 85 µA maximum supply current
- Wide power supply range (+2.2 V to ±18 V)
- Easy to use
  - Gain set with one external resistor
  - Gain range 5 (no resistor) to 1000
- Higher performance than discrete designs
- Rail-to-rail output swing
- High accuracy dc performance
  - 0.03% typical gain accuracy (G = +5) (AD627A)
  - 10 ppm/°C typical gain drift (G = +5)
  - 125 µV maximum input offset voltage (AD627B dual supply)
  - 200 µV maximum input offset voltage (AD627A dual supply)
  - 1 µV/°C maximum input offset voltage drift (AD627B)
  - 3 µV/°C maximum input offset voltage drift (AD627A)
  - 10 nA maximum input bias current
- Noise: 38 nV/√Hz RTI noise @ 1 kHz (G = +100)
- Excellent ac specifications
  - AD627A: 77 dB minimum CMRR (G = +5)
  - AD627B: 83 dB minimum CMRR (G = +5)
  - 80 kHz bandwidth (G = +5)
  - 135 µs settling time to 0.01% (G = +5, 5 V step)

APPLICATIONS

- 4 to 20 mA loop-powered applications
- Low power medical instrumentation—ECG, EEG
- Transducer interfacing
- Thermocouple amplifiers
- Industrial process controls
- Low power data acquisition
- Portable battery-powered instruments

FUNCTIONAL BLOCK DIAGRAM

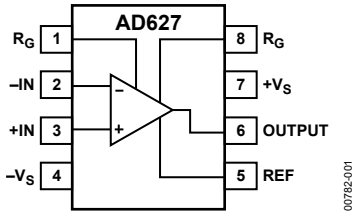

Figure 1. 8-Lead PDIP (N) and SOIC_N (R)

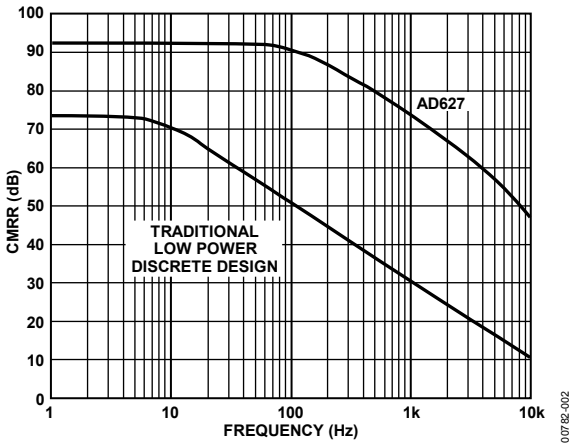

Figure 2. CMRR vs. Frequency, ±5 Vs, Gain = +5

GENERAL DESCRIPTION

The AD627 is an integrated, micropower instrumentation amplifier that delivers rail-to-rail output swing on single and dual (+2.2 V to ±18 V) supplies. The AD627 provides excellent ac and dc specifications while operating at only 85 µA maximum.

The AD627 offers superior flexibility by allowing the user to set the gain of the device with a single external resistor while conforming to the 8-lead industry-standard pinout configuration. With no external resistor, the AD627 is configured for a gain of 5. With an external resistor, it can be set to a gain of up to 1000.

A wide supply voltage range (+2.2 V to ±18 V) and micropower current consumption make the AD627 a perfect fit for a wide range of applications. Single-supply operation, low power consumption, and rail-to-rail output swing make the AD627 ideal for battery-powered applications. Its rail-to-rail output stage maximizes dynamic range when operating from low supply voltages. Dual-supply operation (±15 V) and low power consumption make the AD627 ideal for industrial applications, including 4 to 20 mA loop-powered systems.

The AD627 does not compromise performance, unlike other micropower instrumentation amplifiers. Low voltage offset, offset drift, gain error, and gain drift minimize errors in the system. The AD627 also minimizes errors over frequency by providing excellent CMRR over frequency. Because the CMRR remains high up to 200 Hz, line noise and line harmonics are rejected.

The AD627 provides superior performance, uses less circuit board area, and costs less than micropower discrete designs.

Rev. D

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REVISION HISTORY

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SPECIFICATIONS

SINGLE SUPPLY

Typical @ 25°C single supply, V_S = 3 V and 5 V, and R_L = 20 kΩ, unless otherwise noted.

Table 1.

		AD627A			AD627B			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
GAIN	G = +5 + (200 kΩ/R_G)							
Gain Range		5		1000	5		1000	V/V
Gain Error[1]	V_{OUT} = (–V_S) + 0.1 to (+V_S) – 0.15							
G = +5			0.03	0.10		0.01	0.06	%
G = +10			0.15	0.35		0.10	0.25	%
G = +100			0.15	0.35		0.10	0.25	%
G = +1000			0.50	0.70		0.25	0.35	%
Nonlinearity								
G = +5			10	100		10	100	ppm
G = +100			20	100		20	100	ppm
Gain vs. Temperature[1]								
G = +5			10	20		10	20	ppm/°C
G > +5			–75			–75		ppm/°C
VOLTAGE OFFSET								
Input Offset, V_{OSI}[2]			50	250		25	150	µV
Over Temperature	V_{CM} = V_{REF} = +V_S/2			445			215	µV
Average TC			0.1	3		0.1	1	µV/°C
Output Offset, V_{OSO}				1000			500	µV
Over Temperature				1650			1150	µV
Average TC			2.5	10		2.5	10	µV/°C
Offset Referred to the Input vs. Supply (PSRR)								
G = +5		86	100		86	100		dB
G = +10		100	120		100	120		dB
G = +100		110	125		110	125		dB
G = +1000		110	125		110	125		dB
INPUT CURRENT								
Input Bias Current			3	10		3	10	nA
Over Temperature				15			15	nA
Average TC			20			20		pA/°C
Input Offset Current			0.3	1		0.3	1	nA
Over Temperature				2			2	nA
Average TC			1			1		pA/°C
INPUT								
Input Impedance								
Differential			20||2			20||2		GΩ||pF
Common-Mode			20||2			20||2		GΩ||pF
Input Voltage Range[3]	V_S = 2.2 V to 36 V	(–V_S) – 0.1		(+V_S) – 1	(–V_S) – 0.1		(+V_S) – 1	V
Common-Mode Rejection Ratio[3] DC to 60 Hz with 1 kΩ Source Imbalance	V_{REF} = V_S/2							
G = +5	V_S = 3 V, V_{CM} = 0 V to 1.9 V	77	90		83	96		dB
G = +5	V_S = 5 V, V_{CM} = 0 V to 3.7 V	77	90		83	96		dB
OUTPUT								
Output Swing	R_L = 20 kΩ	(–V_S) + 25		(+V_S) – 70	(–V_S) + 25		(+V_S) – 70	mV
	R_L = 100 kΩ	(–V_S) + 7		(+V_S) – 25	(–V_S) + 7		(+V_S) – 25	mV
Short-Circuit Current	Short circuit to ground		±25			±25		mA

Parameter	Conditions	AD627A Min	AD627A Typ	AD627A Max	AD627B Min	AD627B Typ	AD627B Max	Unit
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = +5			80			80		kHz
G = +100			3			3		kHz
G = +1000			0.4			0.4		kHz
Slew Rate			+0.05/−0.07		+0.05/−0.07			V/µs
Settling Time to 0.01%	V_S = 3 V, 1.5 V output step							
G = +5			65			65		µs
G = +100			290			290		µs
Settling Time to 0.01%	V_S = 5 V, 2.5 V output step							
G = +5			85			85		µs
G = +100			330			330		µs
Overload Recovery	50% input overload		3			3		µs

[1] Does not include effects of External Resistor R_G.
[2] See Table 8 for total RTI errors.
[3] See the Using the AD627 section for more information on the input range, gain range, and common-mode range.

DUAL SUPPLY

Typical @ 25°C dual supply, V_S = ±5 V and ±15 V, and R_L = 20 kΩ, unless otherwise noted.

Table 2.

		AD627A			AD627B			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
GAIN	G = +5 + (200 kΩ/R_G)							
Gain Range		5		1000	5		1000	V/V
Gain Error[1]	V_{OUT} = (–V_S) + 0.1 to (+V_S) – 0.15							
G = +5			0.03	0.10		0.01	0.06	%
G = +10			0.15	0.35		0.10	0.25	%
G = +100			0.15	0.35		0.10	0.25	%
G = +1000			0.50	0.70		0.25	0.35	%
Nonlinearity								
G = +5	V_S = ±5 V/±15 V		10/25	100		10/25	100	ppm
G = +100	V_S = ±5 V/±15 V		10/15	100		10/15	100	ppm
Gain vs. Temperature[1]								
G = +5			10	20		10	20	ppm/°C
G > +5			–75			–75		ppm/°C
VOLTAGE OFFSET	Total RTI error = V_{OSI} + V_{OSO}/G							
Input Offset, V_{OSI}[2]			25	200		25	125	µV
Over Temperature	V_{CM} = V_{REF} = 0 V			395			190	µV
Average TC			0.1	3		0.1	1	µV/°C
Output Offset, V_{OSO}				1000			500	µV
Over Temperature				1700			1100	µV
Average TC			2.5	10		2.5	10	µV/°C
Offset Referred to the Input vs. Supply (PSRR)								
G = +5		86	100		86	100		dB
G = +10		100	120		100	120		dB
G = +100		110	125		110	125		dB
G = +1000		110	125		110	125		dB
INPUT CURRENT								
Input Bias Current			2	10		2	10	nA
Over Temperature				15			15	nA
Average TC			20			20		pA/°C
Input Offset Current			0.3	1		0.3	1	nA
Over Temperature				5			5	nA
Average TC			5			5		pA/°C
INPUT								
Input Impedance								
Differential			20||2			20||2		GΩ||pF
Common Mode			20||2			20||2		GΩ||pF
Input Voltage Range[3]	V_S = ±1.1 V to ±18 V	(–V_S) – 0.1		(+V_S) – 1	(–V_S) – 0.1		(+V_S) – 1	V
Common-Mode Rejection Ratio[3] DC to 60 Hz with 1 kΩ Source Imbalance								
G = +5 to +1000	V_S = ±5 V, V_{CM} = –4 V to +3.0 V	77	90		83	96		dB
G = +5 to +1000	V_S = ±15 V, V_{CM} = –12 V to +10.9 V	77	90		83	96		dB
OUTPUT								
Output Swing	R_L = 20 kΩ	(–V_S) + 25		(+V_S) – 70	(–V_S) + 25		(+V_S) – 70	mV
	R_L = 100 kΩ	(–V_S) + 7		(+V_S) – 25	(–V_S) + 7		(+V_S) – 25	mV
Short-Circuit Current	Short circuit to ground		±25			±25		mA

Parameter	Conditions	AD627A Min	AD627A Typ	AD627A Max	AD627B Min	AD627B Typ	AD627B Max	Unit
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = +5			80			80		kHz
G = +100			3			3		kHz
G = +1000			0.4			0.4		kHz
Slew Rate			+0.05/−0.06			+0.05/−0.06		V/µs
Settling Time to 0.01%	V_S = ±5 V, +5 V output step							
G = +5			135			135		µs
G = +100			350			350		µs
Settling Time to 0.01%	V_S = ±15 V, +15 V output step							
G = +5			330		330			µs
G = +100			560		560			µs
Overload Recovery	50% input overload		3		3			µs

[1] Does not include effects of External Resistor R_G.
[2] See Table 8 for total RTI errors.
[3] See the Using the AD627 section for more information on the input range, gain range, and common-mode range.

DUAL AND SINGLE SUPPLIES

Table 3.

Parameter	Conditions	AD627A Min	AD627A Typ	AD627A Max	AD627B Min	AD627B Typ	AD627B Max	Unit
NOISE								
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e_{ni})^2 + (e_{no}/R_G)^2}$							
Input, Voltage Noise, e_{ni}			38			38		nV/√Hz
Output, Voltage Noise, e_{no}			177			177		nV/√Hz
RTI, 0.1 Hz to 10 Hz								
G = +5			1.2			1.2		µV p-p
G = +1000			0.56			0.56		µV p-p
Current Noise	f = 1 kHz		50			50		fA/√Hz
0.1 Hz to 10 Hz			1.0			1.0		pA p-p
REFERENCE INPUT								
R_{IN}	R_G = ∞		125			125		kΩ
Gain to Output			1			1		
Voltage Range[1]								
POWER SUPPLY								
Operating Range	Dual supply	±1.1		±18	±1.1		±18	V
	Single supply	2.2		36	2.2		36	V
Quiescent Current			60	85		60	85	µA
Over Temperature			200			200		nA/°C
TEMPERATURE RANGE								
For Specified Performance		−40		+85	−40		+85	°C

[1] See Using the AD627 section for more information on the reference terminal, input range, gain range, and common-mode range.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation[1]	
PDIP (N-8)	1.3 W
SOIC_N (R-8)	0.8 W
–IN, +IN	$-V_S$ – 20 V to $+V_S$ + 20 V
Common-Mode Input Voltage	$-V_S$ – 20 V to $+V_S$ + 20 V
Differential Input Voltage (+IN – (–IN))	$+V_S$ – ($-V_S$)
Output Short-Circuit Duration	Indefinite
Storage Temperature Range (N, R)	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Specification is for device in free air:
8-lead PDIP package: θ_{JA} = 90°C/W.
8-lead SOIC_N package: θ_{JA} = 155°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

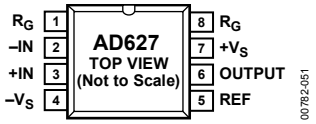

Figure 3. 8-Lead PDIP Pin Configuration

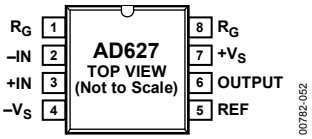

Figure 4. 8-Lead SOIC_N Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_G	External Gain Setting Resistor. Place gain setting resistor across R_G pins to set the gain.
2	−IN	Negative Input.
3	+IN	Positive Input.
4	$-V_S$	Negative Voltage Supply Pin.
5	REF	Reference Pin. Drive with low impedance voltage source to level shift the output voltage.
6	OUTPUT	Output Voltage.
7	$+V_S$	Positive Supply Voltage.
8	R_G	External Gain Setting Resistor. Place gain setting resistor across R_G pins to set the gain.

TYPICAL PERFORMANCE CHARACTERISTICS

At 25°C, V_S = ±5 V, R_L = 20 kΩ, unless otherwise noted.

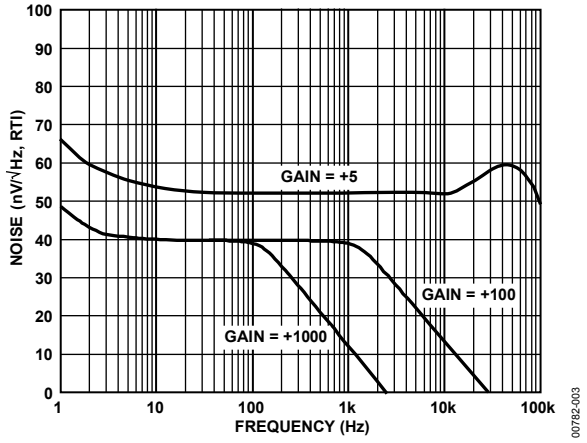

Figure 5. Voltage Noise Spectral Density vs. Frequency

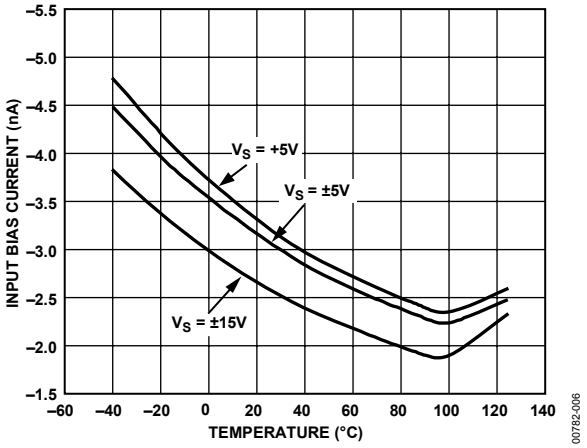

Figure 8. Input Bias Current vs. Temperature

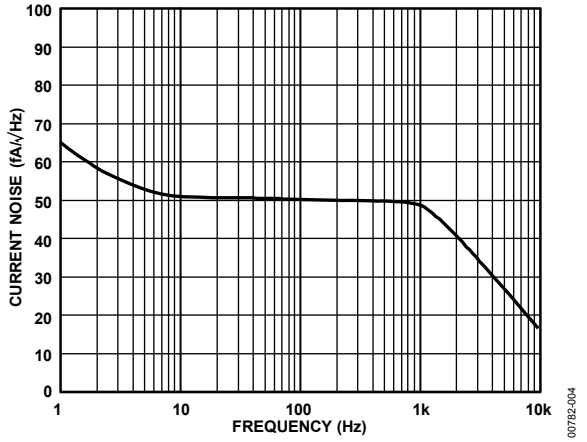

Figure 6. Current Noise Spectral Density vs. Frequency

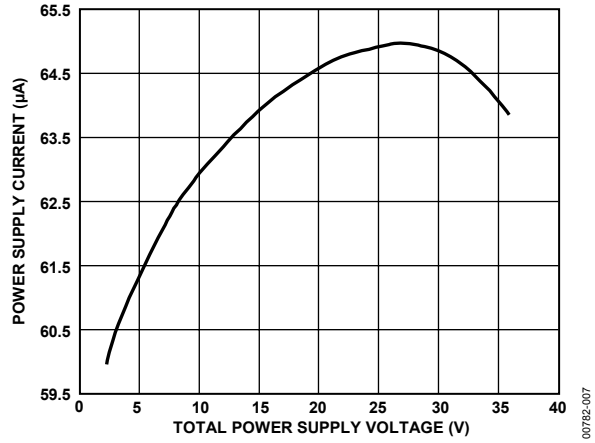

Figure 9. Supply Current vs. Supply Voltage

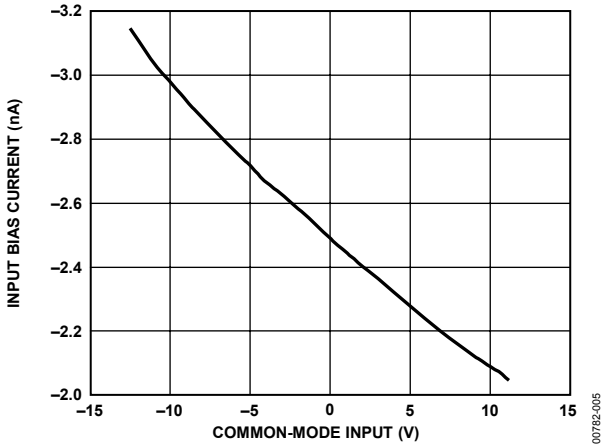

Figure 7. Input Bias Current vs. CMV, V_S = ±15 V

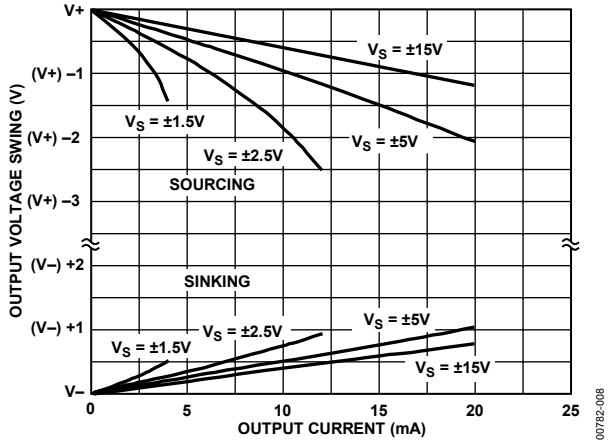

Figure 10. Output Voltage Swing vs. Output Current

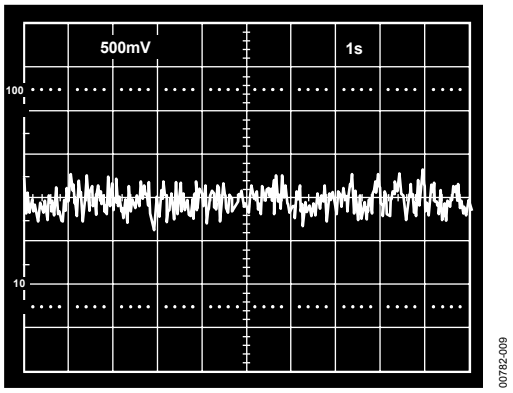

Figure 11. 0.1 Hz to 10 Hz Current Noise (0.71 pA/DIV)

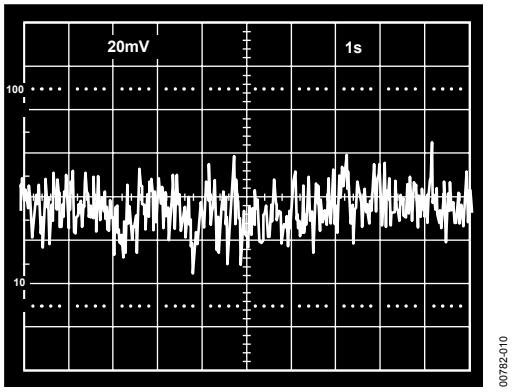

Figure 12. 0.1 Hz to 10 Hz RTI Voltage Noise (400 nV/DIV), G = +5

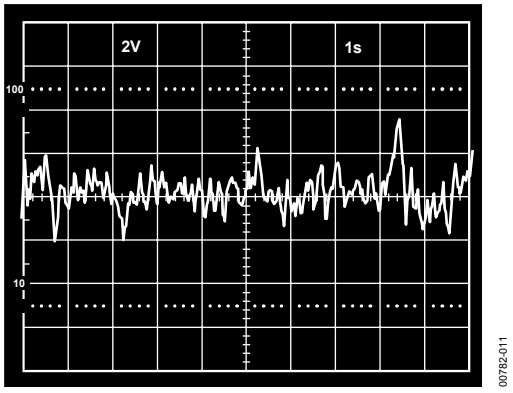

Figure 13. 0.1 Hz to 10 Hz RTI Voltage Noise (200 nV/DIV), G = +1000

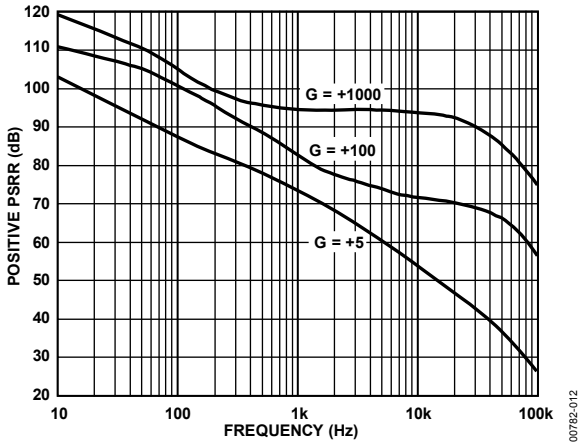

Figure 14. Positive PSRR vs. Frequency, ±5 V

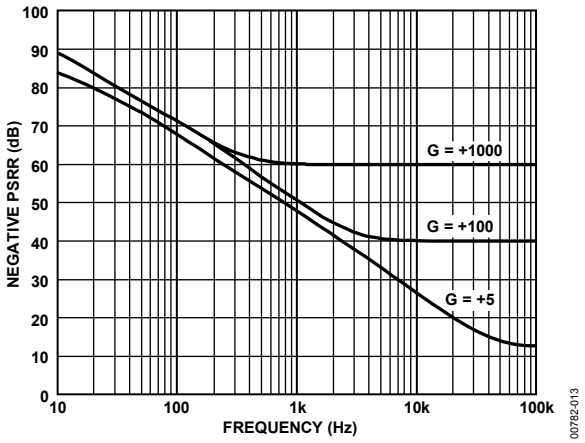

Figure 15. Negative PSRR vs. Frequency, ±5 V

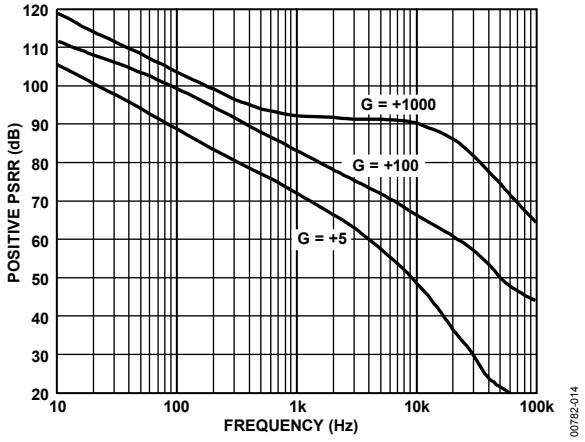

Figure 16. Positive PSRR vs. Frequency (V_S = 5 V, 0 V)

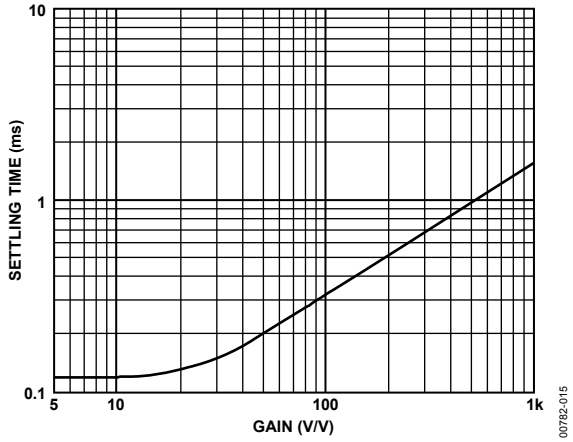

Figure 17. Settling Time to 0.01% vs. Gain for a 5 V Step at Output, R_L = 20 kΩ, C_L = 100 pF, V_S = ±5 V

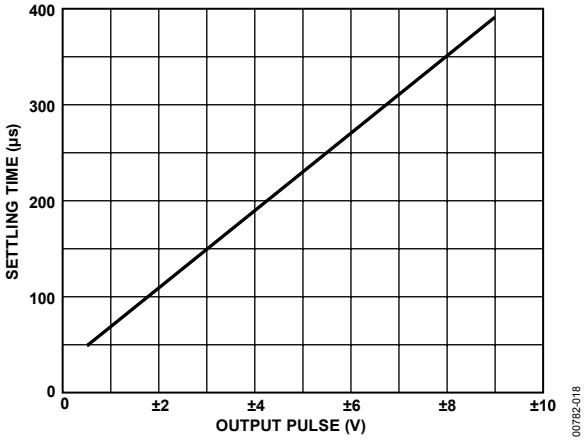

Figure 20. Settling Time to 0.01% vs. Output Swing, G = +5, R_L = 20 kΩ, C_L = 100 pF

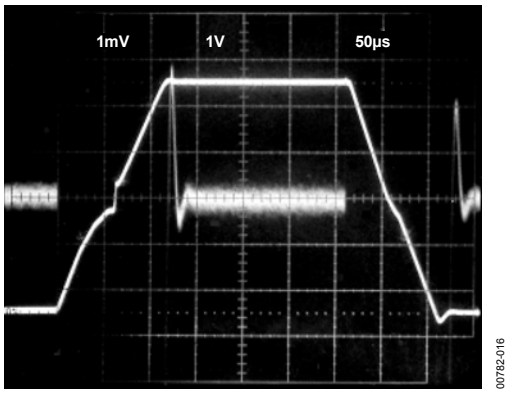

Figure 18. Large Signal Pulse Response and Settling Time, G = –5, R_L = 20 kΩ, C_L = 100 pF (1.5 mV = 0.01%)

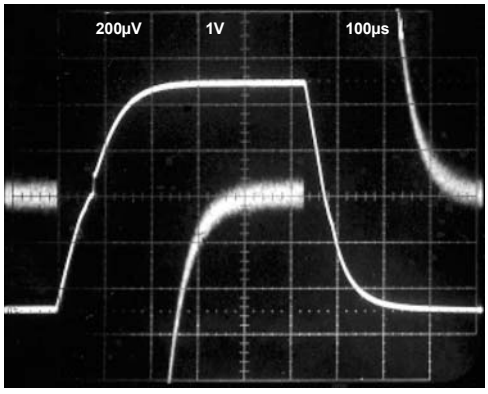

Figure 21. Large Signal Pulse Response and Settling Time, G = –100, R_L = 20 kΩ, C_L = 100 pF (100 µV = 0.01%)

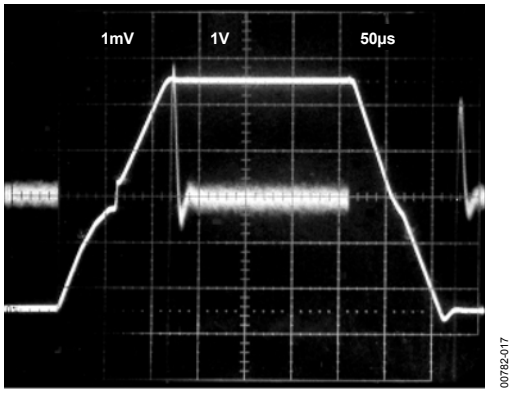

Figure 19. Large Signal Pulse Response and Settling Time, G = –10, R_L = 20 kΩ, C_L = 100 pF (1.0 mV = 0.01%)

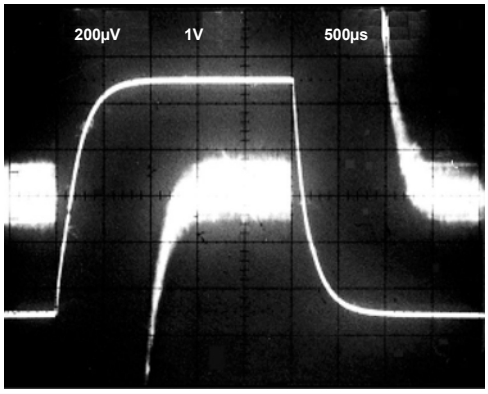

Figure 22. Large Signal Pulse Response and Settling Time, G = –1000, R_L = 20 kΩ, C_L = 100 pF (10 µV = 0.01%)

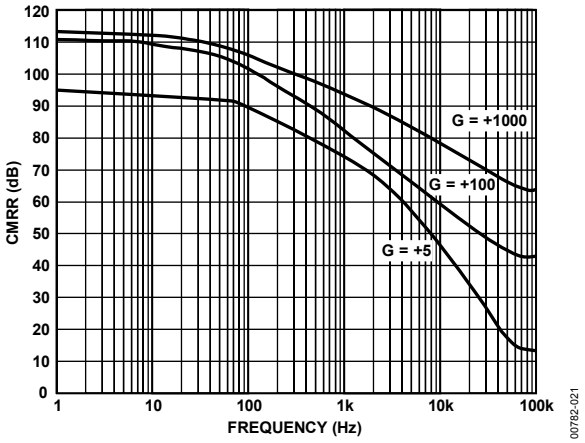

Figure 23. CMRR vs. Frequency, ±5 V_S (CMV = 200 mV p-p)

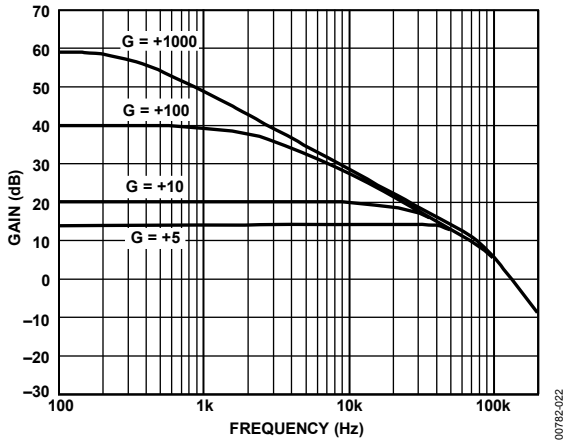

Figure 24. Gain vs. Frequency (V_S = 5 V, 0 V), V_{REF} = 2.5 V

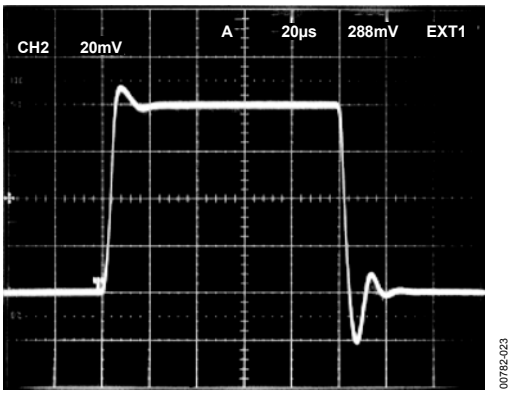

Figure 25. Small Signal Pulse Response, G = +5, R_L = 20 kΩ, C_L = 50 pF

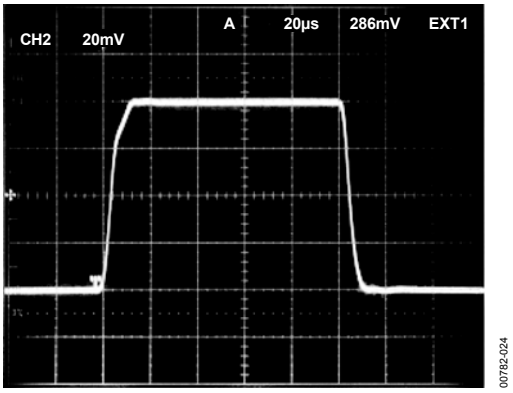

Figure 26. Small Signal Pulse Response, G = +10, R_L = 20 kΩ, C_L = 50 pF

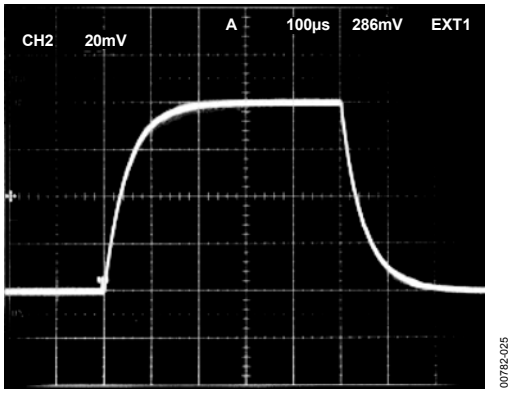

Figure 27. Small Signal Pulse Response, G = +100, R_L = 20 kΩ, C_L = 50 pF

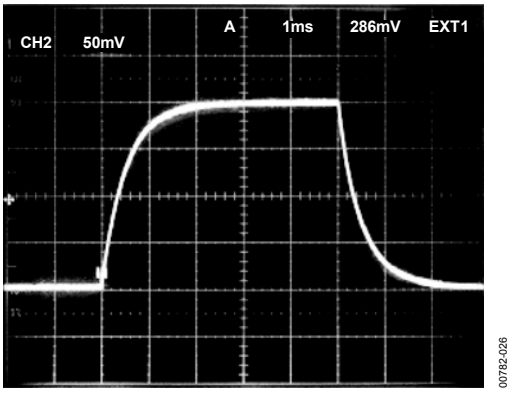

Figure 28. Small Signal Pulse Response, G = +1000, R_L = 20 kΩ, C_L = 50 pF

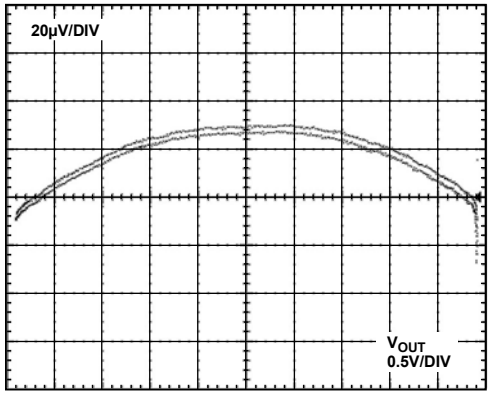

Figure 29. Gain Nonlinearity, Negative Input, V_S = ±2.5 V, G = +5 (4 ppm/DIV)

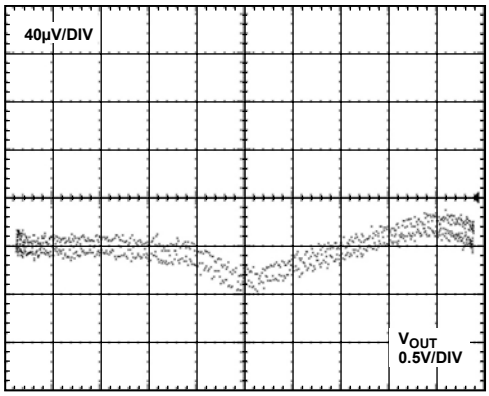

Figure 30. Gain Nonlinearity, Negative Input, V_S = ±2.5 V, G = +100 (8 ppm/DIV)

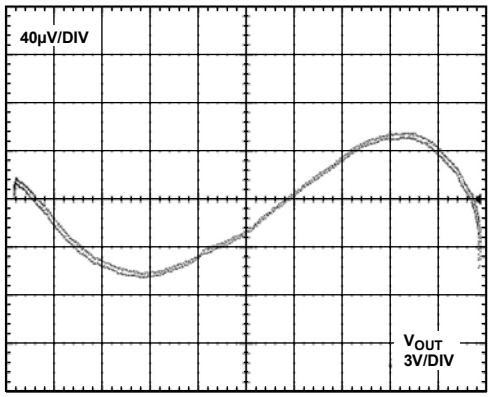

Figure 31. Gain Nonlinearity, Negative Input, V_S = ±15 V, G = +5 (1.5 ppm/DIV)

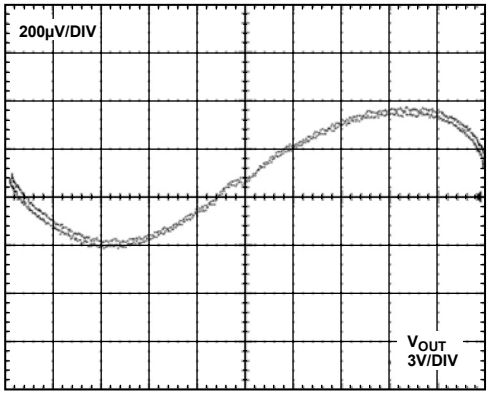

Figure 32. Gain Nonlinearity, Negative Input, V_S = ±15 V, G = +100 (7 ppm/DIV)

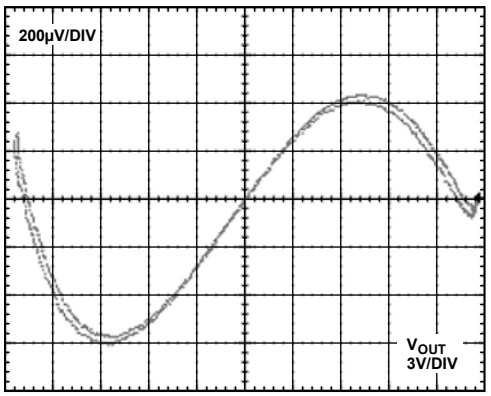

Figure 33. Gain Nonlinearity, Negative Input, V_S = ±15 V, G = +5 (7 ppm/DIV)

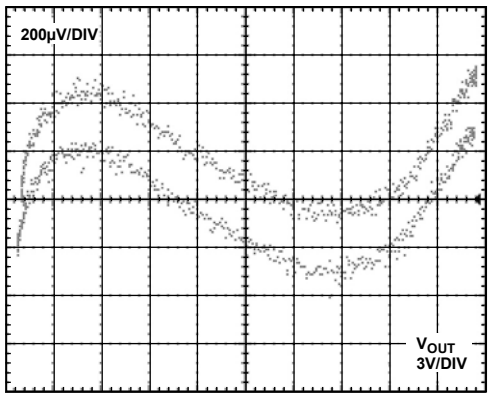

Figure 34. Gain Nonlinearity, Negative Input, V_S = ±15 V, G = +100 (7 ppm/DIV)

THEORY OF OPERATION

The AD627 is a true instrumentation amplifier, built using two feedback loops. Its general properties are similar to those of the classic two-op-amp instrumentation amplifier configuration but internally the details are somewhat different. The AD627 uses a modified current feedback scheme, which, coupled with interstage feedforward frequency compensation, results in a much better common-mode rejection ratio (CMRR) at frequencies above dc (notably the line frequency of 50 Hz to 60 Hz) than might otherwise be expected of a low power instrumentation amplifier.

In Figure 35, A1 completes a feedback loop that, in conjunction with V1 and R5, forces a constant collector current in Q1. Assume that the gain-setting resistor (R_G) is not present. Resistors R2 and R1 complete the loop and force the output of A1 to be equal to the voltage on the inverting terminal with a gain of nearly 1.25. A2 completes a nearly identical feedback loop that forces a current in Q2 that is nearly identical to that in Q1; A2 also provides the output voltage. When both loops are balanced, the gain from the noninverting terminal to V_{OUT} is equal to 5, whereas the gain from the output of A1 to V_{OUT} is equal to −4.

The inverting terminal gain of A1 (1.25) times the gain of A2 (−4) makes the gain from the inverting and noninverting terminals equal.

The differential mode gain is equal to 1 + R4/R3, nominally 5, and is factory trimmed to 0.01% final accuracy. Adding an external gain setting resistor (R_G) increases the gain by an amount equal to (R4 + R1)/R_G. The output voltage of the AD627 is given by

$$V_{OUT} = [V_{IN}(+) - V_{IN}(-)] \times (5 + 200\ \text{k}\Omega/R_G) + V_{REF} \quad (1)$$

Laser trims are performed on R1 through R4 to ensure that their values are as close as possible to the absolute values in the gain equation. This ensures low gain error and high common-mode rejection at all practical gains.

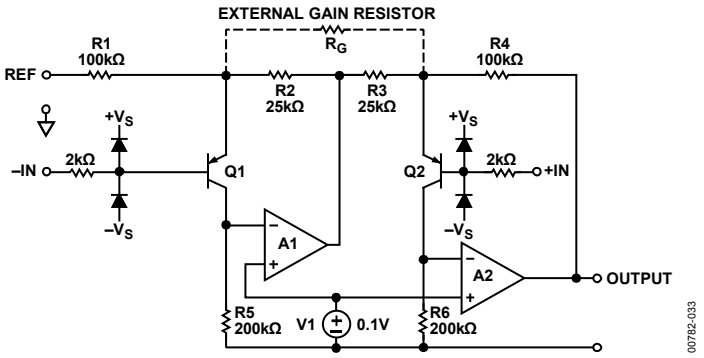

Figure 35. Simplified Schematic

USING THE AD627

BASIC CONNECTIONS

Figure 36 shows the basic connection circuit for the AD627. The $+V_S$ and $-V_S$ terminals connect to the power supply. The supply can be either bipolar (V_S = ±1.1 V to ±18 V) or single supply ($-V_S$ = 0 V, $+V_S$ = 2.2 V to 36 V). Capacitively decouple the power supplies close to the power pins of the device. For best results, use surface-mount 0.1 μF ceramic chip capacitors.

The input voltage can be single-ended (tie either −IN or +IN to ground) or differential. The difference between the voltage on the inverting and noninverting pins is amplified by the programmed gain. The gain resistor programs the gain as described in the Setting the Gain and Reference Terminal sections. Basic connections are shown in Figure 36. The output signal appears as the voltage difference between the output pin and the externally applied voltage on the REF pin, as shown in Figure 37.

SETTING THE GAIN

The gain of the AD627 is resistor programmed by R_G, or, more precisely, by whatever impedance appears between Pin 1 and Pin 8.

The gain is set according to

$$Gain = 5 + (200\ \text{k}\Omega/R_G) \text{ or } R_G = 200\ \text{k}\Omega/(Gain - 5) \quad (2)$$

Therefore, the minimum achievable gain is 5 (for 200 kΩ/(Gain − 5)). With an internal gain accuracy of between 0.05% and 0.7%, depending on gain and grade, a 0.1% external gain resistor is appropriate to prevent significant degradation of the overall gain error. However, 0.1% resistors are not available in a wide range of values and are quite expensive. Table 6 shows recommended gain resistor values using 1% resistors. For all gains, the size of the gain resistor is conservatively chosen as the closest value from the standard resistor table that is higher than the ideal value. This results in a gain that is always slightly less than the desired gain, thereby preventing clipping of the signal at the output due to resistor tolerance.

The internal resistors on the AD627 have a negative temperature coefficient of −75 ppm/°C maximum for gains > 5. Using a gain resistor that also has a negative temperature coefficient of −75 ppm/°C or less tends to reduce the overall gain drift of the circuit.

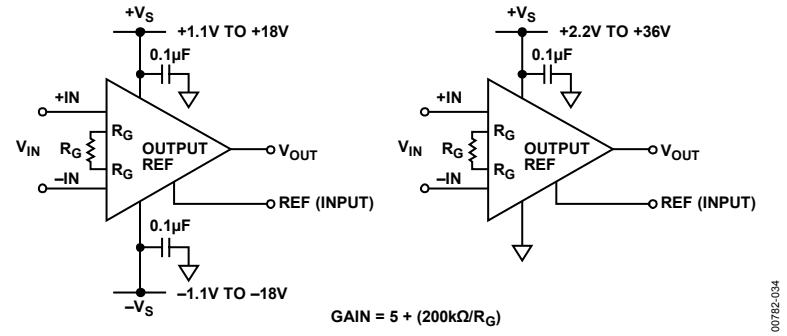

Figure 36. Basic Connections for Single and Dual Supplies

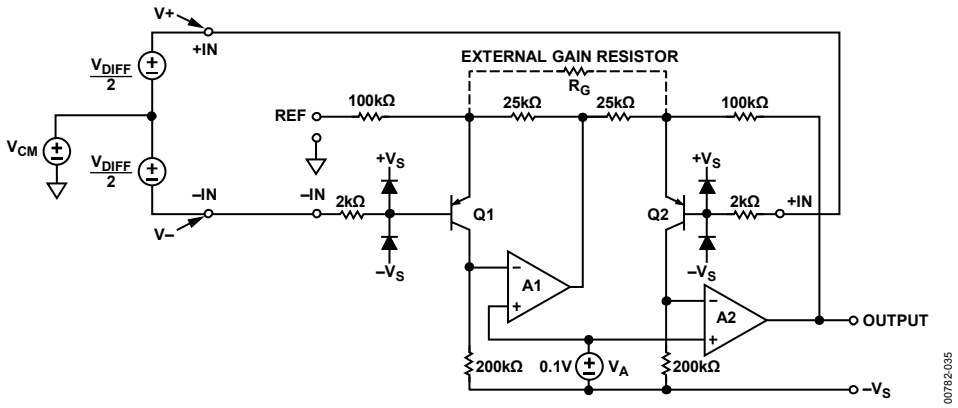

Figure 37. Amplifying Differential Signals with a Common-Mode Component

Table 6. Recommended Values of Gain Resistors

Desired Gain	1% Standard Table Value of R_G	Resulting Gain
5	∞	5.00
6	200 kΩ	6.00
7	100 kΩ	7.00
8	68.1 kΩ	7.94
9	51.1 kΩ	8.91
10	40.2 kΩ	9.98
15	20 kΩ	15.00
20	13.7 kΩ	19.60
25	10 kΩ	25.00
30	8.06 kΩ	29.81
40	5.76 kΩ	39.72
50	4.53 kΩ	49.15
60	3.65 kΩ	59.79
70	3.09 kΩ	69.72
80	2.67 kΩ	79.91
90	2.37 kΩ	89.39
100	2.1 kΩ	100.24
200	1.05 kΩ	195.48
500	412 Ω	490.44
1000	205 Ω	980.61

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output. The reference terminal is also useful when amplifying bipolar signals, because it provides a virtual ground voltage.

The AD627 output voltage is developed with respect to the potential on the reference terminal; therefore, tying the REF pin to the appropriate local ground solves many grounding problems. For optimal CMR, tie the REF pin to a low impedance point.

INPUT RANGE LIMITATIONS IN SINGLE-SUPPLY APPLICATIONS

In general, the maximum achievable gain is determined by the available output signal range. However, in single-supply applications where the input common-mode voltage is nearly or equal to 0, some limitations on the gain can be set. Although the Specifications section nominally defines the input, output, and reference pin ranges, the voltage ranges on these pins are mutually interdependent. Figure 37 shows the simplified schematic of the AD627, driven by a differential voltage (V_{DIFF}) that has a common-mode component, V_{CM}. The voltage on the A1 op amp output is a function of V_{DIFF}, V_{CM}, the voltage on the REF pin, and the programmed gain. This voltage is given by

$$V_{A1} = 1.25\ (V_{CM} + 0.5\ \text{V}) - 0.25\ V_{REF} - V_{DIFF}\ (25\ \text{k}\Omega/R_G - 0.625) \quad (3)$$

The voltage on A1 can also be expressed as a function of the actual voltages on the –IN and +IN pins (V– and V+) such that

$$V_{A1} = 1.25\ ((V-) + 0.5\ V) - 0.25\ V_{REF} - ((V+) - (V-))\ 25\ \text{k}\Omega/R_G \quad (4)$$

The output of A1 is capable of swinging to within 50 mV of the negative rail and to within 200 mV of the positive rail. It is clear, from either Equation 3 or Equation 4, that an increasing V_{REF} (while it acts as a positive offset at the output of the AD627) tends to decrease the voltage on A1. Figure 38 and Figure 39 show the maximum voltages that can be applied to the REF pin for a gain of 5 for both the single-supply and dual-supply cases.

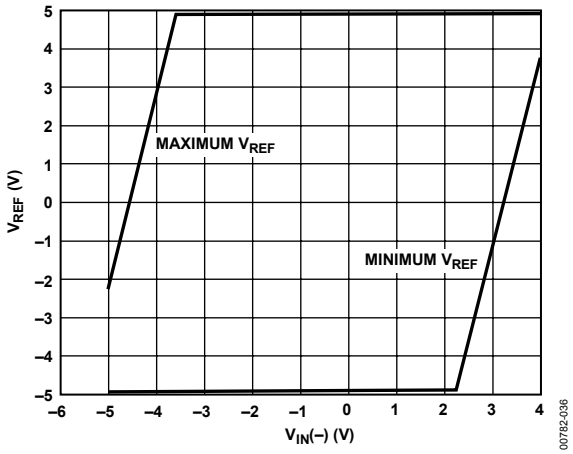

Figure 38. Reference Input Voltage vs. Negative Input Voltage, V_S = ±5 V, G = +5

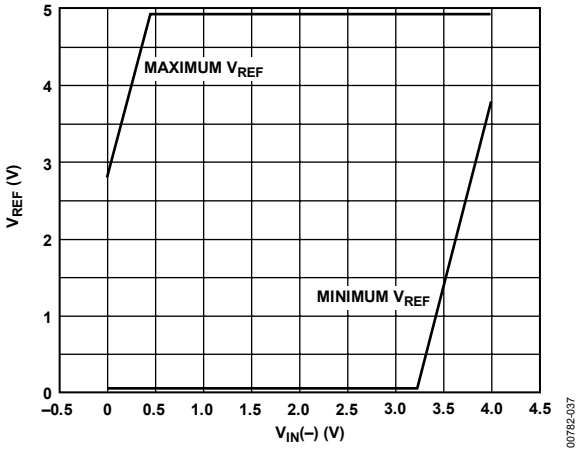

Figure 39. Reference Input Voltage vs. Negative Input Voltage, V_S = 5 V, G = +5

Raising the input common-mode voltage increases the voltage on the output of A1. However, in single-supply applications where the common-mode voltage is low, a differential input voltage or a voltage on REF that is too high can drive the output of A1 into the ground rail. Some low-side headroom is added because both inputs are shifted upwards by about 0.5 V (that is, by the V_{BE} of Q1 and Q2). Use Equation 3 and Equation 4 to check whether the voltage on Amplifier A1 is within its operating range.

Table 7. Maximum Gain for Low Common-Mode, Single-Supply Applications

V_{IN}	REF Pin	Supply Voltage	R_G (1% Tolerance)	Resulting Maximum Gain	Output Swing WRT 0 V
±100 mV, V_{CM} = 0 V	2 V	5 V to 15 V	28.7 kΩ	12.0	0.8 V to 3.2 V
±50 mV, V_{CM} = 0 V	2 V	5 V to 15 V	10.7 kΩ	23.7	0.8 V to 3.2 V
±10 mV, V_{CM} = 0 V	2 V	5 V to 15 V	1.74 kΩ	119.9	0.8 V to 3.2 V
V– = 0 V, V+ = 0 V to 1 V	1 V	10 V to 15 V	78.7 kΩ	7.5	1 V to 8.5 V
V– = 0 V, V+ = 0 mV to 100 mV	1 V	5 V to 15 V	7.87 kΩ	31	1 V to 4.1 V
V– = 0 V, V+ = 0 mV to 10 mV	1 V	5 V to 15 V	787 Ω	259.1	1 V to 3.6 V

Table 8. RTI Error Sources

	Maximum Total RTI Offset Error (µV)		Maximum Total RTI Offset Drift (µV/°C)		Total RTI Noise (nV/√Hz)
Gain	AD627A	AD627B	AD627A	AD627B	AD627A /AD627B
+5	450	250	5	3	95
+10	350	200	4	2	66
+20	300	175	3.5	1.5	56
+50	270	160	3.2	1.2	53
+100	270	155	3.1	1.1	52
+500	252	151	3	1	52
+1000	251	151	3	1	52

Table 7 gives values for the maximum gain for various single-supply input conditions. The resulting output swings refer to 0 V. To maximize the available gain and output swing, set the voltages on the REF pins to either 2 V or 1 V. In most cases, there is no advantage to increasing the single supply to greater than 5 V (the exception is an input range of 0 V to 1 V).

OUTPUT BUFFERING

The AD627 is designed to drive loads of 20 kΩ or greater but can deliver up to 20 mA to heavier loads at lower output voltage swings (see Figure 10). If more than 20 mA of output current is required at the output, buffer the AD627 output with a precision op amp, such as the OP113. Figure 40 shows this for a single supply. This op amp can swing from 0 V to 4 V on its output while driving a load as small as 600 Ω.

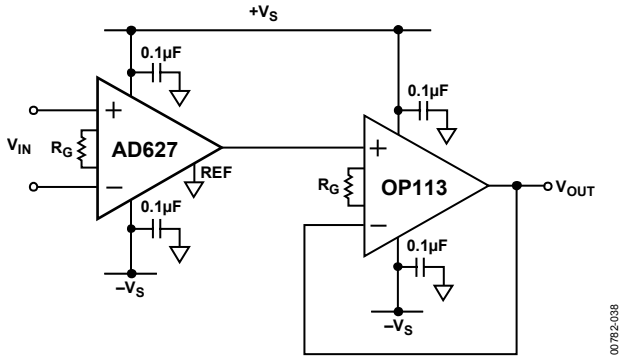

Figure 40. Output Buffering

INPUT AND OUTPUT OFFSET ERRORS

The low errors of the AD627 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, input errors dominate at high gains and output errors dominate at low gains. The total offset error for a given gain is calculated as

$$Total\ Error\ RTI = Input\ Error + (Output\ Error/Gain) \quad (5)$$

$$Total\ Error\ RTO = (Input\ Error \times G) + Output\ Error \quad (6)$$

RTI offset errors and noise voltages for different gains are listed in Table 8.

MAKE vs. BUY: A TYPICAL APPLICATION ERROR BUDGET

The example in Figure 41 serves as a good comparison between the errors associated with an integrated and a discrete in-amp implementation. A ±100 mV signal from a resistive bridge (common-mode voltage = 2.5 V) is amplified. This example compares the resulting errors from a discrete two-op-amp instrumentation amplifier and the AD627. The discrete implementation uses a four-resistor precision network (1% match, 50 ppm/°C tracking).

The errors associated with each implementation (see Table 9) show the integrated in-amp to be more precise at both ambient and overtemperature. Note that the discrete implementation is more expensive, primarily due to the relatively high cost of the low drift precision resistor network.

The input offset current of the discrete instrumentation amplifier implementation is the difference in the bias currents of the two-op amplifiers, not the offset currents of the individual op amps. In addition, although the values of the resistor network are chosen so that the inverting and noninverting inputs of each op amp see the same impedance (about 350 Ω), the offset current of each op amp adds another error that must be characterized.

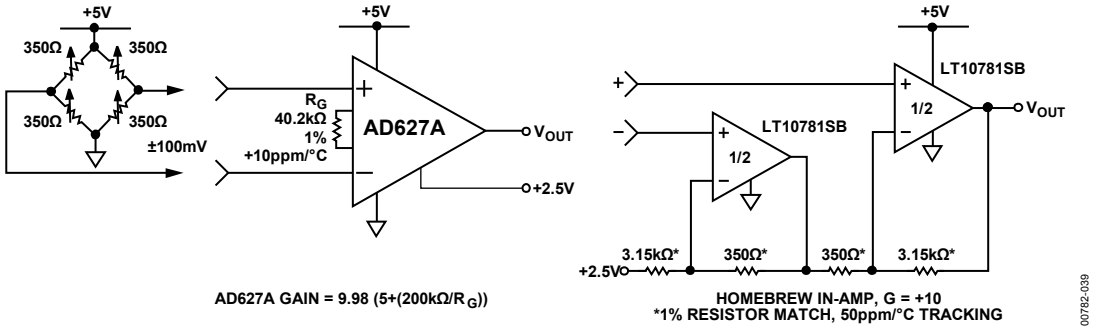

Figure 41. Make vs. Buy

Table 9. Make vs. Buy Error Budget

Error Source	AD627 Circuit Calculation	Homebrew Circuit Calculation	Total Error AD627 (ppm)	Total Error Homebrew (ppm)
ABSOLUTE ACCURACY at T_A = 25°C				
Total RTI Offset Voltage, mV	(250 µV + (1000 µV/10))/100 mV	(180 µV × 2)/100 mV	3,500	3,600
Input Offset Current, nA	1 nA × 350 Ω/100 mV	20 nA × 350 Ω/100 mV	3.5	70
Internal Offset Current (Homebrew Only)	Not applicable	0.7 nA × 350 Ω/100 mV		2.45
CMRR, dB	77 dB→141 ppm × 2.5 V/100 mV	(1% match × 2.5 V)/10/100 mV	3,531	25,000
Gain	0.35% + 0.1%	1% match	13,500	10,000
		Total Absolute Error	**20,535**	**38,672**
DRIFT TO 85°C				
Gain Drift, ppm/°C	(−75 + 10) ppm/°C × 60°C	50 ppm/°C × 60°C	3,900	3,000
Total RTI Offset Voltage, mV/°C	(3.0 µV/°C + (10 µV/°C/10)) × 60°C/100 mV	(2 × 3.5 µV/°C × 60°C)/100 mV	2,600	4,200
Input Offset Current, pA/°C	(16 pA/°C × 350 Ω × 60°C)/100 mV	(33 pA/°C × 350 Ω × 60°C)/100 mV	3.5	7
		Total Drift Error	**6,504**	**7,207**
		Grand Total Error	**27,039**	**45,879**

ERRORS DUE TO AC CMRR

In Table 9, the error due to common-mode rejection results from the common-mode voltage from the bridge 2.5 V. The ac error due to less than ideal common-mode rejection cannot be calculated without knowing the size of the ac common-mode voltage (usually interference from 50 Hz/60 Hz mains frequencies).

A mismatch of 0.1% between the four gain setting resistors determines the low frequency CMRR of a two-op-amp instrumentation amplifier. The plot in Figure 43 shows the practical results of resistor mismatch at ambient temperature.

The CMRR of the circuit in Figure 42 (Gain = +11) was measured using four resistors with a mismatch of nearly 0.1% (R1 = 9999.5 Ω, R2 = 999.76 Ω, R3 = 1000.2 Ω, R4 = 9997.7 Ω). As expected, the CMRR at dc was measured at about 84 dB (calculated value is 85 dB). However, as frequency increases, CMRR quickly degrades. For example, a 200 mV p-p harmonic of the mains frequency at 180 Hz would result in an output voltage of about 800 µV. To put this in context, a 12-bit data acquisition system, with an input range of 0 V to 2.5 V, has an LSB weighting of 610 µV.

By contrast, the AD627 uses precision laser trimming of internal resistors, along with patented CMR trimming, to yield a higher dc CMRR and a wider bandwidth over which the CMRR is flat (see Figure 23).

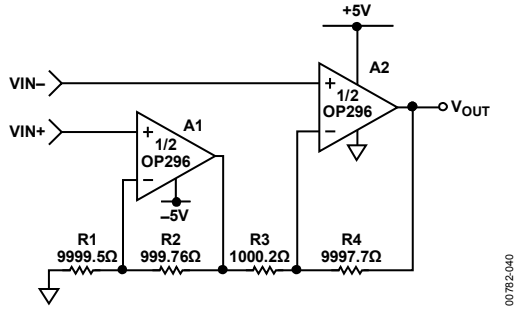

Figure 42. 0.1% Resistor Mismatch Example

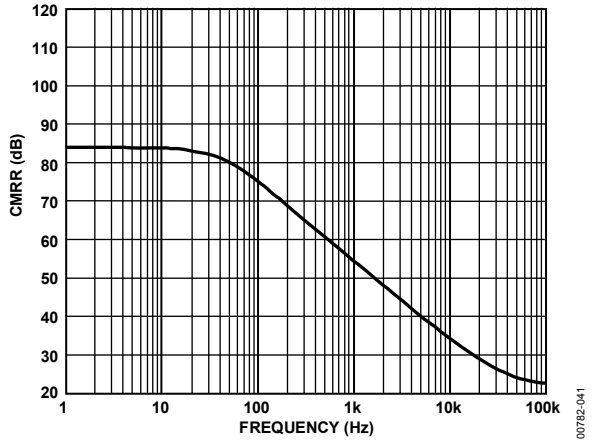

Figure 43. CMRR over Frequency of Discrete In-Amp in Figure 42

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are dc currents that must flow to bias the input transistors of an amplifier. They are usually transistor base currents. When amplifying floating input sources, such as transformers or ac-coupled sources, there must be a direct dc path into each input so that the bias current can flow. Figure 44, Figure 45, and Figure 46 show how to provide a bias current path for the cases of, respectively, transformer coupling, a thermocouple application, and capacitive ac-coupling.

In dc-coupled resistive bridge applications, providing this path is generally not necessary because the bias current simply flows from the bridge supply through the bridge and into the amplifier. However, if the impedance that the two inputs see are large, and differ by a large amount (>10 kΩ), the offset current of the input stage causes dc errors compatible with the input offset voltage of the amplifier.

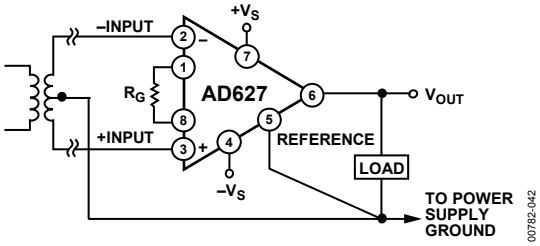

Figure 44. Ground Returns for Bias Currents with Transformer Coupled Inputs

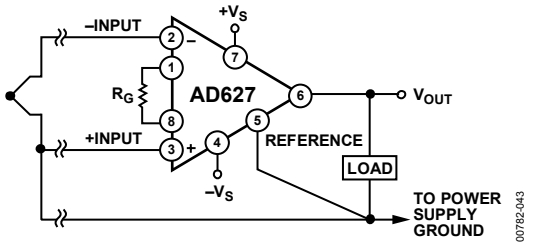

Figure 45. Ground Returns for Bias Currents with Thermocouple Inputs

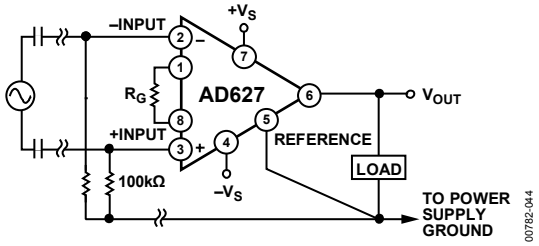

Figure 46. Ground Returns for Bias Currents with AC-Coupled Inputs

LAYOUT AND GROUNDING

The use of ground planes is recommended to minimize the impedance of ground returns (and hence, the size of dc errors). To isolate low level analog signals from a noisy digital environment, many data acquisition components have separate analog and digital ground returns (see Figure 47). Return all ground pins from mixed-signal components, such as analog-to-digital converters, through the high quality analog ground plane. Digital ground lines of mixed-signal components should also be returned through the analog ground plane. This may seem to break the rule of separating analog and digital grounds; however, in general, there is also a requirement to keep the voltage difference between digital and analog grounds on a converter as small as possible (typically, <0.3 V). The increased noise, caused by the digital return currents of the converter flowing through the analog ground plane, is generally negligible. To maximize isolation between analog and digital, connect the ground planes back at the supplies.

If there is only one power supply available, it must be shared by both digital and analog circuitry. Figure 48 shows how to minimize interference between the digital and analog circuitry. As in the previous case, use separate analog and digital ground planes or use reasonably thick traces as an alternative to a digital ground plane. Connect the ground planes at the ground pin of the power supply. Run separate traces (or power planes) from the power supply to the supply pins of the digital and analog circuits. Ideally, each device should have its own power supply trace, but they can be shared by multiple devices if a single trace is not used to route current to both digital and analog circuitry.

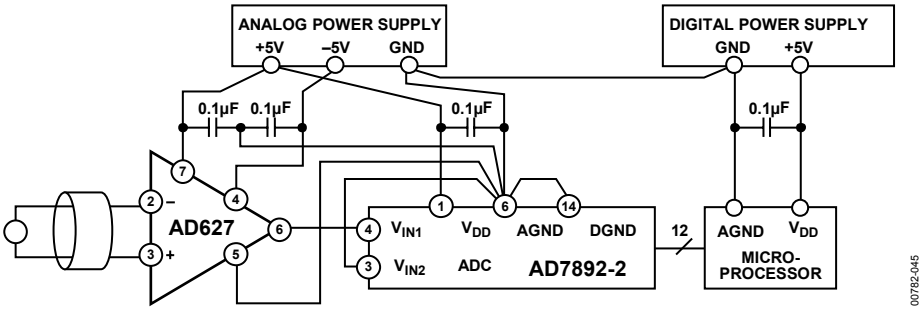

Figure 47. Optimal Grounding Practice for a Bipolar Supply Environment with Separate Analog and Digital Supplies

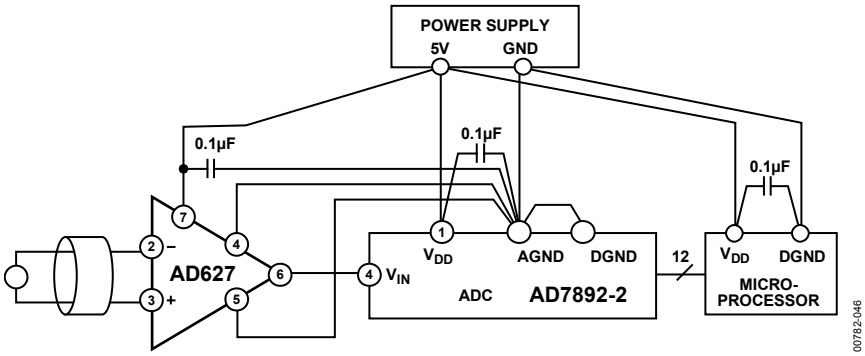

Figure 48. Optimal Ground Practice in a Single-Supply Environment

INPUT PROTECTION

As shown in the simplified schematic (see Figure 35), both the inverting and noninverting inputs are clamped to the positive and negative supplies by ESD diodes. In addition, a 2 kΩ series resistor on each input provides current limiting in the event of an overvoltage. These ESD diodes can tolerate a maximum continuous current of 10 mA. So an overvoltage (that is, the amount by which the input voltage exceeds the supply voltage) of ±20 V can be tolerated. This is true for all gains, and for power on and off. This last case is particularly important because the signal source and amplifier can be powered separately.

If the overvoltage is expected to exceed 20 V, use additional external series current-limiting resistors to keep the diode current below 10 mA.

RF INTERFERENCE

All instrumentation amplifiers can rectify high frequency out-of-band signals. Once rectified, these signals appear as dc offset errors at the output. The circuit in Figure 49 provides good RFI suppression without reducing performance within the pass band of the instrumentation amplifier. Resistor R1 and Capacitor C1 (and likewise, R2 and C2) form a low-pass RC filter that has a –3 dB BW equal to

$$f = 1/(2\pi(R1 \times C1)) \quad (7)$$

Using the component values shown in Figure 49, this filter has a –3 dB bandwidth of approximately 8 kHz. Resistor R1 and Resistor R2 were selected to be large enough to isolate the circuit input from the capacitors but not large enough to significantly increase circuit noise. To preserve common-mode rejection in the amplifier pass band, Capacitor C1 and Capacitor C2 must be 5% mica units, or low cost 20% units can be tested and binned to provide closely matched devices.

Capacitor C3 is needed to maintain common-mode rejection at low frequencies. R1/R2 and C1/C2 form a bridge circuit whose output appears across the input pins of the in-amp. Any mismatch between C1 and C2 unbalances the bridge and reduces common-mode rejection. C3 ensures that any RF signals are common mode (the same on both in-amp inputs) and are not applied differentially. This second low-pass network, R1 + R2 and C3, has a –3 dB frequency equal to

$$1/(2\pi((R1 + R2) \times C3)) \quad (8)$$

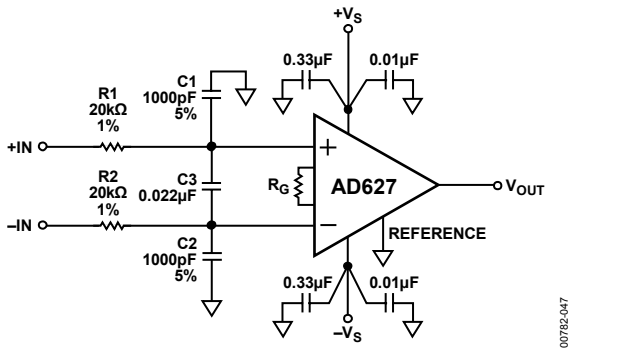

Figure 49. Circuit to Attenuate RF Interference

Using a C3 value of 0.022 µF, as shown in Figure 49, the –3 dB signal bandwidth of this circuit is approximately 200 Hz. The typical dc offset shift over frequency is less than 1 mV and the RF signal rejection of the circuit is better than 57 dB. To increase the 3 dB signal bandwidth of this circuit, reduce the value of Resistor R1 and Resistor R2. The performance is similar to that when using 20 kΩ resistors, except that the circuitry preceding the in-amp must drive a lower impedance load.

When building a circuit like that shown in Figure 49, use a PC board with a ground plane on both sides. Make all component leads as short as possible. Resistor R1 and Resistor R2 can be common 1% metal film units, but Capacitor C1 and Capacitor C2 must be ±5% tolerance devices to avoid degrading the common-mode rejection of the circuit. Either the traditional 5% silver mica units or Panasonic ±2% PPS film capacitors are recommended.

APPLICATIONS CIRCUITS

CLASSIC BRIDGE CIRCUIT

Figure 50 shows the AD627 configured to amplify the signal from a classic resistive bridge. This circuit works in dual-supply mode or single-supply mode. Typically, the same voltage that powers the instrumentation amplifiers excites the bridge. Connecting the bottom of the bridge to the negative supply of the instrumentation amplifiers (usually 0 V, −5 V, −12 V, or −15 V), sets up an input common-mode voltage that is optimally located midway between the supply voltages. It is also appropriate to set the voltage on the REF pin to midway between the supplies, especially if the input signal is bipolar. However, the voltage on the REF pin can be varied to suit the application. For example, the REF pin is tied to the V_{REF} pin of an analog-to-digital converter (ADC) whose input range is ($V_{REF} \pm V_{IN}$). With an available output swing on the AD627 of ($-V_S$ + 100 mV) to ($+V_S$ − 150 mV), the maximum programmable gain is simply this output range divided by the input range.

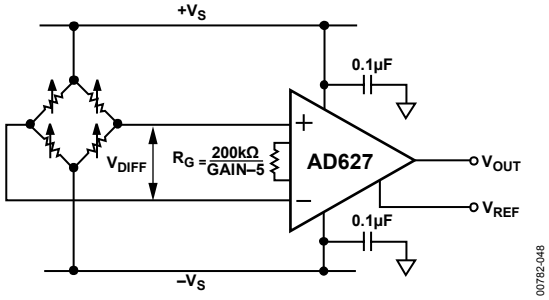

Figure 50. Classic Bridge Circuit

4 TO 20 mA SINGLE-SUPPLY RECEIVER

Figure 51 shows how a signal from a 4 to 20 mA transducer can be interfaced to the ADuC812, a 12-bit ADC with an embedded microcontroller. The signal from a 4 to 20 mA transducer is single-ended, which initially suggests the need for a simple shunt resistor to convert the current to a voltage at the high impedance analog input of the converter. However, any line resistance in the return path (to the transducer) adds a current dependent offset error; therefore, the current must be sensed differentially.

In this example, a 24.9 Ω shunt resistor generates a maximum differential input voltage to the AD627 of between 100 mV (for 4 mA in) and 500 mV (for 20 mA in). With no gain resistor present, the AD627 amplifies the 500 mV input voltage by a factor of 5, to 2.5 V, the full-scale input voltage of the ADC. The zero current of 4 mA corresponds to a code of 819 and the LSB size is 610 µA.

THERMOCOUPLE AMPLIFIER

Because the common-mode input range of the AD627 extends 0.1 V below ground, it is possible to measure small differential signals that have a low, or no, common-mode component. Figure 51 shows a thermocouple application where one side of the J-type thermocouple is grounded.

Over a temperature range from −200°C to +200°C, the J-type thermocouple delivers a voltage ranging from −7.890 mV to +10.777 mV. A programmed gain on the AD627 of 100 (R_G = 2.1 kΩ) and a voltage on the AD627 REF pin of 2 V result in the output voltage of the AD627 ranging from 1.110 V to 3.077 V relative to ground. For a different input range or different voltage on the REF pin, it is important to verify that the voltage on Internal Node A1 (see Figure 37) is not driven below ground. This can be checked using the equations in the Input Range Limitations in Single-Supply Applications section.

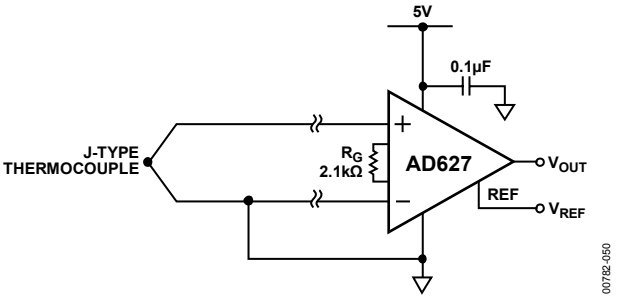

Figure 51. Amplifying Bipolar Signals with Low Common-Mode Voltage

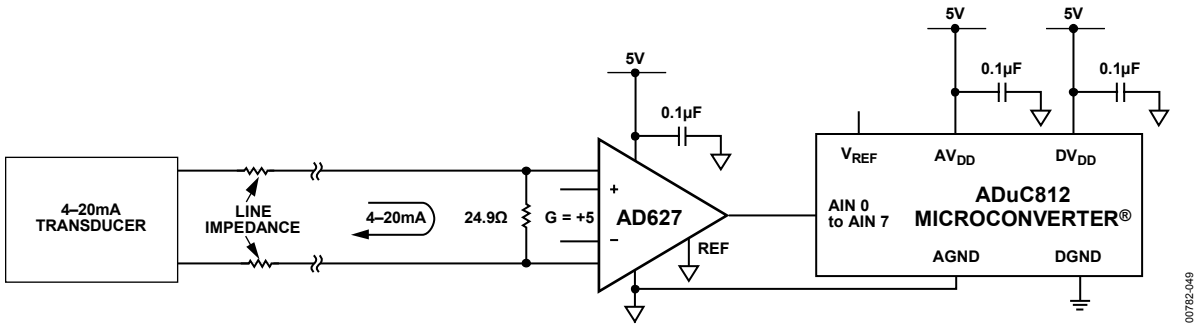

Figure 52. 4 to 20 mA Receiver Circuit

OUTLINE DIMENSIONS

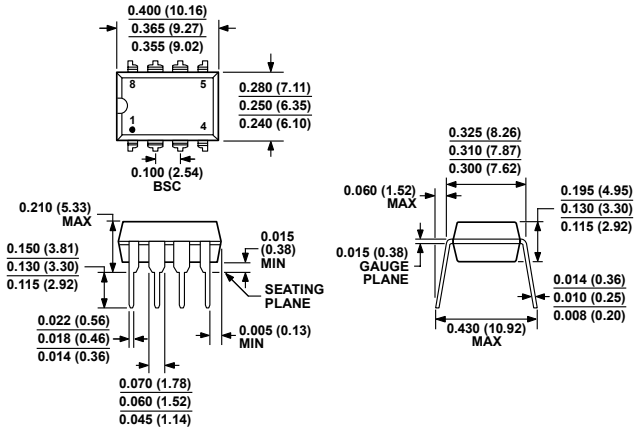

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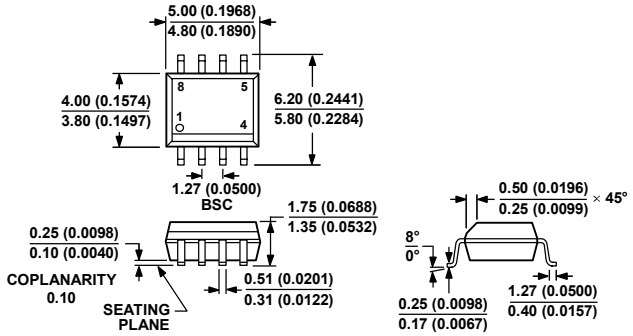
Figure 53. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-8)
Dimensions shown in inches (and millimeters)



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012407-A

Figure 54. 8-Lead Small Standard Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters (and inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD627AN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD627ANZ[1]	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD627AR	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627AR-REEL	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627AR-REEL7	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627ARZ[1]	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627ARZ-R7[1]	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627ARZ-RL[1]	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627BN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD627BNZ[1]	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD627BR	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627BR-REEL	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627BR-REEL7	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627BRZ[1]	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627BRZ-RL[1]	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8
AD627BRZ-R7[1]	−40°C to +85°C	8-Lead Small Standard Outline [SOIC_N]	R-8

[1] Z = RoHS Compliant part.

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