

HIGH-SPEED 16K x 8 DUAL-PORT STATIC RAM

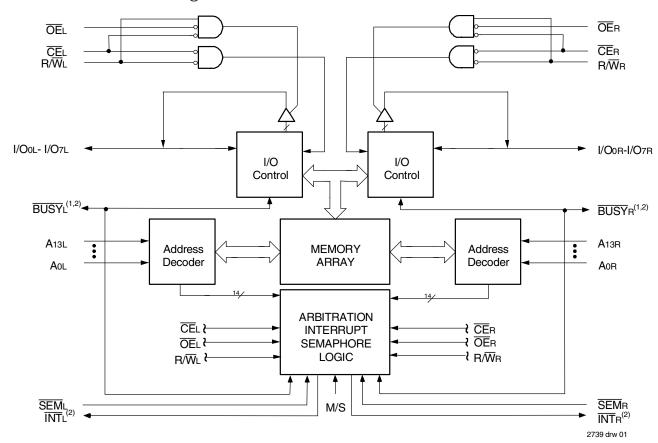
IDT7006S/L

Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
 - Military: 20/25/35/55/70ns (max.)
 - Industrial: 55ns (max.)
 - Commercial: 15/17/20/25/35/55ns (max.)
- Low-power operation
 - IDT7006S
 - Active: 750mW (typ.)
 - Standby: 5mW (typ.)
 - IDT7006L
 - Active: 700mW (typ.)
 - Standby: 1mW (typ.)
- IDT7006 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device

- M/S = H for BUSY output flag on Master,
 M/S = L for BUSY input on Slave
- Busy and Interrupt Flags
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, quad flatpack, PLCC, and a 64-pin TOFP
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



NOTES:

- 1. (MASTER): BUSY is output; (SLAVE): BUSY is input.
- 2. BUSY outputs and INT outputs are non-tri-stated push-pull.

AUGUST 2014

Description

The IDT7006 is a high-speed 16K x 8 Dual-Port Static RAM. The IDT7006 is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

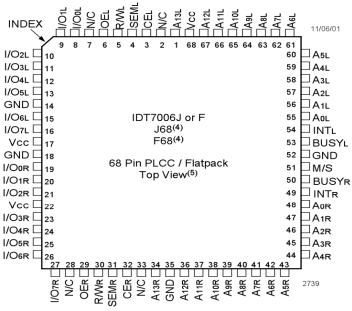
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by \overline{CE} permits the on-chip circuitry of each port to enter

a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500μ W from a 2V battery.

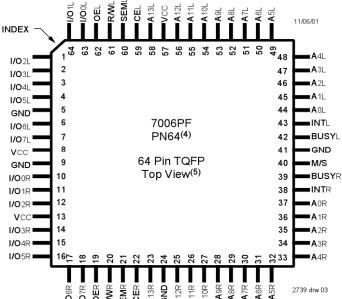
The IDT7006 is packaged in a ceramic 68-pin PGA, an 68-pin quad flatpack, a PLCC, and a 64-pin thin quad flatpack, TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations (1,2,3)



NOTES:

- 1. All Vcc pins must be connected to power supply.
- 2. All GND pins must be connected to ground supply.
- J68-1 package body is approximately .95 in x .95 in. x .17 in. F68-1 package body is approximately .97 in x .97 in x .08 in. PN64-1 package body is approximately 14mm x 14mm x 1.4mm.
- 4. This package code is used to reference the package diagram.
- 5. This text does not indicate orientation of the actual part-marking



Pin Configurations (1,2,3) (con't.)

11		51 A 5L	50 A 4L	48 A 2L	46 A 0L	44 BUSYL	42 M/S	40 INTR	38 A 1R	36 A 3R	11/06/01			
10	53 A 7L	52 A 6L	49 A 3L	47 A 1L	45 INT∟	43 GND	41 BUSYR	39 A 0R	37 A 2R	35 A 4R	34 A 5R			
09	55 A 9L	54 A 8L			32 A 7R	33 A 6R								
08	57 A 11L	56 A 10L				30 A 9R	31 A 8R							
07	59 V CC	58 A 12L				28 A 11R	29 A 10R							
06	61 N/C	60 A 13L				26 GND	27 A 12R							
05	63 SEM∟	62 CE∟	Top View ⁽⁵⁾				68-Pin PGA Top View ⁽⁵⁾							
04	65 OE∟	64 R/W∟								22 SEMR	23 CER			
03	67 I/O _{0L}	66 N/C								20 OER	21 R/WR			
02	68 I/O1L	1 1/02L	3 I/O4L	5 GND	7 1/07L	9 GND	11 I/O1R	13 VCC	15 I/O4R	18 I/O7R	19 N/C			
01	* •	2 1/03L	4 I/O5L	6 I/O ₆ L	8 VCC	10 I/O0R	12 I/O2R	14 I/O3R	16 I/O5R	17 I/O6R				
INDE	A X	В	С	D	E	F	G	Н	J	K	L 2739 drw 04			

NOTES:

- All Vcc pins must be connected to power supply.
 All GND pins must be connected to ground supply.

- Package body is approximately 1.18 in x 1.18 in x .16 in.
 This package code is used to reference the package diagram.
 This text does not indicate orientation of the actual part-marking

Pin Names

Left Port	Right Port	Names				
<u>CĒ</u> .	C Ēr	Chip Enable				
R/WL	R/W̄R	Read/Write Enable				
ŌĒL	OE R	Output Enable				
A0L - A13L	Aor - A13R	Address				
I/O0L - I/O7L	I/Oor - I/O7R	Data Input/Output				
SEML	<u>SEM</u> _R	Semaphore Enable				
ĪNTL	ĪNTr	Interrupt Flag				
BUSYL	BUSYR	Busy Flag				
М	/S	Master or Slave Select				
V	CC	Power				
Gl	ND	Ground				

2739 tbl 01

Truth Table I: Non-Contention Read/Write Control

	Inpu	ıts ⁽¹⁾		Outputs						
CE	R/W	ŌĒ	SEM	I/O ₀₋₇	Mode					
Н	Х	Х	Н	High-Z	Deselected: Power-Down					
L	L	Х	Н	DATAIN	Write to Memory					
L	Н	L	Н	DATAout	Read Memory					
Х	Х	Н	Х	High-Z	Outputs Disabled					

NOTE:

2739 tbl 02

1. AoL - A13L is not equal to AoR - A13R

Truth Table II: Semaphore Read/Write Control(1)

	Inputs ⁽¹⁾			Outputs	
CE	R/W	Œ	SEM	I/O ₀₋₇	Mode
Н	Н	L	L	DATAout	Read in Semaphore Flag Data Out
Н	1	Х	L	DATAIN	Write I/Oo into Semaphore Flag
L,	Х	Χ	L	_	Not Allowed

NOTE:

2739 tbl 03

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	٧
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
Tstg	Storage Temperature	-65 to +150	-65 to +150	۰C
Іоит	DC Output Current	50	50	mA

NOTES:

2739 tbl 04

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sec-tions of this specification is not implied. Exposure to absolute maxi-mum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≤ Vcc + 10%.

Capacitance⁽¹⁾ (TA = +25°C, f = 1.0mhz)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit		
CIN	Input Capacitance	VIN = 3dV	9	pF		
Соит	Output Capacitance	Vout = 3dV	10	pF		

NOTES

2739 tbl 05

- These parameters are determined by device characterization, but are not production tested (TQFP Package Only).
- 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	_	6.0(2)	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	_	0.8	٧

NOTES:

2739 tbl 06

- 1. $VIL \ge -1.5V$ for pulse width less than 10ns.
- 2. VTERM must not exceed Vcc + 10%.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to+125°C	0V	5.0V <u>+</u> 10%
Commercial	0°C to +70°C	0V	5.0V <u>+</u> 10%
Industrial	40°C to +85°C	0V	5.0V <u>+</u> 10%

NOTES:

2739 tbl 07

1. This is the parameter Ta. This is the "instant on" case temperature.

^{1.} There are eight semaphore flags written to via I/Oo and read from I/Oo. I/Oo. These eight semaphores are addressed by Ao. A2.

2739 tbl 08

2739 tbl 09

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($Vcc = 5.0V \pm 10\%$)

			7006S		700		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
Lu	Input Leakage Current ⁽¹⁾	Vcc = 5.5V, ViN = 0V to Vcc	_	10	_	5	μΑ
lLO	Output Leakage Current	$\overline{CE} = V_{H}$, Vout = 0V to Vcc	_	10	-	5	μΑ
Vol	Output Low Voltage	loL = 4mA	-	0.4	ı	0.4	V
Voh	Output High Voltage	IOH = -4mA	2.4	_	2.4	_	V

NOTE:

1. At Vcc ≤ 2.0V input leakages are undefined.

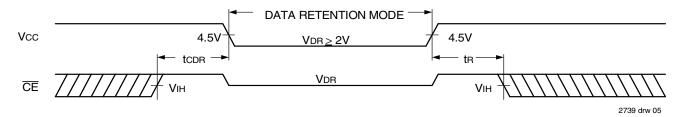
Data Retention Characteristics Over All Temperature Ranges (L Version Only) (VLc = 0.2V, VHC = VCC - 0.2V)

Symbol	Parameter	Test Condition	on	Min.	Typ. (1)	Max.	Unit
Vdr	Vcc for Data Retention	Vcc = 2v	2.0	-	_	V	
ICCDR	Data Retention Current	$\overline{\text{CE}} \geq \text{VHC}$ Mil. & Ind.		_	100	4000	μΑ
		VIN > VHC or < VLC	Com'l.	_	100	1500	
tcdr ⁽³⁾	Chip Deselect to Data Retention Time	SEM > VHC		0	_	_	ns
tR ⁽³⁾	Operation Recovery Time			trc ⁽²⁾	_	_	ns

NOTES:

- 1. TA = +25°C, Vcc = 2V, and are not production tested.
- 2. tRC = Read Cycle Time
- 3. This parameter is guaranteed by characterization, but is not production tested.

Data Retention Waveform



DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range $^{(1)}$ (Vcc = 5.0V \pm 10%)

						7006X15 Com'l Only		7006X17 Com'l Only		X20 I, Ind litary	7006X25 Com'l & Military		
Symbol	Parameter	Test Condition	Version	1	Typ. ⁽²⁾	Max	Typ. ⁽²⁾	Max.	Тур.(2)	Max.	Typ. ⁽²⁾	Max.	Unit
Icc	Dynamic Operating Current (Both Ports Active)	CE = VIL, Outputs Disabled SEM = VIH	COM'L	S L	170 160	310 260	170 160	310 260	160 150	290 240	155 145	265 220	mA
	(Both Polis Active)	$f = fMAX^{(3)}$	MIL & IND	S L	1 1	11	_		160 150	370 320	155 145	340 280	
ISB1	Standby Current (Both Ports - TTL		COM'L	S L	20 10	60 50	20 10	60 50	20 10	60 50	16 10	60 50	mA
	Level inpuis)		MIL & IND	S L	1 1	11			20 10	90 70	16 10	80 65	
ISB2	Standby Current (One Port - TTL		COM'L	S L	105 95	190 160	105 95	190 160	95 85	180 150	90 80	170 140	mA
	Lever inpuis)		MIL & IND	S L		11	_		95 85	240 210	90 80	215 180	
ISB3	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}L$ and $\overline{CER} \ge VCC - 0.2V$ $VIN \ge VCC - 0.2V$ or	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	15 5	mA
	ilipus)	$\begin{array}{l} VIN \leq VCC - 0.2V \text{ of } \\ VIN \leq 0.2V, f = 0^{(4)} \\ \overline{SEMR} = \overline{SEML} \geq VCC - 0.2V \end{array}$	MIL & IND	S L			-		1.0 0.2	30 10	1.0 0.2	30 10	
ISB4	Full Standby Current (One Port - All	$\overline{CE}B = VCC - 0.2V^{(5)}$	COM'L	S L	100 90	170 140	100 90	170 140	90 80	155 130	85 75	145 120	mA
CMOS Level Inputs)	SEMR = SEML > VCC - 0.2V VIN > VCC - 0.2V or VIN < 0.2V Active Port Outputs Disabled f = fMax ⁽³⁾	MIL & IND	S L			_	_	90 80	225 200	85 75	200 170		

2739 tbl 10

2739 tbl 11

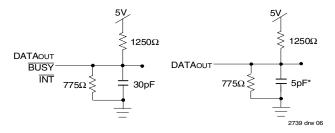
					Cor		7006 Com Mili	n'l &	7006X55 Com'l, Ind & Military		7006X70 Military Only		
Symbol	Parameter	Test Condition	Versio	n	Тур.(2)	Max.	Typ. ⁽²⁾	Max.	Тур.(2)	Max.	Unit		
ICC	Dynamic Operating $\overline{CE} = VIL$, Outputs Disabled $\overline{SEM} = VIH$		COM'L	S L	150 140	250 210	150 140	250 210	_	_	mA		
	(Both Ports Active)	$f = f_{MAX}^{(3)}$	MIL & IND	S L	150 140	300 250	150 140	300 250	140 130	300 250			
ISB1	Standby Current (Both Ports - TTL	$\overline{CEL} = \overline{CER} = VH$ $\overline{SEMR} = \overline{SEML} = VH$ $f = f_{MAX}^{(3)}$	COM'L	S L	13 10	60 50	13 10	60 50			mA		
	Level Inputs)	I = IIVIAX**	MIL & IND	S L	13 10	80 65	13 10	80 65	10 8	80 65			
ISB2	(One Port - TTL Active Port Outputs Disabled,		COM'L	S L	85 75	155 130	85 75	155 130			mA		
	Level Inputs)	$\frac{f = f_{MAX}^{(3)}}{SEMR} = \frac{1}{SEML} = V_{IH}$	MIL & IND	S L	85 75	190 160	85 75	190 160	80 70	190 160			
ISB3	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}L$ and $\overline{CE}R \geq VCC - 0.2V$ $VIN \geq VCC - 0.2V$ or	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5			mA		
	Level inpuis)	$VIN \ge VCC - 0.2V \text{ or } VIN \le 0.2V, f = 0^{(4)} \\ SEMR = SEML \ge VCC - 0.2V$	MIL & IND	S L	1.0 0.2	30 10	1.0 0.2	30 10	1.0 0.2	30 10			
ISB4	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{\text{CE}}$ 'A" \leq 0.2V and $\overline{\text{CE}}$ 'B" \geq VCC - 0.2V ⁽⁵⁾ $\overline{\text{SEMR}}$ = $\overline{\text{SEML}}$ \geq VCC - 0.2V	COM'L	S L	80 70	135 110	80 70	135 110			mA		
	Lever inputs	SEINE SEINL VCC - 0.2V or VIN \leq 0.2V Active Port Outputs Disabled $f = f_{MAX}^{(3)}$	MIL & IND	S L	80 70	175 150	80 70	175 150	75 65	175 150			

1. 'X' in part numbers indicates power rating (S or L) 2. Vcc = 5V, $TA = +25^{\circ}C$, and are not production tested. $Icc \ DC = 120ma$ (typ)

At f = fmax, address and I/O's are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
 f = 0 means no address or control lines change.
 Port "A" may be either left or right port. Port "B"is the opposite from port "A".

AC Test Conditions

Innut Dulas Lavala	CND to 2.01/
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2



2739 tbl 12

Figure 1. AC Output Test Load

Figure 2. Output Test Load (5pF for tLz, tHz, twz, tow) *Including scope and jig.

AC Electrical Oharacteristics Over the Operating temperature and Supply Voltage Range⁽⁴⁾

			6X15 I Only		7006X17 Com'l Only		6X20 'I,Ind litary	7006X25 Com'l & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYC	CLE									
trc	Read Cycle Time	15	_	17	_	20		25		ns
taa	Address Access Time	_	15	_	17	_	20	_	25	ns
tace	Chip Enable Access Time ⁽³⁾	_	15	_	17	_	20	_	25	ns
taoe	Output Enable Access Time	_	10	_	10		12		13	ns
tон	Output Hold from Address Change	3	_	3	_	3		3		ns
tLZ	Output Low-Z Time ^(1,2)	3	_	3	_	3		3		ns
tHZ	Output High-Z Time ^(1,2)		10		10		12		15	ns
tpu	Chip Enable to Power Up Time(2.5)	0	_	0		0		0		ns
tpp	Chip Disable to Power Down Time (2.5)	_	15		17	_	20	_	25	ns
tsop	Semaphore Flag Update Pulse (OE or SEM)	10	_	10	_	10		10		ns
tsaa	Semaphore Address Access Time	_	15	_	17		20		25	ns

2739 tbl 13a

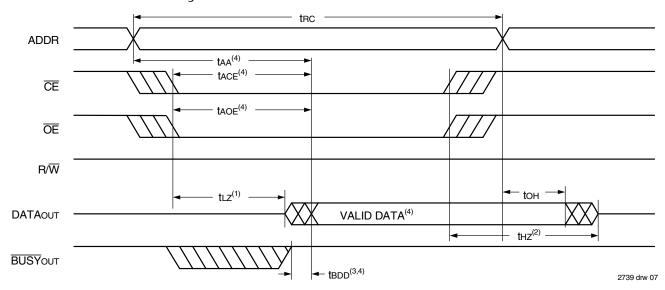
		Cor	7006X35 Com'l & Military		7006X55 Com'l, Ind & Military		7006X70 Military Only	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYC	CLE							
trc	Read Cycle Time	35	-	55	_	70	_	ns
taa	Address Access Time	_	35	_	55	_	70	ns
tace	Chip Enable Access Time ⁽³⁾	_	35	_	55	_	70	ns
taoe	Output Enable Access Time	_	20	_	30	_	35	ns
tон	Output Hold from Address Change	3	-	3	_	3	-	ns
tLZ	Output Low-Z Time ^(1,2)	3	_	3	_	3	_	ns
tHZ	Output High-Z Time ^(1,2)		15	_	25	_	30	ns
tpu	Chip Enable to Power Up Time (2,5)	0		0	_	0	_	ns
tpp	Chip Disable to Power Down Time (2,5)		35	_	50	_	50	ns
tsop	Semaphore Flag Update Pulse (OE or SEM)	15		15	_	15	_	ns
tsaa	Semaphore Address Access Time	_	35		55		70	ns

NOTES:

2739 tbl 13b

- 1. Transition is measured 0mV from Low or High-impedance voltage with load (Figures 1 and 2).
- 2. This parameter is guaranteed by device characterization, but is not production tested.
- 3. To access RAM, $\overline{CE} = VIL$ and $\overline{SEM} = VIH$. To access semaphore, $\overline{CE} = VIH$ and $\overline{SEM} = VIL$.
- 4. $^{\prime}$ X' in part numbers indicates power rating (S or L).

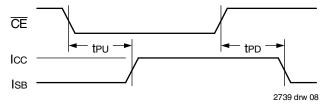
Waveform of Read Cycles⁽⁵⁾



NOTES:

- 1. Timing depends on which signal is asserted last, $\overline{\text{OE}}$ or $\overline{\text{CE}}$.
- 2. Timing depends on which signal is de-asserted first $\overline{\text{CE}}$ or $\overline{\text{OE}}$.
- 3. tepp delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
- 4. Start of valid data depends on which timing becomes effective last taoe, tace, tax or tBDD.
- 5. $\overline{SEM} = VIH.$

Timing of Power-Up Power-Down



AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁵⁾

		7006X15 Com'l Only			6X17 I Only	7006X20 Com'l, Ind & Military		7006X25 Com'l & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCL	E	•								
twc	Write Cycle Time	15		17		20	_	25	_	ns
tew	Chip Enable to End-of-Write ⁽³⁾	12		12		15	_	20	_	ns
taw	Address Valid to End-of-Write	12	_	12		15	_	20	_	ns
tas	Address Set-up Time ⁽³⁾	0	_	0		0	_	0	_	ns
twp	Write Pulse Width	12	_	12		15	_	20	_	ns
twr	Write Recovery Time	0	_	0		0	_	0	_	ns
tow	Data Valid to End-of-Write	10	_	10	_	15	_	15	_	ns
tHZ	Output High-Z Time ^(1,2)		10	_	10		12		15	ns
tон	Data Hold Time ⁽⁴⁾	0		0		0	_	0	_	ns
twz	Write Enable to Output in High-Z ^(1,2)	_	_	_	_		12		15	ns
tow	Output Active from End-of-Write (1,2,4)	0		0		0	_	0	_	ns
tswrd	SEM Flag Write to Read Time	5		5		5		5		ns
tsps	SEM Flag Contention Window	5		5		5	_	5		ns

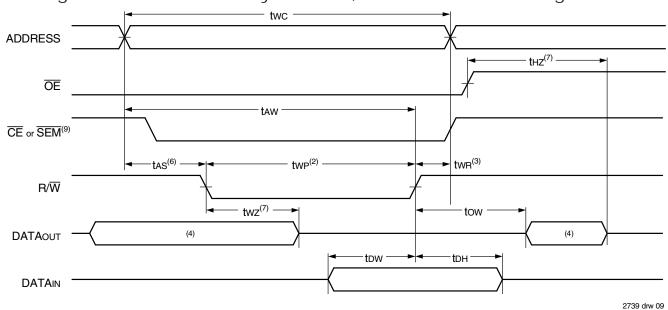
2739 tbl 14a

			6X35 Military	Com	6X55 I, Ind litary	7000 Mili Oi		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE								
twc	Write Cycle Time	35		55	_	70	_	ns
tew	Chip Enable to End-of-Write ⁽³⁾	30		45	_	50	_	ns
taw	Address Valid to End-of-Write	30	_	45	_	50	_	ns
tas	Address Set-up Time ⁽³⁾	0		0	_	0	_	ns
twp	Write Pulse Width	25		40	_	50	_	ns
twr	Write Recovery Time	0		0	_	0	_	ns
tow	Data Valid to End-of-Write	15	_	30	_	40	_	ns
thz	Output High-Z Time ^(1,2)	_	15		25	_	30	ns
tон	Data Hold Time ⁽⁴⁾	0		0	_	0	_	ns
twz	Write Enable to Output in High-Z ^(1,2)	_	15	_	25	_	30	ns
tow	Output Active from End-of-Write ^(1,2,4)	0		0	_	0	_	ns
tswrd	SEM Flag Write to Read Time	5		5	_	5	_	ns
tsps	SEM Flag Contention Window	5		5	_	5	_	ns

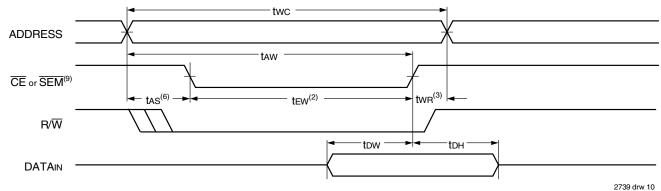
2739 tbl 14b

- 1. Transition is measured 0mV from Low or High-impedance voltage with load (Figure 2).
- This parameter is guaranteed by device characterization, but is not production tested but not tested.
 To access RAM, CE = VIL, SEM = VIH. To access semaphore, CE = VIH and SEM = VIL. Either condition must be valid for the entire tew time.
- 4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tow values will vary over voltage and temperature, the actual toH will always be smaller than the actual tow.
- 5. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Write Cycle No. 1, R/W Controlled Timing (1,5,8)



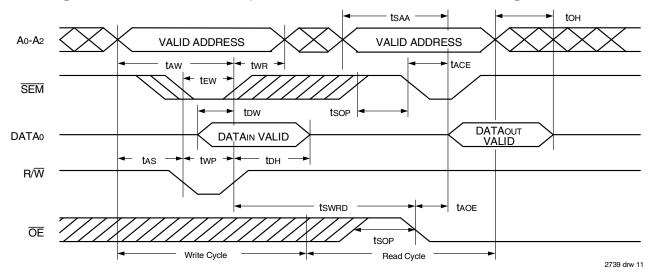
Timing Waveform of Write Cycle No. 2, **CE** Controlled Timing^(1,5)



NOTES

- 1. $R\overline{W}$ or \overline{CE} must be HIGH during all address transitions.
- 2. A write occurs during the overlap (tew or twp) of a LOW $\overline{\text{CE}}$ and a LOW R/W for memory array writing cycle.
- 3. two is measured from the earlier of \overline{CE} or R/\overline{W} (or \overline{SEM} or R/\overline{W}) going HIGH to the end of write cycle.
- 4. During this period, the I/O pins are in the output state and input signals must not be applied.
- 5. If the CE or SEM LOW transition occurs simultaneously with or after the R/W low transition, the outputs remain in the High-impedance state.
- 6. Timing depends on which enable signal is asserted last, $\overline{\text{CE}}$ or R/\overline{W} .
- 7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured by 0mV from steady state with the Output Test Load (Figure 2).
- 8. If \overline{OE} is LOW during $R\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If \overline{OE} is HIGH during an $R\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified
- 9. To access RAM, $\overline{\text{CE}} = \text{V}_{\text{IL}}$ and $\overline{\text{SEM}} = \text{V}_{\text{IH}}$. To access semaphore $\overline{\text{CE}} = \text{V}_{\text{IH}}$ and $\overline{\text{SEM}} = \text{V}_{\text{IL}}$. tew must be met for either condition.

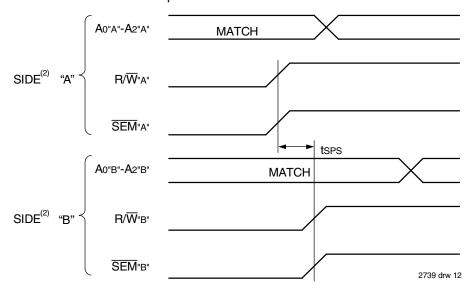
Timing Waveform of Semaphore Read after Write Timing, Either Side(1)



NOTE:

1. \overline{CE} = VIH for the duration of the above timing (both write and read cycle).

Timing Waveform of Semaphore Write Contention (1,3,4)



- 1. DOR = DOL = VIL, $\overline{CE}R = \overline{CE}L = VIH$, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
- All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
 This parameter is measured from R/W-A* or SEM*A* going HIGH to R/W-B* going HIGH.
- 4. If tsps is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁶⁾

			6X15 I Only	7006X17 Com'l Only		Com	6X20 'I, Ind ilitary	Ind Com'l &		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Мах.	Unit
BUSY TIMI										
t BAA	BUSY Access Time from Address Match	_	15	_	17	_	20	_	20	ns
tBDA	BUSY Disable Time from Address Not Matched	_	15	_	17	_	20	_	20	ns
t BAC	BUSY Access Time from Chip Enable Low		15		17		20		20	ns
tBDC	BUSY Access Time from Chip Enable High		15	_	17		17		17	ns
taps	Arbitration Priority Set-up Time ⁽²⁾	5	_	5	_	5	_	5	_	ns
tBDD	BUSY Disable to Valid Data ⁽³⁾	_	18	_	18	_	30	_	30	ns
twн	Write Hold After BUSY ⁽⁵⁾	12		13	_	15		17	_	ns
BUSY TIMII	ng (m/s=vil)									
twB	BUSY Input to Write ⁽⁴⁾	0		0		0		0		ns
twн	Write Hold After BUS Y(5)	12		13	_	15		17	_	ns
PORT-TO-P	ORT DELAY TIMING									
twdd	Write Pulse to Data Delay ⁽¹⁾	_	30	_	30	_	45	_	50	ns
todd	Write Data Valid to Read Data Delay ⁽¹⁾		25		25		35		35	ns

2739 tbl 15a

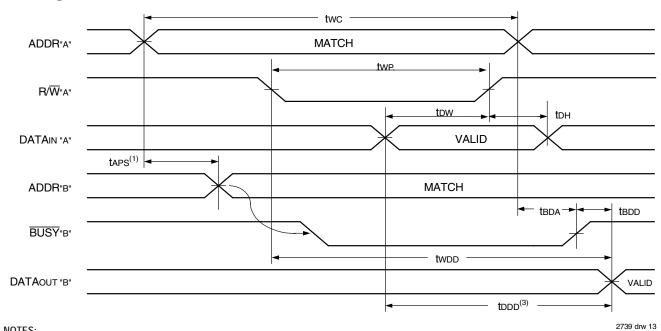
			5 Com'l litary	7006X55 Com'l, Ind & Military		7006X70 Military Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Мах.	Unit
BUSY TIMI	NG (M/S=Vih)							•
t BAA	BUSY Access Time from Address Match		20		45	_	45	ns
t BDA	BUSY Disable Time from Address Not Matched		20	_	40		40	ns
t BAC	BUSY Access Time from Chip Enable Low	_	20	_	40	_	40	ns
tBDC	BUSY Access Time from Chip Enable High	_	20	_	35	_	35	ns
taps	Arbitration Priority Set-up Time ⁽²⁾	5		5		5		ns
tBDD	BUSY Disable to Valid Data ⁽³⁾	_	35	_	40	_	45	ns
twн	Write Hold After BUSY ⁽⁵⁾	25		25		25		ns
BUSY TIMI	NG (M/S=VIL)							
twB	BUSY Input to Write ⁽⁴⁾	0		0		0		ns
twн	Write Hold After BUSY ⁽⁵⁾	25		25		25		ns
PORT-TO-P	ORT DELAY TIMING							
twdd	Write Pulse to Data Delay ⁽¹⁾	_	60	_	80	_	95	ns
tooo	Write Data Valid to Read Data Delay (1)		45		65		80	ns

NOTES:

2739 tbl 15b

- 1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and BUSY".
- 2. To ensure that the earlier of the two ports wins.
- 3. tbdd is a calculated parameter and is the greater of 0, twdd twp (actual) or tddd tdw (actual).
- 4. To ensure that the write cycle is inhibited with port "B" during contention on port "A".
- 5. To ensure that a write cycle is completed on port "B" after contention with port "A".
- 6. 'X' is part numbers indicates power rating (S or L).

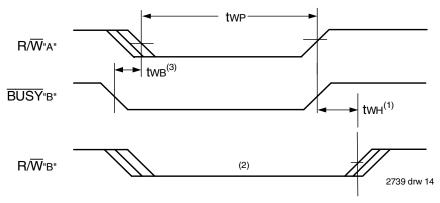
Timing Waveform of Write with Port-to-Port Read and $\overline{\textbf{BUSY}}^{(2,5)}$ (M/ $\overline{\textbf{S}}$ = Vih)⁽⁴⁾



NOTES:

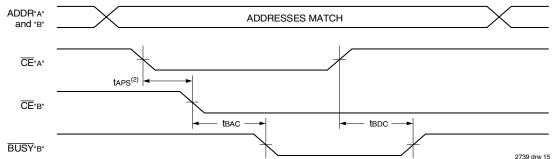
- 1. To ensure that the earlier of the two ports wins. taps is ignored for M/S = VIL (SLAVE).
- 3. $\overline{OE} = V_{IL}$ for the reading port.
- 4. If $M/\overline{S} = VIL(slave)$ then \overline{BUSY} is input $(\overline{BUSY}^*A^* = VIH)$ and $\overline{BUSY}^*B^* = "don't care"$, for this example.
- 5. All timing is the same for left and right port. Port "A' may be either left or right port. Port "B" is the port opposite from Port "A".

Timing Waveform of Write with **BUSY**

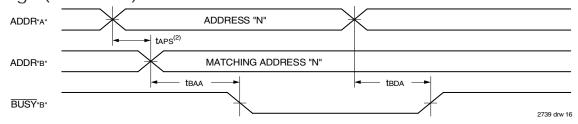


- 1. twh must be met for both BUSY input (slave) and output (master).
- 2. $\overline{\text{BUSY}}$ is asserted on Port "B", blocking R/ $\overline{\text{W}}$ "B", until $\overline{\text{BUSY}}$ "B" goes HIGH.
- 3. two is only for the 'Slave' Version.

Waveform of **BUSY** Arbitration Controlled by \overline{CE} Timing⁽¹⁾ (M/ \overline{S} = VIH)



Waveform of $\overline{\textbf{BUSY}}$ Arbitration Cycle Controlled by Address Match Timing⁽¹⁾(M/ $\overline{\textbf{S}}$ = VIH)



NOTES:

- 1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
- 2. If taps is not satisfied, the BUSY signal will be asserted on one side or another but there is no guarantee on which side BUSY will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾

	<u> </u>	<u> </u>			<u> </u>					
			7006X15 Com'l Only		7006X17 Com'l Only		7006X20 Com'l, Ind & Military		7006X25 Com'l & Military	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Мах.	Unit
INTERRUP	T TIMING									
tas	Address Set-up Time	0	_	0	_	0	_	0		ns
twr	Write Recovery Time	0	_	0	_	0	_	0		ns
tins	Interrupt Set Time	_	15	_	15		20	_	20	ns
tinr	Interrupt Reset Time		15		15		20		20	ns

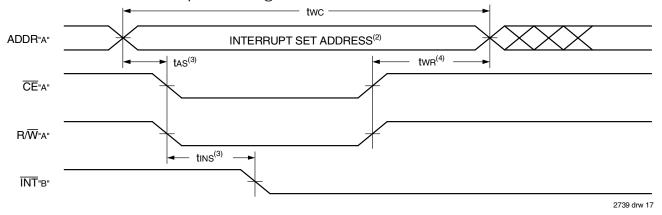
2739 tbl 16a

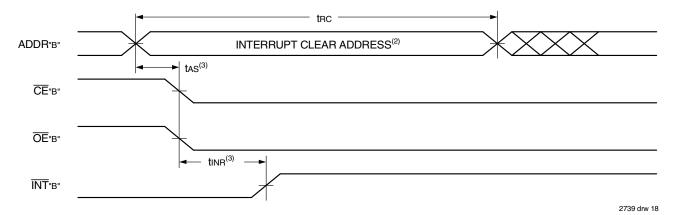
		Cor	6X35 n'I & itary	7006X55 Com'l, Ind & Military		7006X70 Military Only		
Symbol	Parameter	Min.	Мах.	Min.	Max.	Min.	Max.	Unit
INTERRUP	T TIMING							
tas	Address Set-up Time	0		0	_	0		ns
twr	Write Recovery Time	0		0	_	0		ns
tins	Interrupt Set Time	_	25		40		50	ns
tinr	Interrupt Reset Time		25		40	_	50	ns

NOTES:

1. 'X' in part numbers indicates power rating (S or L).

Waveform of Interrupt Timing(1)





NOTES:

- 1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
- 2. See Interrupt Truth Table III.
- Timing depends on which enable signal (CE or RW) is asserted last.
 Timing depends on which enable signal (CE or RW) is de-asserted first.

Truth Tables

Truth Table III — Interrupt Flag^(1,4)

				-						
		Left Port								
R/WL	CEL	ŌĒL	A13L-A0L	ĪNTL	R/W̄R	CER	ŌĒR	A13R-A0R	ĪNTR	Function
L	L	Х	3FFF	Х	Х	Х	Х	Х	L ⁽²⁾	Set Right INTR Flag
Х	Х	Х	Х	Х	Х	L	L	3FFF	H ⁽³⁾	Reset Right INTR Flag
Х	Х	Х	Х	L ⁽³⁾	L	L	Х	3FFE	Х	Set Left INTL Flag
Х	L	L	3FFE	H ⁽²⁾	Х	Х	Х	Х	Х	Reset Left INTL Flag

2739 tbl 17 NOTES:

- 1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = VIH$.
- 2. If $\overline{BUSY}_L = VIL$, then no change.
- 3. If $\overline{BUSY}R = VIL$, then no change.
- 4. INTR and INTL must be initialized at power-up.

Truth Table IV — Address **BUSY** Arbitration

	In	puts	Out	puts	
ΕĒ	C ER	Aol-A13l Aor-A13r	BUSYL ⁽¹⁾	BUSY _R (1)	Function
Χ	Χ	NO MATCH	Н	Н	Normal
Н	Χ	MATCH	Н	Н	Normal
Х	Н	MATCH	Н	Н	Normal
L	L	MATCH	(2)	(2)	Write Inhibit ⁽³⁾

NOTES:

- 2739 tbl 1
- 1. Pins \overline{BUSY}_R and \overline{BUSY}_R are both outputs when the part is configured as a master. Both are inputs when configured as a slave. \overline{BUSY}_R outputs on the IDT7006 are push pull, not open drain outputs. On slaves the \overline{BUSY}_R input internally inhibits writes.
- 2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If taps is not met, either BUSYL or BUSYR = LOW will result. BUSYL and BUSYR outputs cannot be low simultaneously.
- 3. Writes to the left port are internally ignored when BUSYL outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving LOW regardless of actual logic level on the pin.

Truth Table V — Example of Semaphore Procurement Sequence (1,2,3)

Functions	Do - D7 Left	Do - D7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTES: 2739 tbl 19

- 1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7006.
- 2. There are eight semaphore flags written to via I/Oo and read from all I/O's. These eight semaphores are addressed by Ao A2.
- 3. $\overline{CE} = VIH$, $\overline{SEM} = VIL$ to access the semaphores. Refer to the Semaphore Read/Write Control Truth Table.

Functional Description

The IDT7006 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7006 has an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{\text{CE}}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag $(\overline{\text{INT}}\text{L})$ is asserted when the right port writes to memory location 3FFE (HEX) where a write is defined as $\overline{\text{CE}} = R/\overline{\text{W}} = V_{\text{L}}$ per the Truth Table .

The left port clears the interrupt by reading address location 3FFE access when $\overline{\text{CE}}_R = \text{OE}_R = \text{V}_{IL}$, R/\overline{W} is a "don't care". Likewise, the right port interrupt flag ($\overline{\text{INT}}_R$) is asserted when the left port writes to memory location 3FFF (HEX) and to clear the interrupt flag ($\overline{\text{INT}}_R$), the right port must read the memory location 3FFF. The message (8 bits) at 3FFE or 3FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM

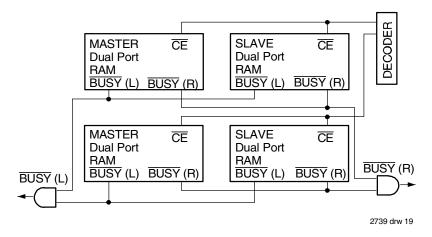


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7006 RAMs.

have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The $\overline{\text{BUSY}}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{\text{BUSY}}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of \overline{BUSY} logic is not required or desirable for all applications. In some cases it may be useful to logically OR the \overline{BUSY} outputs together and use any \overline{BUSY} indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of \overline{BUSY} logic is not desirable, the \overline{BUSY} logic can be disabled by placing the part in slave mode with the $\overline{M/S}$ pin. Once in slave mode the \overline{BUSY} pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the \overline{BUSY} pins HIGH. If desired, unintended write operations can be prevented to a port by tying the \overline{BUSY} pin for that port LOW.

The BUSY outputs on the IDT 7006 RAM in master mode, are pushpull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT7006 RAM array in width while using \overline{BUSY} logic, one master part is used to decide which side of the RAMs array will receive a \overline{BUSY} indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the \overline{BUSY} signal as a write inhibit signal. Thus on the IDT7006 RAM the \overline{BUSY} pin is an output if the part is used as a master ($\overline{M/S}$ pin = VIH), and the \overline{BUSY} pin is an input if the part used as a slave ($\overline{M/S}$ pin = VIL) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating BUSY on one side of the array and another master indicating BUSY on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The BUSY arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In

a master/slave array, both address and chip enable must be valid long enoughfor a $\overline{\text{BUSY}}$ flag to be output from the master before the actual write pulse can be initiated with the R/W signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7006 is an extremely fast Dual-Port 16Kx8CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical infunction to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{\text{CE}}$, the Dual-Port RAM enable, and $\overline{\text{SEM}}$, the semaphore enable. The $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table I where $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ are both HIGH.

Systems which can best use the IDT7006 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7006s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7006 does not use its semaphore flags to control

any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This pro-cessor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7006 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a LOW input on the $\overline{\text{SEM}}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{\text{OE}}$, and $R\overline{\text{IW}}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Dois used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table V). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select (\overline{SEM}) and output enable (\overline{OE}) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must

cause either signal ($\overline{\text{SEM}}$ or $\overline{\text{OE}}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Truth Table V). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7006's Dual-Port RAM. Say the 16K x 8 RAM was to be divided into two 8K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used

to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can

even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

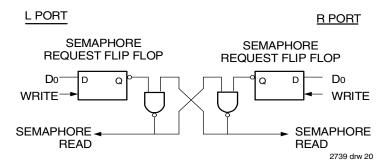
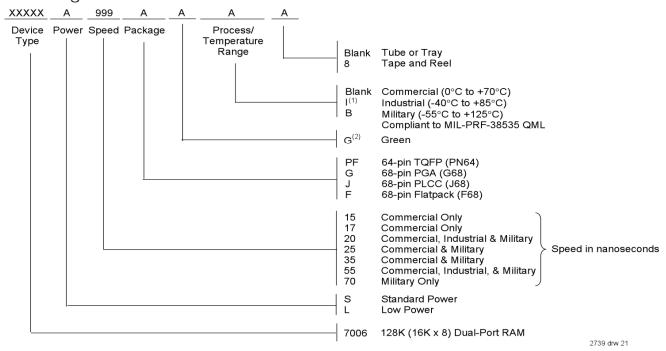


Figure 4. IDT7006 Semaphore Logic

Ordering Information



NOTES:

- Industrial temperature range is available on selected TQFP packages in standard power.
 For other speeds, packages and powers contact your sales office.
- 2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Datasheet Document History

01/04/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
		Added additional notes to pin configurations
06/03/99:		Changed drawing format
09/14/99:	Page 15	Changed 3FFF to 3FFE in Truth Table III
11/10/99:	-	Replaced IDT logo
12/22/99:	Page 1	Corrected drawing error
05/08/00:	Page 1	Added copywright info
	Page 4	Increased storage temperature parameter
		Clarified TA parameter
	Page 6	DC Electrical parameters–changed wording from "open" to "disabled"
		Changed ±500mV to 0mV in notes
09/12/01:	Page 2 & 3	Added date revision for pin configurations
	Page 6	Added Industrial temp to the column heading for 20ns to DC Electrical Characteristics
	Pages 7,9,12&14	Added Industrial temp to the column headings for 20ns to AC Electrical Characteristics
	Page 7	Table 13a appeared twice, corrected and placed table 13b for 35, 55 & 70ns speeds
	Pages 4,6,7,9,	Removed Industrial temp note from all tables
	12 & 14	
	Page 20	Added Industrial temp to 20ns in ordering information

10/21/08:

08/07/14:

Datasheet Document History (cont'd)

01/31/06: Page 1 Added green availability to features

Page 20 Added green indicator to ordering information Page 20 Removed "IDT" from orderable part number Page 20 Added Tape and Reel to Ordering Information

Page 2, 3 & 20 The package codes changed from PN64-1, G68-1, J68-1 & F68-1 to PN64, G68, J68 & F68

respectively to match the standard package codes



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