

KAI-08670

3600 (H) x 2400 (V) Interline CCD Image Sensor

Description

The KAI-08670 Image Sensor is an 8.6-megapixel CCD in an APS-H optical format. Based on the TRUESENSE 7.4 micron Interline Transfer CCD Platform, the sensor provides very high smear rejection and up to 82 dB linear dynamic range through the use of a unique dual-gain amplifier. A flexible readout architecture enables use of 1, 2, or 4 outputs for full resolution readout up to 12 frames per second, while a vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control.

Table 1. GENERAL SPECIFICATIONS

| Parameter | Typical Value |
|---|---|
| Architecture | Interline CCD, Progressive Scan |
| Total Number of Pixels | 3672 (H) × 2472 (V) |
| Number of Effective Pixels | 3624 (H) × 2424 (V) |
| Number of Active Pixels | 3600 (H) × 2400 (V) |
| Pixel Size | 7.4 μm (H) × 7.4 μm (V) |
| Active Image Size | 26.64 mm (H) × 17.76 mm (V), 32 mm (Diagonal), APS-H Optical Format |
| Aspect Ratio | 3:2 |
| Number of Outputs | 1, 2, or 4 |
| Charge Capacity | 44,000 electrons |
| Output Sensitivity | 9.7 μV/e ⁻ (Low), 33 μV/e ⁻ (High) |
| Quantum Efficiency R, G, B (-FXA, -QXA) Pan (-AXA, -QXA) | 33%, 39%, 40% 48% |
| Read Noise (f = 40 MHz) | 12 e ⁻ rms |
| Dark Current Photodiode VCCD | 1 e ⁻ /s 145 e ⁻ /s |
| Dark Current Doubling Temp. Photodiode VCCD | 7°C 9°C |
| Dynamic Range High Gain Amp (40 MHz) Dual Amp, 2×2 Bin (40 MHz) | 70 dB 82 dB |
| Charge Transfer Efficiency | 0.999999 |
| Blooming Suppression | > 1000 X |
| Smear | -115 dB |
| Image Lag | < 10 electrons |
| Maximum Pixel Clock Speed | 40 MHz |
| Maximum Frame Rate Quad Output Dual Output Single Output | 12 fps 6 fps 3 fps |
| Package | 72 Pin PGA |
| Cover Glass | AR Coated, 2 Sides |

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.



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Figure 1. KAI-08670 Interline CCD Image Sensor

Features

- Superior Smear Rejection
- Up to 82 dB Linear Dynamic Range
- Bayer Color Pattern, TRUESENSE Sparse Color Filter Pattern, and Monochrome Configurations
- Progressive Scan & Flexible Readout Architecture
- High Frame Rate
- High Sensitivity – Low Noise Architecture
- Package Pin Reserved for Device Identification

Application

- Industrial Imaging and Inspection
- Traffic
- Surveillance

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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The sensor is available with the TRUESENSE Sparse Color Filter Pattern, a technology which provides a 2x improvement in light sensitivity compared to a standard color Bayer part.

The sensor is package and pin-compatible with the KAI-16050 Image Sensor, and shares common pin-out

and electrical configurations with a full family of ON Semiconductor Interline Transfer CCD image sensors, allowing a single camera design to be leveraged in support of multiple devices.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION – KAI-08670 IMAGE SENSOR

| Part Number | Description | Marking Code |
|---------------------|--|--------------------------------|
| KAI-08670-AXA-JD-B1 | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1 | KAI-08670-AXA Serial Number |
| KAI-08670-AXA-JD-B2 | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 2 | |
| KAI-08670-AXA-JD-AE | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade | |
| KAI-08670-FXA-JD-B1 | Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1 | KAI-08670-FXA Serial Number |
| KAI-08670-FXA-JD-B2 | Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 2 | |
| KAI-08670-FXA-JD-AE | Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade | |
| KAI-08670-QXA-JD-B1 | Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1 | KAI-08670-QXA Serial Number |
| KAI-08670-QXA-JD-B2 | Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 2 | |
| KAI-08670-QXA-JD-AE | Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade | |

Table 3. ORDERING INFORMATION – EVALUATION SUPPORT

| Part Number | Description |
|--------------------------|--|
| G2-FPGA-BD-14-40-A-GEVK | FPGA Board for IT-CCD Evaluation Hardware |
| KAI-72PIN-HEAD-BD-A-GEVB | 72 Pin Imager Board for IT-CCD Evaluation Hardware |
| LENS-MOUNT-KIT-B-GEVK | Lens Mount Kit for IT-CCD Evaluation Hardware |

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

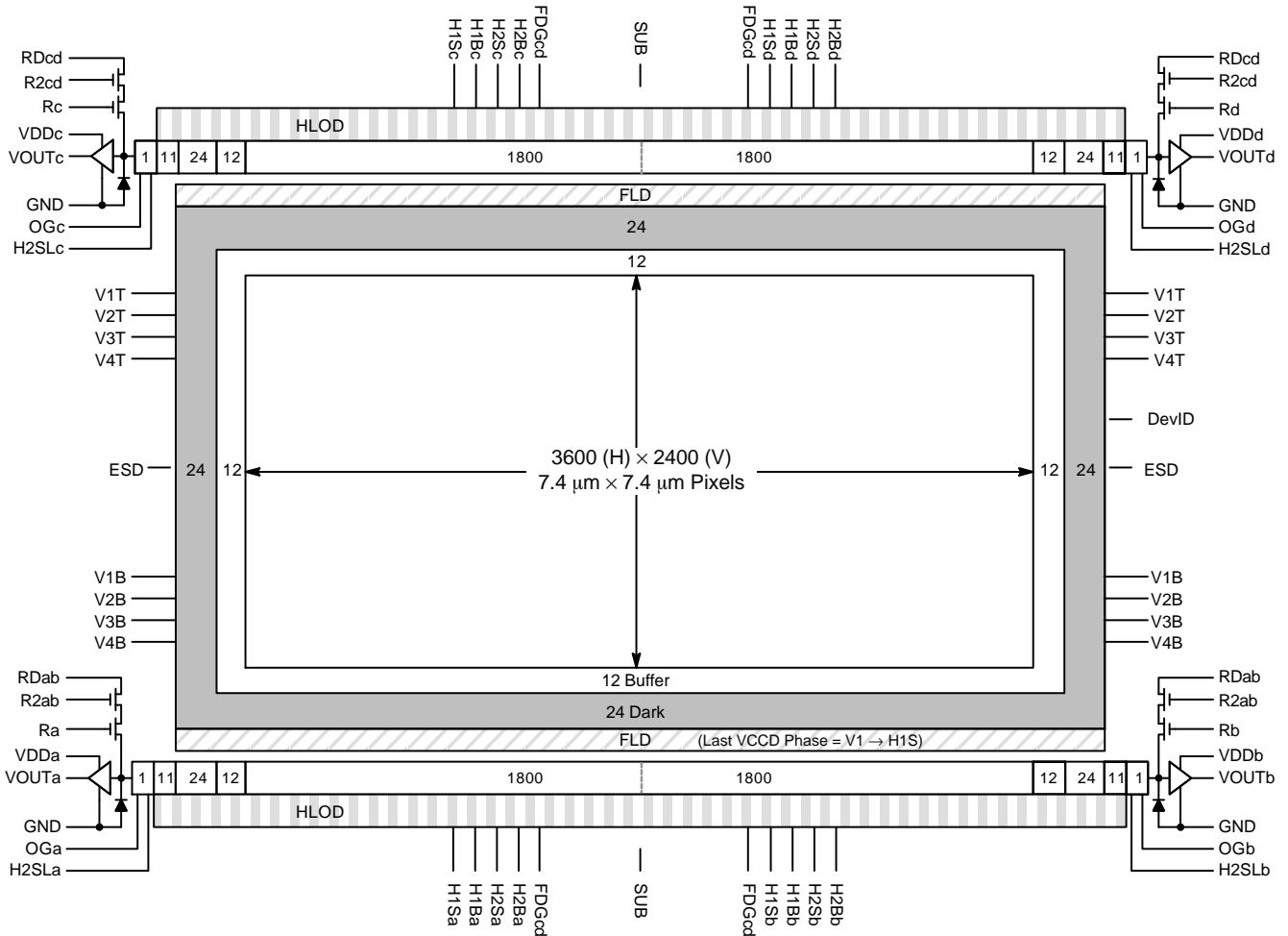


Figure 2. Block Diagram

Dark Reference Pixels

There are 24 dark reference rows at the top and 24 dark rows at the bottom of the image sensor. The 24 dark columns on the left or right side of the image sensor should be used as a dark reference.

Under normal circumstances use only the center 22 columns of the 24 column dark reference due to potential light leakage.

Dummy Pixels

Within each horizontal shift register there are 12 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level. In addition, there is one dummy row of pixels at the top and bottom of the image.

Active Buffer Pixels

12 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

ESD Protection

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

Bayer Color Filter Pattern



Figure 3. Bayer Color Filter Pattern

TRUESENSE Sparse Color Filter Pattern



Figure 4. TRUESENSE Sparse Color Filter Pattern

Physical Description

Pin Description and Device Orientation

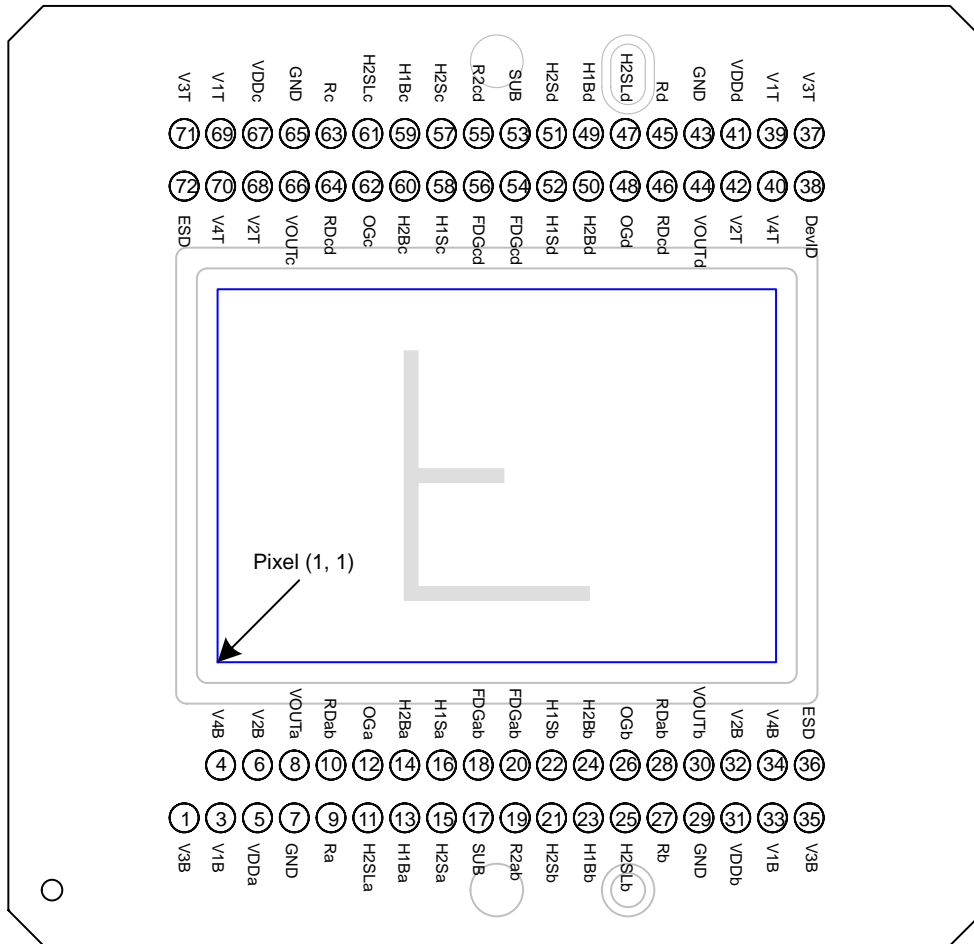


Figure 5. Package Pin Designations – Top View

Table 4. PACKAGE PIN DESCRIPTION

| Pin | Name | Description |
|-----|-------|--|
| 1 | V3B | Vertical CCD Clock, Phase 3, Bottom |
| 3 | V1B | Vertical CCD Clock, Phase 1, Bottom |
| 4 | V4B | Vertical CCD Clock, Phase 4, Bottom |
| 5 | VDDa | Output Amplifier Supply, Quadrant a |
| 6 | V2B | Vertical CCD Clock, Phase 2, Bottom |
| 7 | GND | Ground |
| 8 | VOUTa | Video Output, Quadrant a |
| 9 | Ra | Reset Gate, Standard (High) Gain, Quadrant a |
| 10 | RDaB | Reset Drain, Quadrants a & b |
| 11 | H2SLa | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a |
| 12 | OGa | Output Gate, Quadrant a |
| 13 | H1Ba | Horizontal CCD Clock, Phase 1, Barrier, Quadrant a |
| 14 | H2Ba | Horizontal CCD Clock, Phase 2, Barrier, Quadrant a |
| 15 | H2Sa | Horizontal CCD Clock, Phase 2, Storage, Quadrant a |

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Table 4. PACKAGE PIN DESCRIPTION (continued)

| Pin | Name | Description |
|-----|-----------------------|--|
| 16 | H1Sa | Horizontal CCD Clock, Phase 1, Storage, Quadrant a |
| 17 | SUB | Substrate |
| 18 | FDG a b | Fast Line Dump Gate, Bottom |
| 19 | R2 a b | Reset Gate, Low Gain, Quadrants a & b |
| 20 | FDG a b | Fast Line Dump Gate, Bottom |
| 21 | H2 S b | Horizontal CCD Clock, Phase 2, Storage, Quadrant b |
| 22 | H1 S b | Horizontal CCD Clock, Phase 1, Storage, Quadrant b |
| 23 | H1 B b | Horizontal CCD Clock, Phase 1, Barrier, Quadrant b |
| 24 | H2 B b | Horizontal CCD Clock, Phase 2, Barrier, Quadrant b |
| 25 | H2 SL b | Horizontal CCD Clock, Phase 1, Storage, Last Phase, Quadrant b |
| 26 | O G b | Output Gate, Quadrant b |
| 27 | R b | Reset Gate, Standard (High) Gain, Quadrant b |
| 28 | R D a b | Reset Drain, Quadrants a & b |
| 29 | GND | Ground |
| 30 | V OUT b | Video Output, Quadrant b |
| 31 | V DD b | Output Amplifier Supply, Quadrant b |
| 32 | V 2 B | Vertical CCD Clock, Phase 2, Bottom |
| 33 | V 1 B | Vertical CCD Clock, Phase 1, Bottom |
| 34 | V 4 B | Vertical CCD Clock, Phase 4, Bottom |
| 35 | V 3 B | Vertical CCD Clock, Phase 3, Bottom |
| 36 | ESD | ESD Protection Disable |
| 37 | V 3 T | Vertical CCD Clock, Phase 3, Top |
| 38 | Dev ID | Device Identification |
| 39 | V 1 T | Vertical CCD Clock, Phase 1, Top |
| 40 | V 4 T | Vertical CCD Clock, Phase 4, Top |
| 41 | V DD d | Output Amplifier Supply, Quadrant d |
| 42 | V 2 T | Vertical CCD Clock, Phase 2, Top |
| 43 | GND | Ground |
| 44 | V OUT d | Video Output, Quadrant d |
| 45 | R d | Reset Gate, Standard (High) Gain, Quadrant d |
| 46 | R D c d | Reset Drain, Quadrants c & d |
| 47 | H2 SL d | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d |
| 48 | O G d | Output Gate, Quadrant d |
| 49 | H1 B d | Horizontal CCD Clock, Phase 1, Barrier, Quadrant d |
| 50 | H2 B d | Horizontal CCD Clock, Phase 2, Barrier, Quadrant d |
| 51 | H2 S d | Horizontal CCD Clock, Phase 2, Storage, Quadrant d |
| 52 | H1 S d | Horizontal CCD Clock, Phase 1, Storage, Quadrant d |
| 53 | SUB | Substrate |
| 54 | FDG c d | Fast Line Dump Gate, Top |
| 55 | R2 c d | Reset Gate, Low Gain, Quadrants c & d |
| 56 | FDG c d | Fast Line Dump Gate, Top |
| 57 | H2 S c | Horizontal CCD Clock, Phase 2, Storage, Quadrant c |
| 58 | H1 S c | Horizontal CCD Clock, Phase 1, Storage, Quadrant c |
| 59 | H1 B c | Horizontal CCD Clock, Phase 1, Barrier, Quadrant c |
| 60 | H2 B c | Horizontal CCD Clock, Phase 2, Barrier, Quadrant c |

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Table 4. PACKAGE PIN DESCRIPTION (continued)

| Pin | Name | Description |
|-----|-------|--|
| 61 | H2SLc | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c |
| 62 | OGc | Output Gate, Quadrant c |
| 63 | Rc | Reset Gate, Standard (High) Gain, Quadrant c |
| 64 | RDcd | Reset Drain, Quadrants c & d |
| 65 | GND | Ground |
| 66 | VOUc | Video Output, Quadrant c |
| 67 | VDDc | Output Amplifier Supply, Quadrant c |
| 68 | V2T | Vertical CCD Clock, Phase 2, Top |
| 69 | V1T | Vertical CCD Clock, Phase 1, Top |
| 70 | V4T | Vertical CCD Clock, Phase 4, Top |
| 71 | V3T | Vertical CCD Clock, Phase 3, Top |
| 72 | ESD | EDS Protection Disable |

1. Liked named pins are internally connected and should have a common drive signal.

IMAGING PERFORMANCE

Table 5. TYPICAL OPERATIONAL CONDITIONS

(Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.)

| Description | Condition | Notes |
|--------------|--|-------|
| Light Source | Continuous Red, Green and Blue LED Illumination. | 1 |
| Operation | Nominal Operating Voltages and Timing. | |

1. For monochrome sensor, only green LED used.

Specifications

Table 6. PERFORMANCE SPECIFICATIONS

| Description | Symbol | Min. | Nom. | Max. | Unit | Sampling Plan | Temperature Tested at (°C) |
|---|----------------------------|-------------|-------------|-------------|-----------|---------------|----------------------------|
| ALL CONFIGURATIONS | | | | | | | |
| Dark Field Global Non-Uniformity | DSNU | – | – | 5 | mVpp | Die | 27, 40 |
| Bright Field Global Non-Uniformity (Note 1) | | – | 2 | 5 | % rms | Die | 27, 40 |
| Bright Field Global Peak to Peak Non-Uniformity (Note 1) | PRNU | – | 10 | 30 | % pp | Die | 27, 40 |
| Bright Field Center Non-Uniformity (Note 1) | | – | 1 | 2 | % rms | Die | 27, 40 |
| Maximum Photo-Response Non-Linearity High Gain (4,000 to 20,000 electrons) Low Gain (8,000 to 80,000 electrons) | NL_HG1 NL_HG2 NL_LG1 | – – – | 2 3 6 | – – – | % | Design | |
| Maximum Gain Difference between Outputs (Note 2) | ΔG | – | – | 10 | % | Design | |
| Horizontal CCD Charge Capacity | H_{Ne} | – | 100 | – | ke^- | Design | |
| Vertical CCD Charge Capacity | V_{Ne} | – | 60 | – | ke^- | Design | |
| Photodiode Charge Capacity (Note 3) | P_{Ne} | – | 44 | – | ke^- | Die | 27, 40 |
| Floating Diffusion Capacity – High Gain | FNe_HG | 40 | – | – | ke^- | Die | 27, 40 |
| Floating Diffusion Capacity – Low Gain | FNe_LG | 160 | – | – | ke^- | Die | 27, 40 |
| Horizontal CCD Charge Transfer Efficiency | HCTE | 0.999995 | 0.999999 | – | | Die | |
| Vertical CCD Charge Transfer Efficiency | VCTE | 0.999995 | 0.999999 | – | | Die | |
| Photodiode Dark Current | I_{PD} | – | 1 | 70 | e/p/s | Die | 40 |
| Vertical CCD Dark Current | I_{VD} | – | 145 | 400 | e/p/s | Die | 40 |
| Image Lag | Lag | – | – | 10 | e^- | Design | |
| Anti-Blooming Factor | X_{AB} | 1,000 | – | – | | Design | |
| Vertical Smear | Smr | – | –115 | – | dB | Design | |
| Read Noise (Note 4) High Gain Low Gain | n_{e-T} | – – | 12 35 | – – | e^- rms | Design | |
| Dynamic Range, Standard (Notes 4, 5) | DR | – | 70 | – | dB | Design | |
| Dynamic Range, Extended Linear Dynamic Range Mode (XLDR) (Notes 4, 5) | XLDR | – | 82 | – | dB | Design | |

Table 6. PERFORMANCE SPECIFICATIONS (continued)

| Description | Symbol | Min. | Nom. | Max. | Unit | Sampling Plan | Temperature Tested at (°C) |
|---|---------------------|------|------|------|-------------|---------------|----------------------------|
| ALL CONFIGURATIONS | | | | | | | |
| Output Amplifier DC Offset | V_{ODC} | – | 9.0 | – | V | Die | 27, 40 |
| Output Amplifier Bandwidth (Note 6) | f_{-3db} | – | 250 | – | MHz | Die | |
| Output Amplifier Impedance | R_{OUT} | – | 127 | – | Ω | Die | 27, 40 |
| Output Amplifier Sensitivity | $\Delta V/\Delta N$ | – | 33 | – | $\mu V/e^-$ | Design | |
| High Gain | | – | 9.7 | – | | | |
| Low Gain | | – | | – | | | |
| KAI-08670-AXA AND KAI-08670-QXA CONFIGURATIONS | | | | | | | |
| Peak Quantum Efficiency | QE_{MAX} | – | 48 | – | % | Design | |
| Peak Quantum Efficiency Wavelength | λ_{QE} | – | 490 | – | nm | Design | |
| KAI-08670-FXA AND KAI-08670-QXA CONFIGURATIONS | | | | | | | |
| Peak Quantum Efficiency | QE_{MAX} | – | 33 | – | % | Design | |
| Red | | – | 39 | – | | | |
| Green | | – | 40 | – | | | |
| Blue | | – | | – | | | |
| Peak Quantum Efficiency Wavelength | λ_{QE} | – | 605 | – | nm | Design | |
| Red | | – | 535 | – | | | |
| Green | | – | 455 | – | | | |
| Blue | | – | | – | | | |

1. Per color.
2. Value is over the range of 10% to 100% of linear signal level saturation.
3. The operating value of the substrate voltage, V_{AB} , will be marked on the shipping container for each device. The value of V_{AB} is set such that the photodiode charge capacity is 440 mV. This value is determined while operating the device in the low gain mode. V_{AB} value assigned is valid for both modes; high gain or low gain.
4. At 40 MHz.
5. Uses 20LOG (P_{Ne} / n_{e-T}).
6. Assumes 5 pF load.

Linear Signal Range



Figure 6. High Gain Linear Signal Range

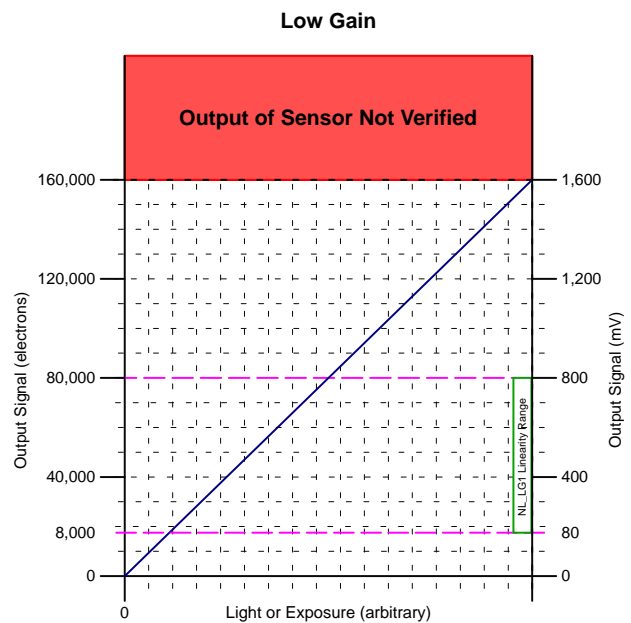


Figure 7. Low Gain Linear Signal Range

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome with Microlens



Figure 8. Monochrome with Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens

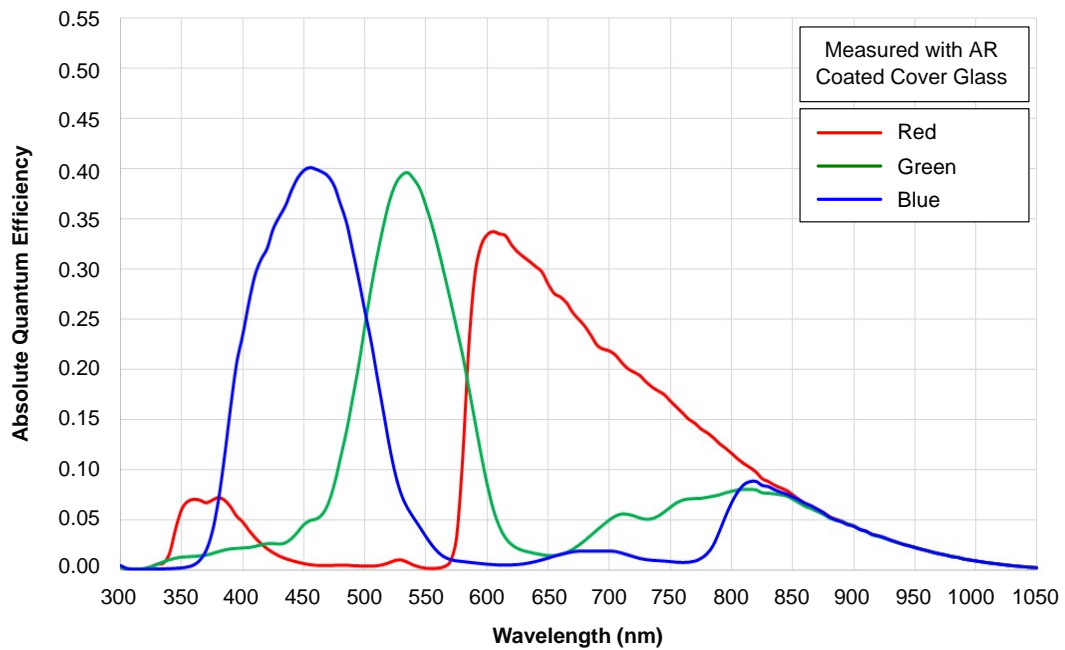


Figure 9. Color (Bayer RGB) with Microlens Quantum Efficiency

Color (TRUESENSE Sparse CFA) with Microlens



Figure 10. Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency

Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD. For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

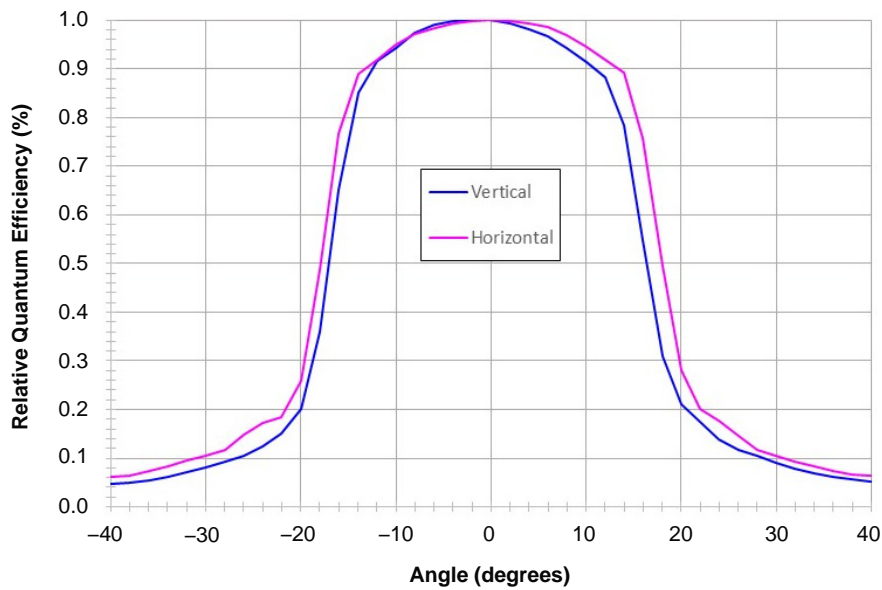


Figure 11. Monochrome with Microlens Angular Quantum Efficiency

Color (Bayer RGB) with Microlens

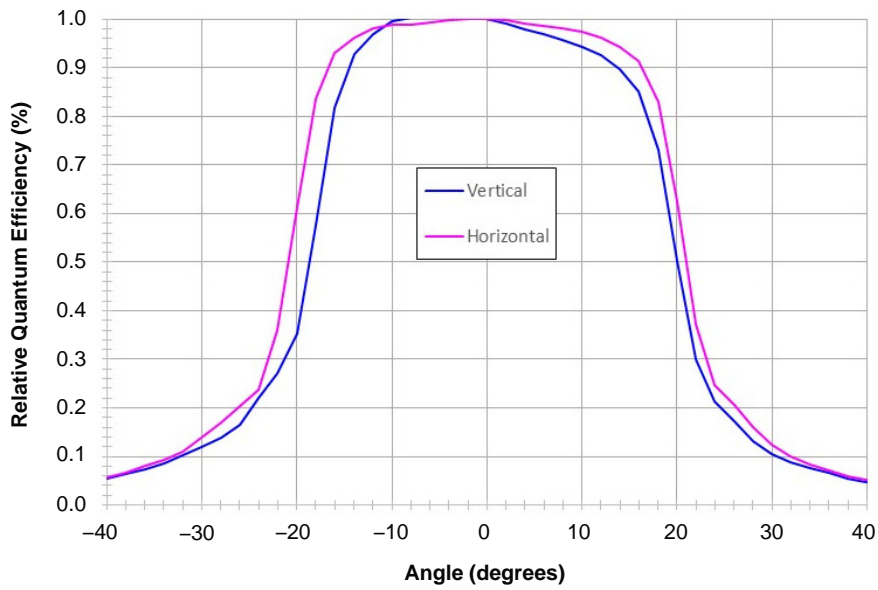


Figure 12. Color (Bayer RGB) with Microlens Angular Quantum Efficiency

Dark Current vs. Temperature



Figure 13. Dark Current vs. Temperature

Power-Estimated

Power-Estimated – Full Resolution

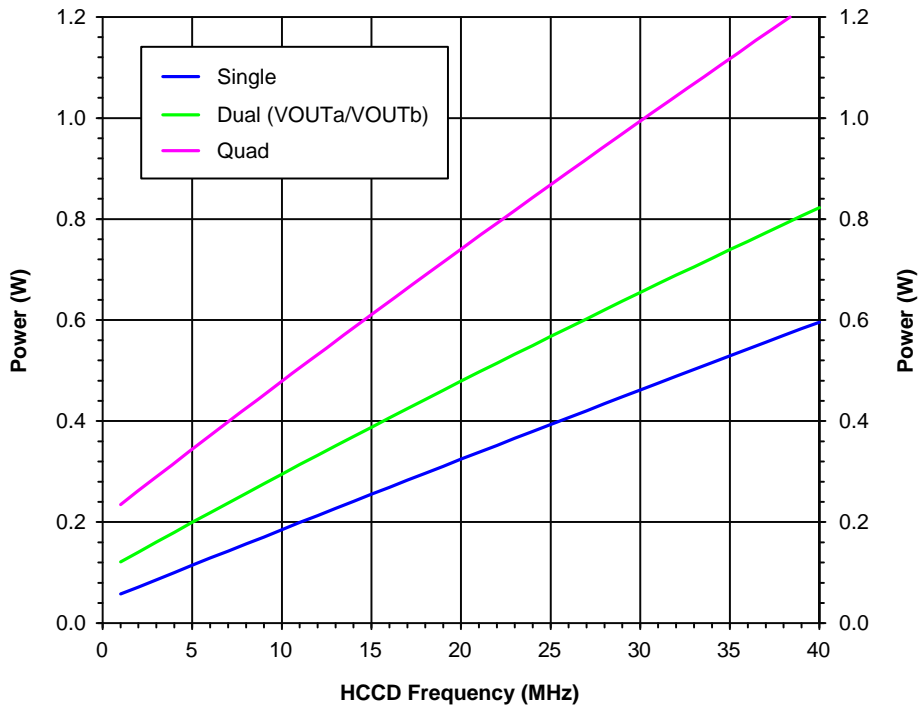


Figure 14. Power – Full Resolution

Power-Estimated – 1/4 Resolution – 2x2 Binning

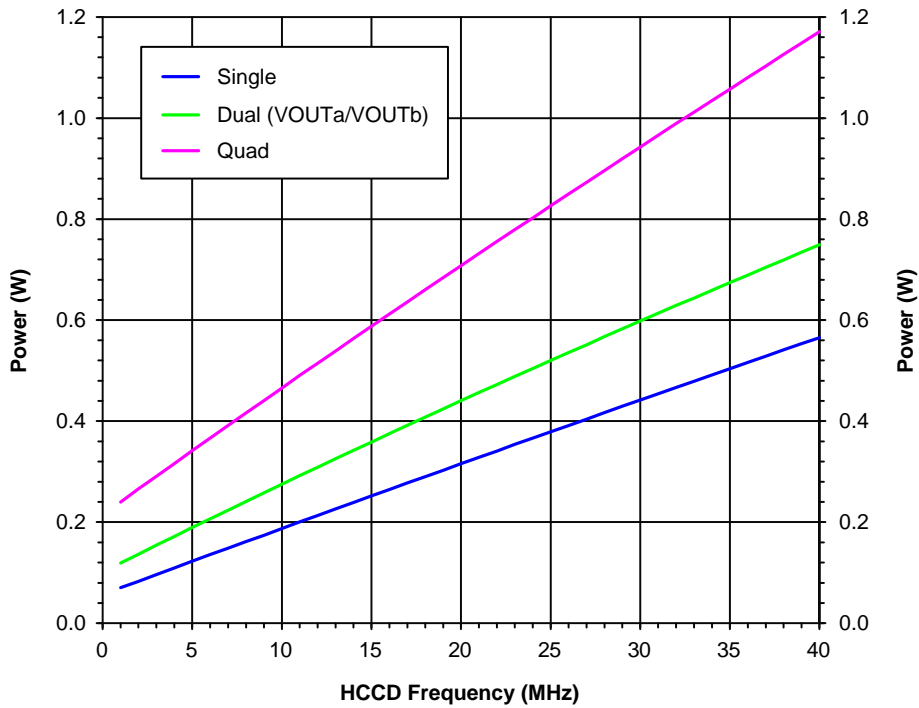


Figure 15. Power – 1/4 Resolution – Constant HCCD

Power-Estimated – 1/4 Resolution – 2x2 Binning using Variable HCCD XLDR



Figure 16. Power – 1/4 Resolution – Variable HCCD XLDR

Power-Estimated – 1/4 Resolution – 2x2 Binning using Constant HCCD XLDR

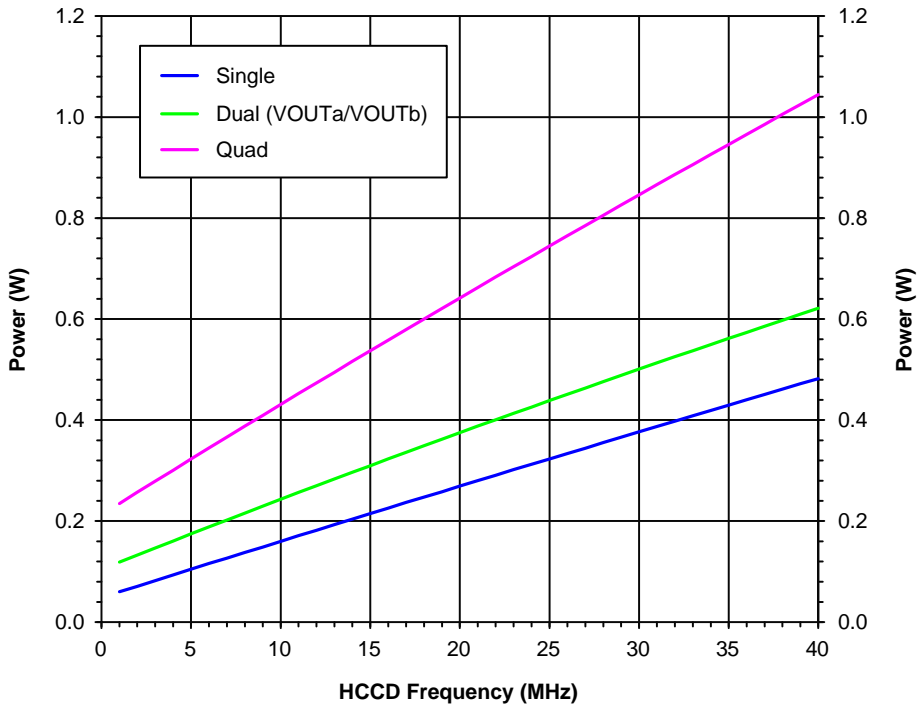


Figure 17. Power – 1/4 Resolution – Constant HCCD XLDR

Frame Rates

Frame Rates – Full Resolution

Frame rates are for low and high gain modes of operation.

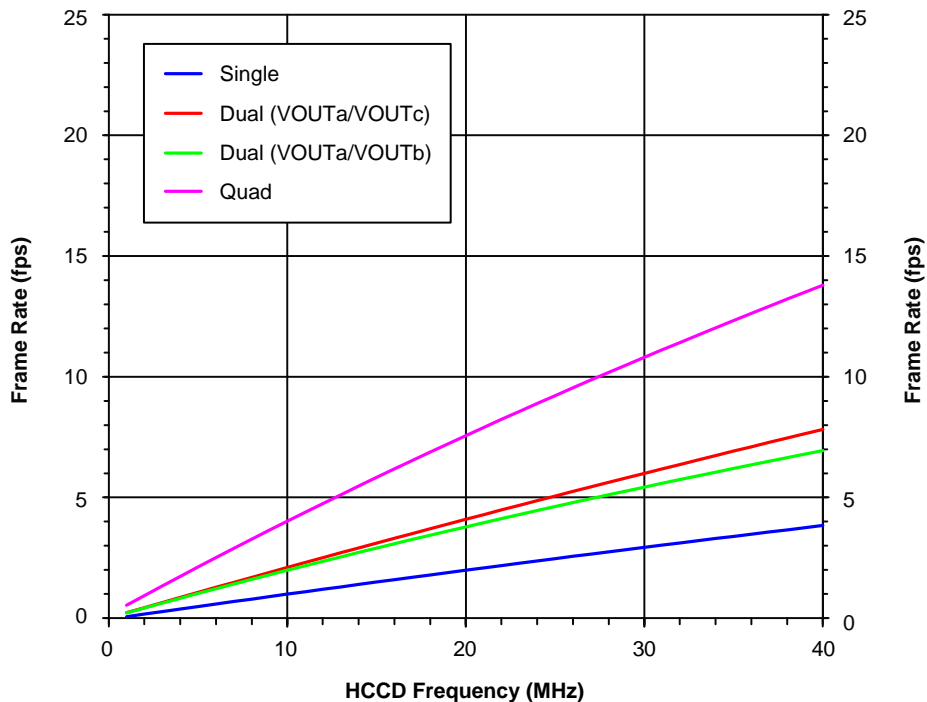


Figure 18. Frame Rates – Full Resolution

Frame Rates – 1/4 Resolution – 2x2 Binning

Frame rates are for low and high gain modes of operation.

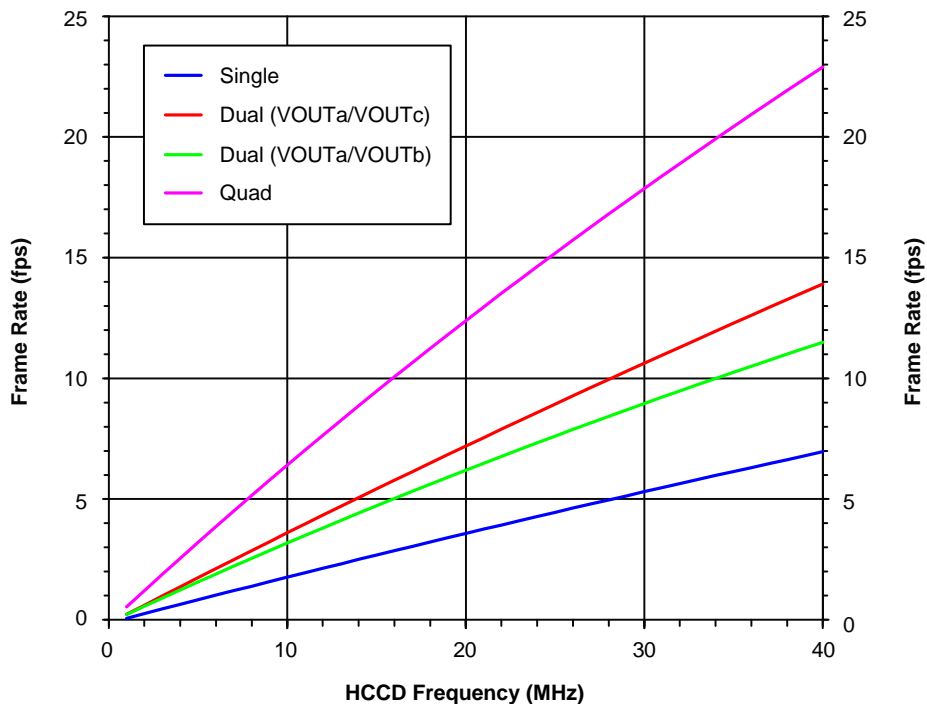


Figure 19. Frame Rates – 1/4 Resolution – Constant HCCD

Frame Rates – 1/4 Resolution – 2x2 Binning using Variable HCCD XLDR

Frame rates for variable HCCD modes of operation.

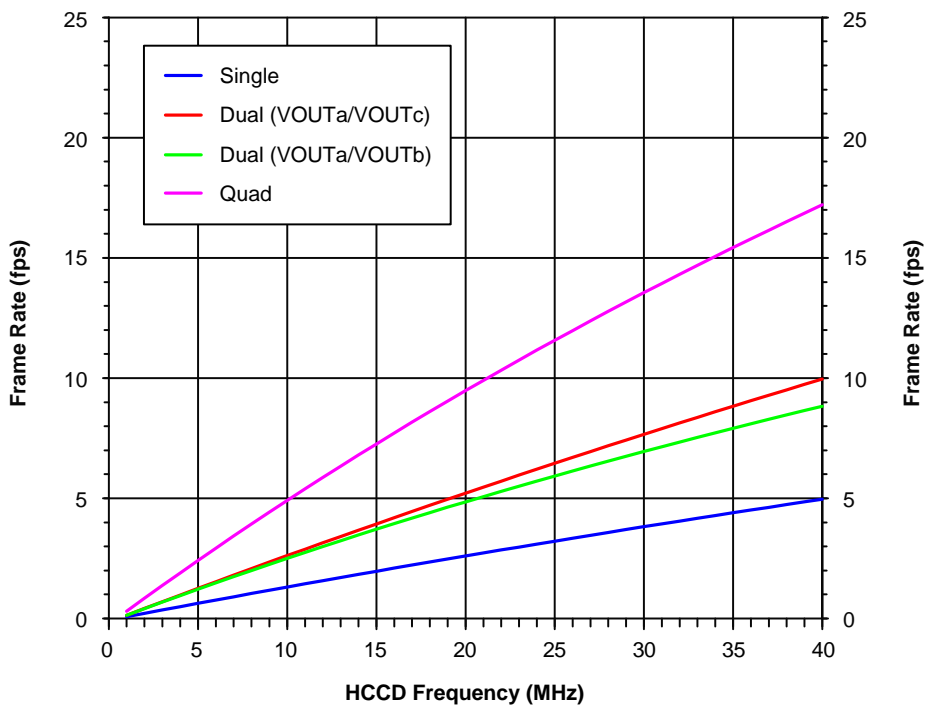


Figure 20. Frame Rates – 1/4 Resolution – Variable HCCD XLDR

Frame Rates – 1/4 Resolution – 2x2 Binning using Constant HCCD XLDR

Frame rates for a constant HCCD mode of operation.

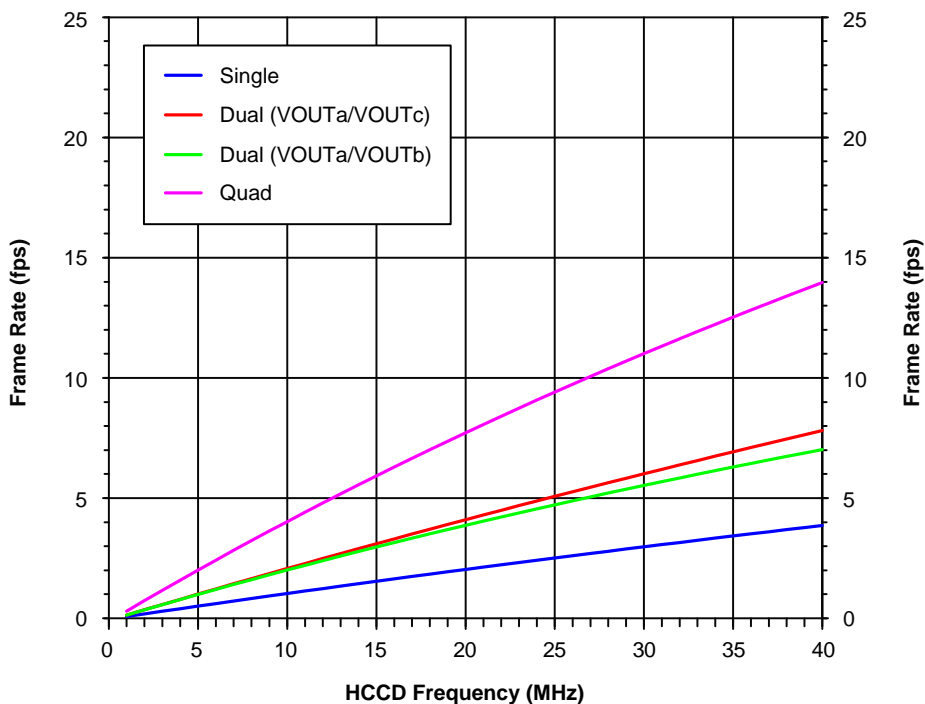


Figure 21. Frame Rates – 1/4 Resolution – Constant HCCD XLDR

DEFECT DEFINITIONS

Table 7. OPERATION CONDITIONS FOR DEFECT TESTING AT 40°C

| Description | Condition | Notes |
|---------------------------------------|---|-------|
| Operational Mode | One Output, Using VOUTa, Continuous Readout | |
| HCCD Clock Frequency | 20 MHz | |
| Pixels per Line | 3,684 | |
| Lines per Frame | 2,472 | |
| Line Time | 196.2 μs | |
| Frame Time | 485.1 ms | |
| Photodiode Integration Time (PD_Tint) | PD_Tint = Frame Time = 495.0 ms, No Electronic Shutter Used | |
| Temperature | 40°C | |
| Light Source | Continuous Red, Green and Blue LED Illumination | 1 |
| Operation | Nominal Operating Voltages and Timing | |

1. For monochrome sensor, only the green LED is used.

Table 8. DEFECT DEFINITIONS FOR TESTING AT 40°C

| Description | Definition | Grade 1 | Grade 2 Mono | Grade 2 Color | Notes |
|---|---|---------|--------------|---------------|-------|
| Major Dark Field Defective Bright Pixel | Defect \geq 325 mV | 85 | 850 | 850 | 1 |
| Major Bright Field Defective Dark Pixel | $-12\% \geq$ Defect \geq 12% | 85 | 850 | 850 | 1 |
| Minor Dark Field Defective Bright Pixel | Defect \geq 163 mV | 170 | 1,700 | 1,700 | |
| Cluster Defect | A group of 2 to 19 (Grade 1) or 2 to 38 (Grade 2) contiguous major defective pixels, but no more than 3 adjacent defect horizontally. | 17 | 17 | 17 | 2 |
| Column Defect | A group of more than 10 contiguous major defective pixels along a single column. | 0 | 2 | 9 | 2 |

1. For the color devices (KAI-08670-FXA and KAI-08670-QXA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Table 9. OPERATION CONDITIONS FOR DEFECT TESTING AT 27°C

| Description | Condition | Notes |
|---------------------------------------|---|-------|
| Operational Mode | One Output, Using VOUTa, Continuous Readout | |
| HCCD Clock Frequency | 20 MHz | |
| Pixels per Line | 3,684 | |
| Lines per Frame | 2,472 | |
| Line Time | 196.2 μs | |
| Frame Time | 485.1 ms | |
| Photodiode Integration Time (PD_Tint) | PD_Tint = Frame Time = 495.0 ms, No Electronic Shutter Used | |
| Temperature | 27°C | |
| Light Source | Continuous Red, Green and Blue LED Illumination | 1 |
| Operation | Nominal Operating Voltages and Timing | |

1. For monochrome sensor, only the green LED is used.

Table 10. DEFECT DEFINITIONS FOR TESTING AT 27°C

| Description | Definition | Grade 1 | Grade 2 Mono | Grade 2 Color | Notes |
|---|---|---------|--------------|---------------|-------|
| Major Dark Field Defective Bright Pixel | Defect ≥ 100 mV | 85 | 850 | 850 | 1 |
| Major Bright Field Defective Dark Pixel | -12% ≥ Defect ≥ 12% | 85 | 850 | 850 | 1 |
| Minor Dark Field Defective Bright Pixel | Defect ≥ 52 mV | 170 | 1,700 | 1,700 | |
| Cluster Defect | A group of 2 to 19 (Grade 1) or 2 to 38 (Grade 2) contiguous major defective pixels, but no more than 3 adjacent defect horizontally. | 17 | 17 | 17 | 2 |
| Column Defect | A group of more than 10 contiguous major defective pixels along a single column. | 0 | 2 | 9 | 2 |

1. For the color devices (KAI-08670-FXA and KAI-08670-QXA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point

defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps. See Figure 22 for the location of pixel 1, 1.

TEST DEFINITIONS

Test Regions of Interest

Image Area ROI: Pixel (1, 1) to Pixel (3624, 2424)
 Active Area ROI: Pixel (13, 13) to Pixel (3612, 2412)
 Center ROI: Pixel (1763, 1163) to
 Pixel (1862, 1262)

Overclocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 22 for a pictorial representation of the regions of interest.

Only the Active Area ROI pixels are used for performance and defect tests.



Figure 22. Regions of Interest

Tests

Dark Field Global Non-Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. The average signal level of each of the 256 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI}[i] = (\text{ROI Average in Counts} - \text{Horizontal Overclock Average in Counts}) \cdot \text{mV per Count}$$

Units : mVpp (millivolts Peak to Peak)

Where $i = 1$ to 256. During this calculation on the 256 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,320 mV. Global non-uniformity is defined as:

$$\text{Global Non-Uniformity} = 100 \cdot \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right)$$

Units : % rms

Active Area Signal = Active Area Average - Dark Column Average

Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,320 mV. The sensor is partitioned into 256 sub regions of interest, each of which is 128 by 128

pixels in size. The average signal level of each of the 256 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI}[i] = (\text{ROI Average in Counts} - \text{Horizontal Overclock Average in Counts}) \cdot \text{mV per Count}$$

Where i = 1 to 256. During this calculation on the 144 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = 100 \cdot \left(\frac{\text{Max. Signal} - \text{Min. Signal}}{\text{Active Area Signal}} \right)$$

Units : % pp

Center Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,320 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 \cdot \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units : % rms

Center ROI Signal = Center ROI Average – Dark Column Average

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 924 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,320 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

$$\text{Dark Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

$$\text{Bright Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

The sensor is then partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 924 mV.
- Dark defect threshold: 924 mV · 12% = 111 mV.
- Bright defect threshold: 924 mV · 12% = 111 mV.
- Region of interest #1 selected. This region of interest is pixels 17, 17 to pixels 144, 144.
 - ◆ Median of this region of interest is found to be 920 mV.
 - ◆ Any pixel in this region of interest that is ≤ (920 – 111 mV) 809 mV in intensity will be marked defective.
 - ◆ Any pixel in this region of interest that is ≥ (920 + 111 mV) 1,031 mV in intensity will be marked defective.
- All remaining 144 sub regions of interest are analyzed for defective pixels in the same manner.

OPERATION

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the

description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

Table 11. ABSOLUTE MAXIMUM RATINGS

| Description | Symbol | Minimum | Maximum | Unit | Notes |
|-----------------------|------------------|---------|---------|------|-------|
| Operating Temperature | T _{OP} | -50 | 70 | °C | 1 |
| Humidity | RH | 5 | 90 | % | 2 |
| Output Bias Current | I _{OUT} | - | 60 | mA | 3 |
| Off-Chip Load | C _L | - | 10 | pF | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Noise performance will degrade at higher temperatures.
- T = 25°C. Excessive humidity will degrade MTTF.
- Total for all outputs. Maximum current is -15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Table 12. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

| Description | Minimum | Maximum | Unit | Notes |
|---|-----------|------------|------|-------|
| VDD _α , VOUT _α , RD _α | -0.4 | 17.5 | V | 1 |
| RD _α | -0.4 | 15.5 | V | 1 |
| V1B, V1T | ESD - 0.4 | ESD + 24.0 | V | |
| V2B, V2T, V3B, V3T, V4B, V4T | ESD - 0.4 | ESD + 14.0 | V | |
| FDG _{ab} , FDG _{cd} | ESD - 0.4 | ESD + 15.0 | V | |
| H1S _α , H1B _α , H2S _α , H2B _α , H2SL _α , R1 _α , R2 _α , OG _α | ESD - 0.4 | ESD + 14.0 | V | 1 |
| ESD | -10.0 | 0.0 | V | |
| SUB | -0.4 | 40.0 | V | 2 |

- α denotes a, b, c or d.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Reset Pin, Low Gain (R2ab and R2cd)

The R2ab and R2bc (pins 19 and 55) each have an internal circuit to bias the pins to 4.3 V. This feature assures the device is set to operate in the high gain mode when pins 19

and 55 are not connected in the application to a clock driver. Typical capacitor coupled drivers will not drive this structure.

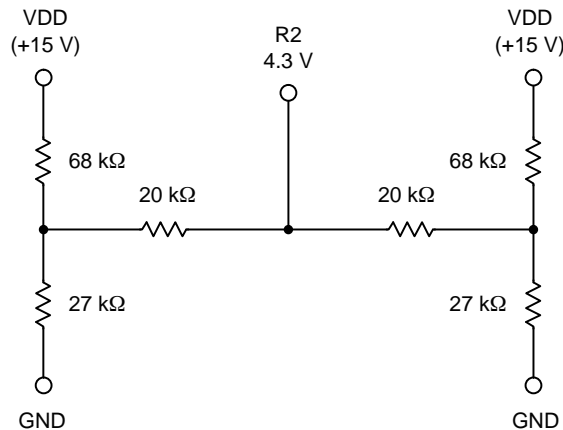
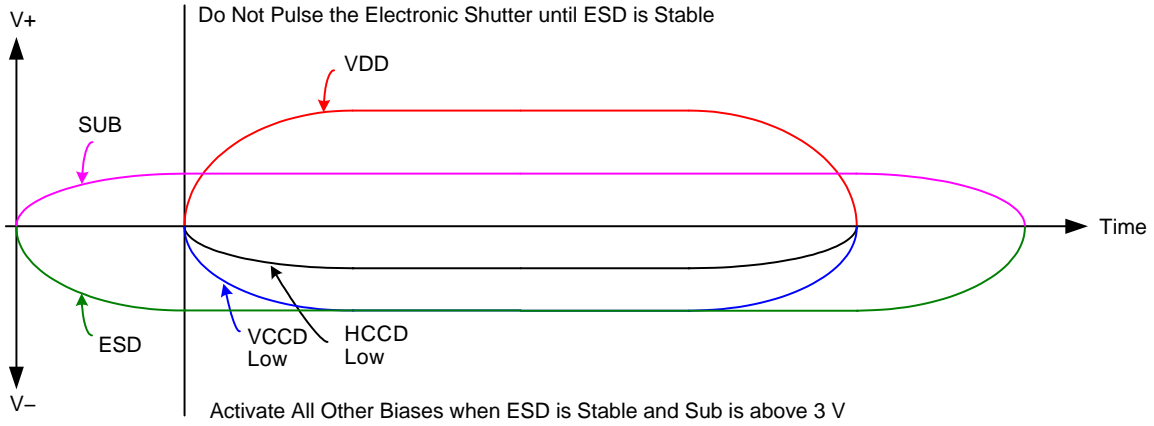


Figure 23. Equivalent Circuit for Reset Gate, Low Gain (R2ab and R2cd)

Power-Up and Power-Down Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.



Notes:

1. Activate all other biases when ESD is stable and SUB is above 3 V.
2. Do not pulse the electronic shutter until ESD is stable.
3. VDD cannot be +15 V when SUB is 0 V.
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

Figure 24. Power-Up and Power-Down Sequence

The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.

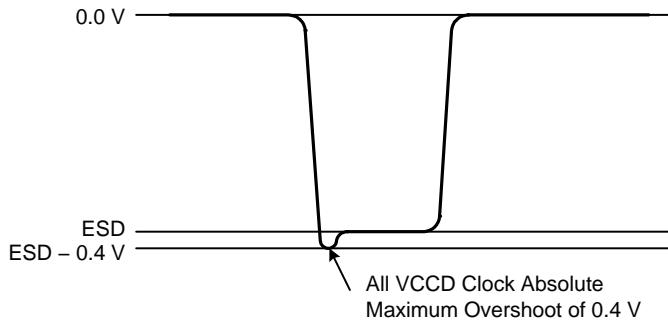


Figure 25. VCCD Clock Waveform

Example of external diode protection for SUB, VDD and ESD. α denotes a, b, c or d.

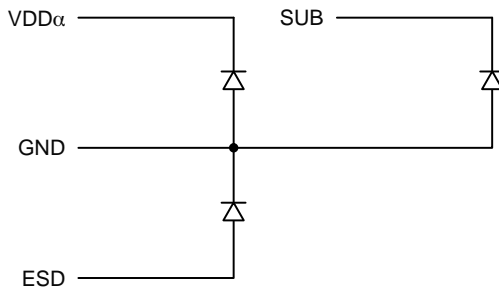


Figure 26. Example of External Diode Protection

DC Bias Operating Conditions

Table 13. DC BIAS OPERATING CONDITIONS

| Description | Pins | Symbol | Min. | Nom. | Max. | Unit | Max. DC Current | Notes |
|-------------------------|--------------|------------------|------|-----------------|------------------|------|-----------------|----------|
| Reset Drain | RD α | RD | 12.4 | 12.6 | 12.8 | V | 10 μ A | 1, 9 |
| Output Gate | OG α | OG | -2.2 | -2.0 | -1.8 | V | 10 μ A | 1 |
| Output Amplifier Supply | VDD α | V _{DD} | 14.5 | 15.0 | 15.5 | V | 11.0 mA | 1, 2 |
| Ground | GND | GND | 0.0 | 0.0 | 0.0 | V | -1.0 mA | |
| Substrate | SUB | V _{SUB} | 5.0 | V _{AB} | V _{DD} | V | 50 μ A | 3, 8 |
| ESD Protection Disable | ESD | ESD | -9.2 | -9.0 | V _{X_L} | V | 50 μ A | 6, 7, 10 |
| Output Bias Current | VOU α | I _{OUT} | -3.0 | -5.0 | -10.0 | mA | - | 1, 4, 5 |

1. α denotes a, b, c or d.
2. The maximum DC current is for one output. $I_{DD} = I_{OUT} + I_{SS}$. See Figure 27.
3. The operating value of the substrate voltage, V_{AB} , will be marked on the shipping container for each device. The value of V_{AB} is set such that the photodiode charge capacity is the nominal P_{Ne} (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40 MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power Up and Power Down Sequence section.
7. ESD maximum value must be less than or equal to $V1_L + 0.4$ V and $V2_L + 0.4$ V.
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.
9. 12.0 V may be used if the total output signal desired is 20,000 e⁻ or less.
10. Where V_{x_L} is the level set for V1_L, V2_L, V3_L, or V4_L in the application.



Figure 27. Output Amplifier

AC Operating Conditions

Table 14. CLOCK LEVELS

| Description | Pins (Note 1) | Symbol | Level | Min. | Nom. | Max. | Unit |
|--|------------------|--------|--------------------|------|------|------|------|
| Vertical CCD Clock, Phase 1 | V1B, V1T | V1_L | Low | -8.2 | -8.0 | -7.8 | V |
| | | V1_M | Mid | -0.2 | 0.0 | 0.2 | |
| | | V1_H | High | 11.5 | 12.0 | 12.5 | |
| Vertical CCD Clock, Phase 2 | V2B, V2T | V2_L | Low | -8.2 | -8.0 | -7.8 | V |
| | | V2_H | High | -0.2 | 0.0 | 0.2 | |
| Vertical CCD Clock, Phase 3 | V3B, V3T | V3_L | Low | -8.2 | -8.0 | -7.8 | V |
| | | V3_H | High | -0.2 | 0.0 | 0.2 | |
| Vertical CCD Clock, Phase 4 | V4B, V4T | V4_L | Low | -8.2 | -8.0 | -7.8 | V |
| | | V4_H | High | -0.2 | 0.0 | 0.2 | |
| Horizontal CCD Clock, Phase 1 Storage | H1S α | H1S_L | Low | -5.2 | -4.0 | -3.8 | V |
| | | H1S_A | Amplitude (Note 3) | 3.8 | 4.0 | 5.2 | |
| Horizontal CCD Clock, Phase 1 Barrier | H1B α | H1B_L | Low | -5.2 | -4.0 | -3.8 | V |
| | | H1B_A | Amplitude (Note 3) | 3.8 | 4.0 | 5.2 | |
| Horizontal CCD Clock, Phase 2 Storage | H2S α | H2S_L | Low | -5.2 | -4.0 | -3.8 | V |
| | | H2S_A | Amplitude (Note 3) | 3.8 | 4.0 | 5.2 | |
| Horizontal CCD Clock, Phase 2 Barrier | H2B α | H2B_L | Low | -5.2 | -4.0 | -3.8 | V |
| | | H2B_A | Amplitude (Note 3) | 3.8 | 4.0 | 5.2 | |
| Horizontal CCD Clock, Last Phase (Note 2) | H2SL α | H2SL_L | Low | -5.2 | -5.0 | -4.8 | V |
| | | H2SL_A | Amplitude (Note 3) | 4.8 | 5.0 | 5.2 | |
| Reset Gate | R α | R_L | Low | -3.2 | -3.0 | -2.8 | V |
| | | R_A | Amplitude | 6.0 | - | 6.4 | |
| Reset Gate 2 | R2 α | R2_L | Low | -2.0 | -1.8 | -1.6 | V |
| | | R2_A | Amplitude | 6.0 | - | 6.4 | |
| Electronic Shutter (Note 4) | SUB | VES | High | 29.0 | 30.0 | 40.0 | V |
| Fast Line Dump Gate | FDG α | FDG_L | Low | -8.2 | -8.0 | -7.8 | V |
| | | FDG_H | High | 4.5 | 5.0 | 5.5 | |

- α denotes a, b, c or d.
- Use separate clock driver for improved speed performance.
- The horizontal clock amplitude should be set such that the high level reaches 0.0 V. Examples:
 - If the minimum horizontal low voltage of -5.2 V is used, then a 5.2 V amplitude clock is required for a clock swing of -5.2 V to 0.0 V.
 - If the maximum horizontal low voltage of -3.8 V is used, then a 3.8 V amplitude clock is required for a clock swing of -3.8 V to 0.0 V.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

The figure below shows the DC bias (V_{SUB}) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

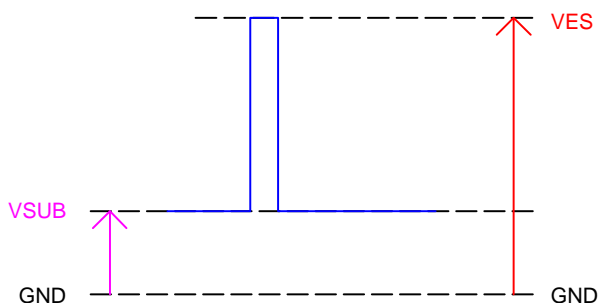


Figure 28. DC Bias and AC Clock Applied to the SUB Pin

Capacitance

Table 15. CAPACITANCE

| | V1B | V2B | V3B | V4B | V1T | V2T | V3T | V4T | GND | All Pins | Unit |
|------|-----|-----|------|------|-----|-----|-----|------|------|----------|------|
| V1B | X | 9.5 | 6.1 | 7.8 | 3.3 | 2.8 | 3.3 | 2.2 | 13.4 | 49.1 | nF |
| V2B | X | X | 11.7 | 5.6 | 2.8 | 1.7 | 2.2 | 1.7 | 3.9 | 41.3 | nF |
| V3B | X | X | X | 10.6 | 3.3 | 2.8 | 3.3 | 2.2 | 4.5 | 46.3 | nF |
| V4B | X | X | X | X | 2.8 | 2.2 | 2.8 | 1.7 | 12.8 | 42.4 | nF |
| V1T | X | X | X | X | X | 7.8 | 6.1 | 9.5 | 13.4 | 48.0 | nF |
| V2T | X | X | X | X | X | X | 8.9 | 3.3 | 12.3 | 41.8 | nF |
| V3T | X | X | X | X | X | X | X | 10.6 | 6.1 | 46.9 | nF |
| V4T | X | X | X | X | X | X | X | X | 2.8 | 40.7 | nF |
| VSUB | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 6.1 | 6.1 | nF |

| | H2S | H1B | H2B | GND | All Pins | Unit |
|-----|-----|-----|-----|-----|----------|------|
| H1S | 34 | 56 | 33 | 146 | 269 | pF |
| H2S | X | 35 | 31 | 210 | 275 | pF |
| H1B | X | X | 9 | 234 | 242 | pF |
| H2B | X | X | X | 219 | 219 | pF |

1. Tables show typical cross capacitance between pins of the device.
2. Capacitance is total for all like pins.
3. Capacitance values are estimated.

Device Identification

The device identification pin (DevID) may be used to determine which 7.4 micron pixel interline CCD sensor is being used.

Table 16. DEVICE IDENTIFICATION

| Description | Pins | Symbol | Min. | Nom. | Max. | Unit | Max. DC Current | Notes |
|-----------------------|-------|--------|---------|---------|---------|----------|-----------------|---------|
| Device Identification | DevID | DevID | 129,000 | 144,000 | 159,000 | Ω | 50 μ A | 1, 2, 3 |

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

Recommended Circuit

Note that V1 must be a different value than V2.

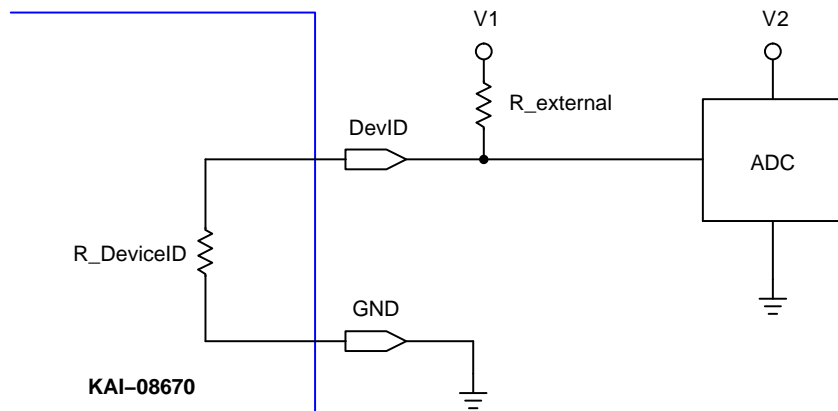


Figure 29. Device Identification Recommended Circuit

TIMING

Requirements and Characteristics

Table 17. REQUIREMENTS AND CHARACTERISTICS

| Description | Symbol | Min. | Nom. | Max. | Unit | Notes |
|---|------------------|-------|------|------|---------------|---------------------|
| Photodiode Transfer | t_{PD} | 2.0 | – | – | μs | |
| VCCD Leading Pedestal | t_{3P} | 4.0 | – | – | μs | |
| VCCD Trailing Pedestal | t_{3D} | 4.0 | – | – | μs | |
| VCCD Transfer Delay | t_D | 1.0 | – | – | μs | |
| VCCD Transfer | t_V | 3.0 | – | – | μs | |
| VCCD Clock Cross-Over | V_{VCR} | 75 | – | 100 | % | 1 |
| VCCD Rise, Fall Times | t_{VR}, t_{VF} | 5 | – | 10 | % | 1, 2 |
| HCCD Delay | t_{HS} | 2.0 | – | – | μs | |
| HCCD Transfer | t_e | 25.0 | – | – | ns | |
| Shutter Transfer | t_{SUB} | 2.0 | – | – | μs | |
| Shutter Delay | t_{HD} | 2.0 | – | – | μs | |
| Reset Pulse | t_R | 2.5 | – | – | ns | |
| Reset – Video Delay | t_{RV} | – | 2.2 | – | ns | |
| H2SL – Video Delay | t_{HV} | – | 3.1 | – | ns | |
| Line Time | t_{LINE} | 58.2 | – | – | μs | Dual HCCD Readout |
| | | 104.1 | – | – | μs | Single HCCD Readout |
| Frame Time | t_{FRAME} | 72.0 | – | – | ms | Quad HCCD Readout |
| | | 143.9 | – | – | ms | Dual HCCD Readout |
| | | 257.4 | – | – | ms | Single HCCD Readout |
| Line Time (XLDR Bin 2x2) | t_{LINE} | 93.3 | – | – | μs | Dual HCCD Readout |
| | | 162.2 | – | – | μs | Single HCCD Readout |
| Frame Time (XLDR Bin 2x2) Constant HCCD Timing | t_{FRAME} | 72.0 | – | – | ms | Quad HCCD Readout |
| | | 143.9 | – | – | ms | Dual HCCD Readout |
| | | 257.4 | – | – | ms | Single HCCD Readout |
| Frame Time (XLDR Bin 2x2) Variable HCCD Timing | t_{FRAME} | 57.7 | – | – | ms | Quad HCCD Readout |
| | | 115.4 | – | – | ms | Dual HCCD Readout |
| | | 200.5 | – | – | ms | Single HCCD Readout |

1. Refer to Figure 48: VCCD Clock Rise Time, Fall Time, and Edge Alignment.
2. Relative to the VCCD Transfer pulse width, t_V .

Timing Flow Charts

In the timing flow charts the number of HCCD clock cycles per row, NH, and the number of VCCD clock cycles per frame, NV, are shown in the following table.

Table 18. VALUES FOR NH AND NV WHEN OPERATING THE SENSOR IN THE VARIOUS MODES OF RESOLUTION

| | Full Resolution | | 1/4 Resolution | | XLDR | |
|-------------------|-----------------|------|----------------|------|------|------|
| | NV | NH | NV | NH | NV | NH |
| Quad | 1236 | 1848 | 618 | 924 | 618 | 924 |
| Dual VOUTa, VOUTc | 1236 | 3696 | 618 | 1848 | 618 | 1848 |
| Dual VOUTa, VOUTb | 2472 | 1848 | 1236 | 924 | 1236 | 924 |
| Single VOUTa | 2472 | 3696 | 1236 | 1848 | 1236 | 1848 |

1. The time to read out one line $t_{LINE} = \text{Line Timing} + NH / (\text{Pixel Frequency})$.
2. The time to read out one frame $t_{FRAME} = NV \cdot t_{LINE} + \text{Frame Timing}$.
3. Line Timing: See Table 20: Line Timing.
4. Frame Timing: See Table 19: Frame Timing.
5. XLDR: eXtended Linear Dynamic Range.

No Electronic Shutter

In this case the photodiode exposure time is equal to the time to read out an image. This flow chart applies to both full and 1/4 resolution modes.

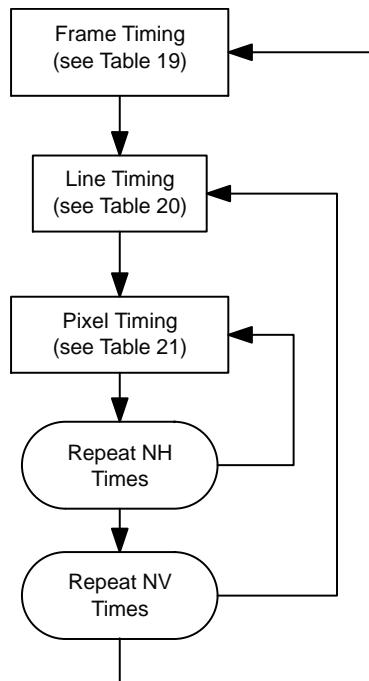
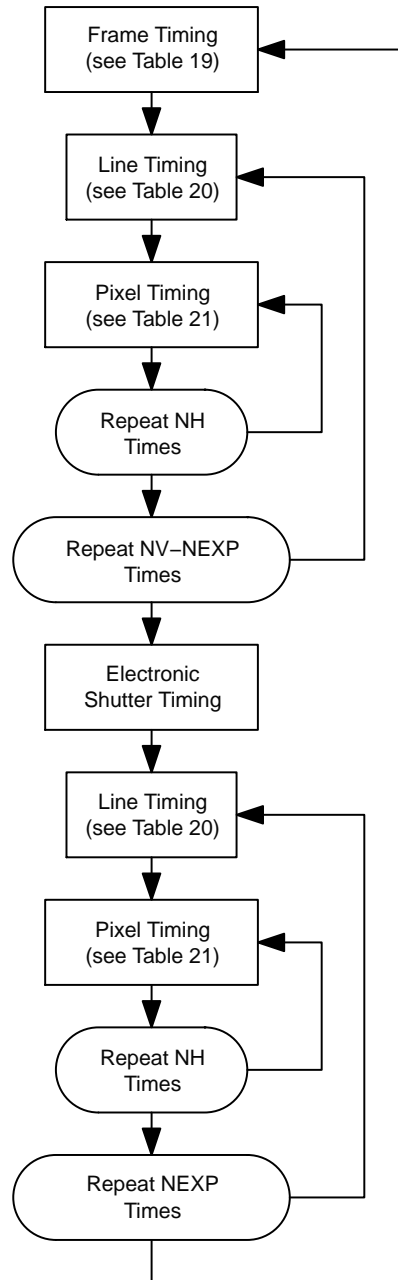


Figure 30. Timing Flow when Electronic Shutter is Not Used

Using the Electronic Shutter

This flow chart applies to both the full and 1/4 resolution modes. The exposure time begins on the falling edge of the electronic shutter pulse on the SUB pin. The exposure time

ends on the falling edge of the photodiode transfer (t_{PD}) of the V1T and V1B pins. The electronic shutter timing is shown in Figure 39.



NOTE: NEXP: Exposure time in increments of number of lines.

Figure 31. Timing Flow Chart using the Electronic Shutter for Exposure Control

Timing Tables

Frame Timing

This timing table is for transferring charge from the photodiodes to the VCCD. See Figure 32 and Figure 33 for frame timing diagrams.

Table 19. FRAME TIMING

| Device Pin | Full Resolution, High Gain or Low Gain | | | | 1/4 Resolution, High Gain or Low Gain | | | | 1/4 Resolution XLDR | | | |
|--------------|--|---------------------|---------------------|--------------|---------------------------------------|---------------------|---------------------|--------------|---------------------|---------------------|---------------------|--------------|
| | Quad | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa |
| V1T | F1T | | F1B | | F1T | | F1B | | F1T | | F1B | |
| V2T | F2T | | F4B | | F2T | | F4B | | F2T | | F4B | |
| V3T | F3T | | F3B | | F3T | | F3B | | F3T | | F3B | |
| V4T | F4T | | F2B | | F4T | | F2B | | F4T | | F2B | |
| V1B | F1B | | | | F1B | | | | F1B | | | |
| V2B | F2B | | | | F2B | | | | F2B | | | |
| V3B | F3B | | | | F3B | | | | F3B | | | |
| V4B | F4B | | | | F4B | | | | F4B | | | |
| H1Sa | P1 | | | | P1Q | | | | P1XL | | | |
| H1Ba | P1 | | | | P1Q | | | | P1XL | | | |
| H2Sa | P2 | | | | P2Q | | | | P2XL | | | |
| H2Ba | P2 | | | | P2Q | | | | P2XL | | | |
| Ra | RHG/RLG | | | | RHGQ/RLGQ | | | | RXL | | | |
| H1Sb | P1 | | | | P1Q | | | | P1XL | | | |
| H1Bb | P1 | P2 | P1 | P2 | P1Q | P2Q | P1Q | P2Q | P1XL | P2XL | P1XL | P2XL |
| H2Sb | P2 | | | | P2Q | | | | P2XL | | | |
| H2Bb | P2 | P1 | P2 | P1 | P2Q | P1Q | P2Q | P1Q | P2XL | P1XL | P2XL | P1XL |
| Rb | RHG/RLG | (Note 1) | RHG/RLG | (Note 1) | RHGQ/RLGQ | (Note 1) | RHGQ/RLGQ | (Note 1) | RXL | (Note 1) | RXL | (Note 1) |
| R2ab | R2HG/R2LG | | | | R2HGQ/R2LGQ | | | | R2XL | | | |
| FDGab | -8 V | | | | -8 V | | | | -8 V | | | |
| H1Sc | P1 | | (Note 1) | | P1Q | | (Note 1) | | P1XL | | (Note 1) | |
| H1Bc | P1 | | (Note 1) | | P1Q | | (Note 1) | | P1XL | | (Note 1) | |
| H2Sc | P2 | | (Note 1) | | P2Q | | (Note 1) | | P2XL | | (Note 1) | |
| H2Bc | P2 | | (Note 1) | | P2Q | | (Note 1) | | P2XL | | (Note 1) | |
| Rc | RHG/RLG | | (Note 1) | | RHGQ/RLGQ | | (Note 1) | | RXL | | (Note 1) | |
| H1Sd | P1 | | (Note 1) | | P1Q | | (Note 1) | | P1XL | | (Note 1) | |
| H1Bd | P1 | P2 | (Note 1) | | P1Q | P2Q | (Note 1) | | P1XL | P2XL | (Note 1) | |
| H2Sd | P2 | | (Note 1) | | P2Q | | (Note 1) | | P2XL | | (Note 1) | |
| H2Bd | P2 | P1 | (Note 1) | | P2Q | P1Q | (Note 1) | | P2XL | P1XL | (Note 1) | |
| Rd | RHG/RLG | (Note 1) | (Note 1) | | RHGQ/RLGQ | (Note 1) | (Note 1) | | RXL | (Note 1) | (Note 1) | |
| R2cd | R2HG/R2LG | | (Note 1) | | R2HGQ/R2LGQ | | (Note 1) | | R2XL | | (Note 1) | |
| FDGcd | -8 V | | | | -8 V | | | | -8 V | | | |
| SHP (Note 2) | SHP1 | | | | SHPQ | | | | (Note 4) | | | |
| SHD (Note 2) | SHD1 | | | | SHDQ | | | | (Note 5) | | | |

1. This clock should be held at its high level voltage (0 V) or held at +5.0 V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products.
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor.
3. This note intentionally left empty.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal.
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal.

Line Timing

This timing is for transferring one line of charge from the VCCD to the HCCD. See Figure 34, Figure 35, Figure 37 and Figure 38 for line timing diagrams.

Table 20. LINE TIMING

| Device Pin | Full Resolution, High Gain or Low Gain | | | | 1/4 Resolution, High Gain or Low Gain | | | | 1/4 Resolution XLDR | | | |
|--------------|--|------------------|------------------|--------------|---------------------------------------|------------------|------------------|--------------|---------------------|------------------|------------------|--------------|
| | Quad | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa |
| V1T | L1T | | L1B | | 2× L1T | | 2× L1B | | 2× L1T | | 2× L1B | |
| V2T | L2T | | L4B | | 2× L2T | | 2× L4B | | 2× L2T | | 2× L4B | |
| V3T | L3T | | L3B | | 2× L3T | | 2× L3B | | 2× L3T | | 2× L3B | |
| V4T | L4T | | L2B | | 2× L4T | | 2× L2B | | 2× L4T | | 2× L2B | |
| V1B | L1B | | | | 2× L1B | | | | 2× L1B | | | |
| V2B | L2B | | | | 2× L2B | | | | 2× L2B | | | |
| V3B | L3B | | | | 2× L3B | | | | 2× L3B | | | |
| V4B | L4B | | | | 2× L4B | | | | 2× L4B | | | |
| H1Sa | P1L | | | | P1LQ | | | | P1XL | | | |
| H1Ba | P1L | | | | P1LQ | | | | P1XL | | | |
| H2Sa | P2L | | | | P2LQ | | | | P2XL | | | |
| H2Ba | P2L | | | | P2LQ | | | | P2XL | | | |
| Ra | RHG/RLG | | | | RHGQ/RLGQ | | | | RXL | | | |
| H1Sb | P1L | | | | P1LQ | | | | P1XL | | | |
| H1Bb | P1L | P2L | P1L | P2L | P1LQ | P2LQ | P1LQ | P2LQ | P1XL | P2XL | P1XL | P2XL |
| H2Sb | P2L | | | | P2LQ | | | | P2XL | | | |
| H2Bb | P2L | P1L | P2L | P1L | P2LQ | P1LQ | P2LQ | P1LQ | P2XL | P1XL | P2XL | P1XL |
| Rb | RHG/RLG | (Note 1) | RHG/RLG | (Note 1) | RHGQ/RLGQ | (Note 1) | RHGQ/RLGQ | (Note 1) | RXL | (Note 1) | RXL | (Note 1) |
| R2ab | R2HG/R2LG | | | | R2HGQ/R2LGQ | | | | R2XL | | | |
| FDGab | -8 V | | | | -8 V | | | | -8 V | | | |
| H1Sc | P1L | | (Note 1) | | P1LQ | | (Note 1) | | P1XL | | (Note 1) | |
| H1Bc | P1L | | (Note 1) | | P1LQ | | (Note 1) | | P1XL | | (Note 1) | |
| H2Sc | P2L | | (Note 1) | | P2LQ | | (Note 1) | | P2XL | | (Note 1) | |
| H2Bc | P2L | | (Note 1) | | P2LQ | | (Note 1) | | P2XL | | (Note 1) | |
| Rc | RHG/RLG | | (Note 1) | | RHGQ/RLGQ | | (Note 1) | | RXL | | (Note 1) | |
| H1Sd | P1L | | (Note 1) | | P1LQ | | (Note 1) | | P1XL | | (Note 1) | |
| H1Bd | P1L | P2L | (Note 1) | | P1LQ | P2LQ | (Note 1) | | P1XL | P2XL | (Note 1) | |
| H2Sd | P2L | | (Note 1) | | P2LQ | | (Note 1) | | P2XL | | (Note 1) | |
| H2Bd | P2L | P1L | (Note 1) | | P2LQ | P1LQ | (Note 1) | | P2XL | P1XL | (Note 1) | |
| Rd | RHG/RLG | (Note 1) | (Note 1) | | RHGQ/RLGQ | (Note 1) | (Note 1) | | RXL | (Note 1) | (Note 1) | |
| R2cd | R2HG/R2LG | | (Note 1) | | R2HGQ/R2LGQ | | (Note 1) | | R2XL | | (Note 1) | |
| FDGcd | -8 V | | | | -8 V | | | | -8 V | | | |
| SHP (Note 2) | SHP1 | | | | SHPQ | | | | (Note 4) | | | |
| SHD (Note 2) | SHD1 | | | | SHDQ | | | | (Note 5) | | | |

1. This clock should be held at its high level voltage (0 V) or held at +5.0 V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products.
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor.
3. The notation 2× L1B means repeat the L1B timing twice for every line. This sums two rows into the HCCD.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal.
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal.

Pixel Timing

This timing is for transferring one pixel from the HCCD to the output amplifier.

Table 21. PIXEL TIMING

| Device Pin | Full Resolution, High Gain or Low Gain | | | | 1/4 Resolution, High Gain or Low Gain | | | | 1/4 Resolution XLDR | | | |
|--------------|--|------------------|------------------|--------------|---------------------------------------|------------------|------------------|--------------|---------------------|------------------|------------------|--------------|
| | Quad | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa |
| V1T | -8 V | | | | -8 V | | | | -8 V | | | |
| V2T | -8 V | | | | -8 V | | | | -8 V | | | |
| V3T | 0 V | | | | 0 V | | | | 0 V | | | |
| V4T | 0 V | | | | 0 V | | | | 0 V | | | |
| V1B | -8 V | | | | -8 V | | | | -8 V | | | |
| V2B | 0 V | | | | 0 V | | | | 0 V | | | |
| V3B | 0 V | | | | 0 V | | | | 0 V | | | |
| V4B | -8 V | | | | -8 V | | | | -8 V | | | |
| H1Sa | P1 | | | | P1Q | | | | P1XL | | | |
| H1Ba | P1 | | | | P1Q | | | | P1XL | | | |
| H2Sa | P2 | | | | P2Q | | | | P2XL | | | |
| H2Ba | P2 | | | | P2Q | | | | P2XL | | | |
| Ra | RHG/RLG | | | | RHGQ/RLGQ | | | | RXL | | | |
| H1Sb | P1 | | | | P1Q | | | | P1XL | | | |
| H1Bb | P1 | P2 | P1 | P2 | P1Q | P2Q | P1Q | P2Q | P1XL | P2XL | P1XL | P2XL |
| H2Sb | P2 | | | | P2Q | | | | P2XL | | | |
| H2Bb | P2 | P1 | P2 | P1 | P2Q | P1Q | P2Q | P1Q | P2XL | P1XL | P2XL | P1XL |
| Rb | RHG/RLG | (Note 1) | RHG/RLG | (Note 1) | RHGQ/RLGQ | (Note 1) | RHGQ/RLGQ | (Note 1) | RXL | (Note 1) | RXL | (Note 1) |
| R2ab | R2HG/R2LG | | | | R2HGQ/R2LGQ | | | | R2XL | | | |
| FDGab | -8 V | | | | -8 V | | | | -8 V | | | |
| H1Sc | P1 | | (Note 1) | | P1Q | | (Note 1) | | P1XL | | (Note 1) | |
| H1Bc | P1 | | (Note 1) | | P1Q | | (Note 1) | | P1XL | | (Note 1) | |
| H2Sc | P2 | | (Note 1) | | P2Q | | (Note 1) | | P2XL | | (Note 1) | |
| H2Bc | P2 | | (Note 1) | | P2Q | | (Note 1) | | P2XL | | (Note 1) | |
| Rc | RHG/RLG | | (Note 1) | | RHGQ/RLGQ | | (Note 1) | | RXL | | (Note 1) | |
| H1Sd | P1 | | (Note 1) | | P1Q | | (Note 1) | | P1XL | | (Note 1) | |
| H1Bd | P1 | P2 | (Note 1) | | P1Q | P2Q | (Note 1) | | P1XL | P2XL | (Note 1) | |
| H2Sd | P2 | | (Note 1) | | P2Q | | (Note 1) | | P2XL | | (Note 1) | |
| H2Bd | P2 | P1 | (Note 1) | | P2Q | P1Q | (Note 1) | | P2XL | P1XL | (Note 1) | |
| Rd | RHG/RLG | (Note 1) | (Note 1) | | RHGQ/RLGQ | (Note 1) | (Note 1) | | RXL | (Note 1) | (Note 1) | |
| R2cd | R2HG/R2LG | | (Note 1) | | R2HGQ/R2LGQ | | (Note 1) | | R2XL | | (Note 1) | |
| FDGcd | -8 V | | | | -8 V | | | | -8 V | | | |
| SHP (Note 2) | SHP1 | | | | SHPQ | | | | (Note 4) | | | |
| SHD (Note 2) | SHD1 | | | | SHDQ | | | | (Note 5) | | | |

1. This clock should be held at its high level voltage (0 V) or held at +5.0 V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products.
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor.
3. This note intentionally left empty.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal.
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal.

Timing Diagrams

The charge in the photodiodes is transferred to the VCCD on the rising edge of the +12 V pulse and is completed by the falling edge of the +12 V pulsed on F1T and F1B. During the

time period when F1T and F1B are at +12 V (t_{PD}) anti-blooming protection is disabled. The photodiode integration time ends on the falling edge of the +12 V pulse.

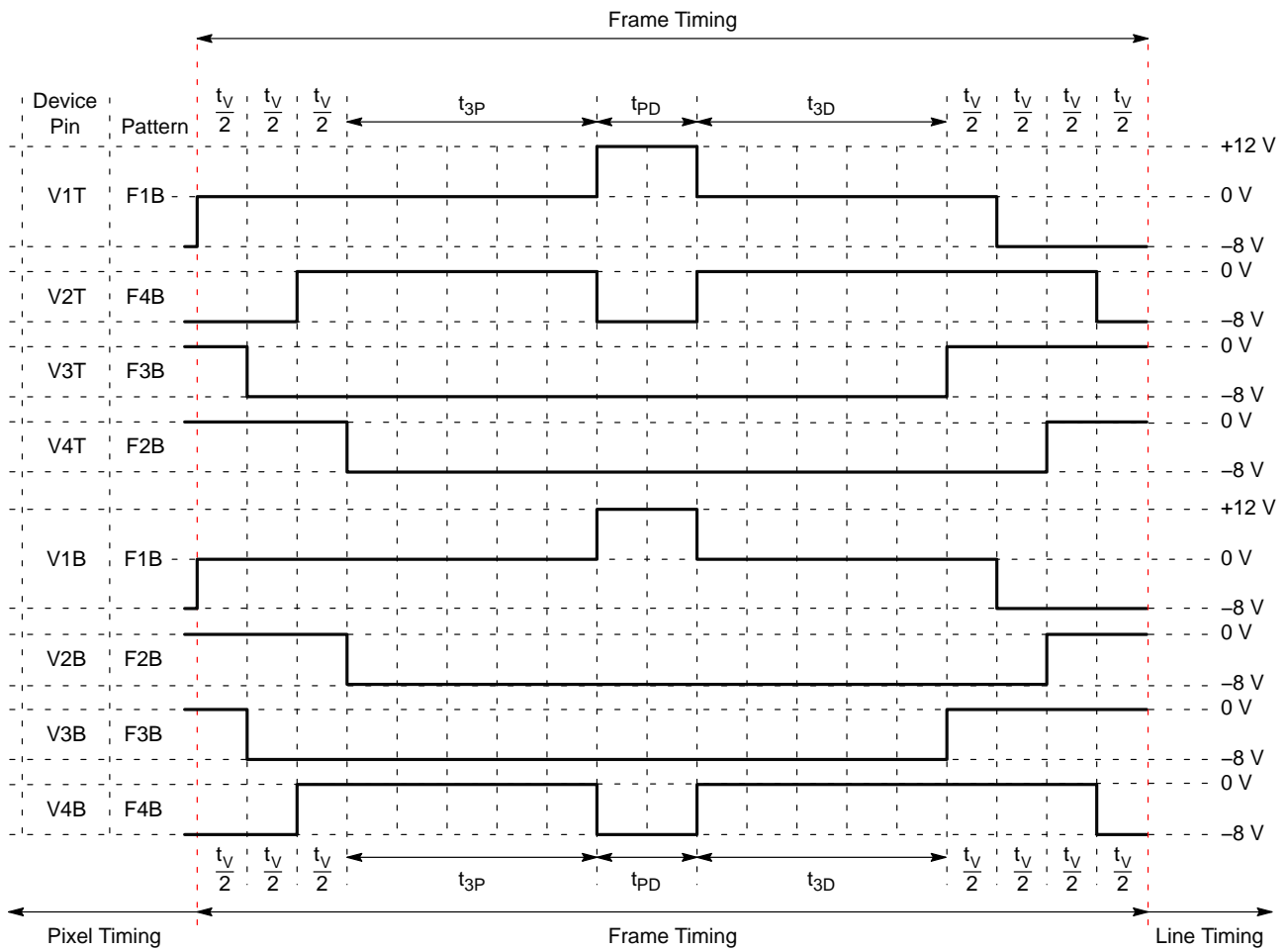
Frame Timing – Quadrant and Dual VOUTa/VOUTc Readout Modes



NOTE: See Table 19 for pin assignments.

Figure 32. Frame Timing Diagram Quadrant and Dual VOUTa/VOUTc Readout Modes

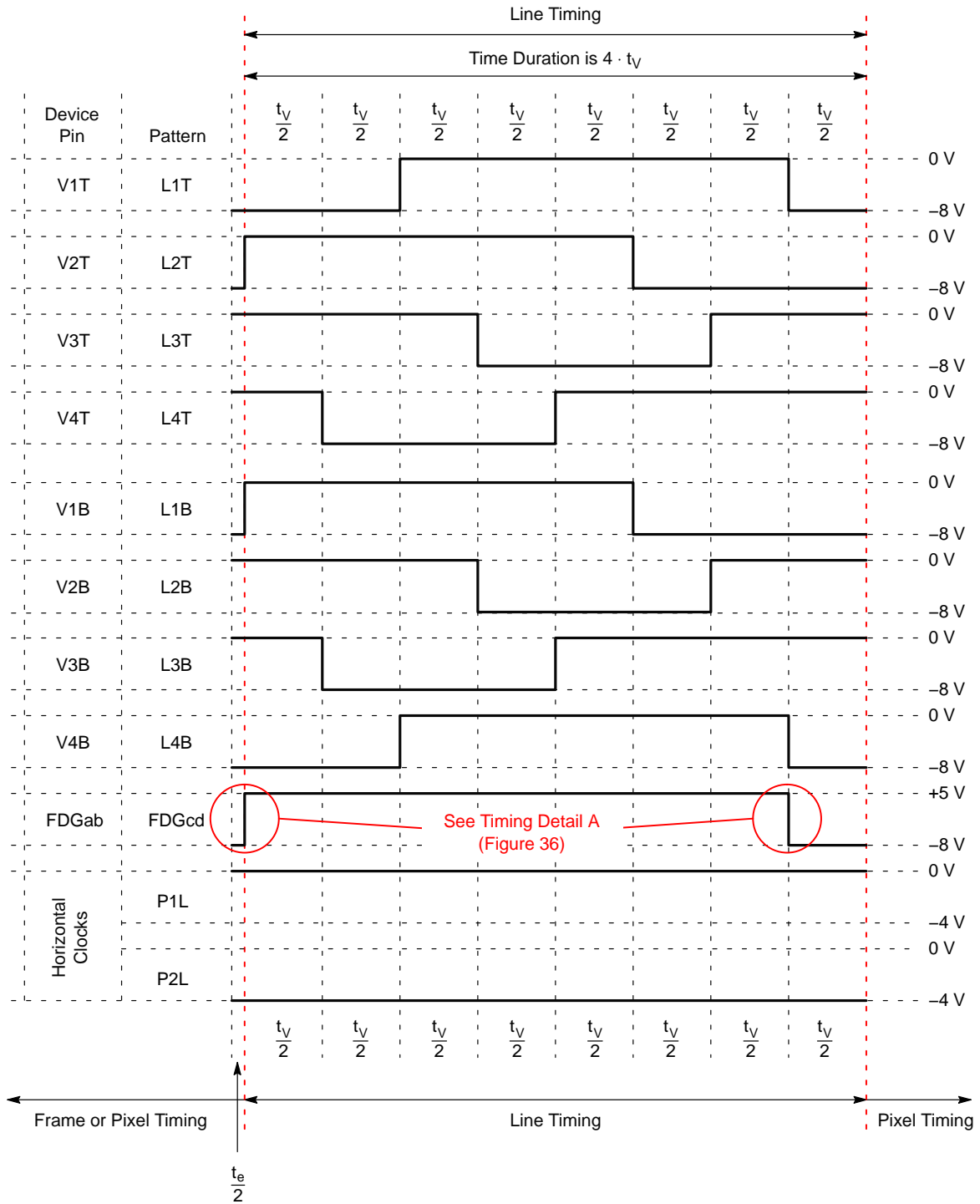
Frame Timing – Single and Dual VOUTa/VOUTb Readout Modes



NOTE: See Table 19 for pin assignments.

Figure 33. Frame Timing Diagram Single and Dual VOUTa/VOUTb Readout Modes

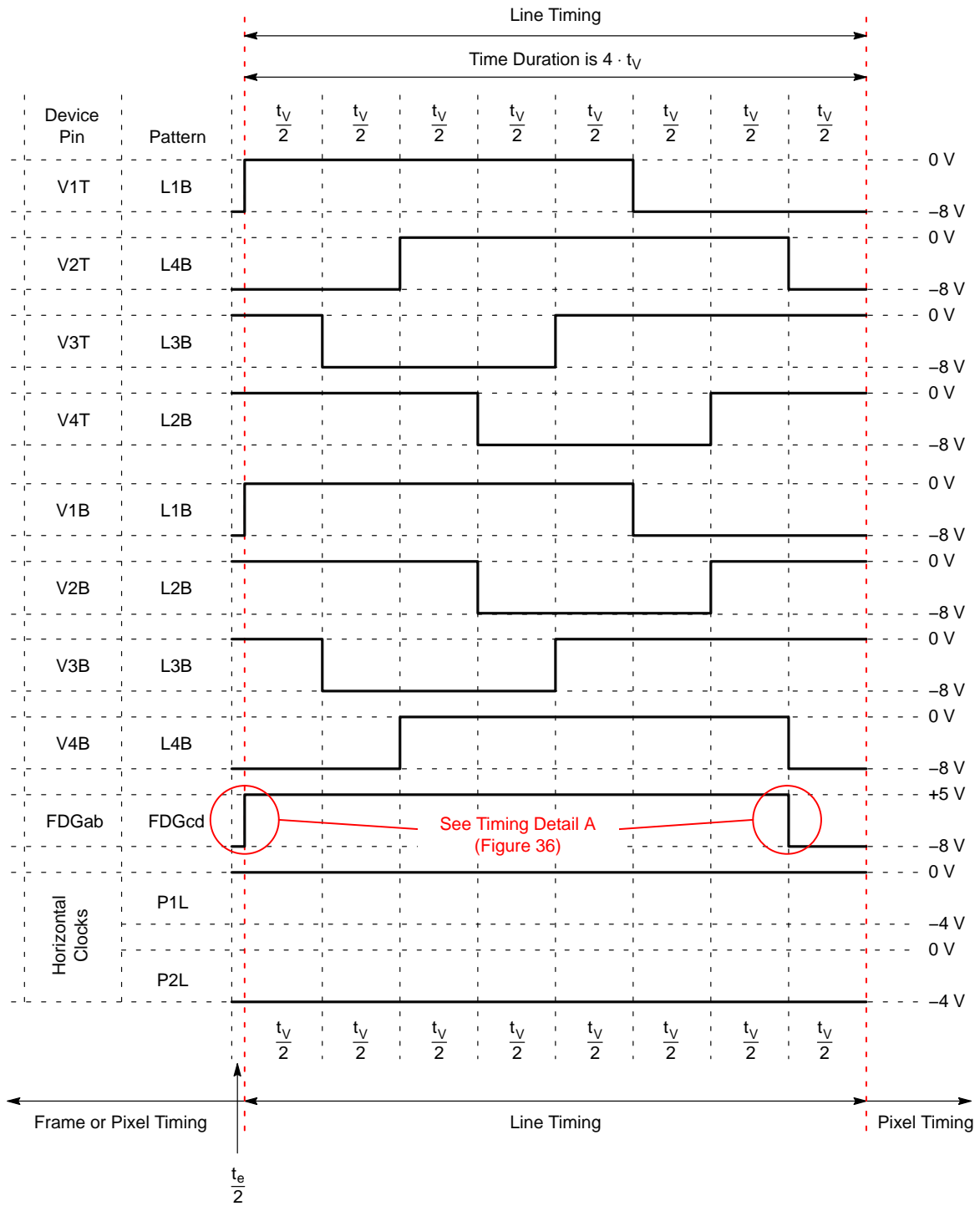
Line Timing – Full Resolution – Quadrant and Dual VOUTa/VOUTc Readout Modes



NOTE: See Table 20 for pin assignments.

Figure 34. Line Timing Diagram – Full Resolution – Quadrant and Dual VOUTa/VOUTc Readout Modes

Line Timing – Full Resolution – Single and Dual VOUTa/VOUTb Readout Modes



NOTE: See Table 20 for pin assignments.

Figure 35. Line Timing Diagram – Full Resolution – Single and Dual VOUTa/VOUTb Readout Modes

If the line is to be dumped then clock the FDGab and FDGcd pins as shown. This dumping process eliminates a line of charge and the HCCD does not have to be clocked.

To transfer a line from the VCCD to the HCCD without dumping the charge, hold the FDGab and FDGcd pins at a constant -8 V.

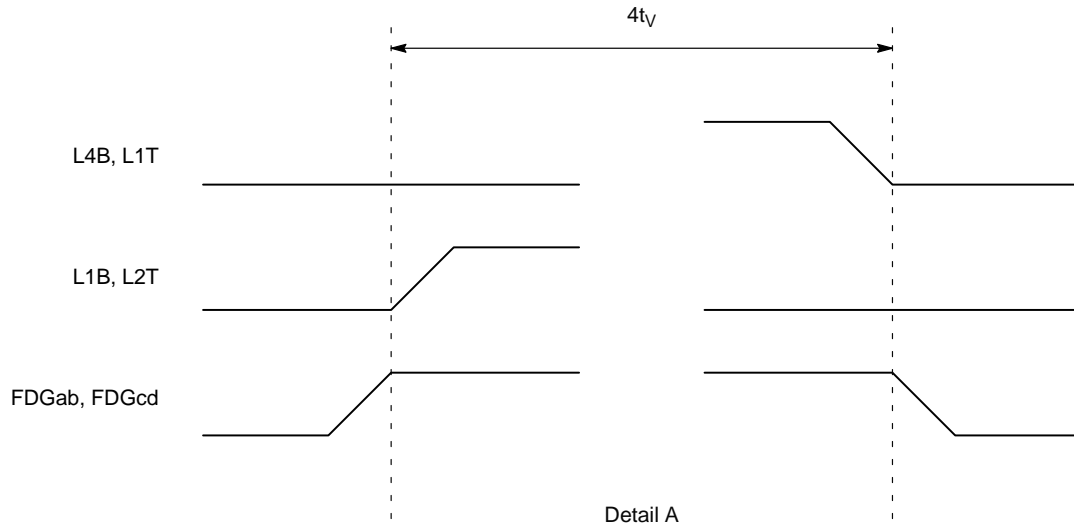
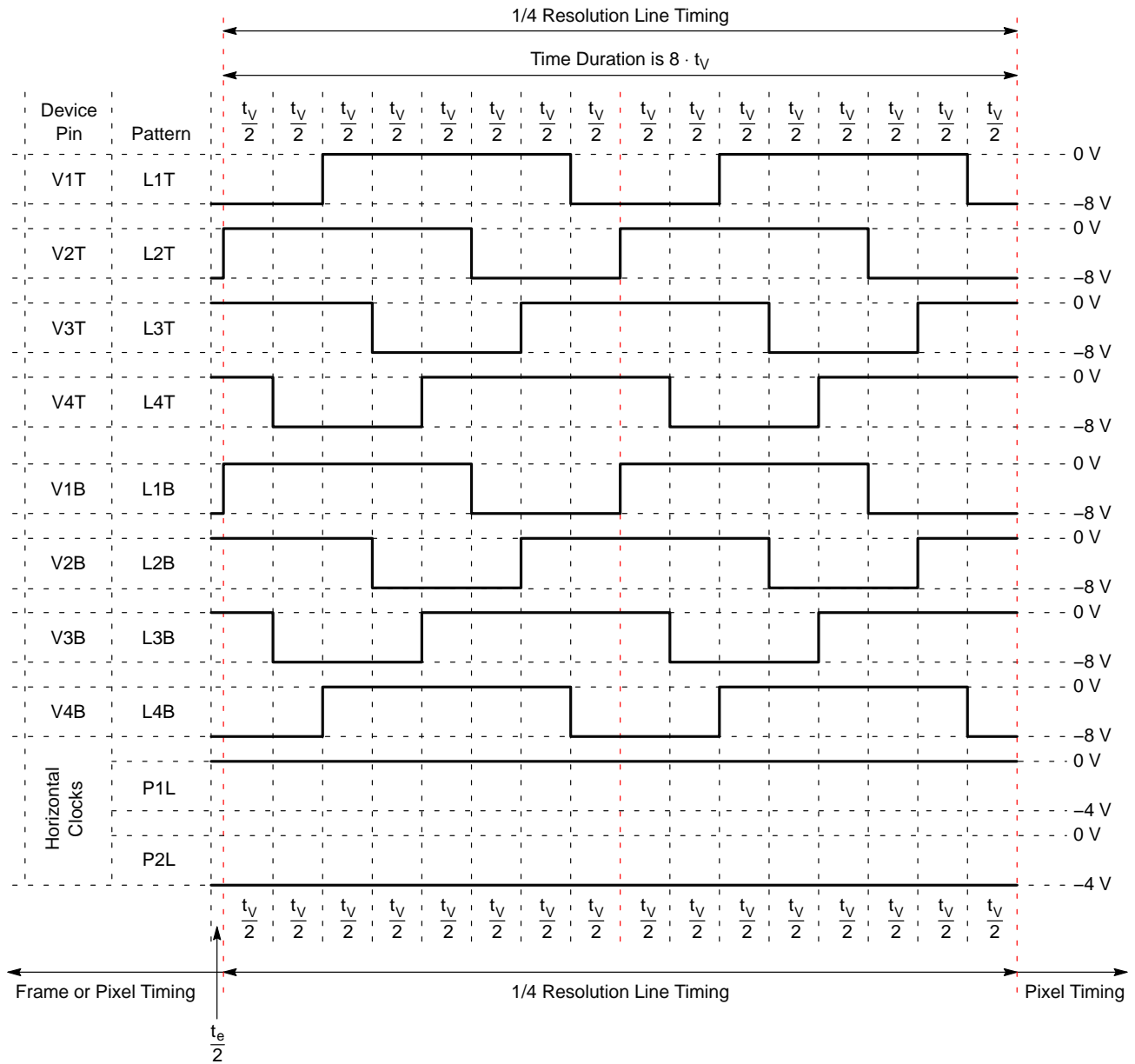


Figure 36. Fast Dump Gate Timing Detail A

When the VCCD is clocked while the FDGab and FDGcd pins are at +5 V, charge is diverted to a drain instead of transferring to the HCCD. The FDG pins must be at +5 V before the first VCCD timing edge begins its transition.

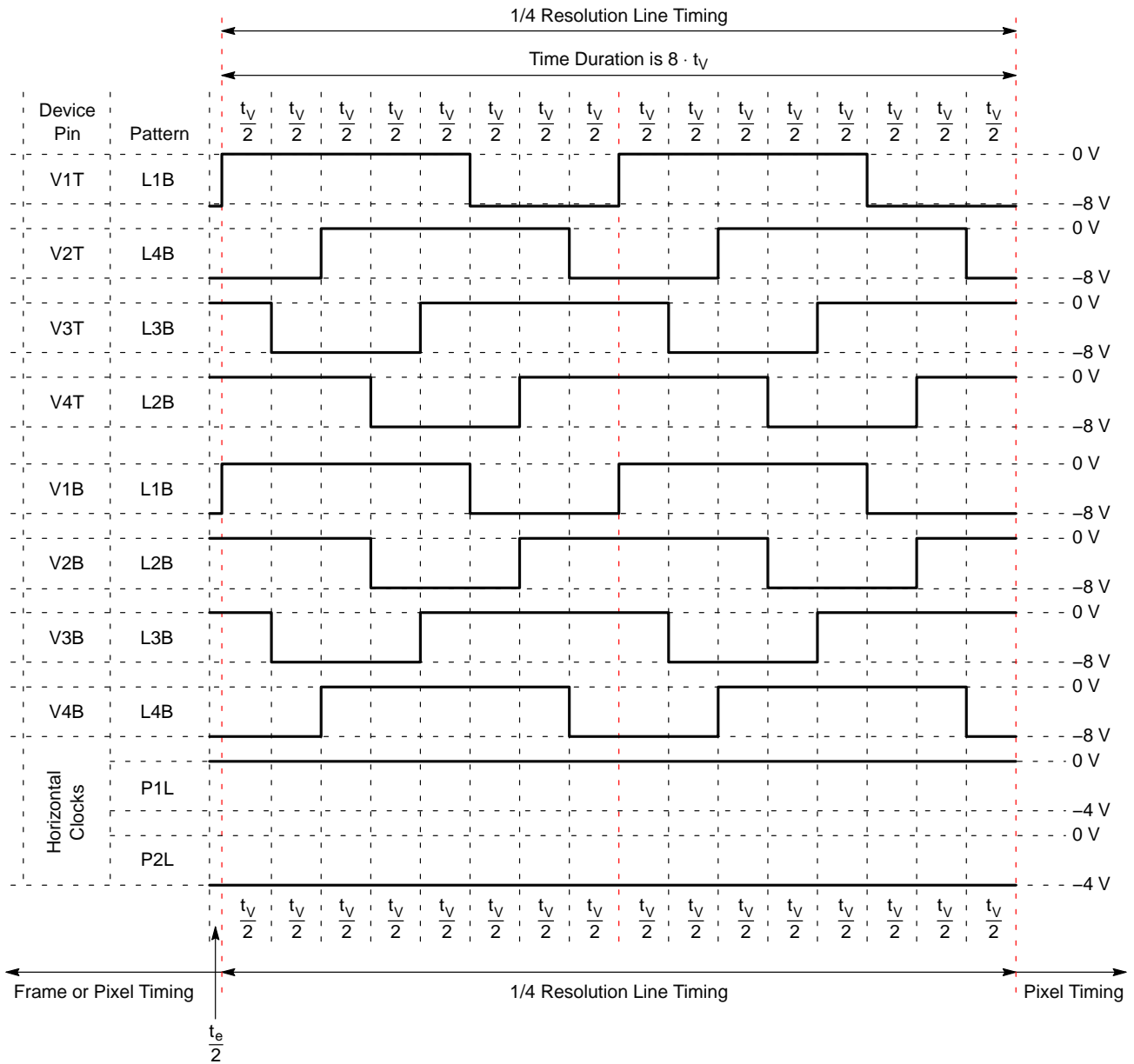
The FDG pin must not begin its transition from +5 V back to -8 V until the last VCCD timing edge has completed its transition.



NOTE: See Table 20 for pin assignments.

Figure 37. Line Timing Diagram – 1/4 Resolution – Quadrant and Dual VOUTa/VOUTc Readout Modes

Line Timing – Low Gain, High Gain and XLDR 1/4 Resolution – Single and Dual VOUTa/VOUTb Readout Modes



NOTE: See Table 20 for pin assignments.

Figure 38. Line Timing Diagram – 1/4 Resolution – Single and Dual VOUTa/VOUTb Readout Modes

Electronic Shutter Timing Diagrams

The electronic shutter pulse can be inserted at the end of any line of the HCCD timing. The HCCD should be empty when the electronic shutter is pulsed. A recommended position for the electronic shutter is just after the last pixel is read out of a line. The VCCD clocks should not resume until at least $t_V/2$ after the electronic shutter pulse has

finished. The HCCD clocks can be run during the electronic shutter pulse as long as the HCCD does not contain valid image data.

For short exposures less than one line time, the electronic shutter pulse can appear inside the frame timing. Any electronic shutter pulse transition should be $t_V/2$ away from any VCCD clock transition.

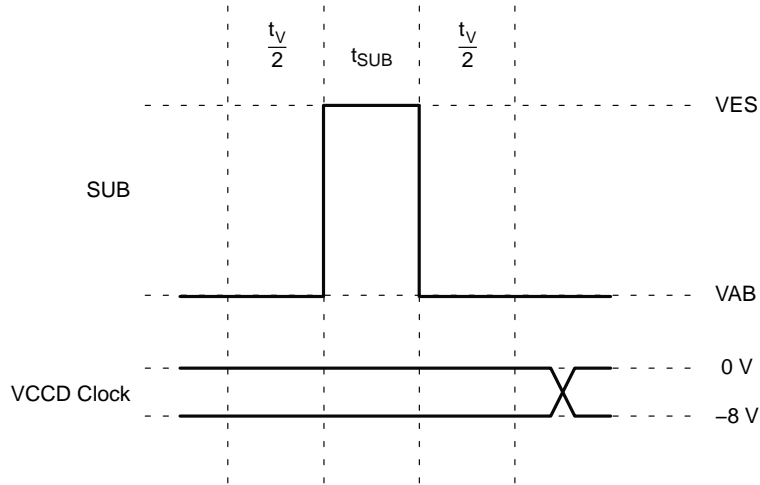


Figure 39. Electronic Shutter Timing

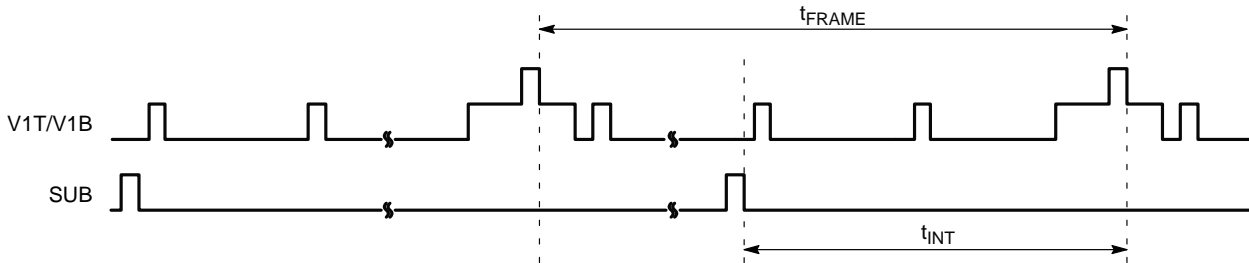


Figure 40. Frame/Electrical Shutter Timing

Pixel Timing – Full Resolution – High Gain Pixel Timing

Use this timing to read out every pixel at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3 V and +5 V. Note the R2ab and R2cd pins are

internally biased to +4.3 V when left floating. The SHP1 and SHD1 pulses indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.

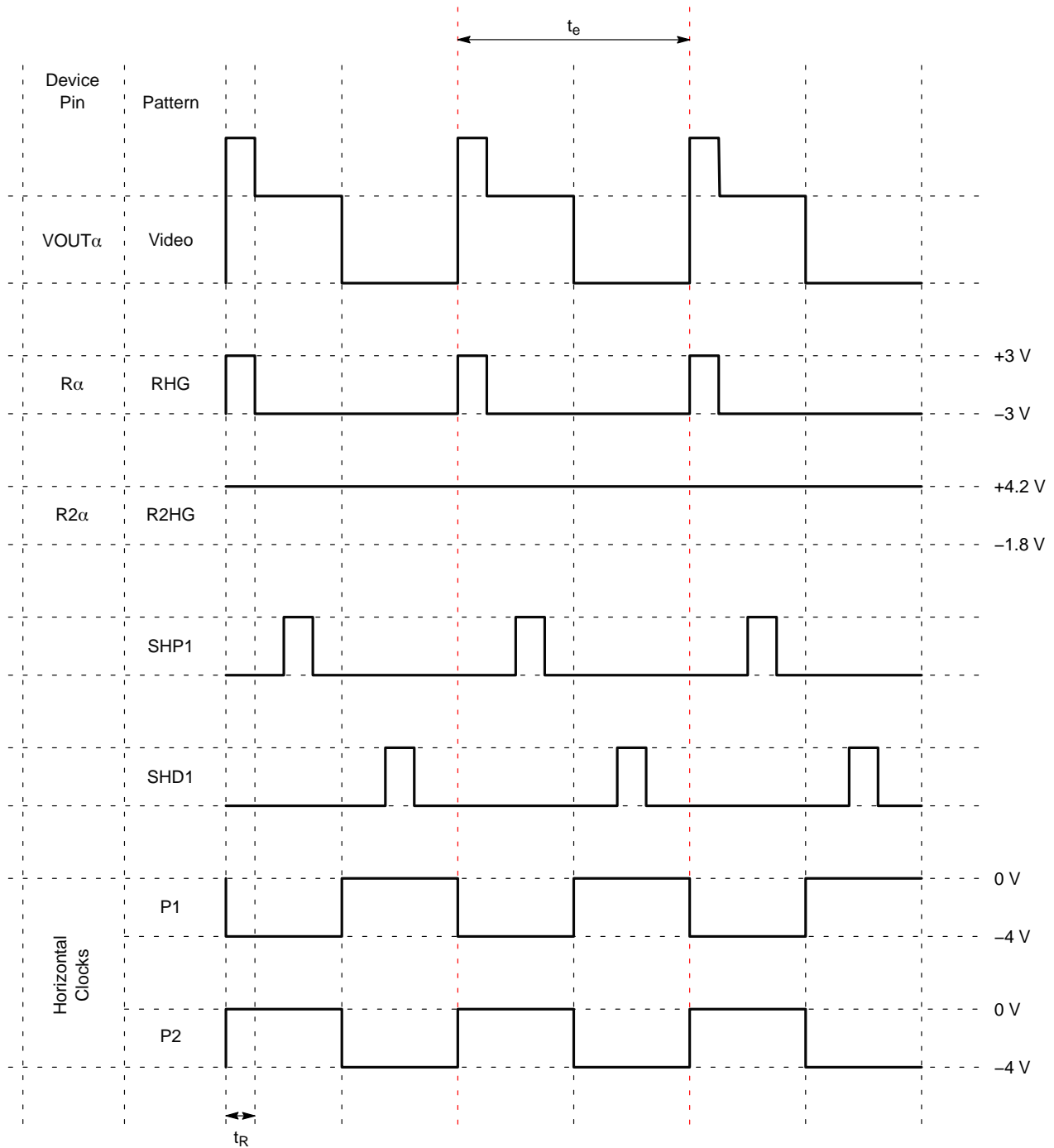


Figure 41. Pixel Timing Diagram – Full Resolution – High Gain

Pixel Timing – Full Resolution – Low Gain Pixel Timing

Use this pixel timing to read out every pixel at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc and Rd pins should be set to any DC voltage between +3 V and +5 V. The SHP1 and SHD1 pulses

indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.

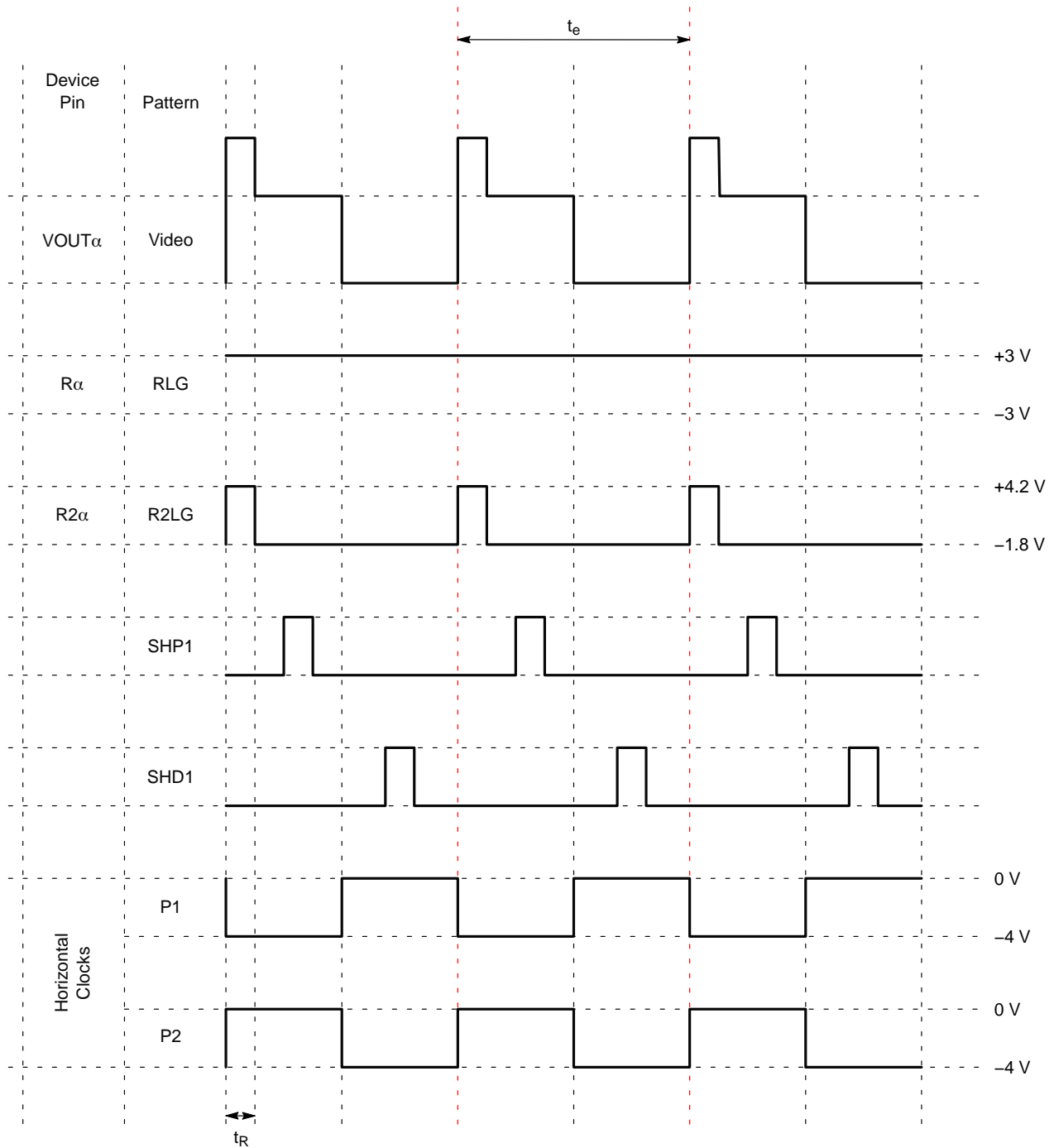


Figure 42. Pixel Timing Diagram – Full Resolution – Low Gain

Pixel Timing – 1/4 Resolution – High Gain Pixel Timing

Use this timing to read out two pixels summed on the output amplifier sense node at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3 V and +5 V. Note the R2ab and R2cd pins are internally biased to +4.3 V when left floating. The SHPQ and SHDQ pulses indicate where the camera electronics should sample

the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The Ra, Rb, Rc, and Rd pins are pulsed at half the frequency of the horizontal CCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the horizontal CCD clocks.



Figure 43. Pixel Timing Diagram – 1/4 Resolution – High Gain

Pixel Timing – 1/4 Resolution – Low Gain Pixel Timing

Use this timing to read out two pixels summed on the output amplifier sense node at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc and Rd pins can be set to any DC voltage between +3 V and +5 V. The SHPQ and SHDQ pulses indicate where the camera electronics should sample the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The R2ab and R2cd pins are pulsed at half the frequency of the horizontal CCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the horizontal CCD clocks.

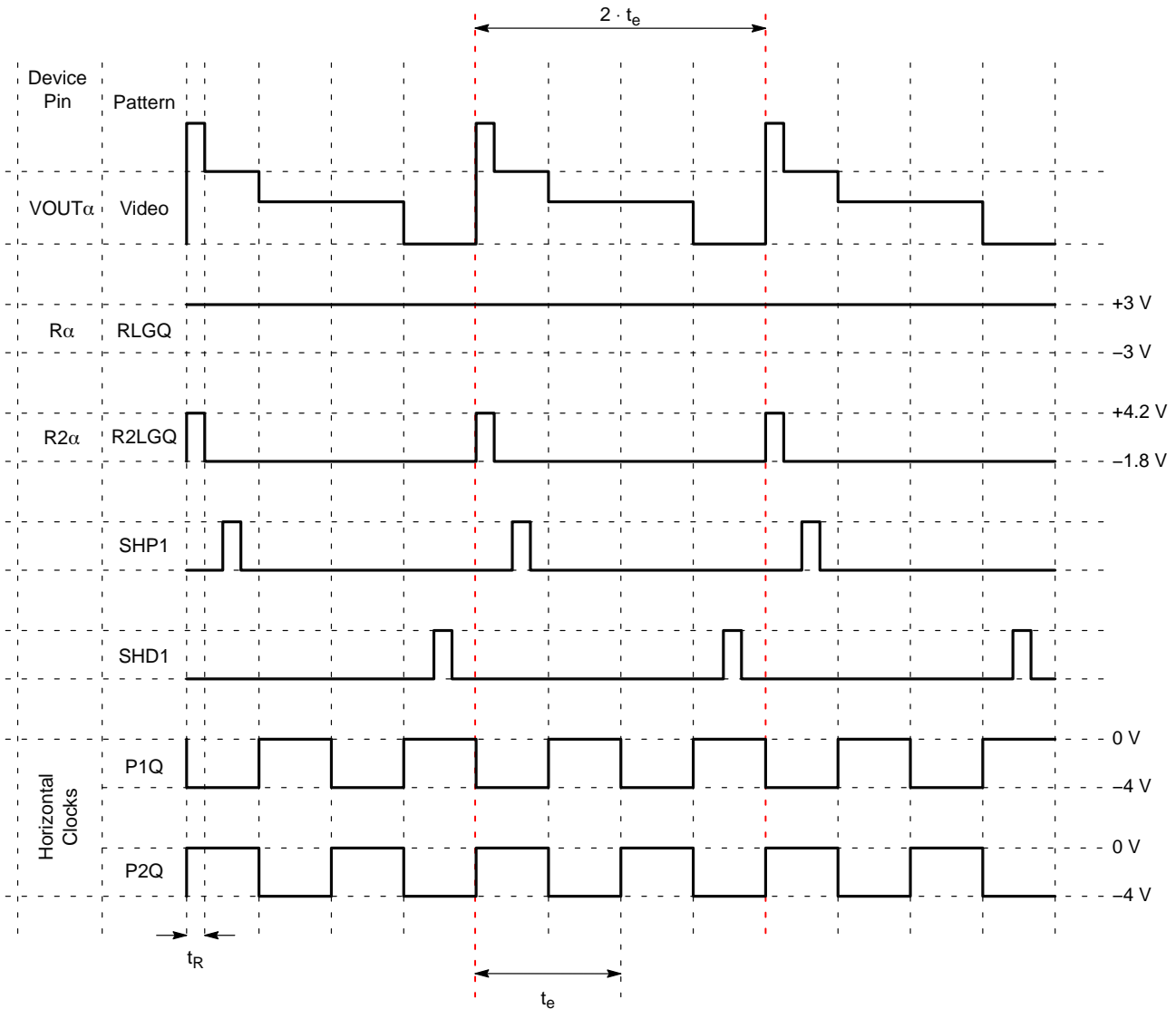


Figure 44. Pixel Timing Diagram – 1/4 Resolution – Low Gain

XLDR Pixel Timing

To operate the sensor in extended linear dynamic range (XLDR) mode, the following pixel timing should be used. This mode requires two sets of analog front end (AFE) signal processing electronic units for each output. As shown in Figure 45 one AFE samples the pixel at low gain (SHPLG and SHDLG) and the other AFE samples the pixel at high gain (SHPHG and SHDHG).

Two HCCD pixels are summed on the output amplifier node to obtain enough charge to fully use the 82 dB range of the XLDR timing. Combined with two-line VCCD summing, a total of 160,000 electrons of signal ($4 \times 40,000$)

can be sampled with 12 electrons or less noise. Note that a linear dynamic range of 82 dB is very large. Ensure that the camera optics is capable of focusing an 82 dB dynamic range image on the sensor. Lens flare caused by inexpensive optics or even dust on the lens will limit the dynamic range.

The timing shown in Figure 47 shows the HCCD not being clocked at a constant frequency. If the HCCD cannot be clocked at a variable frequency, then the HCCD may be clocked at a constant frequency (Figure 46) at the expense of about 33% slower frame rate.



Figure 45. XLDR Timing – AFE Connections Block Diagram

Pixel Timing – 1/4 Resolution – XLDR Pixel Timing – Constant HCCD Timing



Figure 46. Pixel Timing Diagram – 1/4 Resolution – XLDR – Constant HCCD Timing

Pixel Timing – 1/4 Resolution – XLDR Pixel Timing – Variable HCCD Timing

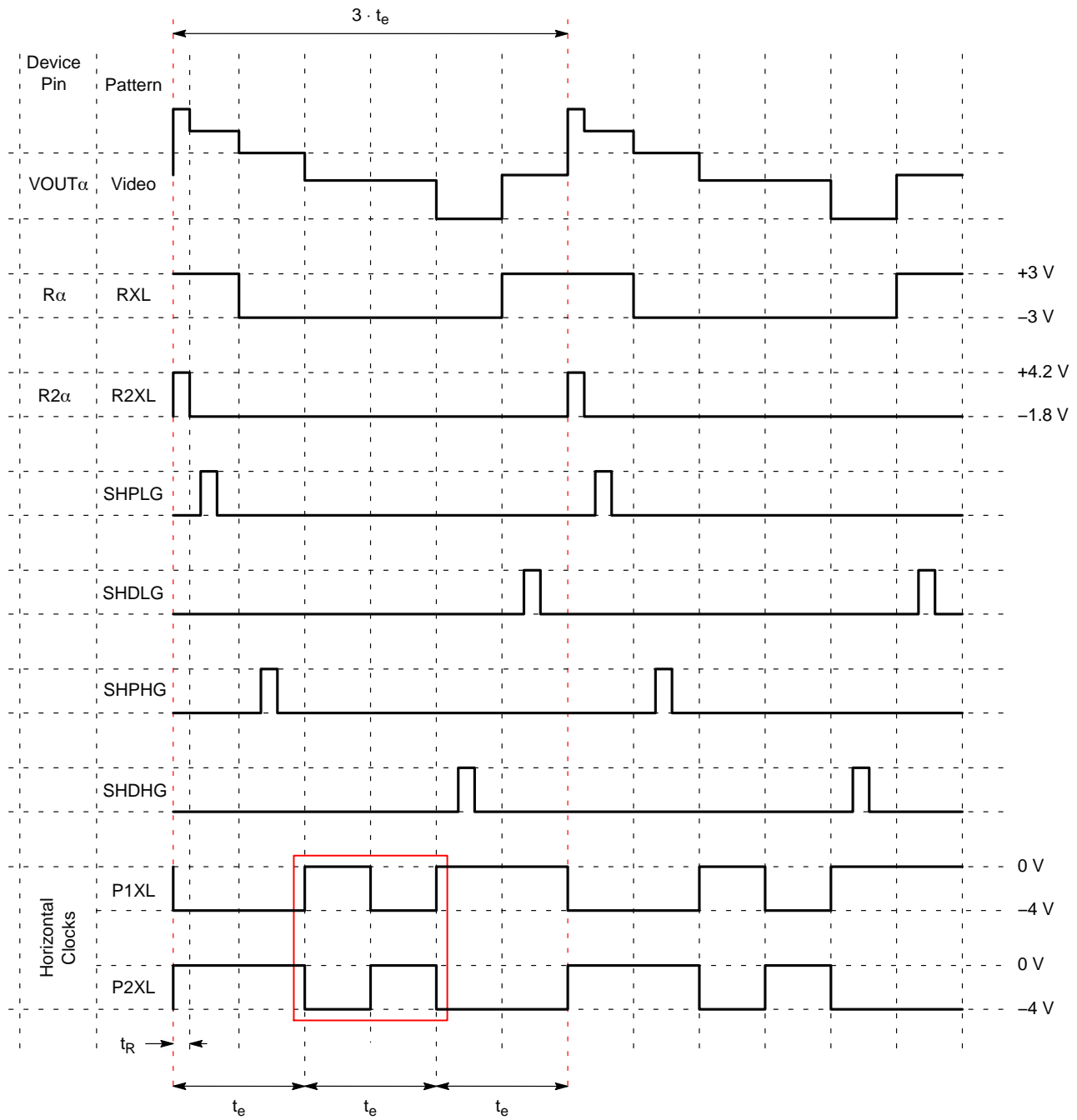


Figure 47. Pixel Timing Diagram – 1/4 Resolution – XLDR – Variable HCCD Timing

VCCD Clock Edge Alignment



Figure 48. VCCD Clock Rise Time, Fall Time and Edge Alignment

STORAGE AND HANDLING

Table 22. STORAGE CONDITIONS

| Description | Symbol | Minimum | Maximum | Unit | Notes |
|---------------------|-----------------|---------|---------|------|-------|
| Storage Temperature | T _{ST} | -55 | 80 | °C | 1 |
| Humidity | RH | 5 | 90 | % | 2 |

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the *Soldering and Mounting Techniques Reference Manual* (SOLDERRM/D) from www.onsemi.com.

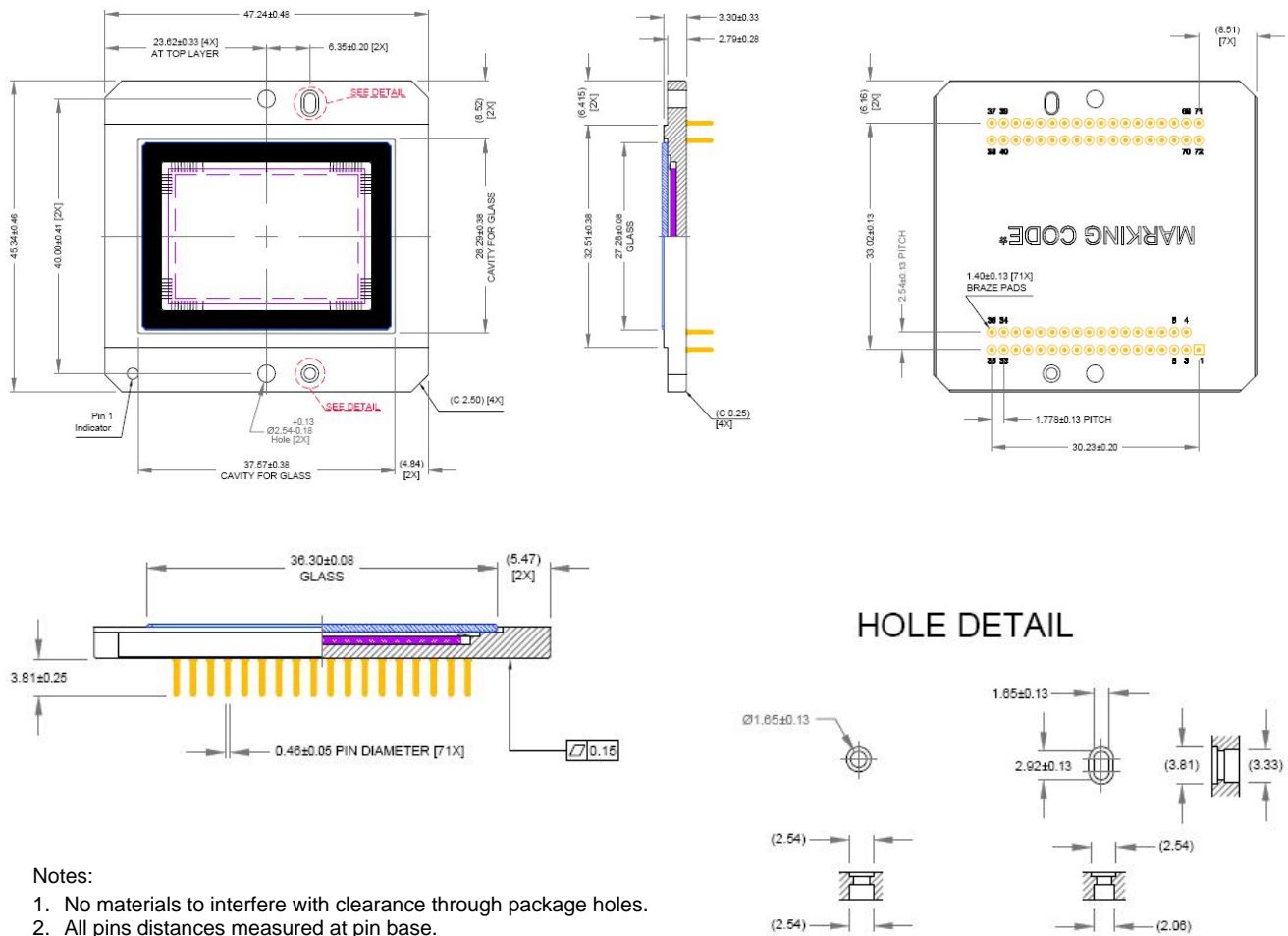
For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](http://www.onsemi.com) from www.onsemi.com.

MECHANICAL INFORMATION

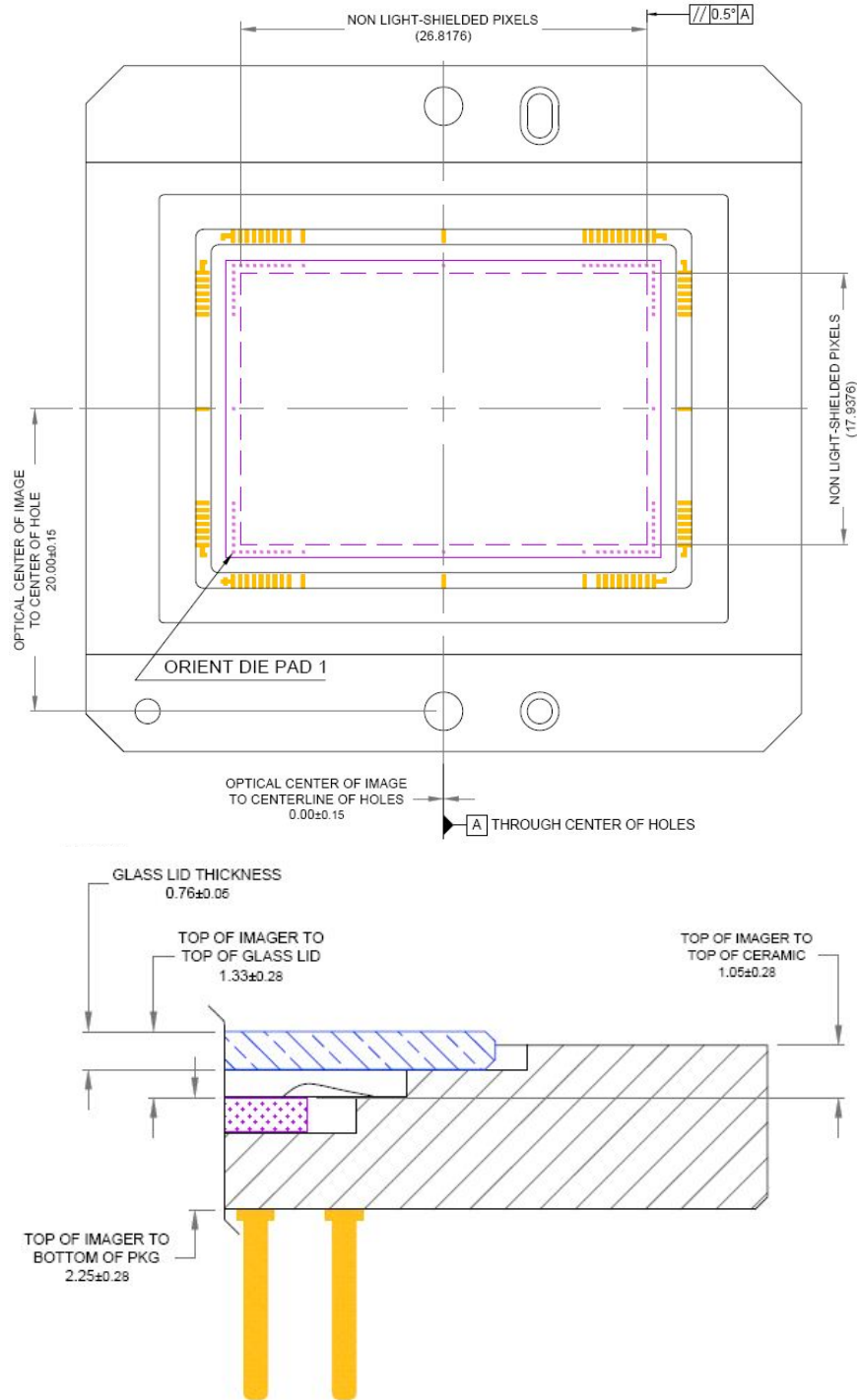
Completed Assembly



Notes:

1. No materials to interfere with clearance through package holes.
2. All pins distances measured at pin base.

Figure 49. Completed Assembly (1 of 2)

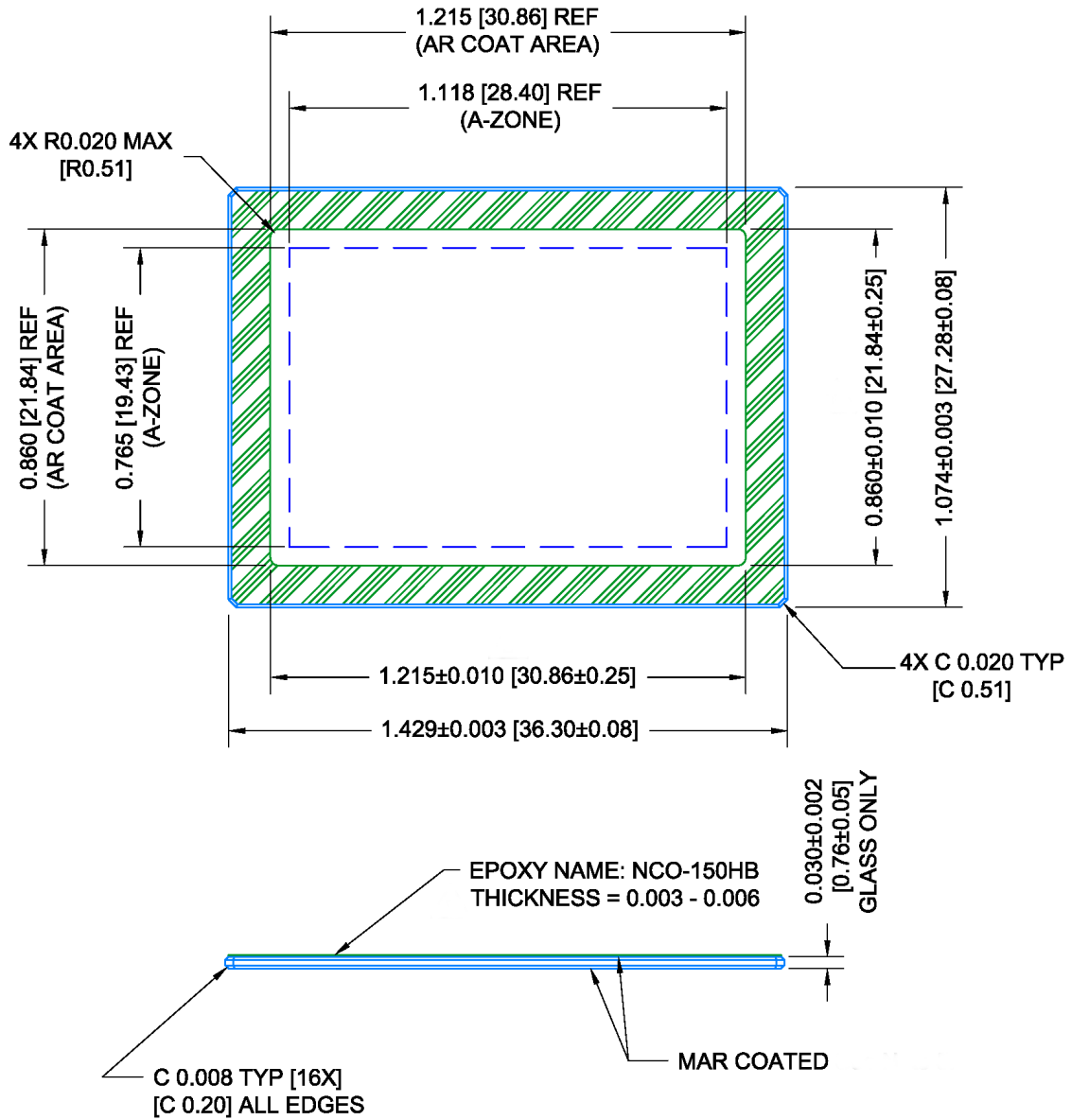


Notes:

1. Die thickness is 0.675 ± 0.025 mm.
2. Imager is stepped at (X) 28.760 and (Y) 19.740 mm or standard 150 mm wafer
3. Assuming a 50 micron kerf, singulated die are approximately 28.71×19.69 mm.
4. Center of image array is at center of die.

Figure 50. Completed Assembly (2 of 2)

Cover Glass



Notes:


1. Substrate = Schott D263T eco.
2. Dust, Scratch, Inclusion Specification: 10 μm maximum size in Zone A.
3. MAR coated both sides.
4. Spectral Transmission:
 - a. T > 98.0% 420-435 nm
 - b. T > 99.2% 435-630 nm
 - c. T > 98.0% 630-680 nm
5. Units: mm.

Figure 51. Cover Glass

Cover Glass Transmission



Figure 52. Cover Glass Transmission

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<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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