# MIC2186

## Low Voltage PWM Control IC

## General Description

Micrel's MIC2186 is a high efficiency boost PWM control IC. With its wide input voltage range of 2.9V to 14V, the MIC2186 can be used to efficiently boost voltages in 1- or 2-cell Li Ion battery powered applications, as well as to boost voltages in fixed 3.3V, 5V, or 12V systems. Its powerful 1.6Ω output driver allows the MIC2186 to supply large output currents with the selection of proper external MOSFETs.

The MIC2186 can be configured to operate at 100kHz, 200kHz, or 400kHz. With it's fixed frequency PWM architecture, and easily synchronized drive, the MIC2186 is ideal for noise-sensitive telecommunications applications.

MIC2186 also features a low current shutdown mode of 0.5μA and programmable undervoltage lockout. A manually selectable SKIP Mode allows high efficiencies in light load situations.

The MIC2186 is available in 16 pin SOIC and QSOP package options with an operating range from –40°C to 125°C.

## Features

- Input voltage range: 2.9V to 14V
- 1.6Ω output driver
- Oscillator frequency of 100kHz/200kHz/400kHz
- Frequency sync to 600kHz
- Front edge blanking
- PWM Current Mode Control
- Selectable light load SKIP mode
- 600μA quiescent current (SKIP-Mode)
- 0.5μA shutdown current
- Cycle-by-Cycle current limiting
- Frequency foldback protection
- Adjustable under-voltage lockout
- Precision 1.245V reference output
- 16 pin SOIC and QSOP package options
- Selectable 50% maximum duty cycle for flyback applications

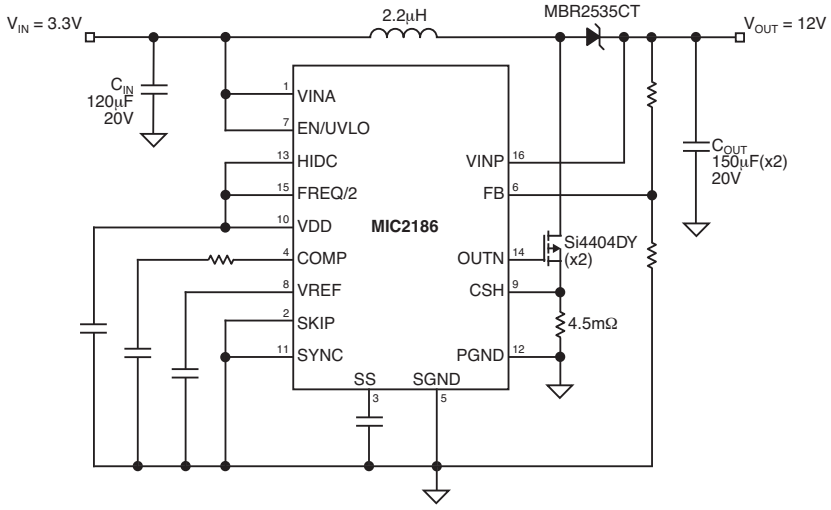
## Applications

- DC power distribution systems
- Wireless Modems
- ADSL line cards
- SLIC power supplies
- 1-and 2-cell Li Ion battery operated equipment

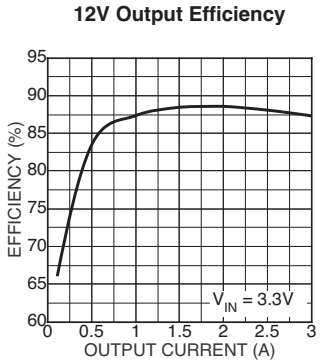
## Ordering Information

| Part Number | | Frequency (kHz) | Voltage | Ambient Temp. Range | Package |
|---|---|---|---|---|---|
| Standard | Pb-Free | | | | |
| MIC2186BM | MIC2186YM | 100 / 200 / 400 | Adj | –40°C to +125°C | 16-lead SOP |
| MIC2186BQS | MIC2186YQS | 100 / 200 / 400 | Adj | –40°C to +125°C | 16-lead QSOP |

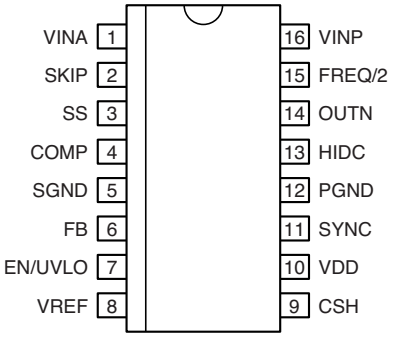
## Typical Application




Adjustable Output Boost Converter



## Pin Configuration




**16-pin Narrow Body SOP (M)**
**16-pin QSOP (QS)**

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1 | VINA | Input voltage to control circuitry (2.9V to 14V). |
| 2 | SKIP | SKIP (Input): Regulator operates in PWM mode (no pulse skipping) when pin is pulled low, and skip mode when raised to Vdd. There is no automatic switching between PWM and skip mode available on this device. |
| 3 | SS | Soft start reduces the inrush current and delays and slows the output voltage rise time. A 5μA current source will charge the capacitor up to Vdd. |
| 4 | COMP | Compensation (Output): Internal error amplifier output. Connect to a capacitor or series RC network to compensate the regulator's control loop. |
| 5 | SGND | Small signal ground: must be routed separately from other grounds to the (-) terminal of Cout. |
| 6 | FB | Feedback Input - regulates FB to 1.245V. |
| 7 | EN/UVLO | Enable/Undervoltage Lockout (input): A low level on this pin will power down the device, reducing the quiescent current to under 0.5μA. This pin has two separate thresholds, below 1.5V the output switching is disabled, and below 0.9V the device is forced into a complete micropower shutdown. The 1.5V threshold functions as an accurate undervoltage lockout (UVLO) with 135mV hysteresis. |
| 8 | VREF | The 1.245V reference is available on this pin. A 0.1μF capacitor should be connected form this pin to SGnd. |
| 9 | CSH | The (+) input to the current limit comparator. A built in offset of 100mV between CSH and SGnd in conjunction with the current sense resistor sets the current limit threshold level. This is also the (+) input to the current amplifier. |
| 10 | VDD | 3V internal linear-regulator output. Vdd is also the supply voltage bus for the chip. Bypass to SGND with 1μF. Maximum source current is 0.5mA. |
| 11 | SYNC | Frequency Synchronization (Input): Connect an external clock signal to synchronize the oscillator. Leading edge of signal above 1.5V starts switching cycle. Connect to SGND if not used. |
| 12 | PGND | MOSFET driver power ground, connects to the bottom of the current sense resistor and the (–) terminal of $C_{IN}$. |
| 13 | HIDC | High Duty Cycle. Sets duty cycle and frequency along with Freq/2. Logic HIGH sets 85% maximum duty cycle. Logic LOW sets 50% maximum duty cycle. See applications section for more information. |
| 14 | OUTN | High current drive for N channel MOSFET. Voltage swing is from ground to $V_{IN}$. $R_{ON}$ is typically 1.6Ω. |
| 15 | FREQ/2 | Sets duty cycle and frequency along with HiDC. See applications section for more information. |
| 16 | VINP | Power input voltage to the gate drive circuitry (2.9V to 14V). This pin is normally connected to the output voltage. |

## Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{IN}A$, $V_{IN}P$) ..... 15V
Digital Supply Voltage ($V_{DD}$) ..... 7V
SKIP Pin Voltage ($V_{SKIP}$) ..... –0.3V to 7V
Max Duty Cycle Pin Voltage ($V_{HIDC}$) ..... –0.3V to 7V
Frequency Divider Pin Voltage ($V_{FREQ/2}$) ..... –0.3V to 7V
Sync Pin Voltage ($V_{SYNC}$) ..... –0.3V to 7V
Comp Pin Voltage ($V_{COMP}$) ..... –0.3V to 3V
Feedback Pin Voltage ($V_{FB}$) ..... –0.3V to 3V
Enable Pin Voltage ($V_{EN/UVLO}$) ..... –0.3V to 15V
Current Sense Voltage ($V_{CSH}$) ..... –0.3V to 1V
Power Dissipation ($P_D$)
16 lead SOP ..... 400mW @ $T_A$ = 85°C
16 lead QSOP ..... 245mW @ $T_A$ = 85°C
Ambient Storage Temp ..... –65°C to +150°C
ESD Rating (Note 3)

## Operating Ratings (Note 2)

Supply Voltage ($V_{IN}A$, $V_{IN}P$) ..... +2.9V to +14V
Operating Ambient Temperature ..... $-40°C \le T_A \le +85°C$
Junction Temperature ..... $-40°C \le T_J \le +125°C$
PackageThermal Resistance
$\theta_{JA}$ 16-lead SOP ..... 100°C/W
$\theta_{JA}$ 16-lead QSOP ..... 163°C/W

## Electrical Characteristics

$V_{IN}A$ = 5V, $V_{IN}P$ = $V_{OUT}$ = 12V, SKIP = 0V, FREQ/2 = 0V, HiDC = 3V, $V_{CSH}$ = 0V, $T_J$ = 25°C, unless otherwise specified. **Bold** values indicate $-40°C < T_J < +125°C$.

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Regulation** | | | | | |
| Feedback Voltage Reference | (±1%) | 1.233 | 1.245 | 1.258 | V |
| | (±2%) | **1.220** | | **1.270** | V |
| | 3V ≤ $V_{IN}A$ ≤ 9V; 0mV ≤ CSH ≤ 75mV; (±3%) | 1.208 | 1.245 | 1.282 | V |
| Feedback Bias Current | | | 50 | | nA |
| Output Voltage Line Regulation | 3V ≤ $V_{IN}A$ ≤ 9V | | +0.08 | | % / V |
| Output Voltage Load Regulation | 0mV ≤ CSH ≤ 75mV | | –1.2 | | % |
| **Input & $V_{DD}$ Supply** | | | | | |
| $V_{IN}A$ Input Current, PWM mode | $V_{SKIP}$ = 0V | | 0.7 | | mA |
| $V_{IN}P$ Input Current, PWM mode | $V_{SKIP}$ = 0V (excluding external MOSFET gate current) | | 2.8 | | mA |
| $V_{IN}A$ Input Current, SKIP mode | $V_{SKIP}$ = 5V | | 0.6 | | mA |
| Shutdown Quiescent Current | VEN/UVLO = 0V; ($I_{VINA}$ + $I_{VINP}$) | | 0.5 | 5 | μA |
| Digital Supply Voltage (VDD) | $I_L$ = 0 | 2.82 | 3.0 | 3.18 | V |
| Digital Supply Load Regulation | $I_L$ = 0 to 0.5mA | | 0.03 | | V |
| Undervoltage Lockout | $V_{DD}$ upper threshold (turn on threshold) | 2.9 | 2.75 | | V |
| | $V_{DD}$ lower threshold (turn off threshold) | | 2.65 | | V |
| **Reference Output ($V_{REF}$)** | | | | | |
| Reference Voltage | (±1.5%) | 1.226 | 1.245 | 1.264 | V |
| | (±2.5%) | **1.213** | | **1.276** | V |
| Reference Voltage Line Regulation | 5V < VinA < 9V | | 2 | | mV |
| Reference Voltage Load Regulation | 0 < $I_{REF}$ < 100μA | | 1 | | mV |

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Enable/UVLO** | | | | | |
| Enable Input Threshold | | 0.6 | 0.9 | 1.2 | V |
| UVLO Threshold | | 1.4 | 1.5 | 1.6 | V |
| UVLO Hysteresis | | | 140 | | mV |
| Enable Input Current | $V_{EN/UVLO}$ = 5V | | 0.2 | 5 | µA |
| **Soft Start** | | | | | |
| Soft Start Current | | | 5 | | µA |
| **Current Limit** | | | | | |
| Current Limit Threshold Voltage | (Voltage on CSH to trip current limit) | 80 | 100 | 120 | mV |
| **Error Amplifier** | | | | | |
| Error Amplifier Gain | | | 20 | | V/V |
| **Current Amplifier** | | | | | |
| Current Amplifier Gain | | | 3.7 | | V/V |
| **SKIP Input** | | | | | |
| SKIP Threshold | | 0.6 | 1.4 | 2.2 | V |
| SKIP Input Current | $V_{SKIP}$ = 3V | | 0.1 | 5 | µA |
| **HIDC Input** | | | | | |
| HIDC Threshold | | 0.6 | 1.4 | 2.2 | V |
| **Oscillator Section** | | | | | |
| Oscillator Frequency ($f_O$) | | 360 | 400 | 440 | kHz |
| Maximum Duty Cycle | $V_{FB}$ = 1.0V, $V_{HIDC}$ = 3V<br>$V_{FB}$ = 1.0V, $V_{HIDC}$ = 0V | | 85<br>50 | | % |
| Minimum On Time | $V_{FB}$ = 1.5V, $V_{HiDC}$ = 3V | | 180 | | ns |
| FREQ/2 Frequency ($f_O$) | $V_{HiDC}$ = 3V, $V_{FREQ/2}$ = 3V | 170 | 200 | 230 | kHz |
| Frequency Foldback Threshold | Measured on FB | | 0.3 | | V |
| Frequency Foldback Frequency | $V_{HiDC}$ = 3V, $V_{FREQ/2}$ = 0V | | 90 | | kHz |
| SYNC Threshold Level | | 0.6 | 1.4 | 2.2 | V |
| SYNC Input Current | | | 0.1 | 5 | µA |
| SYNC Minimum Pulse Width | | 200 | | | ns |
| SYNC Capture Range | **Note 4** | $f_O$ + 15 % | | 600 | kHz |
| **Gate Drivers** | | | | | |
| Rise/Fall Time | $C_L$ = 3300pF | | 50 | | ns |
| Output Driver Impedance | source; $V_{IN}P$ = 12V | | 1.8 | **4** | Ω |
| | sink; $V_{IN}P$ = 12V | | 1.6 | **3.5** | Ω |
| | source; $V_{IN}P$ =5V | | 2.6 | | Ω |
| | sink; $V_{IN}P$ = 5V | | 2.4 | | Ω |

**Note 1.** Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its operating ratings. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(max)}$, the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$.

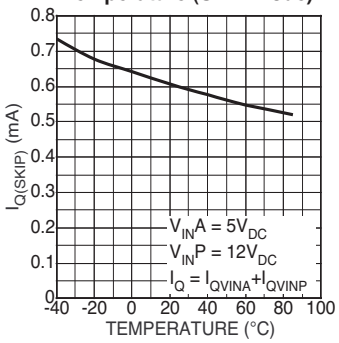
**Note 2.** The device is not guaranteed to function outside its operating rating.

**Note 3.** Devices are ESD sensitive. Handling precautions recommended.

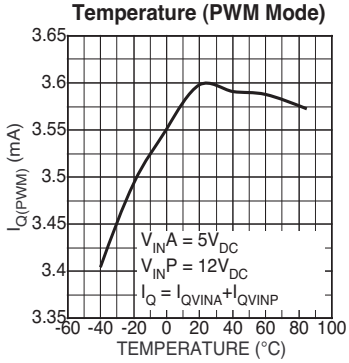
**Note 4.** See application information for limitations on maximum operating frequency.

## Typical Characteristics

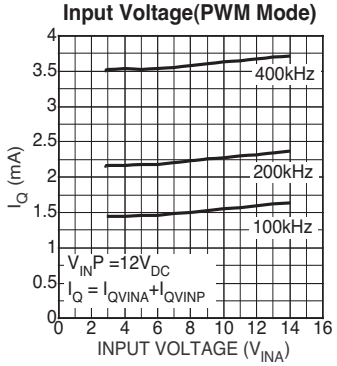
**Quiescent Current vs. Temperature (SKIP Mode)**



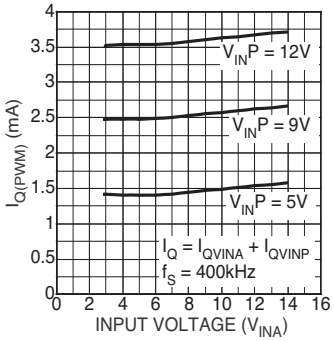

**Quiescent Current vs. Temperature (PWM Mode)**



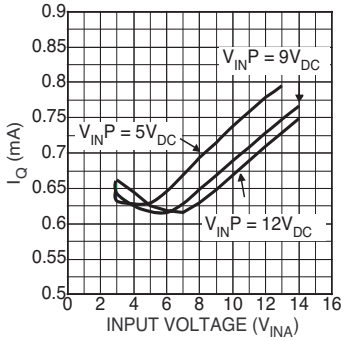

**Quiescent Current vs. Input Voltage(PWM Mode)**



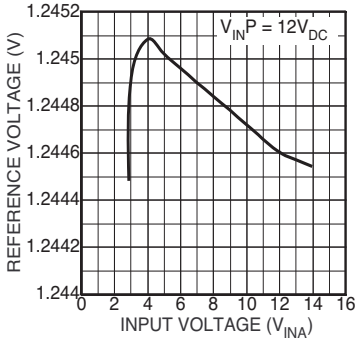

**Quiescent Current vs. Input Voltage (PWM Mode)**



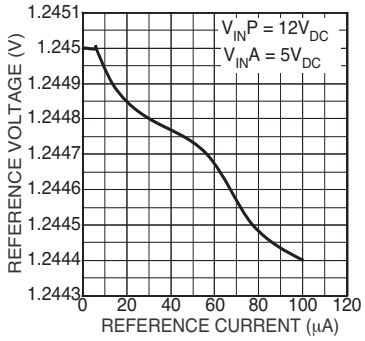

**Quiescent Current vs. Input Voltage (SKIP Mode)**



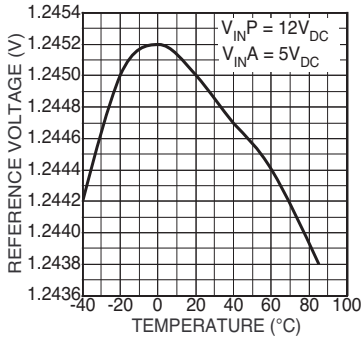

**Reference Voltage vs. Input Voltage**



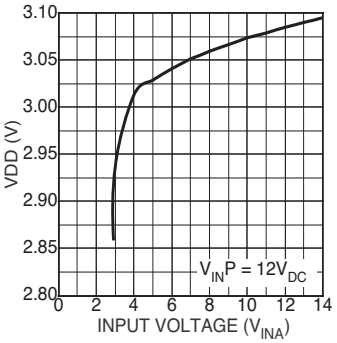

**Reference Voltage vs. Reference Current**



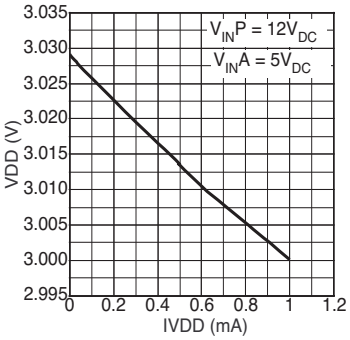

**Reference Voltage vs. Temperature**



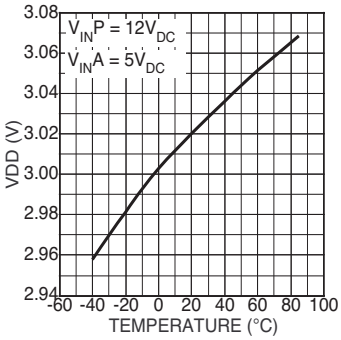

**VDD vs. Input Voltage**



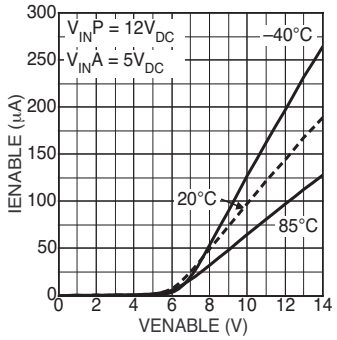

**VDD vs. Load Current**



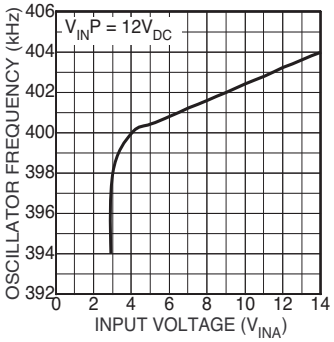

**VDD vs. Temperature**



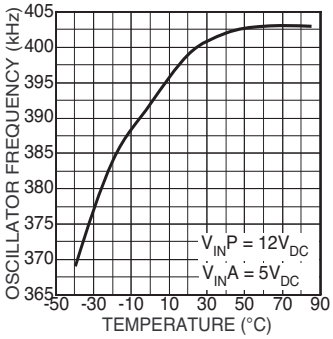

**Ienable vs. Venable**



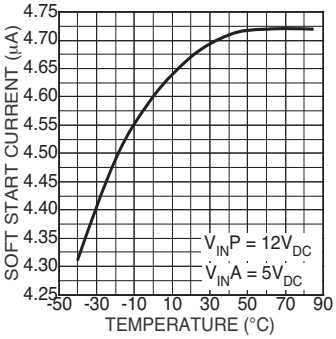
**Oscillator Frequency vs. Input Voltage**



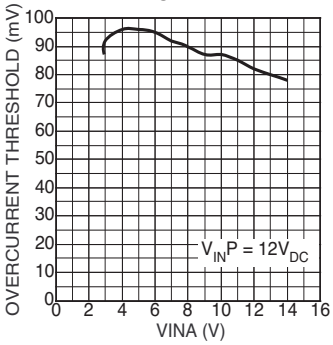

**Oscillator Frequency vs. Temperature**




**Soft Start vs. Temperature**




**Overcurrent Threshold vs. VINA**



## Functional Diagram

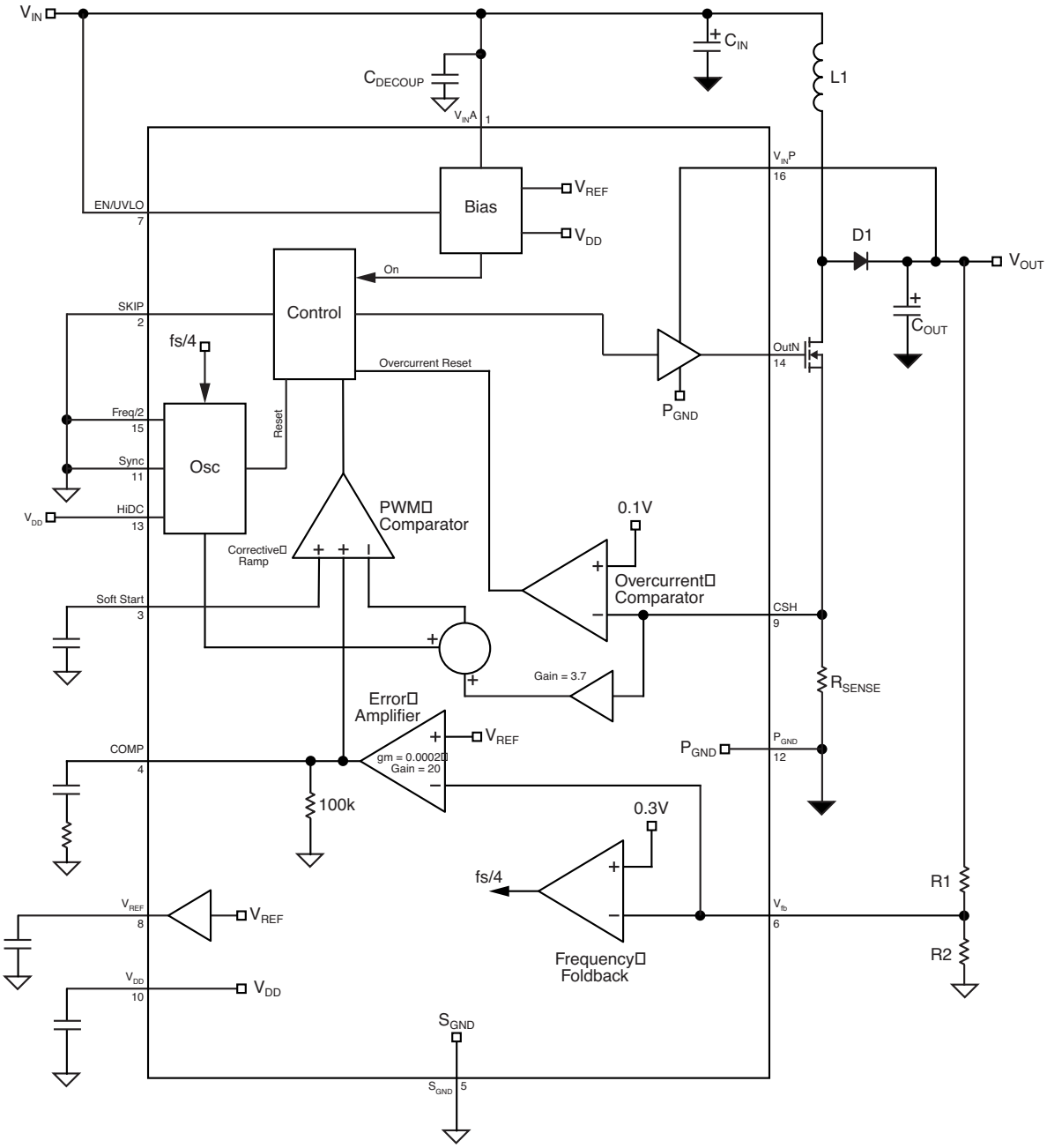



**Figure 1. MIC2186 PWM Block Diagram**

## Functional Description

The MIC2186 is a BiCMOS, switched mode multi-topology controller. It will operate most low side drive topologies including boost, SEPIC, flyback and forward. The controller has a low impedance driver capable of switching large N-channel MOSFETs. It features multiple frequency and duty cycle settings. Current mode control is used to achieve superior transient line and load regulation. An internal corrective ramp provides slope compensation for stable operation above a 50% duty cycle. The controller is optimized for high efficiency, high performance DC-DC converter applications. Figure 1 shows a block diagram of the MIC2186 configured as a PWM boost converter.

The switching cycle starts when OutN goes high and turns on the low side, N-channel MOSFET, Q1. The Vgs of the MOSFET is equal to $V_{IN}P$. This forces current to ramp up in the inductor. The inductor current flows through the current sense resistor, Rsense. The voltage across the resistor is amplified and combined with an internal ramp for stability. This signal is compared with the error voltage signal from the error amplifier. When the current signal equals the error voltage signal, the low side MOSFET is turned off. The inductor current then flows through the diode, D1, to the output. The MOSFET remains off until the beginning of the next switching cycle.

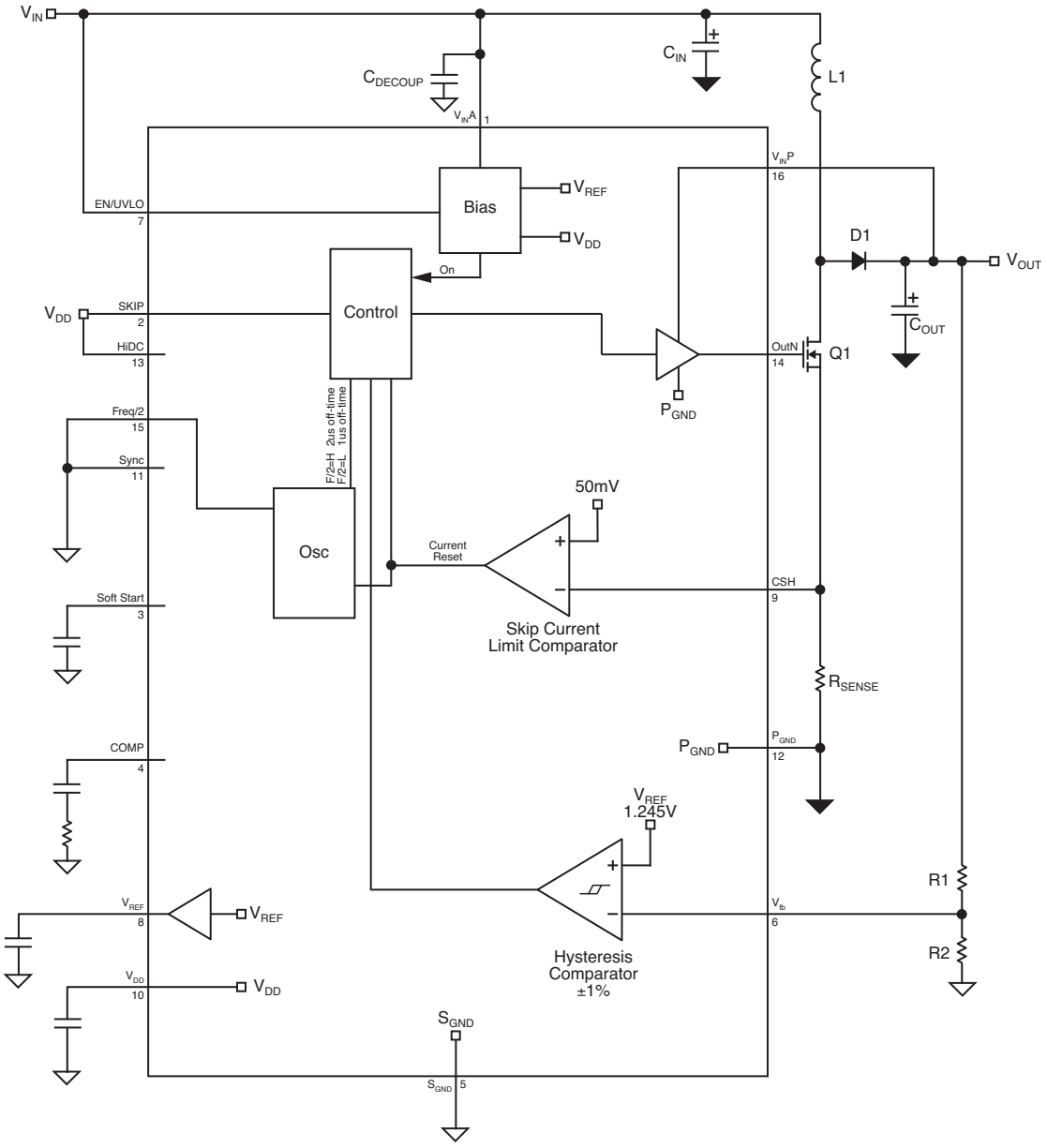



**Figure 2. MIC2186 SKIP Mode Block Diagram**

The description of the MIC2186 controller is broken down into 6 basic functions.

- Control Loop
  - PWM Operation
  - SKIP Mode Operation
- Current Limit
- MOSFET gate drive
- Reference, enable & UVLO
- Oscillator & Sync
- Soft start

## Control Loop

### PWM and SKIP modes of operation

The MIC2186 can operate in either PWM (pulse width modulated) or SKIP mode. The efficiency of the boost converter can be improved at lower output loads by manually selecting the skip mode of operation. The potential disadvantage of skip mode is the variable switching frequency that accompanies this mode of operation. The occurrence of switching pulses depends on component values as well as line and load conditions. PWM mode is the best choice of operation at higher output loads. PWM mode has the advantages of lower output ripple voltage and higher efficiencies at higher output loads. Pulling the SKIP pin (pin 3) low will force the controller to operate in PWM mode for all load conditions. Pulling the SKIP pin high will force the controller to operate in SKIP mode.

### SKIP Mode Operation

This control method is used to improve efficiency at low output loads. A block diagram of the MIC2186 SKIP mode is shown in Figure 2. The power drawn by the MIC2186 control IC is ($I_{VIN}A \cdot V_{IN}A$ )+ ($I_{VIN}P \cdot V_{IN}P$). The power dissipated by the IC can be a significant portion of the total output power during periods of low output current, which lowers the efficiency of the power supply. In SKIP mode the MIC2186 lowers the IC supply current by turning off portions of the control and drive circuitry when the IC is not switching. The disadvantage of this method is greater output ripple and variable switching frequency. The soft start, HiDC and Sync pins have no effect when operating in SKIP mode.

In SKIP mode, switching starts when the feedback voltage drops below the lower threshold level of the hysteresis comparator. The OutN pin goes high, turning on the N-channel MOSFET, Q1. Current ramps up in the inductor until either the current limit comparator or the hysteretic voltage comparator turns off Q1's gate drive. If the feedback voltage exceeds the upper hysteretic threshold, Q1's gate drive is terminated. However, if the voltage at the CSH pin exceeds the SKIP mode current limit threshold, it terminates the gate drive for that switching cycle. The gate drive remains off for a constant period at the end of each switching cycle. This off time period is typically 1μs when the F/2 pin is low and 2μs when the F/2 pin is high. Figure 3 shows some typical SKIP mode switching waveforms.

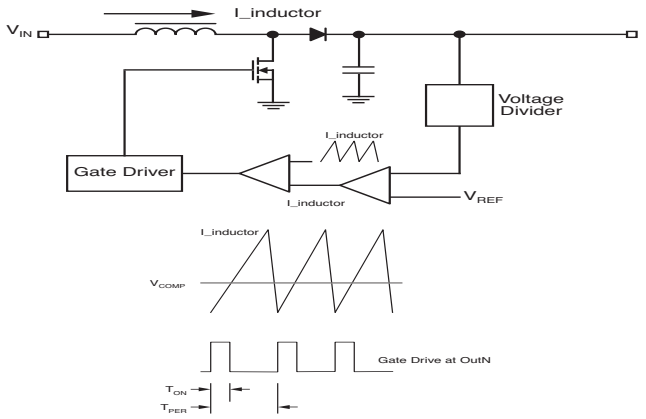



**Figure 3. SKIP Mode Waveform**

The SKIP mode current threshold limits the peak inductor current per cycle. Depending on the input, output and circuit parameters, many switching cycles can occur before the feedback voltage exceeds the upper hysteretic threshold. Once the voltage on the feedback pin exceeds the upper hysteretic threshold the gate drive is disabled. The output load discharges the output capacitance causing Vout to decrease until the feedback voltage drops below the lower threshold voltage limit. The switching converter then turns the gate drive back on. While the gate drive is disabled, the MIC2186 draws less IC supply current then while it is switching, thereby improving efficiency at low output loads. Figure 4 shows the efficiency improvement at low output loads when SKIP mode is selected.

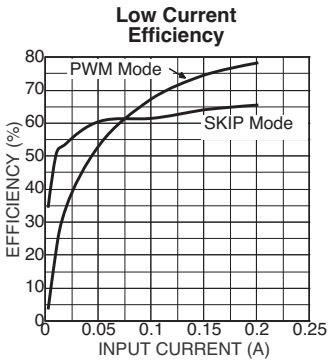



**Figure 4.**

The maximum peak inductor current depends on the skip current limit threshold and the value of the current sense resistor, Rsense. For a typical 50mV current limit threshold in SKIP Mode, the peak inductor current is:

$$I_{INDUCTOR_pk} = \frac{50mV}{R_{SENSE}}$$

The maximum output current is SKIP mode depends on the input conditions, output conditions and circuit component values. Assuming a discontinuous mode where the inductor current starts from zero at each cycle, the maximum output current is calculated below:

$$I_{O(max)} = \frac{2.5 \times 10^{-3} \times L \times fs}{2 \times R_{SENSE}^{2} \times \left(V_O - \eta \times V_{IN}\right)}$$

where:

Iomax is the maximum output current

Vo is the output voltage

Vin is the input voltage

L is the value of the boost inductor

fs is the switching frequency

$\eta$ is the efficiency of the boost converter

Rsense it the value of the current sense resistor

$2.5 \cdot 10^{-3}$ is a constant based on the SKIP mode current threshold $(50mV)^2$

### PWM Operation

Figure 5 shows typical waveforms for PWM mode of operation. The gate drive signal turns on the external MOSFET which allows the inductor current to ramp up. When the MOSFET turns off, the inductor forces the MOSFET drain voltage to rise until the boost diode turns on and the voltage is clamped at approximately the output voltage.

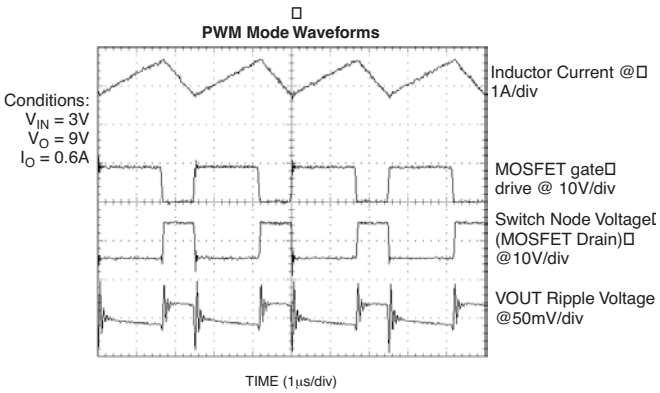



**Figure 5 - PWM mode waveforms**

The MIC2186 uses current mode control to improve output regulation and simplify compensation of the control loop. Current mode control senses both the output voltage (outer loop) and the inductor current (inner loop). It uses the inductor current and output voltage to determine the duty cycle (D) of the buck converter. Sampling the inductor current effectively removes the inductor from the control loop, which simplifies compensation. A simplified current mode control diagram is shown in Figure 6.

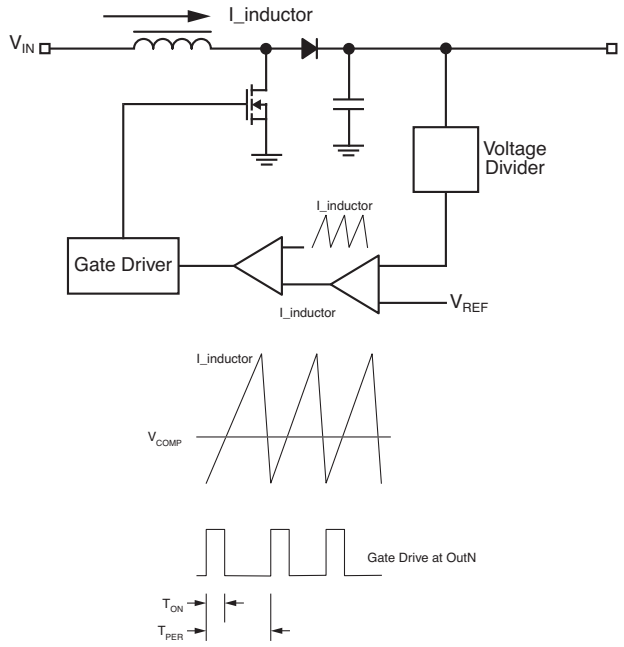



**Figure 6: PWM Control Loop**

A block diagram of the MIC2186 PWM current mode control loop is shown in Figure 1. The inductor current is sensed by measuring the voltage across a resistor, Rsense. The current sense amplifier buffers and amplifies this signal. A ramp is added to this signal to provide slope compensation, which is required in current mode control to prevent unstable operation at duty cycles greater than 50%.

A transconductance amplifier is used as an error amplifier, which compares an attenuated output voltage with a reference voltage. The output of the error amplifier is compared to the current sense waveform in the PWM block. When the current signal rises above the error voltage, the comparator turns off the low side drive. The error signal is brought out to the COMP pin (pin 4) to provide access to the output of the error amplifier. This allows the use of external components to stabilize the voltage loop.

**Current Sensing and Overcurrent Protection**

The inductor current is sensed during the switch on time by a current sense resistor located between the source of the MOSFET and ground (Rsense in Figure 1). Exceeding the current limit threshold will immediately terminate the gate drive of the N-channel MOSFET, Q1. This forces the Q1 to operate at a reduced duty cycle, which lowers the output voltage. **In a boost converter, the overcurrent limit will not protect the power supply or load during a severe overcurrent condition or short circuit condition.** If the output is short-circuited to ground, current will flow from the input, through the inductor and output diode to ground. Only the impedance of the source and components limits the current.

The mode of operation (continuous or discontinuous), the minimum input voltage, maximum output power and the minimum value of the current limit threshold determine the value of the current sense resistor. Discontinuous mode is where all the energy in the inductor is delivered to the output at each switching cycle. Continuous mode of operation occurs when current always flows in the inductor, during both the low-side MOSFET on and off times. The equations below will help to determine the current sense resistor value for each operating mode.

The critical value of output current in a boost converter is calculated below. The operating mode is discontinuous if the output current is below this value and is continuous if above this value.

$$I_{CRIT} = \frac{V_{IN}^2 \times (V_O - V_{IN}) \times \eta}{2 \times fs \times L \times V_O^2}$$

where:

$\eta$ is the efficiency of the boost converter

Vin is the minimum input voltage

L is the value of the boost inductor

Fs is the switching frequency

Vo is the output voltage

Maximum Peak Current in Discontinuous Mode:

The peak inductor current is:

$$I_{IND(pk)} = \sqrt{\frac{2 \times I_O \times (V_O - \eta \times V_{IN})}{L \times fs}}$$

where:

Io is the maximum output current

Vo is the output voltage

Vin is the minimum input voltage

L is the value of the boost inductor

fs is the switching frequency

$\eta$ is the efficiency of the boost converter

The maximum value of current sense resistor is:

$$R_{SENSE} = \frac{V_{SENSE}}{I_{IND(pk)}}$$

where:

Vsense is the minimum current sense threshold of the CSH pin

**Maximum Peak Current in Continuous Mode:**

The peak inductor current is equal to the average inductor current plus one half of the peak to peak inductor current.

The peak inductor current is:

$$I_{IND(pk)} = I_{IND(ave)} + \frac{1}{2} \times I_{IND(pp)}$$

$$I_{IND(pk)} = \frac{V_O \times I_O}{V_{IN} \times \eta} + \frac{V_L \times \left(V_O - V_{IN} \times \eta\right)}{2 \times V_O \times fs \times L}$$

where:

Io is the maximum output current

Vo is the output voltage

Vin is the minimum input voltage

L is the value of the boost inductor

fs is the switching frequency

$\eta$ is the efficiency of the boost converter

VL is the voltage across the inductor

VL may be approximated as Vin for higher input voltage. However, the voltage drop across the inductor winding resistance and low side MOSFET on-resistance must be accounted for at the lower input voltages that the MIC2186 operates at.

$$V_L = V_{IN} - \frac{V_O \times I_O}{V_{IN} \times \eta} \times \left(R_{WINDING} + R_{DSON}\right)$$

where:

Rwinding is the winding resistance of the inductor

Rdson is the on resistance of the low side switching MOSFET

The maximum value of current sense resistor is:

$$R_{SENSE} = \frac{V_{SENSE}}{I_{IND(pk)}}$$

where:

$V_{SENSE}$ is the minimum current sense threshold of the CSH pin

The current sense pin, CSH, is noise sensitive due to the low signal level. The current sense voltage measurement is referenced to the signal ground pin of the MIC2186. The current sense resistor ground should be located close to the IC ground. Make sure there are no high currents flowing in this trace. The PCB trace between the high side of the current sense resistor and the CHS pin should also be short and routed close to the ground connection. The input to the internal current sense amplifier has a 30nS dead time at the beginning of each switching cycle. This dead time prevents leading edge current spikes from prematurely terminating the switching cycle. A small RC filter between the current sense pin and current sense resistor may help to attenuate larger switching spikes or high frequency switching noise. Adding the filter slows down the current sense signal, which has the effect of slightly raising the overcurrent limit threshold.

**MOSFET Gate Drive**

The MIC2186 converter drives a low side N-channel MOSFET. The driver for the OutN pin has a 1.6Ω typical source and sink impedance. The VinP pin is the supply pin for the gate drive circuit. It typically connected to the output. The maximum supply voltage to the VinP pin is 14V. If the output voltage is greater than 14V or if it is desired to drive the MOSFET with a voltage less than Vout, the VinP pin can be connected to the input or to an separate supply voltage.

**MOSFET Selection**

In a boost converter, the Vds of the MOSFET is approximately equal to the output voltage. The maximum Vds rating of the MOSFET must be high enough to allow for ringing and spikes in addition to the output voltage.

The VinP pin supplies the N-channel gate drive voltage. The Vgs threshold voltage of the N-channel MOSFET must be low enough to operate at the minimum VinP voltage to guarantee the boost converter will start up.

The maximum amout of MOSFET gate charge that can be driven is limited by the power dissipation in the MIC2186. The power dissipated by the gate drive circuitry is calculated below:

P_gate_drive=Q_gate * VinP * fs

where:

Q_gate is the total gate charge of the external MOSFET

The graph in Figure 7 shows the total gate charge which can be driven by the MIC2186 over the input voltage range, for different values of switching frequency. Higher gate charge will slow down the turn-on and turn-off times of the MOSFET, which increases switching losses.

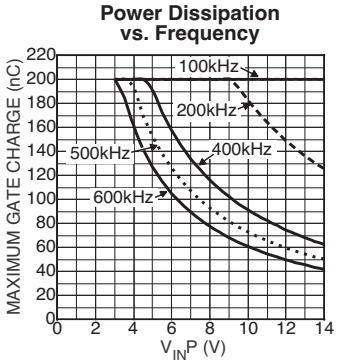



**Figure 7 - MIC2186 freq vs pdiss**

**External Schottky Diode**

In a boost converter topology, the boost diode, D1 must be rated to handle the peak and average current. The average current through the diode is equal to the average output current of the boost converter. The peak current is calculated in the current limit section of this specification.

The reverse voltage requirement of the diode is:

For the MIC2186, Schottky diodes are recommended when they can be used. They have a lower forward voltage drop than ultra-fast rectifier diodes, which lowers power dissipation and improves efficiency. They also do not have a recovery time mechanism, which results in less ringing and noise when the diode turns off. If the output voltage of the circuit prevents the use of a Schottky diode, then only ultra-fast recovery diodes should be used. Slower diodes will dissipate more power in both the MOSFET and the diode. The will also cause excessive ringing and noise when the diode turns off.

**Reference, Enable and UVLO Circuits**

The output drivers are enabled when the following conditions are satisfied:

- The Vdd voltage (pin 10) is greater than its undervoltage threshold.
- The voltage on the enable pin is greater than the enable UVLO threshold.

The internal bias circuitry generates a 1.245V bandgap reference for the voltage error amplifier and a 3V Vdd voltage for the internal supply bus. The reference voltage in the MIC2186 is buffered and brought out to pin 8. The Vref pin must be bypassed to GND (pin 4) with a 0.1uf capacitor. The Vdd pin must be decoupled to ground with a 1uf ceramic capacitor.

The enable pin (pin 7) has two threshold levels, allowing the MIC2186 to shut down in a micro-current mode, or turn off output switching in standby mode. Below 0.9V, the device is forced into a micro-power shutdown. If the enable pin is between 0.9V and 1.5V the output gate drive is disabled but the internal circuitry is powered on and the soft start pin voltage is forced low. There is typically 135mV of hysteresis below the 1.5V threshold to insure the part does not oscillate on and off due to ripple voltage on the input. Raising the enable voltage above the UVLO threshold of 1.5V enables the output drivers and allows the soft start capacitor to charge. The enable pin may be pulled up to VinA.

**Oscillator & Sync**

The internal oscillator is self-contained and requires no external components. The HiDC and f/2 pins allow the user to select from three different switching frequencies and two maximum duty cycles. The chart in Table 1 shows the four combinations that can be programmed along with the typical minimum and maximum duty cycles.

| F/2 pin Level | HiDC Level | Switching Frequency | Maximum Duty Cycle | Typical Minimum Duty Cycle | $T_{OFF}$ in Skip Mode |
|---|---|---|---|---|---|
| 0 | 1 | 400kHz | 85% | 7% | 1$\mu$s |
| 1 | 1 | 200kHz | 85% | 6% | 2$\mu$s |
| 0 | 0 | 200kHz | 50% | 4% | 1$\mu$s |
| 1 | 0 | 100kHz | 50% | 3% | 2$\mu$s |

**Table 1**

Minimum duty cycle becomes important in a boost converter as the input voltage approaches the output voltage. At lower duty cycles, the input voltage can be closer to the output voltage without the output rising out of regulation.

A frequency foldback mode is enabled if the voltage on the feedback pin (pin 6) is less than 0.3V. In frequency foldback the oscillator frequency is reduced by approximately a factor of 4. For the 400kHz setting, the oscillator runs at 100khz in frequency foldback. For a 200kHz setting the oscillator runs at approximately 50kHz and for a 100kHz setting, the oscillator runs at approximately 25kHz.

The SYNC input (pin 11) allows the MIC2186 to synchronize with an external CMOS or TTL clock signal. Depending on the setting of the HiDC pin,the output frequency is either equal to or 1/2 of the sync input frequency. If the HiDC level is low, the output switching frequency is half the sync frequency. If the HiDC level is high, the output switching frequency is equal to the sync frequency.

The rising edge of the sync signal generates a reset signal in the oscillator, which turns off the high-side gate drive output. The low-side drive is turned on, restarting the switching cycle. The sync signal is inhibited when the controller operates in skip mode or frequency foldback. The sync signal frequency must be greater than the maximum specified free running frequency of the MIC2186. If the synchronizing frequency is lower, double pulsing of the gate drive outputs will occur. When not used, the sync pin must be connected to ground. Table 2 shows the minimum recommended sync frequencies for the different combinations of f/2 and HiDC inputs.

Figure 8a shows the timing between the external sync signal (trace 2) and the low-side drive (trace 1) for a high level on the HiDC pin. Figure 8b shows the timing between the external sync signal (trace 2) and the low-side drive (trace 1) for a low level on the HiDC pin. The sync frequency is twice the output switching frequency.

| F/2 pin Level | HiDC Level | Self Oscillating Frequency | Minimum Recommended Sync Frequency | Sync Input Frequency<br>$f_S$=output switching frequency<br>$f_{SYNC}$=sync input frequency |
|---|---|---|---|---|
| 0 | 1 | 400kHz | 480kHz | $f_S = f_{SYNC}$ |
| 1 | 1 | 200kHz | 250kHz | $f_S = f_{SYNC}$ |
| 0 | 0 | 200kHz | 480kHz | $f_S = {}^1/_2\, f_{SYNC}$ |
| 1 | 0 | 100kHz | 250kHz | $f_S = {}^1/_2\, f_{SYNC}$ |

**Table 2**

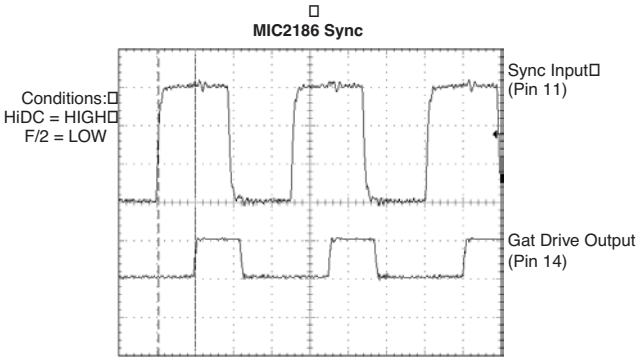



**Figure 8a.**

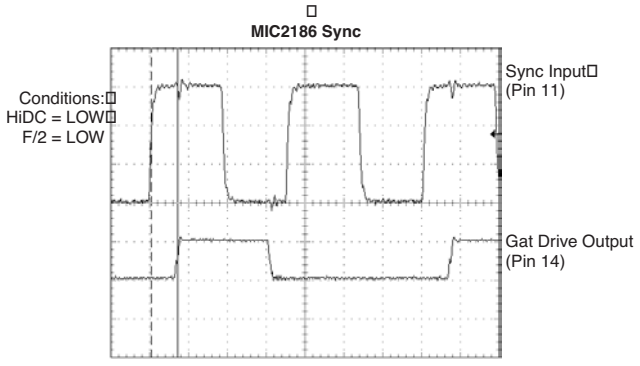



**Figure 8b.**

The maximum recommended output switching frequency is 600kHz. Synchronizing to higher frequencies may be possible, however there are some concerns. As the switching frequency is increased, the switching period decreases. The minimum on-time in the MIC2186 becomes a greater part of the total switching period. This may prevent proper operation as Vin approaches Vout and may also minimize the effectiveness of the current limit circuitry. The maximum duty cycle decreases as the sync frequency is increased. Figure 9 shows the relationship between the minimum/maximum duty cycle and frequency.

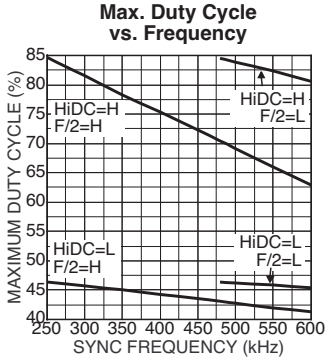



**Figure 9.**

### Soft start

Soft start reduces the power supply input surge current at start up by limiting the output voltage risetime. Input surge current occurs when the boost converter charges up the output capacitance. Slowing the output risetime lowers the input surge current. Soft start may also be used for power supply sequencing. The soft start cannot control the initial surge in current in a boost converter when Vin is applied. This surge current is caused by the output capacitance charging up to the input voltage. The current flows from the input through the inductor and output diode to the output capacitors.

The soft start voltage is applied directly to the PWM comparator. A 5uA internal current source is used to charge up the soft start capacitor. Either of 2 UVLO conditions will pull the soft start capacitor low.

* When the Vdd voltage drops below its UVLO threshold
* When the enable pin drops below its 1.5V UVLO threshold

The part switches at a low duty cycle when the soft start pin voltage zero. As the soft start voltage rises from 0V to 0.7V, the duty cycle increases from the minimum duty cycle to the operating duty cycle. The oscillator runs at the foldback frequency until the feedback voltage rises above 0.3V. In a boost converter the output voltage is equal to the input voltage before the MIC2186 starts switching. If the ratio of Vout/Vin is low, the voltage on the feedback pin will already be greater than 0.3V and the converter begin switching at the selected operating frequency.

The risetime of the output is dependent on the soft start capacitor, output capacitance, input and output voltage and load current. The scope photo in Figure 10 show the output voltage and the soft start pin voltage at startup. The output voltage is initially at the input voltage less a diode drop. After the converter is enabled the output slowly rises due to the minimum duty cycle of the controller. As the soft start voltage increases, the output voltage rises in a controlled fashion until the output voltage reaches the regulated value.

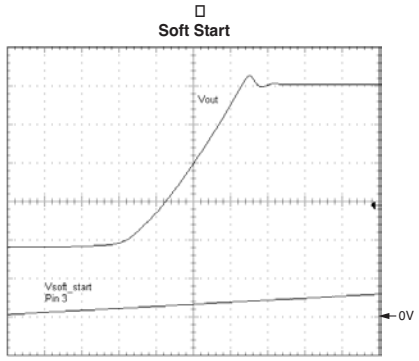



**Figure 10.**

### Voltage Setting Components

The MIC2186 requires two resistors to set the output voltage as shown in figure 11

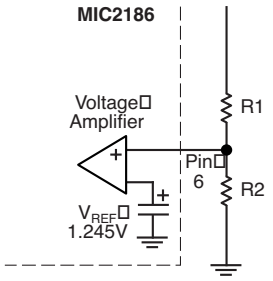



**Figure 11.**

The output voltage is determined by the equation below.

$$V_O = V_{REF} \times 1 + \frac{R1}{R2}$$

Where: Vref for the MIC2186 is nominally 1.245V. Lower values of resistance are preferred to prevent noise from apprearing on the Vfb pin. A typically recommended value for R1 is 10K.

**Decoupling Capacitor Selection**

The 1uf decoupling capacitor is used to stabilize the internal regulator and minimize noise on the Vdd pin. Placement of this capacitor is critical to the proper operation of the MIC2186. It must be next to the Vdd and signal ground pins and routed with wide etch. The capacitor should be a good quality ceramic. Incorrect placement of the Vdd decoupling capacitor will cause jitter and/or oscillations in the switching waveform as well as variations in the overcurrent limit.

A minimum 0.1uf ceramic capacitor is required to decouple the Vin. The capacitor should be placed near the IC and connected directly between pins 10 (Vcc) and 5 (SGND). A 0.1uf capacitor is required to decouple Vref. It should be located near the Vref pin.

**Efficiency calculation and considerations**

Efficiency is the ratio of output power to input power. The difference is dissipated as heat in the boost converter. The significant contributors at light output loads are:

* The VinA pin supply current.
* The VinP pin supply current which includes the current required to switch the external MOSFETs
* Core losses in the inductor

To maximize efficiency at light loads:

* Use a low gate charge MOSFET or use the smallest MOSFET, which is still adequate for the maximum output current.
* Allow the MIC2186 to run in skip mode at lower currents. If running in PWM mode, set the MIC2186 to switch at a lower frequency.
* se a ferrite material for the inductor core, which has less core loss than an MPP or iron power core.

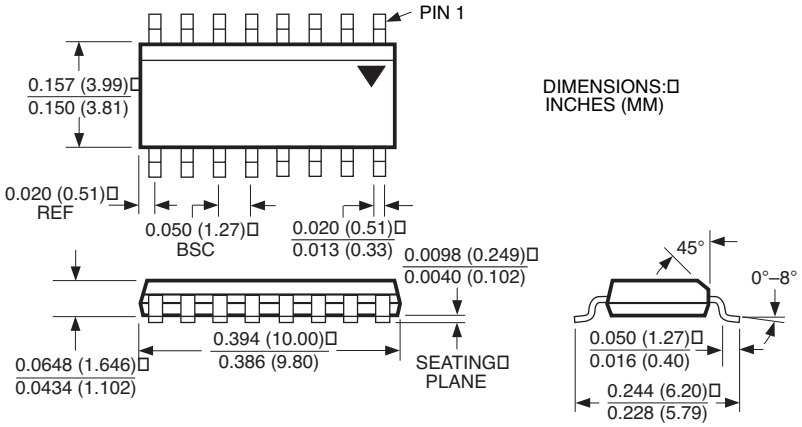
The significant contributors to power loss at higher output loads are (in approximate order of magnitude):

* Resistive on-time losses in the MOSFET
* Switching transition losses in the MOSFET
* Inductor resistive losses
* Current sense resistor losses
* Output capacitor resistive losses (due to the capacitor's ESR)

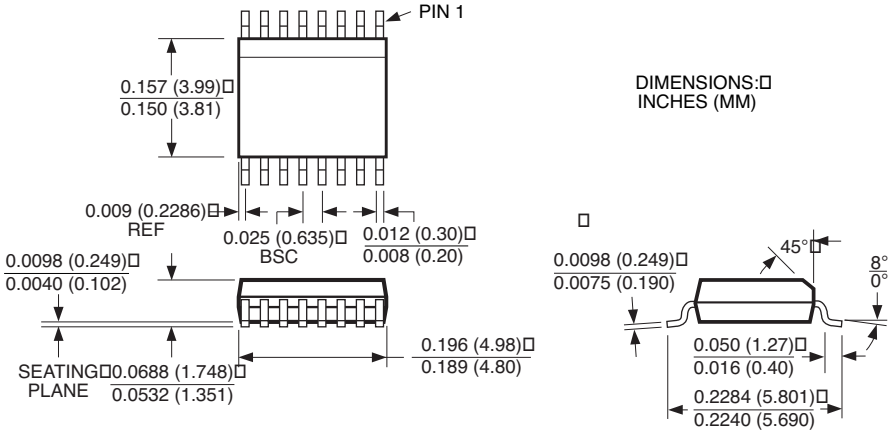
To minimize power loss under heavy loads:

* Use Logic level, low on resistance MOSFETs. Multiplying the gate charge by the on resistance gives a figure of merit, providing a good balance between switching and resistive power dissipation.
* Slow transition times and oscillations on the voltage and current waveforms dissipate more power during the turn-on and turn-off of the low side MOSFET. A clean layout will minimize parasitic inductance and capacitance in the gate drive and high current paths. This will allow the fastest transition times and waveforms without oscillations. Low gate charge MOSFETs will switch faster than those with higher gate charge specifications.
* For the same size inductor, a lower value will have fewer turns and therefore, lower winding resistance. However, using too small of a value will increase the inductor current and therefore require more output capacitors to filter the output ripple.
* Lowering the current sense resistor value will decrease the power dissipated in the resistor. However, it will also increase the overcurrent limit and may require larger MOSFETs and inductor components to handle the higher currents.
* Use low ESR output capacitors to minimize the power dissipated in the capacitor's ESR.

## Package Information




**16-Pin SOIC (M)**




**16-Pin QSOP (QS)**

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