

## Quad, Ultra-Low-Power, **200Mbps ATE Drivers/Comparators**

#### **General Description**

**Features** 

The MAX19005 four-channel, ultra-low-power, pinelectronics IC includes a two-level pin driver, a window comparator, a passive load, and force-and-sense Kelvin-switched parametric measurement unit (PMU) connections for each channel. The driver features a -1V to +5.2V voltage range, includes high-impedance modes, and is highly linear even at low voltage swings. The window comparator features 240MHz equivalent input bandwidth and programmable output voltage levels. The passive load provides pullup and pulldown voltages to the device-under-test (DUT).

Low leakage and high impedance are operational configurations that are programmed through a 3-wire, low-voltage, CMOS-compatible serial interface. Highspeed PMU switching is realized through dedicated digital control inputs.

This device is available in an 80-pin, 12mm x 12mm body, 0.5mm pitch TQFP with an exposed 6mm x 6mm die pad on the bottom of the package for efficient heat removal. The device is specified to operate over the 0°C to +70°C commercial temperature range and features a die temperature monitor output.

Ordering Information appears at end of data sheet.

- ♦ Small Footprint: Four Channels in 0.3in<sup>2</sup>
- **♦** Low-Power Dissipation: 340mW/Channel (typ)
- ♦ High Speed: 200Mbps at 3Vp-p
- ♦ -1V to +5.2V Operating Range
- ♦ Integrated Pin Switch (with -1V to +24V Off Range)
- ♦ Integrated PMU Switches with -1V to +24V **Operating Range**
- **♦ Passive Load**
- ♦ Low-Leakage Mode by Pin Switch Off: 10nA (max)
- ♦ Low Gain and Offset Error

#### **Applications**

NAND Flash Testers

**DRAM Probe Testers** 

Low-Cost Mixed-Signal/System-on-Chip (SoC) Testers

Active Burn-In Systems

Structural Testers

For related parts and recommended products to use with this part, refer to: www.maxim-ic.com/MAX19005.related

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **ABSOLUTE MAXIMUM RATINGS**

\/ to OND	2 4 1 / 1 /
$V_{DD}$ to GND0.3V to +9	$V_{DI}$
V <sub>SS</sub> to GND6.25V to +0	
V <sub>DD</sub> - V <sub>SS</sub> +15.	65V V <sub>S</sub>
V <sub>L</sub> to GND0.3V to -	+5V DÜ
DHV_, DLV_ to GND with	DC
Integrated Pin Switch OffV <sub>SS</sub> - 0.3V to V <sub>DD</sub> + 0	).3V TEI
DHV_, DLV_ to GND with	TEI
Integrated Pin Switch On V <sub>SSSW</sub> - 0.3V to V <sub>DD</sub> + 0	).3V PM
DATA_, RCV_, VBBI to GND0.3V to -	+5V PM
LDV_ to GND $V_{SSSW}$ - 0.3V to $V_{DD}$ + 0	).3V PM
CHV_, CLV_ COMPHI, COMPLO	PM
to GNDV <sub>SS</sub> - 0.3V to V <sub>DD</sub> + 0	0.3V All
CMPH_, CMPL_, VBBO to GND0.3V to \	
LD, DIN, SCLK, CS, SWEN to GND0.3V to	+VL 7
CHV_, CLV_ to DUT_ with Integrated Pin Switch On	8V Sto
DUT_ to GND with Integrated Pin Switch OffV <sub>SSSW</sub> to V <sub>DI</sub>	<sub>DSW</sub> Jur
DUT_ to GND with Integrated Pin Switch On V <sub>SSSW</sub> to \	√ <sub>DD</sub> Lea
FORCE, SENSE, PMU_ to GNDVSSW to VDE	osw Sol
V <sub>DDSW</sub> to V <sub>SSSW</sub> +	

V <sub>DDSW</sub> to V <sub>SS</sub>	+31.35V
V <sub>DDSW</sub> to GND	
V <sub>SSSW</sub> to GND	
DUT_, CMPH_, CMPL_ Short-Circuit Duration	Continuous
DOUT to GND	0.3V to +VL
TEMP to GND	
TEMP Short-Circuit Duration	Continuous
PMU Force Switch Continuous Current	
PMU Force Switch Peak Current	±160mA
PMU Sense Switch Continuous Current	±1mA
PMU Sense Switch Peak Current	±30mA
All Digital Inputs	±30mA
Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
TQFP (derate 35.7mW/°C above +70°C)	2857mW
Storage Temperature Range	
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS		
DRIVER (all specifications apply when DUT_ = DHV_ or DUT_ = DLV_)								
DC CHARACTERISTICS (R <sub>DUT</sub> ≥ 1	10M $\Omega$ , unless	otherwise noted)						
Voltage Range			-1.0		+5.2	V		
Gain		Measured at 0V and +3V	0.995	1	1.005	V/V		
Gain Temperature Coefficient				50		ppm/°C		
Offset		$V_{DHV} = +2V, V_{DLV} = 0V$			±10	mV		
Offset Temperature Coefficient		V <sub>DHV</sub> _ = +1.5V		±250		μV/°C		
	PSRR	$V_{DD}$ , $V_{SS}$ independently varied over full range, $V_{DHV} = +1.5V$			±18	mV/V		
Power-Supply Rejection Ratio	Fonn	V <sub>DDSW</sub> , V <sub>SSSW</sub> independently varied over full range, V <sub>DHV</sub> = +1.5V			±10	mV/V		
Maximum DC Drive Current	I <sub>DUT_</sub>		±40			mA		
DC Output Resistance		$I_{DUT}$ = ±10mA, DATA_ = 1, trim condition, target = 49.5 $\Omega$	47.5	49.5	51.5	Ω		
DC Output Resistance (V <sub>DDSW</sub> = + 15V)		I <sub>DUT_</sub> = ±10mA, DATA_ = 1	49.0	52.0	55.0	Ω		

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **ELECTRICAL CHARACTERISTICS (continued)**

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
DC Output Resistance Variation		I <sub>DUT</sub> = -40m/ (Note 2)	A to +40mA, DATA_ = 1			5.0	Ω
DC Output Resistance Variation (V <sub>DDSW</sub> = +15V)		I <sub>DUT</sub> = -40m/ (Note 2)	A to +40mA, DATA_ = 1			8.0	Ω
DC Crosstalk, DHV_ to DLV_,		$V_{DLV} = +1.5$	/, V <sub>DHV</sub> = -1V, +5.2V			±5	mV
DLV_ to DHV_		$V_{DHV} = +1.5$	V, V <sub>DLV</sub> = -1V, +5.2V			±5	IIIV
Linearity Error		+1.5V (Note 3)	)			±5	mV
Linearity Error		-1V and +5.2V	(Note 3)			±15	IIIV
AC CHARACTERISTICS (R <sub>DUT</sub> = 50	$\Omega$ to GND,	unless otherwi	se noted) (Note 4)				
Dynamic Output Current		(Note 5)			±60		mA
Drive Mode Overshoot, Undershoot, and Preshoot		+0.2V to 4V <sub>P-F</sub>	swing (Note 6)		5% + 10		mV
History and a Control		DHV_/high-Z, V <sub>DLV</sub> _ = -1V, V <sub>DHV</sub> _ = 0V DLV_/high-Z, V <sub>DLV</sub> _ = 0V, V <sub>DHV</sub> _ = +1V		25 25			\/
High-Impedance Mode Spike							- mV
Propagation Delay, Data to Output		$V_{DHV_{-}} = +3V$ , $V_{DLV_{-}} = 0V$ , average of $t_{LH}$ and $t_{HL}$		2.5	3.5	5.1	ns
Propagation Delay Temperature Coefficient		V <sub>DHV</sub> _ = +3V,	V <sub>DLV</sub> = 0V		1		ps/°C
Propagation Delay Match, t <sub>LH</sub> vs. t <sub>HL</sub>		$V_{DHV_{-}} = +3V,$	V <sub>DLV</sub> _ = 0V		70		ps
Propagation Delay Skew, Drivers Within Package		V <sub>DHV</sub> _ = +3V,			100		ps
Propagation Delay Change		Relative to	3V <sub>P-P</sub> , 40MHz, PW = 4ns to 21ns		±40		
vs. Pulse Width		12.5ns pulse	1V <sub>P-P</sub> , 40MHz, PW = 2.5ns to 22.5ns		±90		- ps
Propagation Delay Change vs. Common-Mode Voltage		$1V_{P-P}$ , $V_{DLV}$ = 0V to +3V, relative to delay at $V_{DLV}$ = +1V			±80		ps
Propagation Delay, Drive to High Impedance, High Impedance to Drive		$V_{DHV_{-}}$ = +1.5V, $V_{DLV_{-}}$ = -1V, average of both directions of $t_{LH}$ and $t_{HL}$			3.9		ns
Minimum Voltage Swing		(Note 7)			100		mV

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **ELECTRICAL CHARACTERISTICS (continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		V <sub>DHV</sub> = +0.2V, V <sub>DLV</sub> = 0V, 20% to 80%		0.8		
		V <sub>DHV</sub> = +1V, V <sub>DLV</sub> = 0, 20% to 80%		0.8		
Rise/Fall Time		V <sub>DHV</sub> = +3V, V <sub>DLV</sub> = 0V, 10% to 90%	1.4	2.0	2.7	
(Average Rise/Fall Time)		$V_{DHV_{-}} = +4V, V_{DLV_{-}} = 0V,$ $R_{DUT_{-}} = 500\Omega, 10\% \text{ to } 90\%$		2.5		ns
		$V_{DHV_{-}} = +5V, V_{DLV_{-}} = 0V,$ $R_{DUT_{-}} = 500\Omega, 10\% \text{ to } 90\%$		3.1		
		V <sub>DHV</sub> _ = +0.2V		±50		
Rise/Fall Time Matching		$V_{DHV} = +1V$ $V_{DLV} = 0V$		±15		%
		V <sub>DHV</sub> _ = +3V and +5V		±5		
Minimum Pulse Width		$0.2V_{P-P}, V_{DHV} = +0.2V, V_{DLV} = 0V$		1.8		
(Average Positive/Negative Pulse)		$1V_{P-P}, V_{DHV} = +1V, V_{DLV} = 0V$		2.0		ns
(Note 8)		$3V_{P-P}, V_{DHV} = +3V, V_{DLV} = 0V$		2.6		
COMPARATOR (driver in high-impe	dance mod	e) (Note 9)				
DC CHARACTERISTICS						
Input Voltage Range			-1.0		+5.2	V
Differential Input Voltage		V <sub>DUT_</sub> - V <sub>CHV_</sub> , V <sub>DUT_</sub> - V <sub>CLV_</sub>	-6.2		+6.2	V
Hysteresis		V <sub>CHV</sub> = V <sub>CLV</sub> = +1.5V		8		mV
Input Offset Voltage		V <sub>DUT</sub> = +1.5V, V <sub>COMPHI</sub> = +0.8V, V <sub>COMPLO</sub> = +0.2V (Note 10)			±10	mV
Input Offset Temperature Coefficient		(Note 10)		±25		μV/°C
Common-Mode Rejection Ratio	CMRR	V <sub>DUT</sub> _ = 0V and +3V (Note 10)	60			dB
Linearity Error		V <sub>DUT</sub> _ = +1.5V (Notes 3, 10)			±5	mV
Linearity Error		V <sub>DUT</sub> _ = -1V, +5.2V (Notes 3, 10)			±10	IIIV
Power-Supply Rejection Ratio	PSRR	V <sub>DUT</sub> = +1.5V, V <sub>DD</sub> , V <sub>SS</sub> , V <sub>DDSW</sub> , V <sub>SSSW</sub> supplies independently varied over full range (Note 10)			±5	mV/V
AC CHARACTERISTICS (Note 11)						
Equivalent Input Bandwidth		$V_{DLV}$ = 0V termination mode, $V_{DUT}$ = 1 $V_{P-P}$ , $t_{R}$ = $t_{F}$ = 500ps input, calculated from 10% to 90% redigitization waveform		300		MHz
Prop Delay		$V_{DUT}$ = 1 $V_{P-P}$ , $V_{CHV}$ or $V_{CLV}$ = +0.5 $V$	1.1	2.0	3.3	ns
Prop-Delay Temperature Coefficient		$V_{DUT}$ = 1 $V_{P-P}$ , $V_{CHV}$ or $V_{CLV}$ = +0.5 $V$		2		ps/°C
Prop-Delay Match, t <sub>LH</sub> to t <sub>HL</sub>		Absolute value of delta for each comparator, V <sub>DUT</sub> = 1V <sub>P-P</sub>		±250		ps

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{DD}=+8V,\,V_{SS}=-5V,\,V_{L}=+3V,\,V_{DDSW}=+24.6V,\,V_{SSSW}=-1.25V,\,V_{COMPHI}=+1V,\,V_{COMPLO}=0V,\,V_{LDV}=0V,\,LOAD\,EN\,LOW_=LOAD\,EN\,HIGH_=0,\,SWEN=1,\,T_{J}=+70^{\circ}C$  with an accuracy of  $\pm 15^{\circ}C$ . Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^{\circ}\text{C}$  to  $+90^{\circ}\text{C}$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prop-Delay Skew, Comparators Within Package		Same edges (LH and HL), V <sub>DUT</sub> _ = 1V <sub>P-P</sub>		±100		ps
Prop-Delay Dispersions vs.		$V_{CHV}$ or $V_{CLV}$ = 0 to +4.9V, $V_{DUT}$ = 0.2V <sub>P-P</sub>		±20		ps
Common-Mode Voltage (Note 12)		$V_{CHV}$ or $V_{CLV}$ = -0.9 to +4.9V, $V_{DUT}$ = 0.2V <sub>P-P</sub>		±30		μο
Prop-Delay Dispersions vs. Overdrive		$V_{DLV\_}$ = 0V termination mode, $V_{DUT\_}$ = 1V <sub>P-P</sub> , t <sub>R</sub> = t <sub>F</sub> = 500ps input, 90% (rising edge) and 10% (falling edge) relative to timing at 50% point		±600		ps
Prop-Delay Dispersions vs. Pulse Width		2ns to 23ns pulse width, relative to 12.5ns pulse width		±60		ps
Prop-Delay Dispersions vs. Slew Rate		+0.5V/ns to +2V/ns		±50		ps
LOGIC INPUTS AND OUTPUTS (COI	<b>ИРНІ, СОМ</b>	PLO, CMPH_, CMPL_, V <sub>BBO</sub> )				
Input Voltage Range, V <sub>COMPHI</sub> and V <sub>COMPLO</sub>			0		3.6	V
Differential Input Voltage, VCOMPHI - VCOMPLO		V <sub>COMPHI</sub> ≥ V <sub>COMPLO</sub> , CMPH_ and CMPL_ with no load	0		3.6	V
Differential Input Voltage, VCOMPHI - VCOMPLO		$V_{COMPHI} \ge V_{COMPLO}$ , CMPH_ and CMPL_ with $50\Omega$ to $V_{TTCMP}$ , $V_{COMPHI} \ge V_{TTCMP} \ge V_{COMPLO}$	0		1.0	V
Reference Output, V <sub>BBO</sub>		Relative to (V <sub>COMPHI</sub> + V <sub>COMPLO</sub> )/2 at V <sub>COMPHI</sub> = +1V and V <sub>COMPLO</sub> = 0V			±50	mV
Output High-Voltage Offset		I <sub>OUT</sub> = 0mA, relative to V <sub>COMPHI</sub> at V <sub>COMPHI</sub> = +1V			±65	mV
Output Low-Voltage Offset		I <sub>OUT</sub> = 0mA, relative to V <sub>COMPLO</sub> at V <sub>COMPLO</sub> = 0V			±65	mV
Output Resistance, CMPH_ and CMPL_		I <sub>CMPH</sub> _ = I <sub>CMPL</sub> _ = ±10mA, V <sub>COMPHI</sub> = +1V, V <sub>COMPLO</sub> = 0V, CMPH_, CMPL_ at high-level output	40	50	60	Ω
Maximum Current Limit, CMPH_ and CMPL_		V <sub>COMPHI</sub> = +1.8V, V <sub>COMPLO</sub> = 0V, CMPH_, CMPL_ at high-level output, V <sub>FORCE</sub> = 0V, +3.6V	-15		+15	mA
Maximum Current Limit, V <sub>BBO</sub>		$V_{COMPHI} = +1V$ , $V_{COMPLO} = 0V$ , at $V_{BBO} = +0.5V$ output	-1		+1	mA

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **ELECTRICAL CHARACTERISTICS (continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise/Fall Time, CMPH_ and CMPL_		20% to 80%, $V_{COMPHI}$ = +1V, $V_{COMPLO}$ = 0V, load = T-line, $50\Omega$ > 1ns, $50\Omega$ to GND		0.7		ns
PASSIVE LOAD (driver in high-imp	oedance mod	le) (Note 13)				
DC CHARACTERISTICS R <sub>DUT</sub> ≥ 1	<b>0M</b> $\Omega$ , unless	otherwise noted)				
LDV_ Voltage Range			-1.0		+5.2	V
Gain		Measured at 0V and +3V	0.99		1.01	V/V
Gain Temperature Coefficient		Measured at 0V and +3V		50		ppm/°C
Offset		V <sub>LDV</sub> = +1.5V			±100	mV
Offset Temperature Coefficient				0.02		mV/°C
Dawer Cumply Delegation Datio	PSRR	$V_{DD}$ and $V_{SS}$ independently varied over full range, $V_{LDV} = +1.5V$	-18		+18	mV/V
Power-Supply Rejection Ratio	PSRR	V <sub>DDSW</sub> and V <sub>SSSW</sub> independently varied over full range, V <sub>LDV</sub> = +1.5V	-10		+10	mV/V
Output Resistance Tolerance— High Value		I <sub>DUT_</sub> = ±2mA, V <sub>LDV_</sub> = +1.5V	710	750	790	Ω
Output Resistance Tolerance— Low Value		I <sub>DUT_</sub> = ±4mA, V <sub>LDV_</sub> = +1.5V	335	375	415	Ω
Output Resistance, Tolerance— High Value (V <sub>DDSW</sub> = +15V)		I <sub>DUT_</sub> = ±2mA, V <sub>LDV_</sub> = +1.5V	735	800	865	Ω
Output Resistance, Tolerance— Low Value (V <sub>DDSW</sub> = +15V)		I <sub>DUT_</sub> = ±4mA, V <sub>LDV_</sub> = +1.5V	360	425	490	Ω
0.31.0		0 to +3V (relative to +1.5V)		±10		0/
Switch Resistance Variation		Full range (relative to +1.5V)		±30		- %
Switch Resistance Variation		0 to +3V (relative to +1.5V)		±10		0/
$(V_{DDSW} = +15V)$		Full range (relative to +1.5V)		±30		- %
M : 0 + 10 - 1		V <sub>LDV</sub> = -1V, V <sub>DUT</sub> = +5V	-4			
Maximum Output Current		V <sub>LDV</sub> _ = +5V, V <sub>DUT</sub> _ = -1V			+4	- mA
Linearity Error, Full Range		Measured at -1V, +1.5V, and +5.2V (Notes 3, 14)			±25	mV
AC CHARACTERISTICS					-	
Settling Time, LDV_ to Output		$V_{LDV}$ = -1V to +5V step, $R_{DUT}$ = 100k $\Omega$ (Note 15)		0.5		μs
Output Transient Response		$V_{LDV}$ = +1.5V, $V_{DUT}$ = -1V to +5V square wave at 1MHz, $R_{DUT}$ = 50k $\Omega$		20		ns



## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **ELECTRICAL CHARACTERISTICS (continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
PMU SWITCHES (FORCE, SENSE, PI	MU_) (Note	13)					
Voltage Range			-1.0		+24	V	
Voltage Range (V <sub>DDSW</sub> = +15V)			-1.0		+10	V	
Force Switch Resistance		V <sub>FORCE</sub> = +1.5V, I <sub>PMU</sub> = ±10mA			40	Ω	
Force Switch Resistance (V <sub>DDSW</sub> = +15V)		V <sub>FORCE</sub> = +1.5V, I <sub>PMU</sub> = ±10mA			47	Ω	
Force Path Current		V <sub>PMU</sub> = -1V to +24V, V <sub>FORCE</sub> = -1V to +24V			±30	mA	
Force Path Current (V <sub>DDSW</sub> = +15V)		V <sub>PMU</sub> = -1V to +10V, V <sub>FORCE</sub> = -1V to +10V			±30	mA	
Force Christop Decistors of Veriation		0V to +3V (relative to V <sub>FORCE</sub> = +1.5V)		±10		0/	
Force Switch Resistance Variation		Full range (Note 16)		±40		- %	
Force Switch Resistance Variation		0V to +3V (relative to V <sub>FORCE</sub> = +1.5V)		±15		- %	
$(V_{DDSW} = +15V)$		Full range (Note 16)		±45			
Sense Switch Resistance		V <sub>SENSE</sub> = +1.5V, I <sub>PMU</sub> = ±0.4mA	650	1000	1350	Ω	
Sense Switch Resistance (V <sub>DDSW</sub> = +15V)		V <sub>SENSE</sub> = +1.5V, I <sub>PMU</sub> = ±0.4mA	850	1250	1800	Ω	
Sense Switch Resistance Variation		Relative to +11.5V, full range		±40		%	
Sense Switch Resistance Variation (V <sub>DDSW</sub> = +15V)		Relative to +4.5V, full range		±40		%	
PMU_ Capacitance		Force and sense switches open		6		рF	
FORCE Capacitance		All channels of force and sense switches open		36		pF	
SENSE Capacitance		All channels of force and sense switches open		8		pF	
FORCE External Capacitance		Allowable external capacitance		2		nF	
SENSE External Capacitance		Allowable external capacitance		1		nF	
FOROE and OFNICE Cuitable of Canada		Connect, PMU_ = +5V, FORCE or SENSE $10M\Omega$ II 8pF		10			
FORCE and SENSE Switching Speed		Disconnect, PMU_ = +5V, FORCE or SENSE 10MΩ II 8pF		100		– µs	
PMU_ Leakage		SWEN = 0, or PMU EN_ = 0, VFORCE_ = VSENSE_ = -1V to +24V		±0.5	±5	nA	
PMU_ Leakage (V <sub>DDSW</sub> = +15V)		SWEN = 0, or PMU EN_ = 0, VFORCE_ = VSENSE_ = -1V to +10V		±0.5	±5	nA	



## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **ELECTRICAL CHARACTERISTICS (continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN T	YP MAX	UNITS
TOTAL FUNCTION	-1				
DUT_					
Leakage, High-Impedance Mode		Passive load switches open, pin switch short, V <sub>DUT</sub> = +5.2V, V <sub>CLV</sub> = V <sub>CHV</sub> = -1V, V <sub>DUT</sub> = -1V, V <sub>CLV</sub> = V <sub>CHV</sub> = +5.2V, full range		2	μΑ
Low-Leakage Recovery Time		Confirmed simulation only (Note 17)		10	μs
Combined Capacitance		High-impedance mode, passive load switches open, pin switch short		10	рF
Load Resistance Range		(Note 18)		1	GΩ
Load Capacitance Range		(Note 18)		12	nF
Leakage, Pin Switch Off Mode		-1V to +24V, pin switch open		±1 ±10	nA
Leakage, Pin Switch Off Mode (V <sub>DDSW</sub> = +15V)		-1V to +10V, pin switch open		±1 ±10	nA
Pin Switch Switching Speed		Connect or disconnect, $V_{DH_{-}} = +5V$ , $DUT_{-} = 10M\Omega$    8pF		10	μs
VOLTAGE REFERENCE INPUTS (D	HV_, DLV_,	CHV_, CLV_, LDV_, COMPHI, COMPLO)			
Input Bias Current				±100	μΑ
SINGLE-ENDED CONTROL INPUTS	(DATA_, RO	CV_)			
Input High Voltage			V <sub>BBI</sub> + 0.2	3.2	V
Input Low Voltage			0	V <sub>BBI</sub> - 0.2	V
Voltage Between Inputs and V <sub>BBI</sub>			V <sub>BBI</sub> - 1.6	V <sub>BBI</sub> + 1.6	V
Input Offset Voltage				±50	mV
Input Bias Current				±100	μΑ
REFERENCE INPUT (V <sub>BBI</sub> )					
Input Voltage Range			0.2	3.0	V
Input Bias Current				±100	μΑ
DIGITAL INPUTS (LD, DIN, SCLK, C	S)				
Input High Voltage		(Note 19)	2/3 (V <sub>L</sub> )	$V_{L}$	V
Input Low Voltage		(Note 19)	-0.1	1/3 (V <sub>L</sub> )	V
Input Bias Current				±1	μΑ
SERIAL-DATA OUTPUT (DOUT)					
Output High Voltage		I <sub>OH</sub> = -1mA	V <sub>L</sub> - 0.4	V <sub>L</sub> + 0.1	V
Output Low Voltage		$I_{OL} = +1mA$	V <sub>DGND</sub> - 0.1	V <sub>DGND</sub> + 0.4	V
Output Rise-and-Fall Time		$C_L = 10pF$	į	5.0	ns

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **ELECTRICAL CHARACTERISTICS (continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Low to DOUT Delay		$C_L = 10pF$	4		45	ns
SERIAL-INTERFACE TIMING	<u>'</u>		'			
SCLK Frequency					20	MHz
SCLK Pulse-Width High	t <sub>CH</sub>		20			ns
SCLK Pulse-Width Low	t <sub>CL</sub>		20			ns
CS Low to SCLK High Setup	t <sub>CSS0</sub>		5		-	ns
SCLK High to CS Low Hold	t <sub>CSH0</sub>		0			ns
CS High to SCLK High Setup	t <sub>CSS1</sub>		20			ns
SCLK High to CS High Hold	t <sub>CSH1</sub>		20			ns
DIN to SCLK High Setup	t <sub>DS</sub>		10			ns
DIN to SCLK High Hold	t <sub>DH</sub>		10			ns
CS High to LD Low Hold	tcshld		20			ns
CS High Pulse Width	tcswh		20			ns
LD Low Pulse Width	t <sub>LDW</sub>		20			ns
V <sub>L</sub> Rising to $\overline{\text{CS}}$ Low		Power-on delay		2		μs
TEMPERATURE SENSOR						
Nominal Voltage		$T_J = +70^{\circ}C, R_L \ge 10M\Omega$		3.43		V
Temperature Coefficient				+10		mV/°C
Output Resistance				17		kΩ
POWER SUPPLIES	·					
Positive Supply Voltage	V <sub>DD</sub>	(Note 20)	7.6	8	8.4	V
Negative Supply Voltage	V <sub>SS</sub>	(Note 20)	-5.25	-5	-4.75	V
Logic Supply Voltage	VL		2.3	3	3.6	V
Switch Positive Supply Voltage	V <sub>DDSW</sub>	(Notes 20, 21)	24.1	24.6	25.1	V
Switch Positive Supply Voltage	V <sub>DDSW</sub>	(Notes 20, 22)	14.5	15	15.5	V
Switch Negative Supply Voltage	V <sub>SSSW</sub>	(Note 20)	-1.4	-1.25	-1.1	V
Positive Supply Current	I <sub>DD</sub>	$f_{OUT} = OMHz$		105	120	mA
Negative Supply Current	I <sub>SS</sub>	$f_{OUT} = OMHz$		105	120	mA
Logic Supply Current	IL	f <sub>OUT</sub> = 0MHz		1	4	mA
Switch Positive Supply Current	I <sub>DDSW</sub>	f <sub>OUT</sub> = 0MHz		2	6	mA
Switch Negative Supply Current	I <sub>SSSW</sub>	f <sub>OUT</sub> = 0MHz		1.5	5	mA
Static Power Dissipation		f <sub>OUT</sub> = 0MHz		1.35	1.56	W
Operating Power Dissipation		f <sub>OUT</sub> = 100Mbps (Note 23)		1.45		W

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

#### **ELECTRICAL CHARACTERISTICS (continued)**

(VDD = +8V, VSS = -5V, VL = +3V, VDDSW = +24.6V, VSSW = -1.25V, VCOMPHI = +1V, VCOMPLO = 0V, VLDV = 0V, LOAD EN LOW\_ = LOAD EN HIGH\_ = 0, SWEN = 1, T<sub>.I</sub> = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^{\circ}\text{C}$  to  $+90^{\circ}\text{C}$ , unless otherwise noted.) (Note 1)

- All minimum and maximum DC, rise/fall time at +3V swing tests are 100% production tested. The propagation-delay data to output and propagation-delay comparator tests are guaranteed by design. All specifications are with DUT\_ and PMU\_ electrically isolated, unless otherwise noted.
- Resistance measurements are made using ±2.5mA current changes in the loading instrument about the noted value. Note 2: Absolute value of the difference in measured resistance over the specified range, tested separately for each current polarity. Test conditions are at IDUT =  $\pm 1$ mA,  $\pm 12$ mA, and  $\pm 40$ mA, respectively.
- Relative to a straight line through 0V and +3V. Note 3:
- V<sub>DHV</sub> = +3V, V<sub>DLV</sub> = 0V, unless otherwise specified. DATA\_ and RCV\_V<sub>HIGH</sub> = +2V, V<sub>LOW</sub> = 1V, V<sub>BBI</sub> = +1.5V.
- Note 5: Current supplied for a minimum of 10ns. Verified to be greater than or equal to DC drive current by design and characterization.
- Note 6: Undershoot is any reflection of the signal back towards its starting voltage after it has reached 90% of its swing. Preshoot is any aberration in the signal before it reaches 10% of its swing.
- Note 7: At the minimum voltage swing, undershoot is less than 20%. DHV\_ and DLV\_ references are adjusted to result in the specified swing
- At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at Note 8:
- With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.
- Note 10: Measured by using a servo to locate comparator thresholds.
- Note 11: Unless otherwise noted, all propagation delays are measured at 40MHz, V<sub>DUT</sub> = 0 to +1V, V<sub>CHV</sub> = V<sub>CLV</sub> = +0.5V,  $t_{\rm R}=t_{\rm F}=500{\rm ps},\,Z_{\rm S}=50\Omega,\,$  driver in high-impedance mode. Comparator outputs are terminated with  $50\Omega$  to GND. Measured from V<sub>DUT</sub> crossing calibrated CHV\_/CLV\_ threshold to midpoint of nominal comparator output swing.
- **Note 12:**  $V_{DUT} = 200 \text{mV}_{P-P}$ . Propagation delay is compared to a reference time at +2V.
- Note 13: Operating output voltage/current range of passive load and PMU force switch at +24.6V supply. See Figure 1.
- Note 14: LOAD EN LOW\_ = LOAD EN HIGH\_ = 1.
- **Note 15:** Waveform settles to within 5% of final value into  $100k\Omega$  load.
- Note 16: I<sub>PMU</sub> = ±2mA at V<sub>FORCF</sub> = -1V, +11.5V, and +24V. Percent variation relative to value calculated at V<sub>FORCF</sub> = +11.5V.
- Note 17: Time to return to the specified maximum leakage after a +3V, +4V/ns step at DUT\_.
- Note 18: Load at end of 2ns transmission line; for stability only, AC performance could be degraded.
- Note 19: The driver meets all of its timing specifications at the specified digital input voltages.
- Note 20: Specifications are simulated and characterized over the full power-supply range. Production tests are performed with power supplies at typical values.
- Note 21: DUT\_ (pin switch off), PMU\_ maximum voltage is +24V.
- Note 22: DUT\_ (pin switch off), PMU\_ maximum voltage is +10V.
- **Note 23:** All channels driven at  $3V_{P-P}$ , load = 2ns,  $50\Omega$  transmission line terminated with 3pF.

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

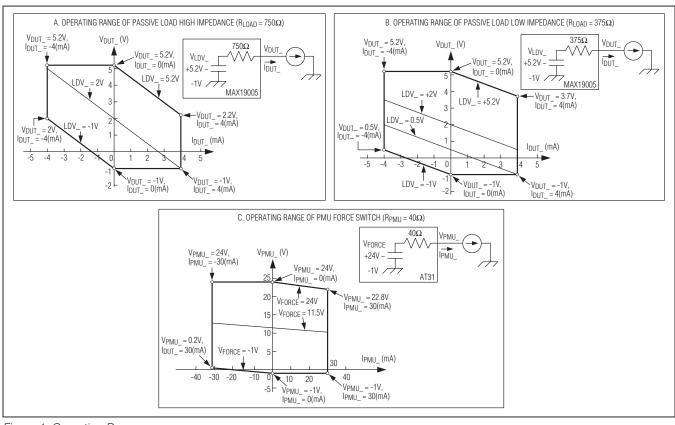
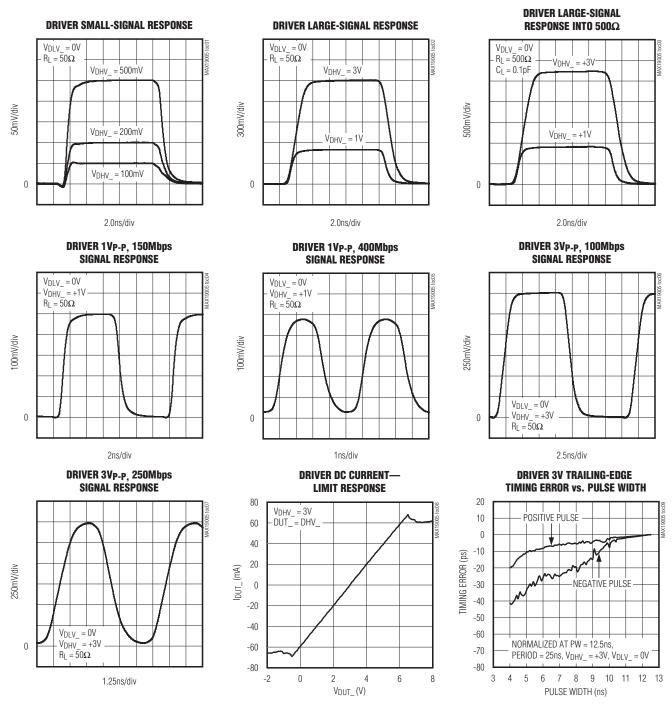


Figure 1. Operating Ranges

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

### **Typical Operating Characteristics**

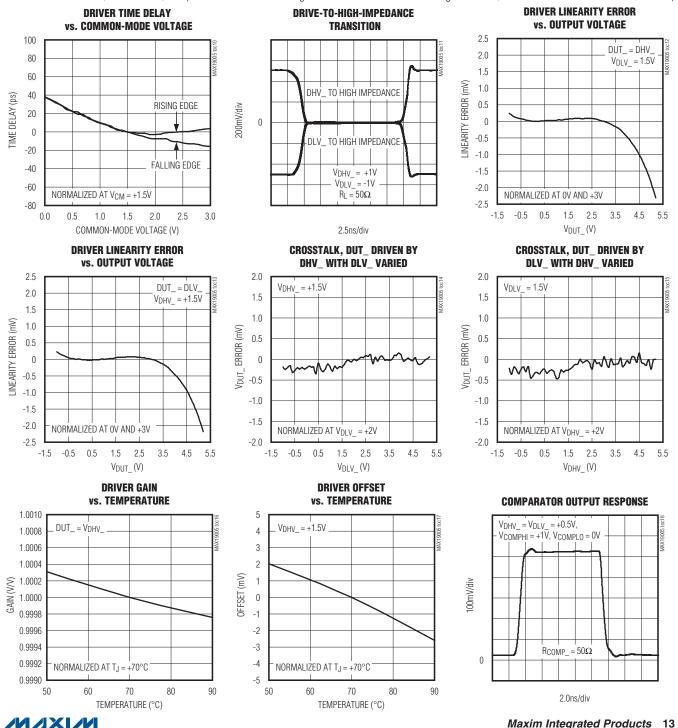
 $(V_{DD}=8V,\ V_{SS}=-5V,\ V_L=3V,\ V_{DDSW}=24.6V,\ V_{SSSW}=1.25V,\ V_{COMPHI}=1V,\ V_{COMPLO}=0V,\ V_{LDV}=0V,\ LOAD\ EN\ LOW=LOAD\ EN\ HIGH=0,\ SWEN=1,\ temperature\ coefficients\ T_J=+70^{\circ}C\ are\ measured\ at\ T_J=+50^{\circ}C\ to\ +90^{\circ}C,\ unless\ otherwise\ noted.)$ 



## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

### Typical Operating Characteristics (continued)

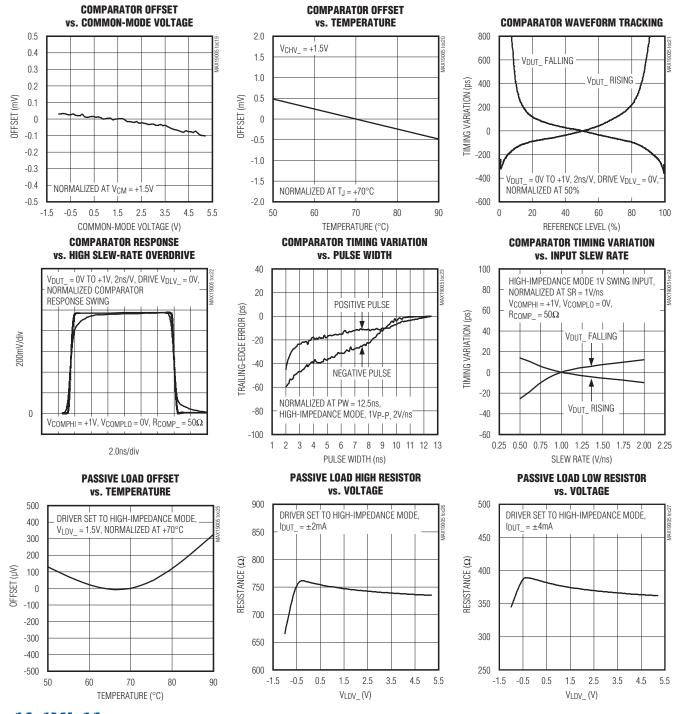
 $(V_{DD}=8V,\ V_{SS}=-5V,\ V_L=3V,\ V_{DDSW}=24.6V,\ V_{SSSW}=1.25V,\ V_{COMPHI}=1V,\ V_{COMPLO}=0V,\ V_{LDV}=0V,\ LOAD\ EN\ LOW=LOAD\ EN\ HIGH=0,\ SWEN=1,\ temperature\ coefficients\ T_J=+70^{\circ}C\ are\ measured\ at\ T_J=+50^{\circ}C,\ to\ +90^{\circ}C\ unless\ otherwise\ noted.)$ 



## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

## Typical Operating Characteristics (continued)

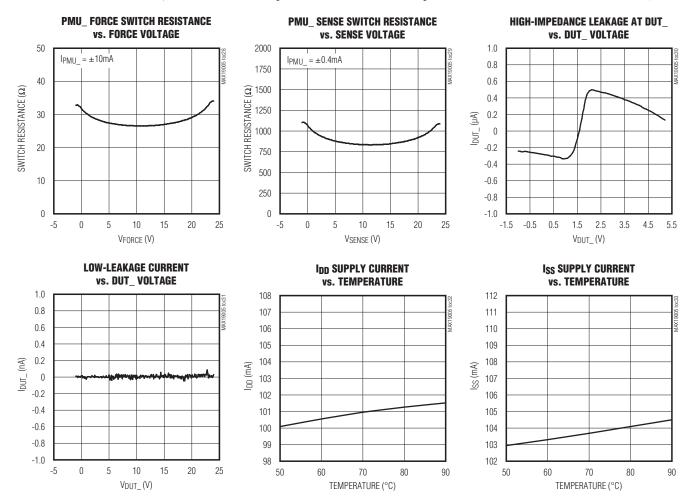
 $(V_{DD} = 8V, V_{SS} = -5V, V_{L} = 3V, V_{DDSW} = 24.6V, V_{SSSW} = 1.25V, V_{COMPHI} = 1V, V_{COMPLO} = 0V, V_{LDV} = 0V, LOAD EN LOW = 1.25V, V_{COMPHI} = 1V, V_{COMPLO} = 0V, V_{LDV} = 0V, V_{$ LOAD EN HIGH = 0, SWEN = 1, temperature coefficients  $T_{J} = +70^{\circ}\text{C}$  are measured at  $T_{J} = +50^{\circ}\text{C}$ , to  $+90^{\circ}\text{C}$  unless otherwise noted.)



## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

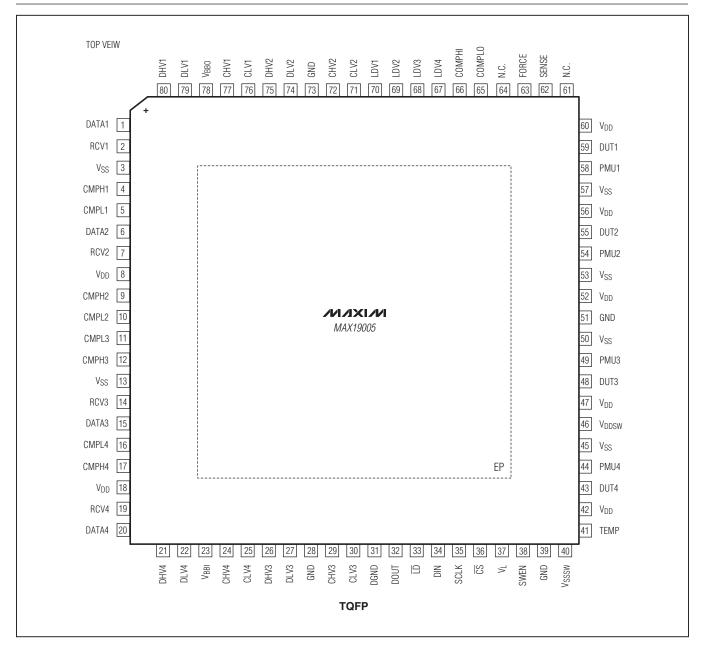
### **Typical Operating Characteristics (continued)**

 $(V_{DD} = 8V, V_{SS} = -5V, V_{L} = 3V, V_{DDSW} = 24.6V, V_{SSSW} = 1.25V, V_{COMPHI} = 1V, V_{COMPLO} = 0V, V_{LDV} = 0V, LOAD EN LOW = LOAD EN HIGH = 0, SWEN = 1, temperature coefficients <math>T_{J} = +70^{\circ}C$  are measured at  $T_{J} = +50^{\circ}C$ , to  $+90^{\circ}C$  unless otherwise noted.)



## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

## **Pin Configuration**



## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

## **Pin Description**

PIN	NAME	FUNCTION
1	DATA1	Channel 1 Multiplexer Control Input. Selects the driver 1 input from DHV1 or DLV1 in drive mode. See Table 1 and Figure 2.
2	RCV1	Channel 1 Multiplexer Control Input. Sets the channel 1 mode to drive or receive. See Table 1 and Figure 2.
3, 13, 45, 50, 53, 57	V <sub>SS</sub>	Negative Power-Supply Input
4	CMPH1	Channel 1 High-Side Comparator Output
5	CMPL1	Channel 1 Low-Side Comparator Output
6	DATA2	Channel 2 Multiplexer Control Input. Selects the driver 2 input from DHV2 or DLV2 in drive mode. See Table 1 and Figure 2.
7	RCV2	Channel 2 Multiplexer Control Input. Sets the channel 2 mode to drive or receive. See Table 1 and Figure 2.
8, 18, 42, 47, 52, 56, 60	V <sub>DD</sub>	Positive Power-Supply Input
9	CMPH2	Channel 2 High-Side Comparator Output
10	CMPL2	Channel 2 Low-Side Comparator Output
11	CMPL3	Channel 3 Low-Side Comparator Output
12	CMPH3	Channel 3 High-Side Comparator Output
14	RCV3	Channel 3 Multiplexer Control Input. Sets the channel 3 mode to drive or receive. See Table 1 and Figure 2.
15	DATA3	Channel 3 Multiplexer Control Input. Selects the driver 3 input from DHV3 or DLV3 in drive mode. See Table 1 and Figure 2.
16	CMPL4	Channel 4 Low-Side Comparator Output
17	CMPH4	Channel 4 High-Side Comparator Output
19	RCV4	Channel 4 Multiplexer Control Input. Sets the channel 4 mode to drive or receive. See Table 1 and Figure 2.
20	DATA4	Channel 4 Multiplexer Control Input. Selects driver 4 input from DHV4 or DLV4 in drive mode. See Table 1 and Figure 2.
21	DHV4	Channel 4 Driver High-Voltage Input
22	DLV4	Channel 4 Driver Low-Voltage Input
23	V <sub>BBI</sub>	DATA_/RCV_ Threshold Voltage Input
24	CHV4	Channel 4 High-Side Comparator Threshold Voltage Input
25	CLV4	Channel 4 Low-Side Comparator Threshold Voltage Input
26	DHV3	Channel 3 Driver High-Voltage Input
27	DLV3	Channel 3 Driver Low-Voltage Input
28, 39, 51, 73	GND	Analog Ground
29	CHV3	Channel 3 High-Side Comparator Threshold Voltage Input
30	CLV3	Channel 3 Low-Side Comparator Threshold Voltage Input
31	DGND	Digital Ground Connection

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

## **Pin Description (continued)**

PIN	NAME	FUNCTION
32	DOUT	Serial-Interface Data Output
33	ĪD	Load Input. Latches data from the serial input register to the control register on rising edge.  Transparent when low.
34	DIN	Serial-Interface Data Input
35	SCLK	Serial Clock
36	CS	Chip Select
37	VL	Logic Power-Supply Input
38	SWEN	PMU Switch and Pin Switch Enable Input
40	V <sub>SSSW</sub>	PMU Switch and Pin Switch Negative Power-Supply Input
41	TEMP	Temperature Sensor Output
43	DUT4	Channel 4 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 4.
44	PMU4	Channel 4 Parametric Measurement Unit Connection. PMU switch I/O node for channel 4.
46	V <sub>DDSW</sub>	Positive PMU Switch and Pin Switch Power-Supply Input
48	DUT3	Channel 3 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 3.
49	PMU3	Channel 3 Parametric Measurement Unit Connection. PMU switch I/O node for channel 3.
54	PMU2	Channel 2 Parametric Measurement Unit Connection. PMU switch I/O node for channel 2.
55	DUT2	Channel 2 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 2.
58	PMU1	Channel 1 Parametric Measurement Unit Connection. PMU switch I/O node for channel 1.
59	DUT1	Channel 1 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 1.
61, 64	N.C.	No Connection. Not internally connected.
62	SENSE	PMU Sense Connection
63	FORCE	PMU Force Connection
65	COMPLO	Comparator Output Low-Voltage Reference Input
66	COMPHI	Comparator Output High-Voltage Reference Input
67	LDV4	Channel 4 Load Voltage Input
68	LDV3	Channel 3 Load Voltage Input
69	LDV2	Channel 2 Load Voltage Input
70	LDV1	Channel 1 Load Voltage Input
71	CLV2	Channel 2 Low-Side Comparator Threshold Voltage Input
72	CHV2	Channel 2 High-Side Comparator Threshold Voltage Input
74	DLV2	Channel 2 Driver Low-Voltage Input
75	DHV2	Channel 2 Driver High-Voltage Input
76	CLV1	Channel 1 Low-Side Comparator Threshold Voltage Input
77	CHV1	Channel 1 High-Side Comparator Threshold Voltage Input
78	V <sub>BBO</sub>	Comparator Output Threshold Voltage Output
79	DLV1	Channel 1 Driver Low-Voltage Input
80	DHV1	Channel 1 Driver High-Voltage Input
_	EP	Exposed Pad. Leave unconnected or connect to GND

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

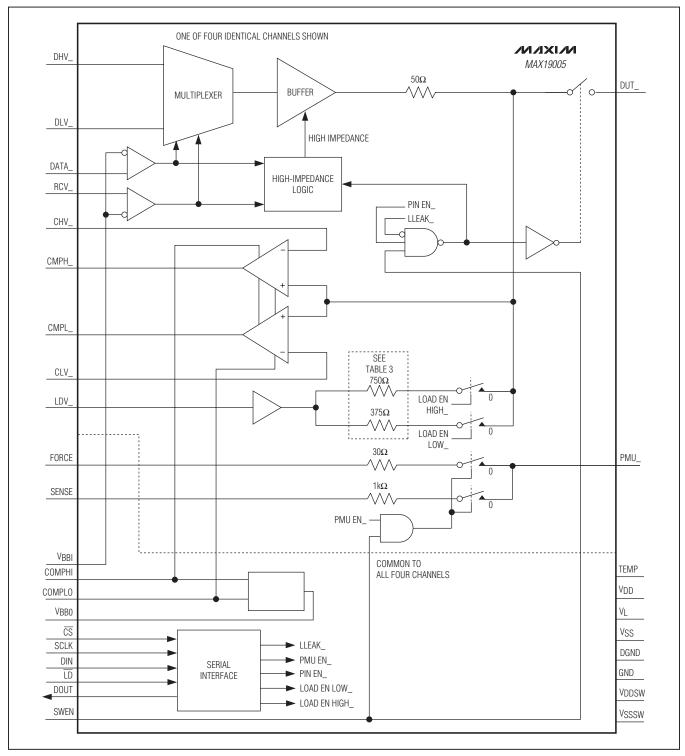


Figure 2. Block Diagram

## Quad, Ultra-Low-Power, **200Mbps ATE Drivers/Comparators**

### **Detailed Description**

The MAX19005 is a four-channel, ultra-low-power, pin-electronics IC for automated test equipment that includes, for each channel, a two-level pin driver, a window comparator, a passive load, and a Kelvin instrument connection (Figure 2). All functions feature a -1V to +5.2V operating range and the drivers include a highimpedance mode. The comparators feature programmable output voltages, allowing optimization for different CMOS interface standards. The loads have selectable output resistance for optimizing DUT\_ current loading. The Kelvin paths allow accurate connection of an instrument with ±25mA source/sink capability. Additionally, the IC offers a low-leakage mode that reduces DUT\_leakage current to less than 20nA.

Each of the four channels feature single-ended CMOScompatible inputs (DATA\_ and RCV\_) for control of the driver signal path (Figure 3). The IC mode operations

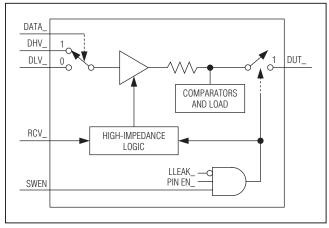


Figure 3. Multiplexer and Driver Channel

are programmed through a 3-wire, low-voltage CMOScompatible serial interface.

The driver input is a high-speed multiplexer that selects one of two voltage inputs: DHV\_ and DLV\_. This switching is controlled by high-speed inputs DATA\_ and RCV\_. DATA\_ and RCV\_ are single-ended inputs with threshold levels (VBBI). Each channel's threshold levels are independently buffered to minimize crosstalk.

DUT can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 3, Table 1). High-speed input RCV\_ and mode-control bit LLEAK\_ control these modes. In high-impedance mode, the bias current at DUT\_ is less than 2µA over the -1V to +5.2V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT is further reduced to less than 20nA, and signal tracking slows.

The nominal driver output resistance is  $49.5\Omega$ .

#### **Comparators**

The IC provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT\_ and the other input connected to either CHV\_ or CLV\_ (Figure 2). Comparator outputs are a logical result of the input conditions, as indicated in Table 2.

The comparator output voltages are easily interfaced to a wide variety of logic standards. Use buffered inputs COMPHI and COMPLO to set the high and low output voltages. For correct operation, COMPHI should be greater than or equal to COMPLO. The comparator  $50\Omega$  output impedance provides source termination (Figure 4). VBBO output voltage is provided, (COMPHI + COMPLO)/2.

Tab	le 1.	Con	npon	ent	List
-----	-------	-----	------	-----	------

EXTERN	EXTERNAL PIN CONNE		INTERNAL REGISTER CONTROL BITS		DRIVER STATUS	PIN SWITCH STATUS	
RCV_	DATA_	SWEN	PIN EN_	LLEAK_		SIAIUS	
0	0	1	1	0	DUT_ = DLV_	Short	
0	1	1	1	0	DUT_ = DHV_	Short	
1	X	1	1	0	High impedance	Short	
X	X	0	X	0	OV	Open	
X	X	Х	0	0	OV	Open	
X	X	Х	X	1	0V (low power)	Open	

X = Don't care.

## Quad, Ultra-Low-Power, **200Mbps ATE Drivers/Comparators**

**Table 2. Comparator Logic** 

COND	CMPH_	CMPL_	
DUT_ < CHV_	DUT_ < CLV_	0	0
DUT_ < CHV_	DUT_ > CLV_	0	1
DUT_ > CHV_	DUT_ < CLV_	1	0
DUT_ > CHV_	DUT_ > CLV_	1	1

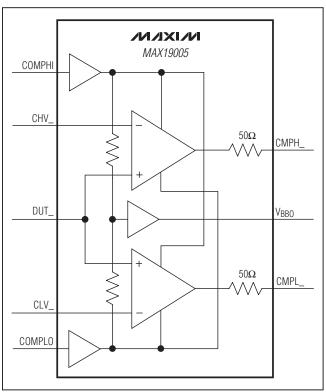


Figure 4. Complementary 50Ω Comparator Outputs

#### **Passive Load**

The IC channels each feature a passive load consisting of a buffered input voltage (LDV\_) connected to DUT\_ through two resistive paths (Figure 2). Each path connects to DUT\_ individually by a switch controlled through the serial interface. Programming options include none (load disconnected), either, or both paths connected. The loads facilitate fast open/short testing in conjunction with the comparator, and pullup of open-drain DUT\_ outputs. See Table 3.

**Table 3. Passive Load Logic** 

INTERNAL CO	ONTROL BITS	DACCIVE LOAD	
LOAD EN HIGH_	LOAD EN LOW_	PASSIVE LOAD STATUS	
0	0	Disconnect	
0	1	$375\Omega$ load connect	
1	0	750Ω load connect	
1	1	750Ω II 375Ω load connect	

**Table 4. PMU Switch Logic** 

EXTERNAL CONNECTION	INTERNAL CONTROL BIT	PMU SWITCH STATUS	
SWEN	PMU EN_	OTATOO	
0	X	Open	
1	0	Open	
1	1	Short	

X = Don't care

#### **Parametric Switches**

Each of the four IC channels provide force-and-sense paths for connection of a PMU or other DC resource to the device-under-test (Figure 2). Both force and sense switches are simultaneously controlled through the serial interface providing maximum application flexibility. PMU and DUT\_ are provided on separate pins, allowing designs that do not require the parametric switch feature to avoid the added capacitance of PMU. It also allows PMU\_ to connect to DUT\_, either directly or with an impedance-matching network. See Table 4.

#### Low-Leakage Mode (LLEAK\_)

Asserting LLEAK through the serial port places the IC into a very-low-leakage state. See the *Electrical* Characteristics section. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK\_ control is independent for each channel.

When DUT\_ is driven with a high-speed signal while LLEAK\_ is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the Electrical Characteristics section indicates device behavior under this condition.

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **Temperature Monitor**

Each device supplies a single temperature output signal (TEMP) that asserts a nominal +3.43V output voltage at a +70°C (343K) die temperature. The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is  $17k\Omega$  (typ).

#### **Serial Interface and Device Control**

A CMOS-compatible serial interface controls the IC modes (Figure 5). Control data flow into a 12-bit shift register (LSB first) and are latched when  $\overline{\text{CS}}$  is taken high. Data from the shift register are then loaded to the per-channel control latches, as determined by bits D[8:11] (Figure 5 and Table 5). The latches contain the five mode bits for each channel of the device. The mode bits, in conjunction with external inputs DATA and RCV\_, manage the features of each channel. Transfer data asynchronously from the input registers to the channel registers by forcing LD low. With LD always low, data transfer on the rising edge of  $\overline{CS}$ .

#### **Heat Removal**

With adequate airflow, no external heat sinking is needed under most operating conditions. If excess heat must be dissipated through the exposed pad, solder it to circuitboard copper. The exposed pad must be either left unconnected, isolated, or connected to GND.

#### **Power Minimization**

To minimize power consumption, activate only the needed channels. Each channel placed in low-leakage mode saves approximately 240mW.

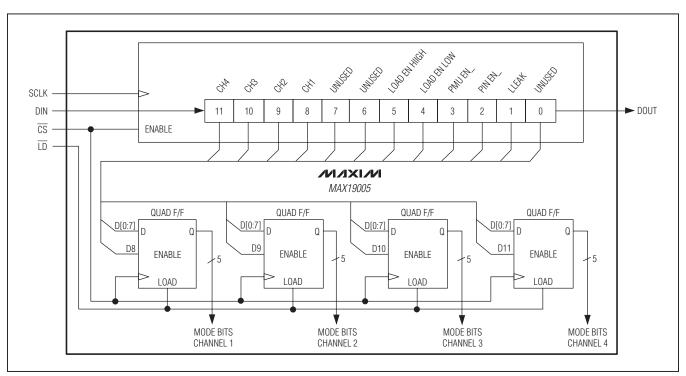


Figure 5. Serial Interface

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

**Table 5. Control Register Bits** 

BIT NAME		FUNCTION	BIT S	POWER-UP	
БП	INAIVIE	FUNCTION	0	1	STATE
D0	_	Unused	X	X	0
D1	LLEAK	Assert low-leakage mode	Active	Low leakage	0
D2	PIN EN	Enable pin switch	Disabled	Enabled	0
D3	PMU EN	Enable PMU switch	Disabled	Enabled	0
D4	LOAD EN LOW	Enable low load resistor	Disabled	Enabled	0
D5	LOAD EN HIGH	Enable high load resistor	Disabled	Enabled	0
D6	_	Unused	X	X	0
D7	_	Unused	X	X	0
D8	CH1	Update channel 1 control register	Disabled	Enabled	1
D9	CH2	Update channel 2 control register	Disabled	Enabled	1
D10	CH3	Update channel 3 control register	Disabled	Enabled	1
D11	CH4	Update channel 4 control register	Disabled	Enabled	1

X = Don't care.

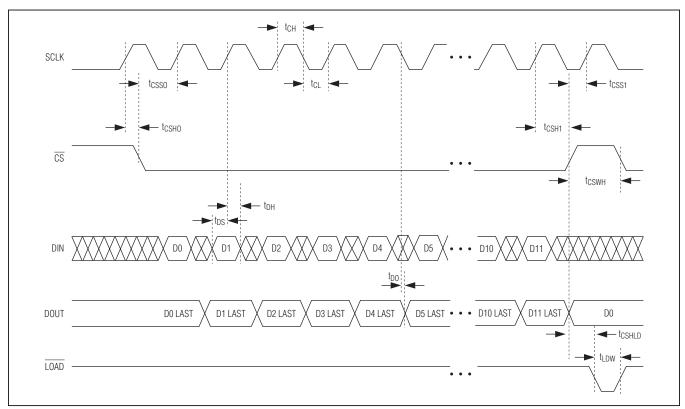


Figure 6. Serial-Interface Timing

## **Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators**

#### **Ordering Information**

PART	TEMP	PIN-	HEAT
	RANGE	PACKAGE	EXTRACTION
MAX19005CCS+	0°C to +70°C	80 TQFP-EP*	Bottom

<sup>+</sup>Denotes a lead(Pb)-free/RoHS-compliant package. \*EP = Exposed pad.

#### **Chip Information**

PROCESS: BICMOS

#### **Package Information**

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE	LAND
TYPE	CODE	NO.	PATTERN NO.
80 TQFP-EP	C80E+4	<u>21-0115</u>	<u>90-0152</u>

# Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

## **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	_

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

## **ПОСТАВКА** ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

## Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

#### http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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