Data Sheet August 24, 2006 FN2958.5

CMOS Asynchronous

The 82C50A Asynchronous Communication Element (ACE) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Using Intersil's advanced Scaled SAJI IV CMOS Process, the ACE will support data rates from DC to 625K baud (0-10MHz clock).

The ACE's receiver circuitry converts start, data, stop, and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity, and stop bits. The word length is programmable to 5, 6, 7, or 8 data bits. Stop bit selection provides a choice of 1,1.5, or 2 stop bits.

The Baud Rate Generator divides the clock by a divisor programmable from 1 to 2^{16}-1 to provide standard RS-232C baud rates when using any one of three industry standard baud rate crystals (1.8432MHz, 2.4576MHz, or 3.072MHz). A programmable buffered clock output (BAUDOUT) provides either a buffered oscillator or 16X (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals $\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, $\overline{DCD}$ are provided. Inputs and outputs have been designed with full TTL/CMOS compatibility in order to facilitate mixed TTL/NMOS/CMOS system design.

Features

- Single Chip UART/BRG
- DC to 625K Baud (DC to 10MHz Clock)
- Crystal or External Clock Input
- On Chip Baud Rate Generator 1 to 65535 Divisor Generates 16X Clock
- Prioritized Interrupt Mode
- Fully TTL/CMOS Compatible
- Microprocessor Bus Oriented Interface
- 80C86/80C88 Compatible
- Scaled SAJI IV CMOS Process
- Low Power - 1mA/MHz Typical
- Modem Interface
- Line Break Generation and Detection
- Loopback and Echo Modes
- Doubled Buffered Transmitter and Receiver
- Single 5V Supply
- Pb-Free Plus Anneal Available (RoHS Compliant)

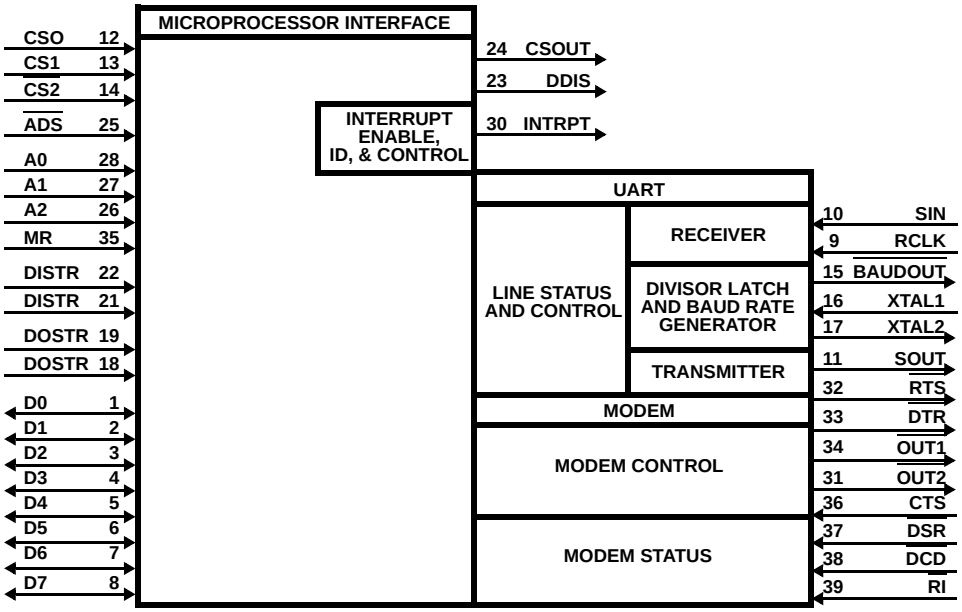
Ordering Information

625K BAUD	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
CP82C50A-5	CP82C50A-5	0 to +70	40 Ld PDIP	E40.6
CP82C50A-5Z (Note)	CP82C50A-5Z	0 to +70	40 Ld PDIP (Pb-free)	E40.6
CS82C50A-596	CS82C50A-5	0 to +70	44 Ld PLCC Tape and Reel	N44.65
CS82C50A-5Z (Note)	CS82C50A-5Z	0 to +70	44 Ld PLCC (Pb-free)	N44.65
CS82C50A-5Z96 (Note)	CS82C50A-5Z	0 to +70	44 Ld PLCC Tape and Reel (Pb-free)	N44.65
IS82C50A-5	IS82C50A-5	-40 to +85	44 Ld PLCC	N44.65
IS82C50A-5Z (Note)	IS82C50A-5Z	-40 to +85	44 Ld PLCC (Pb-free)	N44.65

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

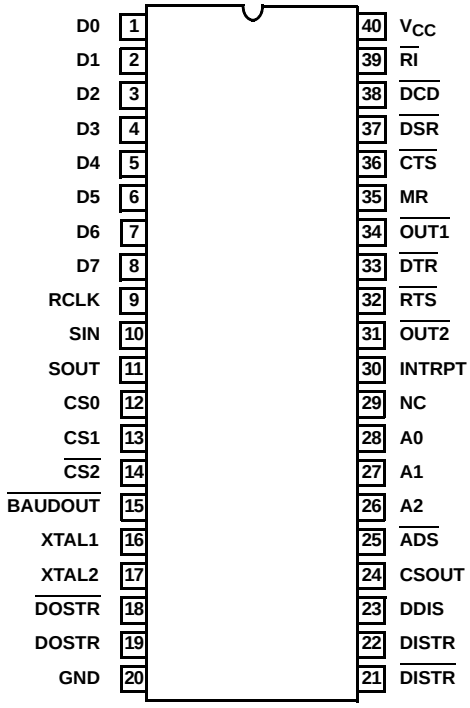
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Functional Diagram

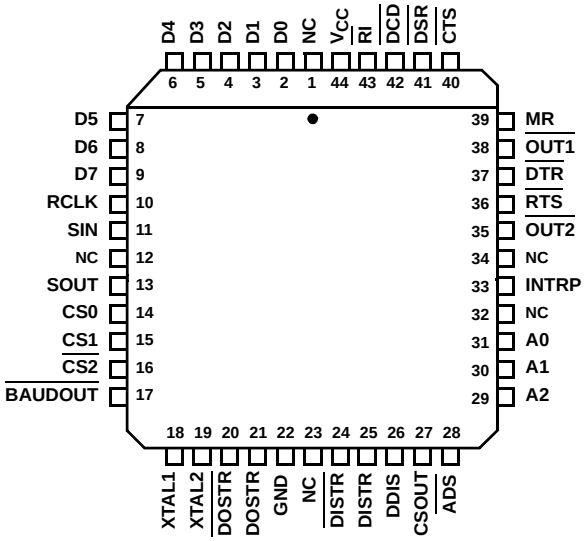


Pinout

82C50A (PDIP)
TOP VIEW



82C50A (PLCC)
TOP VIEW



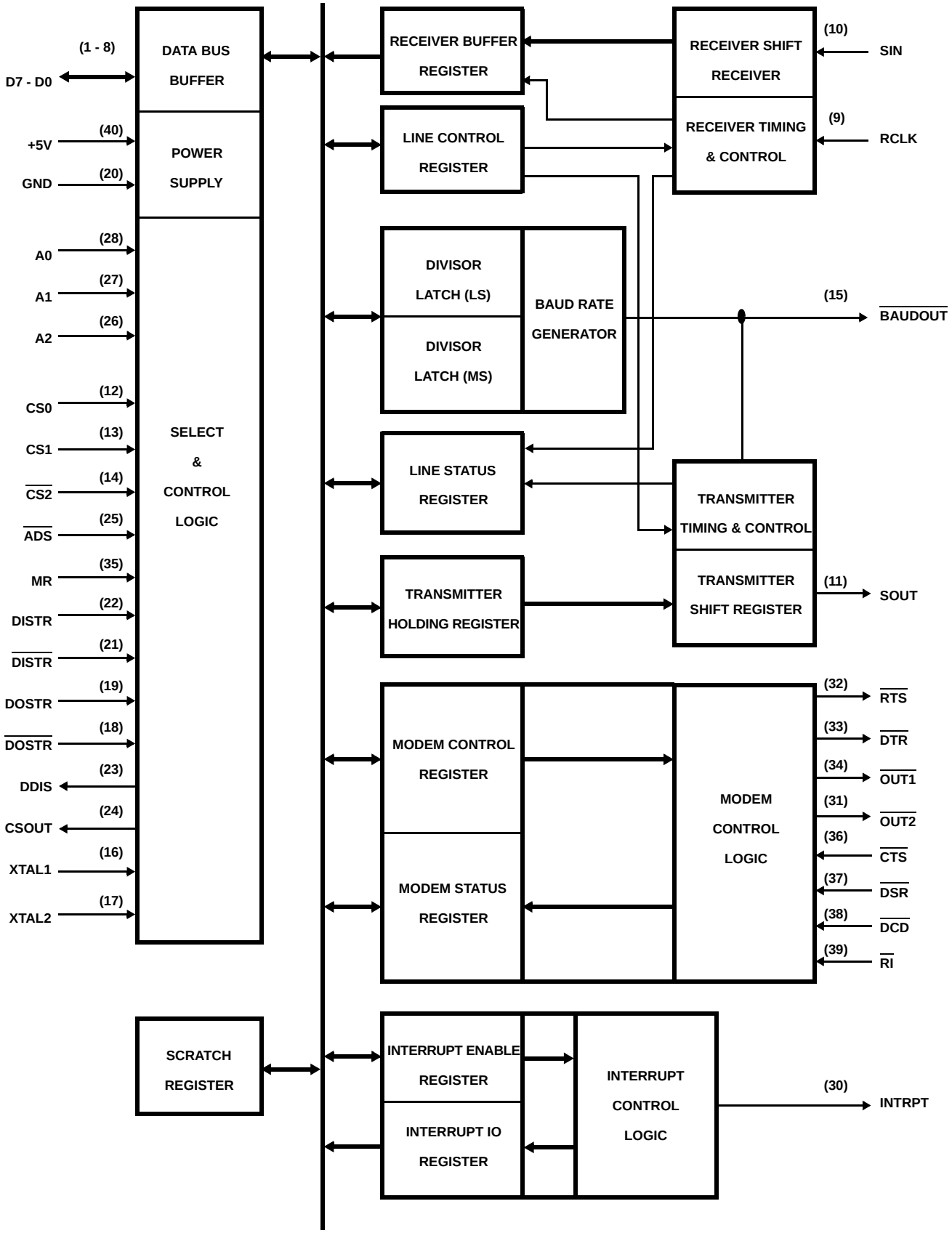
Pin Description

SYMBOL	PIN NUMBER	TYPE	ACTIVE LEVEL	DESCRIPTION
DISTR, DISTR	22 21	I I	H L	DATA IN STROBE, DATA IN STROBE: DISTR, DISTR are read inputs which cause the 82C50A to output data to the data bus (D0-D7). The data output depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs CS0, CS1, CS2 enable the DISTR, DISTR inputs. Only an active DISTR or DISTR, not both, is used to receive data from the 82C50A during a read operation. If DISTR is used as the read input, DISTR should be tied high. If DISTR is used as the active read input, DISTR should be tied low.
DOSTR, DOSTR	19 18	I I	H L	DATA OUT STROBE, DATA OUT STROBE: DOSTR, DOSTR are write inputs which cause data from the data bus (D0-D7) to be input to the 82C50A. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs CS0, CS1, CS2 enable the DOSTR, DOSTR inputs. Only an active DOSTR or DOSTR, not both, is used to transmit data to the 82C50A during a write operation. If DOSTR is used as the write input, DOSTR should be tied high. If DOSTR is used as the write input, DOSTR should be tied low.
D0-D7	1-8	I/O		DATA BITS 0-7: The Data Bus provides eight, three-state input/output lines for the transfer of data, control and status information between the 82C50A and the CPU. For character formats of less than 8 bits, D7, D6 and D5 are “don’t cares” for data write operations and 0 for data read operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1, A2	28, 27, 26	I I	H	REGISTER SELECT: The address lines select the internal registers during CPU bus operations. See Table 1.
XTAL1, XTAL2	16 17	I O		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. XTAL1 can also be used as an external clock input, in which case XTAL2 should be left open.
SOUT	11	O		SERIAL DATA OUTPUT: Serial data output from the 82C50A transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is a logic zero (low). SOUT is held in the Mark condition when the transmitter is disabled, MR is true, the Transmitter Register is empty, or when in the Loop Mode. SOUT is not affected by the CTS input.
GND	20		L	GROUND: Power supply ground connection (V_{SS}).
CTS	36	I	L	CLEAR TO SEND: The logical state of the CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register (CTS is bit 4 of the MSR, written MSR (4)). A change of state in the CTS pin since the previous reading of the MSR causes the setting of DCTS (MSR(O)) of the Modem Status Register. When CTS pin is ACTIVE (low), the modem is indicating that data on SOUT can be transmitted on the communications link. If CTS pin goes INACTIVE (high), the 82C50A should not be allowed to transmit data out of SOUT. CTS pin does not affect Loop Mode operation.
DSR	37	I	L	DATA SET READY: The logical state of the DSR pin is reflected in MSR(5) of the Modem Status Register. DDSR (MSR(1)) indicates whether the DSR pin has changed state since the previous reading of the MSR. When the DSR pin is ACTIVE (low), the modem is indicating that it is ready to exchange data with the 82C50A, while the DSR Pin INACTIVE (high) indicates that the modem is not ready for data exchange. The ACTIVE condition indicates only the condition of the local Data Communications Equipment (DCE), and does not imply that a data circuit as been established with remote equipment.
DTR	33	O	L	DATA TERMINAL READY: The DTR pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0. This signal is cleared (high) by writing a logic 0 to the DTR bit (MCR(0)) or whenever a MR ACTIVE (high) is applied to the 82C50A. When ACTIVE (low), DTR pin indicates to the DCE that the 82C50A is ready to receive data. In some instances, DTR pin is used as a power on indicator. The INACTIVE (high) state causes the DCE to disconnect the modem from the telecommunications circuit.
RTS	32	O	L	REQUEST TO SEND: The RTS signal is an output used to enable the modem. The RTS pin is set low by writing a logic 1 to MCR (1) bit 1 of the Modem Control Register. The RTS pin is reset high by Master Reset. When ACTIVE, the RTS pin indicates to the DCE that the 82C50A has data ready to transmit. In half duplex operations, RTS is used to control the direction of the line.
BAUDOUT	15	O		BAUDOUT: This output is a 16X clock out used for the transmitter section (16X = 16 times the data rate). The BAUDOUT clock rate is equal to the reference oscillator frequency divided by the specified divisor in the Baud Rate Generator Divisor Latches DLL and DLM. BAUDOUT may be used by the Receiver section by tying this output to RCLK.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	ACTIVE LEVEL	DESCRIPTION
$\overline{OUT1}$	34	O	L	OUTPUT 1: This is a general purpose output that can be programmed ACTIVE (low) by settingVCR(2) (OUT1) of the Modem Control Register to a high level. The $\overline{OUT1}$ pin is set high by Master Reset. The $\overline{OUT1}$ pin is INACTIVE (high) during loop mode operation.
$\overline{OUT2}$	31	O	L	OUTPUT 2: This is a general purpose output that can be programmed ACTIVE (low) by setting MCR(3) (OUT1) of the Modem Control Register to a high level. The $\overline{OUT2}$ pin is set high by Master Reset. The $\overline{OUT2}$ signal is INACTIVE (high) during loop mode operation.
$\overline{RI}$	39	1	L	RING INDICATOR: When low, $\overline{RI}$ indicates that a telephone ringing signal has been received by the modem or data set. The $\overline{RI}$ signal is a modem control input whose condition is tested by reading MSR(6) (RI). The Modem Status Register output TERI (MSR(2)) indicates whether the $\overline{RI}$ input has changed from a Low to High since the previous reading of the MSR. If the interrupt is enabled (IER (3) = 1) and $\overline{RI}$ changes from a Low to High, an interrupt is generated. The ACTIVE (low) state of $\overline{RI}$ indicates that the DCE is receiving a ringing signal. $\overline{RI}$ will appear ACTIVE for approximately the same length of time as the ACTIVE segment of the ringing cycle. The INACTIVE state of $\overline{RI}$ will occur during the INACTIVE segments not detected by the DCE. This circuit is not disabled by the INACTIVE condition of $\overline{DTR}$.
$\overline{DCD}$	38	I	L	DATA CARRIER DETECT: When ACTIVE (low), $\overline{DCD}$ indicates that the data carrier has been detected by the modem or data set. $\overline{DCD}$ is a modem input whose condition can be tested by the CPU by reading MSR(7) (DCD) of the Modem Status Register. MSR(3) (DDCD) of the Modem Status Register indicates whether the $\overline{DCD}$ input has changed since the previous reading of the MSR. $\overline{DOD}$ has no effect on the receiver. If the $\overline{DCD}$ changes state with the modem status interrupt enabled, an interrupt is generated. When $\overline{DCD}$ is ACTIVE (low), the received line signal from the remote terminal is within the limits specified by the DCE manufacturer. The INACTIVE (high) signal indicates that the signal is not within the specified limits, or is not present.
MR	35	1	H	MASTER RESET: The MR input forces the 82C50A into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. The 82C50A remains in an idle state until programmed to resume serial data activities. The MR input is a Schmitt trigger input. See the DC Electrical Characteristics for Schmitt trigger logic input voltage levels. See Table 7 for a summary of Master Reset's effect on 82C50A operation.
INTRPT	30	O	H	INTERRUPT REQUEST: The INTRPT output goes ACTIVE (high) when one of the following interrupts has an ACTIVE (high) condition and is enabled by the Interrupt Enable Register: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The INTRPT is reset low upon appropriate service or a MR operation. See Figure 1. Interrupt Control Structure.
SIN	10	I	H	SERIAL DATA INPUT: The SIN input is the serial data input from the communication line or modem to the 82C50A receiver circuits. A mark (1) is high, and a space (0) is low. Data inputs on SIN are disabled when operating in the loop mode.
V_{CC}	40		H	V_{CC}: +5V positive power supply pin. A 0.1µA decoupling capacitor from V_{CC} (pin 40) to GND (pin 20) is recommended.
$\overline{CS0}$, CS1, $\overline{CS2}$	12,13, 14	I I	H, H, L	CHIP SELECT: The Chip Select inputs act as enable signals for the write (DOSTR, $\overline{DOSTR}$) and read (DISTR, $\overline{DISTR}$) input signals. The Chip Select inputs are latched by the $\overline{ADS}$ input.
NC	29			Do Not Connect
CSOUT	24	O	H	CHIP SELECT OUT: When ACTIVE (high), this pin indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until CSOUT is a logic 1, ACTIVE (high).
DDIS	23	O	H	DRIVER DISABLE: This output is INACTIVE (low) when the CPU is reading data from the 82C50A. An ACTIVE (high) Dells output can be used to disable an external transceiver when the CPU is reading data.
$\overline{ADS}$	25	I	L	ADDRESS STROBE: When ACTIVE (low), $\overline{ADS}$ latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) inputs. An active $\overline{ADS}$ is required when the Register Select pins are not stable for the duration of the read or write operation, multiplexed mode. If not required, the $\overline{ADS}$ input should be tied low, non-multiplexed mode.
RCLK	9	I		This input is the 16X Baud Rate Clock for the receiver section of the 82C50A. This input may be provided from the $\overline{BAUDOUT}$ output or an external clock.

Block Diagram



Accessible Registers

The three types of internal registers in the 82C50A used in the operation of the device are control, status, and data registers. The control registers are the Bit Rate Select Register DLL and DLM, Line Control Register, Interrupt Enable Register and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register (LCR(7)) to select the register to be written or read (see Table 1.). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

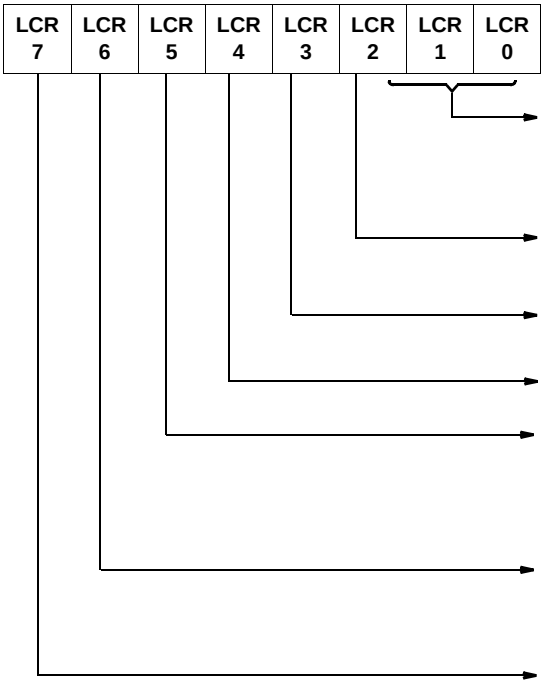
The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from 5-8 data bits. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The 82C50A data registers are double buffered so that read and write operations can be performed at the same time the UART is performing the parallel to serial and serial to parallel conversion. This provides the microprocessor with increased flexibility in its read and write timing.

TABLE 1. ACCESSING 82C50A INTERNAL REGISTERS

DLAB	A2	A1	A0	MNEMONIC	REGISTER
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	lER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

NOTE: X = “Don’t Care”, 0 = Logic Low, 1 = Logic High

Line Control Register (LCR)



Word Length Select
0 0 = 5 Data Bits
0 1 = 6 Data Bits
1 0 = 7 Data Bits
1 1 = 8 Data Bits

Stop Bit Select
0 = 1 Stop Bit
1 = 1.5 Stop Bits if 5 Data Bit Word Length is Selected 2 Stop Bits if 6, 7, or 8 Data Bit Word Length is Selected

Parity Enable
0 = Parity Disabled
1 = Parity Enabled (Generated & Checked)

Even Parity Select
0 = Odd Parity When Parity is Enabled
1 = Even Parity When Parity is Enabled

Stick Parity
0 = Stick Parity Disabled
1 = When Parity is Enabled Forces the Transmission and Checking of a Parity Bit of a Known State. Parity Bit Forced to a Logic 1 if LCR (4) = 0 or to a Logic 0 If LCR (4) = 1.

Break Control
0 = Break Disabled
1 = Break Enabled. The Serial Output (SOUT) is Forced to the Spacing (Logic 0) State.

Divisor Latch Access Bit
0 = Must be Low to Access the Receiver Buffer. Transmitter Holding Register or the Interrupt Enable Register.
1 = Must be High to Access the Divisor Latches DLL and DLM of the Baud Rate Generator During a Read or Write Operation.

LINE CONTROL REGISTER (LCR)

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below.

LCR BITS 0 THRU 7

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LCR (3) Parity Enable (PEN)
LCR (4) Even Parity Select (EPS)
LCR (5) Stick Parity
LCR (6) Set Break
LCR (7) Divisor Latch Access Bit (DLAB)

LCR(0) and LCR(1) Word Length Select Bit 0, Word Length Select Bit 1: The number of bits in each transmitted or received serial character is programmed as follows:

LCR(1)	LCR(0)	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled (LCR(3) = 1), LCR(4) = 0 selects odd parity, and LCR(4) = 1 selects even parity.

LCR(5) Stick Parity: When parity is enabled (LCR(3) = 1), LCR(5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to logic-1, the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic-0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all Os pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic 1) to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

LINE STATUS REGISTER (LSR)

The LSR is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the 82C50A.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character, with the entire character, including parity and stop bits, logic zero.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and ready to receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the 82C50A has completed transmission of the last character. If the interrupt is enabled (IER(1)), an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR (1) - LSR (4). (OE, PE, FE and BI).

LSR BITS 0 THRU 7

			LOGIC 1	LOGIC 0
LSR	(0)	Data Ready (DR)	Ready	Not Ready
LSR	(1)	Overrun Error (OE)	Error	No Error
LSR	(2)	Parity Error (PE)	Error	No Error
LSR	(3)	Framing Error (FE)	Error	No Error
LSR	(4)	Break Interrupt (BI)	Break	No Break
LSR	(5)	Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR	(6)	Transmitter Empty (TEMT)	Empty	Not Empty
LSR	(7)	Not Used		

The contents of the Line Status Register are indicated in the above table and are described below.

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR (4)). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The B indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting lER (2) = 1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the 82C50A is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER(1) = 1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, lNTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is permanently set to logic 0.

MODEM CONTROL REGISTER (MCR)

The MCR controls the interface with the modem or data set as described below. The MCR can be written and read. The $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$ and $\overline{OUT2}$ outputs are directly controlled by their control bits in this register. **A high input asserts a low (true) at the output pins.**

MCR BITS 0 THRU 7

			MCR BIT LOGIC 1	MCR BIT LOGIC 0
MCR	(0)	Data Terminal Ready (DTR)	$\overline{DTR}$ Output Low	$\overline{DTR}$ Output High
MCR	(1)	Request to Send (RTS)	$\overline{RTS}$ Output Low	$\overline{RTS}$ Output High
MCR	(2)	OUT1	$\overline{OUT1}$ Output Low	$\overline{OUT1}$ Output High
MCR	(3)	OUT2	$\overline{OUT2}$ Output Low	$\overline{OUT2}$ Output High
MCR	(4)	LOOP	LOOP Enabled	LOOP Disabled
MCR	(5)	0		
MCR	(6)	0		
MCR	(7)	0		

MCR(0): When MCR(0) is set high, the $\overline{DTR}$ output is forced low. When MCR(0) is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the 82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the $\overline{RTS}$ output is forced low. When MCR(1) is reset low, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the 82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

MCR(2): When MCR(2) is set high, the $\overline{OUT1}$ output is forced low. When MCR(2) is reset low, the $\overline{OUT1}$ output is forced high. $\overline{OUT1}$ is an user designated output.

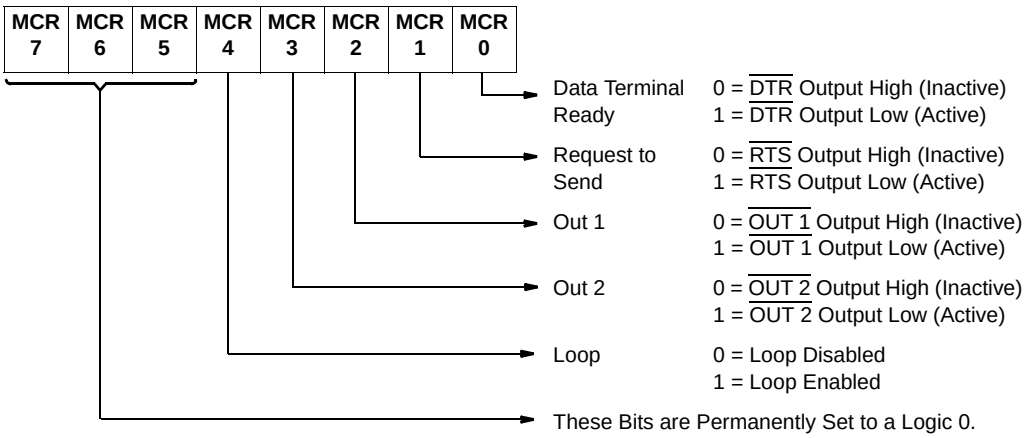
MCR(3): When MCR(3) is set high, the $\overline{OUT2}$ output is forced low. When MCR(3) is reset low, the $\overline{OUT2}$ output is forced high. $\overline{OUT2}$ is an user designated output.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the 62C50A. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic 1) state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, DC, and $\overline{RI}$) are disconnected. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the 82C50A.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. The interrupts are still controlled by the Interrupt Enable Register.

MCR(5) - MCR(7): These bits are permanently set to logic 0.

MODEM CONTROL REGISTER (MCR)



MODEM STATUS REGISTER (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral device. The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the 82C50A. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$ (pin 36), $\overline{DSR}$ (pin 37), $\overline{RI}$ (pin 39), and $\overline{DCD}$ (pin 38). MSR(4) - MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled (IER(3)), a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described below:

Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR BITS 0 THRU 7

MSR BIT	MNEMONIC	DESCRIPTION
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear To Send
MSR (3)	DDCD	Delta Data Carrier Detect
MSR (4)	CTS	Clear To Send
MSR (5)	DSR	Data Set Ready
MSR (6)	RI	Ring Indicator
MSR (7)	DCD	Data Carrier Detect

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the $\overline{CTS}$ input (Pin-36) to the 82C50A has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the $\overline{DSR}$ input (Pin-37) to the 62C50A has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the $\overline{RI}$ input (Pin-39) to the 82C50A has Changed state from Low to High since the last time it was read by the CPU. High to Low transitions on $\overline{RI}$ do not activate TERI.

MSR(3) Delta Data Carrier Detect (DDCD): DDCD indicates that the $\overline{DCD}$ input (Pin-36) to the 82C50A has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the $\overline{CTS}$ input (Pin-36) from the modem indicating to the 82C50A that the modem is ready to receive data from the 62C50A transmitter output (SOUT). If the 82C50A is in the loop mode (MCR(4)=1), MSR(4) is equivalent to RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the $\overline{DSR}$ input (Pin-37) from the modem to the 82C50A which indicates that the modem is ready to provide received data to the 82C50A receiver circuitry. If the 82C50A is in the loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR in the MCR.

MSR(6) Ring Indicator MSR(6): Indicates the status of the RI input (Pin-39). If the 82C50A is in the loop mode (MCR(4) = 1), MSR(6) is equivalent to OUT1 in the MCR.

MSR(7) Data Carrier Detect (MSR(7)): Data Carrier Detect indicates the status of the Data Carrier Detect ($\overline{DCD}$) input (Pin-38). If the 82C50A is in the loop mode (MCR(4) = 1), MSR(4) is equivalent to OUT2 of the MCR.

The modem status inputs (RI, DCD, DSR and CTS) reflect the modem input lines with any change of status. **Reading the MSR register will clear the delta modem status indications but has no effect on the status bits.** The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DDCD are true and a state change occurs during a read operation (DISTR, $\overline{DISTR}$), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DDCD are false and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read (DISTR, $\overline{DISTR}$) operations. If a status condition is generated during a read (DISTR, $\overline{DISTR}$) operation, the status bit is not set until the trailing edge of the read (DISTR, $\overline{DISTR}$).

If a status bit is set during a read (DISTR, $\overline{DISTR}$) operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read (DISTR, $\overline{DISTR}$) instead of being set again.

BAUD RATE SELECT REGISTER (BRSR)

The 82C50A contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 10MHz) by any divisor from 1 to 2^{16}-1 (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = frequency input ÷ (baud rate x 16)]. **Two 8-bit divisor latch registers store the divisor in a 16-bit binary format.** These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Sample Divisor Number Calculation:

Given: Desired Baud Rate 1200 Baud
Frequency Input 1.8432MHz

Formula: Divisor # = Frequency Input ÷ (Baud Rate x 16)
Divisor # = 1843200 ÷ (1200 x 16)

Answer: Divisor # = 96 = 60_{HEX} → DLL = 01100000
DLM = 00000000

Check: The Divisor # 96 will divide the input frequency 1.8432MHz down to 19200 which is 16 times the desired baud rate.

Divisor Latch Least Significant BYTE

DLL (0)	Bit 0
DLL (1)	Bit 1
DLL (2)	Bit 2
DLL (3)	Bit 3
DLL (4)	Bit 4
DLL (5)	Bit 5
DLL (6)	Bit 6
DLL (7)	Bit 7

Divisor Latch Most Significant BYTE

DLM (0)	Bit 8
DLM (1)	Bit 9
DLM (2)	Bit 10
DLM (3)	Bit 11
DLM (4)	Bit 12
DLM (5)	Bit 13
DLM (6)	Bit 14
DLM (7)	Bit 15

RECEIVER BUFFER REGISTER (RBR)

The receiver circuitry in the 82C50A is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit (LSB = Data Bit 0 (RBR(0)). Data Bit 0 of a data word (RBR(0)) is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the 82C50A.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the 82C50A, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the

data in the RBR before complete reception of the next character result in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7

RBR (0)	Data Bit 0
RBR (1)	Data Bit 1
RBR (2)	Data Bit 2
RBR (3)	Data Bit 3
RBR (4)	Data Bit 4
RBR (5)	Data Bit 5
RBR (6)	Data Bit 6
RBR (7)	Data Bit 7

TRANSMITTER HOLDING REGISTER (THR)

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 (THR(0)) is the first serial data bit transmitted. The THRE flag (LSR(5)) reflect the status of the THR. The TEMT flag (LSR(6)) indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR (0)	Data Bit 0
THR (1)	Data Bit 1
THR (2)	Data Bit 2
THR (3)	Data Bit 3
THR (4)	Data Bit 4
THR (5)	Data Bit 5
THR (6)	Data Bit 6
THR (7)	Data Bit 7

SCRATCHPAD REGISTER (SCR)

This 8-bit Read/Write register has no effect on the 82C50A. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR (0)	Data Bit 0
SCR (1)	Data Bit 1
SCR (2)	Data Bit 2
SCR (3)	Data Bit 3
SOR (4)	Data Bit 4
SCR (5)	Data Bit 5
SOR (6)	Data Bit 6
SCR (7)	Data Bit 7

Interrupt Structure

INTERRUPT IDENTIFICATION REGISTER (IIR)

The 82C50A has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the 82C50A prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (Priority 1)
2. Received Data Ready (Priority 2)
3. Transmitter Holding Register Empty (Priority 3)
4. Modem Status (Priority 4).

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

IIR(0): IIR(0) can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2): IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

TABLE 2. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
BIT 2	**BIT 1**	**BIT 0**	**PRIORITY LEVEL**	**INTERRUPT FLAG**	**INTERRUPT SOURCE**	**INTERRUPT RESET CONTROL**
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Receiver Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, $\overline{DCD}$	MSR Read

NOTE: X = Not Defined, May Be 0 or 1

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) is a Write register used to independently enable the four 82C50A interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 3 and are described below.

IER(0): When programmed high (IER(0) = Logic 1), IER(0) enables Received Data Available interrupt.

IER(1): When programmed high (IER(1) = Logic 1), IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When Programmed high (IER(2) = Logic 1), IER(2) enables the Receiver Line Status interrupt.

IER(3): When programmed high (IER(3) = Logic 1), IER(3) enables the Modem Status interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

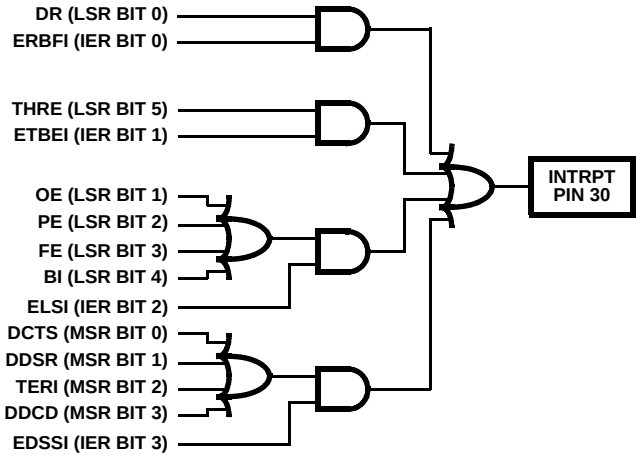


FIGURE 1. 82C50A INTERRUPT CONTROL STRUCTURE

TABLE 3. 82C50A ACCESSIBLE REGISTER SUMMARY

(NOTE: See Table 1 for how to access these registers.)

REGISTER MNEMONIC	REGISTER BIT NUMBER							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)†
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	“0” 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request to Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Set Ready	(CTS) Clear to Send	(DDCD) Delta Data Carrier Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

†LSB, Data Bit 0 is the first bit transmitted or received.

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5-8 bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, both THRE and TEMT are high. The first word written causes THRE to be reset to 0. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid bit sample of the start bit. Verifying the start bit prevents the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status information for the receiver is provided in the Line Status Register. When a character is transferred from the Receiver Shift Register to the Receiver Buffer Register, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR (2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG may be provided either with the addition of an external crystal to the XTAL1 and XTAL2 inputs, or an external clock into XTAL1. In either case, a buffered clock output, $\overline{\text{BAUDOUT}}$, is provided for other system clocking. If two 82C50As are used on the same board, one can use a crystal, and the buffered clock output can be routed directly into the XTAL1 of the second 82C50A.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency or crystal input, with the $\overline{\text{BAUDOUT}}$ providing an output 16X the data rate. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at XTAL1). The on-chip oscillator is optimized for a 10MHz crystal. Usually, higher frequency are less expensive than lower frequency crystals.

The BRG can use any of three different popular crystals to provide standard baud rates. The frequency of these three common crystals on the market are 1.8432MHz, 2.4576MHz, and 3.072MHz. With these standard crystals, standard bit rates from 50 to 38.5kbps are available. The following tables illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

TABLE 4. BAUD RATES USING 1.8432MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 5. BAUD RATES USING 2.4576MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

TABLE 6. BAUD RATES USING 3.072MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

Reset

After powerup, the 82C50A Master Reset Schmitt trigger input (MR) should be held high for TMRW ns to reset the 82C50A circuits to an idle mode until initialization. A high on MR causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TE MT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (MR low), the 82C50A remains in the idle mode until programmed.

A hardware reset of the 82C50A sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a Master Reset on the 82C50A is given in Table 7.

TABLE 7. 82C50A RESET OPERATIONS

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bit 0-3 Low Bits 4-7 Input Signal
SOUT	Master Reset	High
lntrpt (RCVR Errs)	Read LSR/MR	Low
lntrpt (RCVR Data Ready)	Read RBR/MR	Low
lntrpt (THRE)	Read IIR/Write THR/MR	Low
lntrpt (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{Out2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{Out1}}$	Master Reset	High

Programming

The 82C50A is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the 82C50A is programmed and operational, these registers can be updated any time the 82C50A is not transmitting or receiving data.

The control signals required to access 82C50A internal registers are shown below.

Software Reset

A software reset of the 82C50A is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Crystal Operation

The 82C50A crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. Table 8 shows the required crystal parameters and crystal circuit configuration, respectively.

When using an external clock source, the XTAL1 input is driven and the XTAL2 output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

The maximum frequency of the 82C50A is 10MHz with an external clock or a crystal attached to XTAL1 and XTAL2. Using the external clock or crystal, and a divide by one divisor, the maximum $\overline{\text{BAUDOUT}}$ is 10MHz, and the maximum data rate is 625Kbps.

TABLE 8. TYPICAL CRYSTAL OSCILLATOR CIRCUIT

PARAMETER	
Frequency	1.0 to 10MHz
Type of Operation	Parallel Resonant, Fundamental Mode
Load Capacitance (CL)	20 or 32pF (Typ)
R_{SERIES} (Max)	100Ω (f = 10MHz, CL = 32pF) 200Ω (f = 10MHz, CL = 20pF)

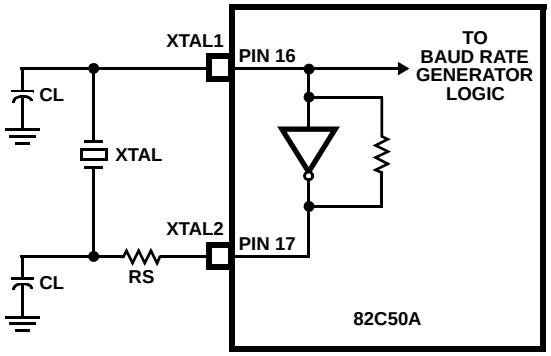


FIGURE 2. TYPICAL CRYSTAL OSCILLATOR CIRCUIT

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V

Operating Conditions

Operating Voltage Range. . . . . +4.5V to +5.5V
Operating Temperature Range
CX82C50A-5 . . . . . 0^oC to $+70^oC$
IX82C50A-5 . . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
Plastic DIP Package.	45	N/A
Plastic LCC Package	50	N/A

Maximum Junction Temperature
Plastic Package . . . . . $+150^oC$
Max Storage Temperature Range . . . . . -65^oC to $+150^oC$
Max Lead Temperature (Soldering 10s) . . . . . $+300^oC$
(Lead Tips Only for Surface Mount Packages)

Die Characteristics

Gate Count . . . . . 1788 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5.0V ±10%, T_A = 0^oC to $+70^oC$ (CX82C50A-5) T_A = -40^oC to $+85^oC$ (IX82C50A-5)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
VTH	Schmitt Trigger Logic One Input Voltage	2.0	-	V	MR Input
VTL	Schmitt Trigger Logic Zero Input Voltage	-	0.8	V	MR Input
VIH (CLK)	Logical One Clock Voltage	V_{CC}-0.8	-	V	External Clock
VIL (CLK)	Logical Zero Clock Voltage	-	0.8	V	External Clock
V_{OH}	Output High Voltage	3.0	-	V	I_{OH} = -2.5mA
		V_{CC}-0.4	-	V	I_{OH} = -100µA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = +2.5mA,
II	Input Leakage Current	-1.0	+1.0	µA	V_{IN} = GND or V_{CC}, DIP Pins 9,10,12, 13, 14, 18, 19, 21, 22, 25-28, 35-39
IO	Input/Output Leakage Current	-10.0	+10.0	µA	V_O = GND or V_{CC}, DIP Pins 1-8
ICCOP	Operating Power Supply Current	-	6	mA	External Clock F = 2.4576MHz, V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open
ICCSB	Standby Supply Current	-	100	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open

Capacitance

T_A = 25^oC

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	15	pF	FREQ = 1MHz, all measurements are referenced to device GND
COUT	Output Capacitance	15	pF	
CI/O	I/O Capacitance	20	pF	

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C (CX82C50A-5) T_A = -40°C to +85°C (IX82C50A-5)

Timing Requirements

SYMBOL		PARAMETER	82C50A-5 MIN	82C50A-5 MAX	UNITS	TEST CONDITIONS
(1)	TAW	Address Strobe Width	50	-	ns	
(2)	TAS	Address Setup Time	60	-	ns	Note 1
(3)	TAH	Address Hold Time	0	-	ns	
(4)	TCS	Chip Select Setup Time	60	-	ns	Note 1
(5)	TCH	Chip Select Hold Time	0	-	ns	
(6)	TDIW	DISTR $\overline{\text{DISTR}}$ Strobe Width	150	-	ns	
(7)	TRC	Read Cycle Delay	270	-	ns	Note 1
(8)	RC	Read Cycle = TAR + TDIW + TRC	500	-	ns	
(9)	TDD	DISTR $\overline{\text{DISTR}}$ to Driver Disable Delay	-	75	ns	
(10)	TDDD	Delay From DISTR $\overline{\text{DISTR}}$ to Data	-	120	ns	
(11)	THZ	DISTR $\overline{\text{DISTR}}$ to Floating Data Delay	10	75	ns	
(12)	TDOW	DOSTR $\overline{\text{DOSTR}}$ Strobe Width	150	-	ns	
(13)	TWC	Write Cycle Delay	270	-	ns	Note 1
(14)	WC	Write Cycle = TAW + TDOW + TWC	500	-	ns	
(15)	TDS	Data Setup Time	90	-	ns	
(16)	TDH	Data Hold Time	60	-	ns	

NOTE:

1. “When using the 82C50A in the multiplexed mode ($\overline{\text{ADS}}$ operational), it will operate in 80C86/88 systems with a maximum 3MHz operating frequency.”

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C (CX82C50A-5) T_A = -40°C to +85°C (IX82C50A-5)

Timing

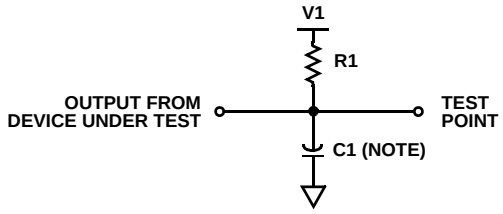
SYMBOL		PARAMETER	82C50A-5 MIN	82C50A-5 MAX	UNITS	TEST CONDITIONS
DEMULTIPLEXED OPERATION						
(17)	TCSC	Chip Select Output Delay from Select	-	125	ns	
(18)	TRA	Address Hold Time from DISTR $\overline{\text{DISTR}}$	20	-	ns	
(19)	TRCS	Chip Select Hold Time from DISTR $\overline{\text{DISTR}}$	20	-	ns	
(20)	TAR	DISTR $\overline{\text{DISTR}}$ Delay from Address	80	-	ns	
(21)	TCSR	DISTR $\overline{\text{DISTR}}$ Delay from Chip Select	80	-	ns	
(22)	TWA	Address Hold Time from DOSTR $\overline{\text{DOSTR}}$	20	-	ns	
(23)	TWCS	Chip Select Hold Time from DOSTR $\overline{\text{DOSTR}}$	20	-	ns	
(24)	TAW	DOSTR $\overline{\text{DOSTR}}$ Delay from Address	80	-	ns	
(25)	TCSW	DOSTR $\overline{\text{DOSTR}}$ Delay from Select	80	-	ns	
(26)	TMRW	Master Reset Pulse Width	500	-	ns	
(27)	TXH	Duration of Clock High Pulse	40	-	ns	
(28)	TXL	Duration of Clock Low Pulse	40		ns	

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C (CX82C50A-5) T_A = -40°C to +85°C (IX82C50A-5)

Timing (Continued)

SYMBOL		PARAMETER	82C50A-5 MIN	82C50A-5 MAX	UNITS	TEST CONDITIONS
BAUD GENERATOR						
(29)	N	Baud Divisor	1	2^{16}-1		
(30)	TBLD	Baud Output Negative Edge Delay	-	250	ns	
(31)	TBHD	Baud Output Positive Edge Delay	-	250	ns	
(32)	TLW	Baud Output Down Time	40	-	ns	T_{XL} = 50ns
(33)	THW	Baud Output Up Time	40	-	ns	T_{XH} = 50ns
RECEIVER						
(34)	TSCD	Delay from RCLK to Sample Time	-	250	ns	
(35)	TSlNT	Delay from Stop to Set Interrupt	1	1	$\overline{\text{BAUDOUT}}$ Cycles	
(36)	TRlNT	Delay from DISTR $\overline{\text{DISTR}}$ (RD RBR) to Reset Interrupt	-	250	ns	
TRANSMITTER						
(37)	THR	Delay from DOSTR $\overline{\text{DOSTR}}$ to Reset Interrupt	-	250	ns	
(38)	TIRS	Delay from Initial INTR Reset to Transmit Start	8	24	$\overline{\text{BAUDOUT}}$ Cycles	
(39)	TS1	Delay from Initial Write to Interrupt	16	32	$\overline{\text{BAUDOUT}}$ Cycles	
(40)	TSTI	Delay from Stop to Interrupt (THRE)	8	24	$\overline{\text{BAUDOUT}}$ Cycles	
(41)	TIR	Delay from DISTR $\overline{\text{DISTR}}$ (RD lIR) to Reset Interrupt (THRE)	-	250	ns	
MODEM CONTROL						
(42)	TMDO	Delay from DOSTR $\overline{\text{DOSTR}}$ to Output	-	500	ns	
(43)	TSIM	Delay to Set Interrupt from Modem Input	-	500	ns	
(44)	TRIM	Delay to Reset Interrupt from DISTR $\overline{\text{DISTR}}$ (RD MSR)	-	500	ns	

AC Test Circuit

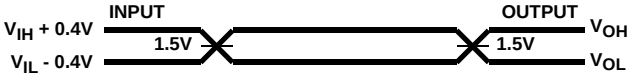


NOTE: Includes stay and jig capacitance.

TEST CONDITION DEFINITION TABLE

IOH	IOL	V1	R1	C1
-2.5mA	+2.5mA	1.7V	520Ω	100pF

AC Testing Input, Output Waveform



AC Testing: All input signals must switch between V_{IL} -0.4V and V_{IH} +0.4V. Input rise and fall times are driven at 1ns/V.

Timing Waveforms

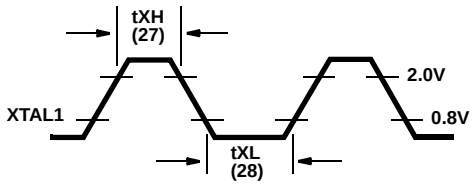


FIGURE 3. EXTERNAL CLOCK INPUT

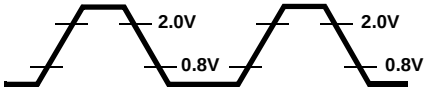
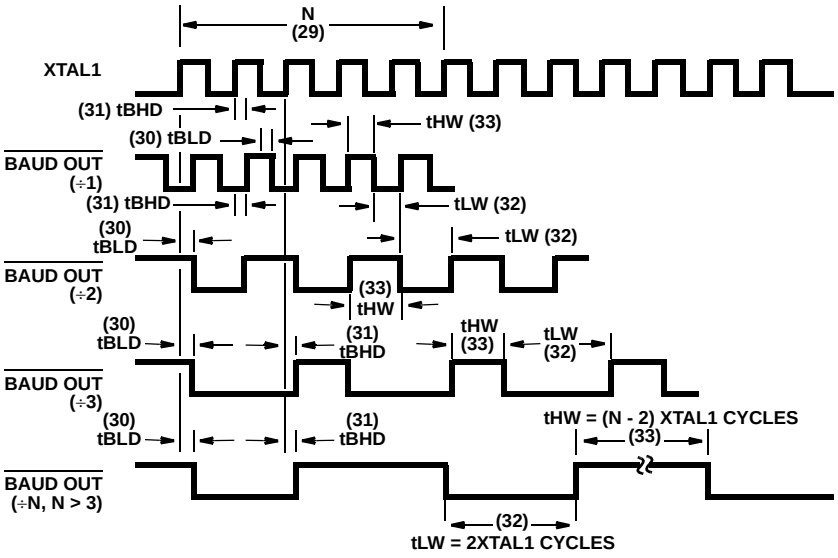


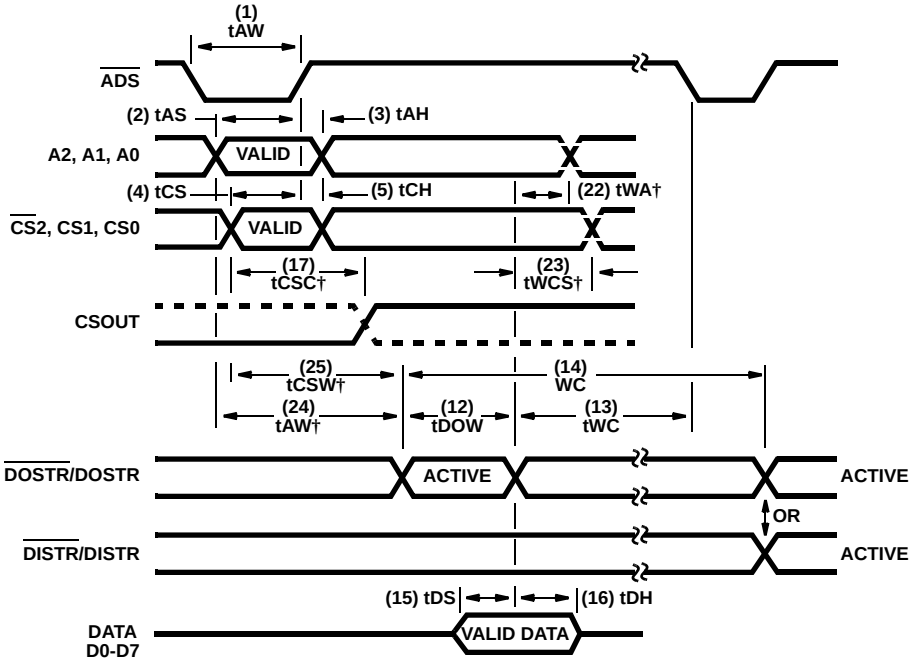
FIGURE 4. AC TEST POINTS



NOTE: tBLD (÷1) is the only spec measure from XTL1 falling edge. All other tBLD's and tBHD's are measured from XTAL1 rising edge.

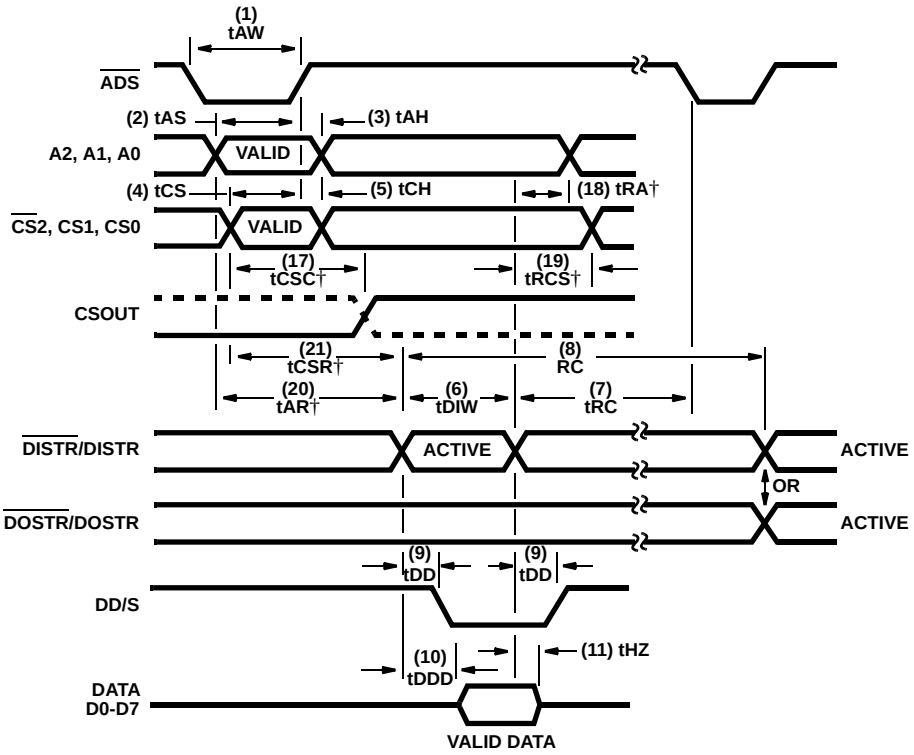
FIGURE 5. $\overline{\text{BAUDOUT}}$ TIMING

Timing Waveforms (Continued)



† Applicable only when $\overline{ADS}$ is tied low.

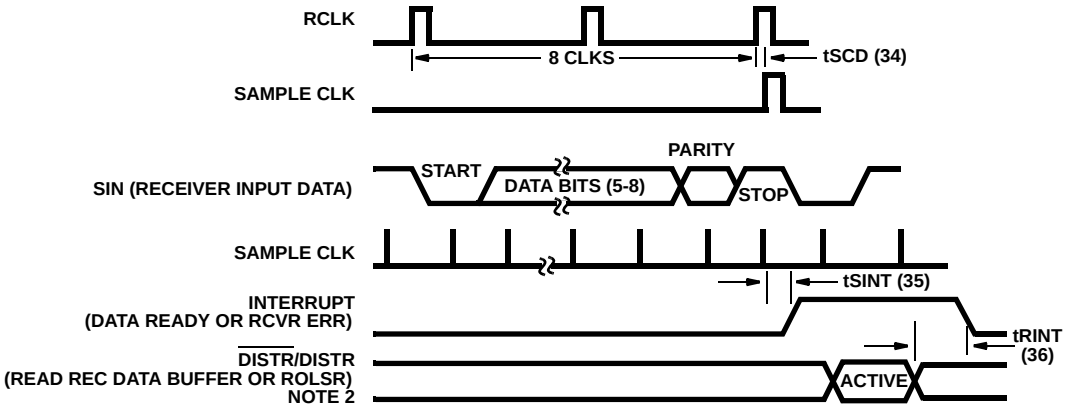
FIGURE 6. WRITE CYCLE



† Applicable only when $\overline{ADS}$ is tied low.

FIGURE 7. READ CYCLE

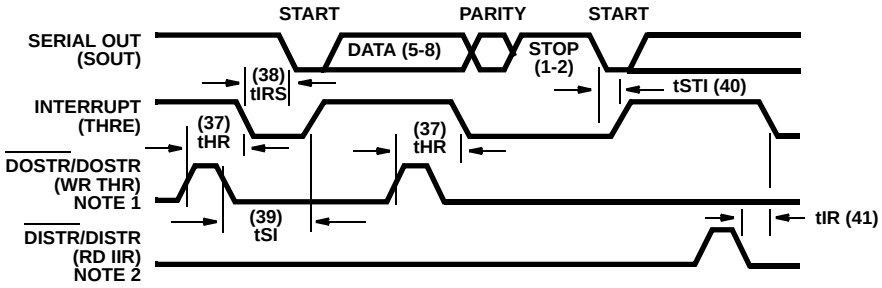
Timing Waveforms (Continued)



NOTES:

1. See Write Cycle Timing.
2. See Read Cycle Timing.

FIGURE 8. RECEIVER TIMING

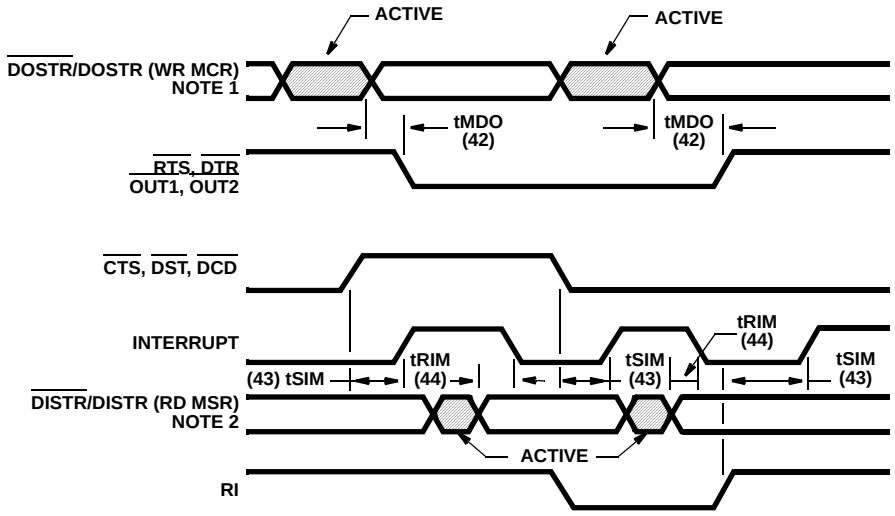


NOTES:

1. See Write Cycle Timing.
2. See Read Cycle Timing.

FIGURE 9. TRANSMITTER TIMING

Timing Waveforms (Continued)

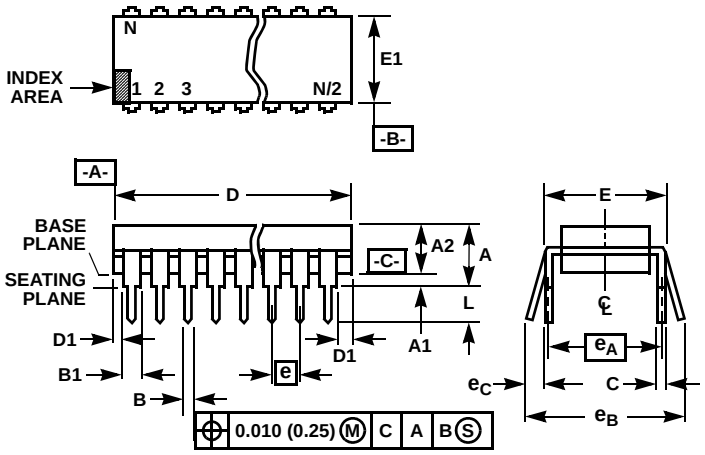


NOTES:

1. See Write Cycle Timing.
2. See Read Cycle Timing.

FIGURE 10. MODEM CONTROLS TIMING

Dual-In-Line Plastic Packages (PDIP)



NOTES:

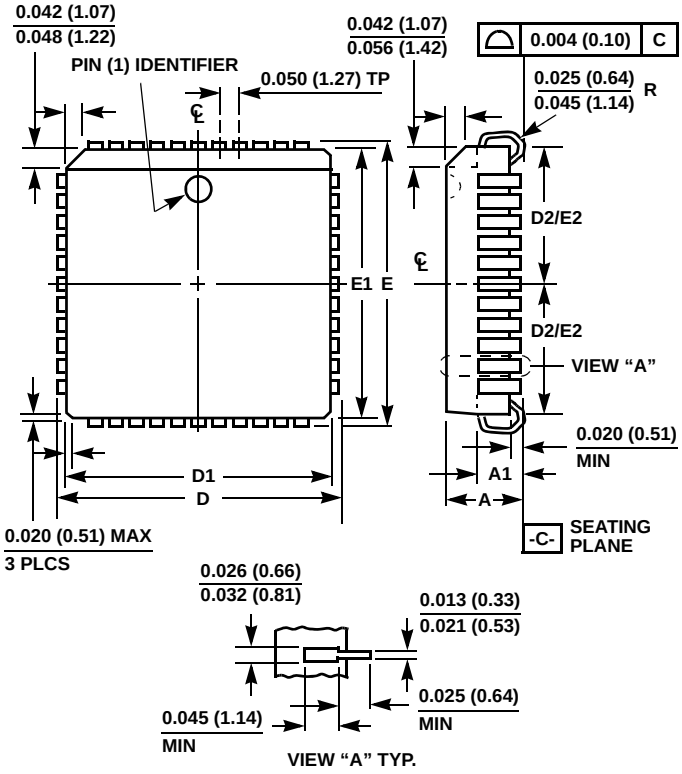
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

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Plastic Leaded Chip Carrier Packages (PLCC)



N44.65 (JEDEC MS-018AC ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9