AN-REF-15W_CE1K0 ADAPTER

15W 5V Adapter Reference Board with ICE2QS03G, IPS65R1K0CE, BSC067N06LS3 G & BAS21-03W

Application Note

About this document

Scope and purpose

This document is a 15W 5.0V high efficiency USB adapter reference design using Infineon Quasi-Resonant PWM IC ICE2QS03G with CoolMOS™ IPS65R1K0CE (IPAK) and secondary side synchronous rectification IC with OptiMOS™ BSC067N06LS3 G (ThinPAK 5x6) in a small form factor, high efficiency and various mode of protections for a high reliable system.

Intended audience

This document is intended for users who wish to design high efficiency, very small form factor universal 15W 5V AC-DC adapter with Infineon CoolMOS™ CE series, OptiMOS™, Quasi-Resonant PWM IC ICE2QS03G and synchronous rectification.

Table of Contents

About this document **1**

Table of Contents **2**

1 Abstract **4**

2 Reference board **4**

3 Specifications **5**

4 Circuit description **6**
4.1 Mains input rectification and filtering 6
4.2 PWM control and switching MOSFET 6
4.3 Snubber network 6
4.4 Output stage 6
4.5 Feedback loop 6

5 Circuit operation **7**
5.1 Startup operation 7
5.2 Normal mode operation 7
5.3 Primary side peak current control 7
5.4 Digital frequency reduction 7
5.5 Burst mode operation 7

6 Protection features **8**
6.1 V_{CC} over voltage and under voltage protection 8
6.2 Over load/Open loop protection 8
6.3 Auto restart for over temperature protection 8
6.4 Adjustable output overvoltage protection 8
6.5 Short winding protection 8
6.6 Foldback point protection 9

7 Circuit diagram **10**

8 PCB layout **11**
8.1 Top side 11
8.2 Bottom side 11

9 Bill of material (BOM) **12**

10 Transformer construction **13**

11 Test results **14**
11.1 Efficiency, regulation and output ripple 14
11.2 Standby power 15
11.3 Line regulation 16
11.4 Load regulation 16
11.5 Maximum power 17
11.6 ESD immunity (EN61000-4-2) 17
11.7 Surge immunity (EN61000-4-5) 17
11.8 Conducted emissions (EN55022 class B) 18
11.9 Thermal measurement 20

Abstract

12 Waveforms and scope plots 20
12.1 Start up at low/high AC line input voltage with maximum load 20
12.2 Soft start 21
12.3 Drain voltage and current at maximum load 21
12.4 Zero crossing point during normal operation 22
12.5 Load transient response (Dynamic load from 10% to 100%) 22
12.6 Output ripple voltage at maximum load 23
12.7 Output ripple voltage during burst mode at 1 W load 23
12.8 Active Burst mode operation 24
12.9 Over load protection (Auto restart mode) 24
12.10 Output overvoltage protection (Latched off mode) 25
12.11 V_{CC} under voltage/Short optocoupler protection (Auto restart mode) 25

13 References 26

Revision History 26

1 Abstract

This application note is an engineering report of a very small form factor reference design for universal input 15W 5V adapter. The adapter is using **ICE2QS03G**, a second generation current mode control Quasi-Resonant flyback topology controller, **IPS65R1K0CE**, a CE series of high voltage power CoolMOS™ and **BSC067N06LS3 G**, a third series of medium voltage power OptiMOS™, optimized for Synchronous Rectification. The distinguishing features of this reference design are very small form factor, Best-in-Class low standby power, very high efficiency, good EMI performance and various modes of protection for high reliable system.

2 Reference board

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are showed at the rear of the report.

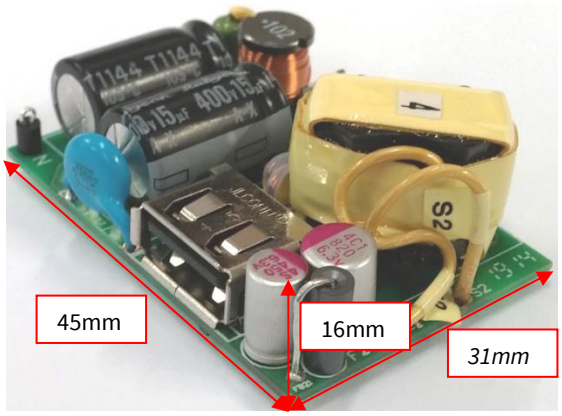
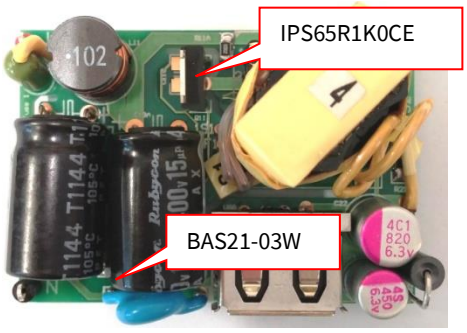
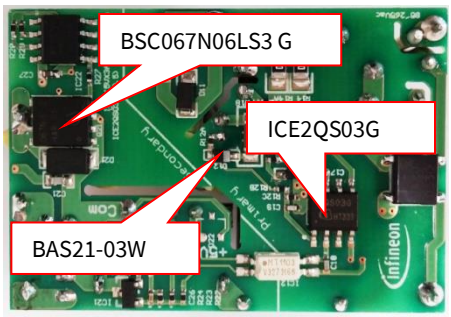


Figure 1 REF-15W_CE1K0 ADAPTER [Dimensions L x W x H: 45mm x 31mm x 16mm]



(Top view)



(Bottom view)

Figure 2 REF-15W_CE1K0 ADAPTER [Top & Bottom View]

3 Specifications

Table 1 Specifications of REF-15W_CE1K0 ADAPTER

Input voltage	85Vac~265Vac
Input frequency	50~60Hz
Output voltage	5V
Output current	3A
Output power	15W
Minimum switching frequency at full load and minimum input voltage	45kHz
Maximum input power for universal mains	< ±6% of input power
No-load power consumption (EU CoC Version 5, Tier 2 and EPS of DOE USA)	< 40mW
Active mode four point average efficiency (25%,50%,75% & 100%load) (EU CoC Version 5, Tier 2 and EPS of DOE USA) Active mode at 10% load efficiency (EU CoC Version 5, Tier 2)	>88% at 115Vac & >87% at 230Vac >86% at 115Vac & >85% at 230Vac
Steady state output ripple	+/-1% of nominal output voltage ($V_{ripple_p_p}$<100mV)
Dynamic load response undershoot & overshoot	+/-3% of nominal output voltage ($V_{ripple_p_p}$ <300mV)
Conducted emissions (EN55022 class B)	Pass with 8 dB margin
ESD immunity (EN61000-4-2)	level 3 (±6kV) contact discharge
Surge immunity (EN61000-4-5)	Installation class 3 (2kV: common mode)
Form factor case size (L x W x H)	(45 x 31 x 16) mm^3

4 Circuit description

4.1 Mains input rectification and filtering

The AC line input side comprises the input fuse F1 as over-current protection. A rectified DC voltage (120V ~ 374V) is obtained through a bridge rectifier BR1 and a pi filter C13, FB21 and C22. The pi filer also attenuates the differential mode conducted EMI.

4.2 PWM control and switching MOSFET

The PWM pulse is generated by the Quasi Resonant PWM current-mode Controller **ICE2QS03G** and this PWM pulse drives the high voltage power CoolMOS™, **IPS65R1K0CE (CE)** which designed a$_{CC}$ording to the revolutionary Superjunction (SJ) principle. The CoolMOS™ CE provides all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. It achieves extremely low conduction and switching losses and can make switching applications more efficient, more compact, lighter and cooler. The PWM switch-on is determined by the zero-crossing input signal and the value of the up/down counter. The PWM switch-off is determined by the feedback signal V_{FB} and the current sensing signal V_{CS}. **ICE2QS03G** also performs all necessary protection functions in flyback converters. Details about the information mentioned above are illustrated in the product datasheet.

4.3 Snubber network

A snubber network R11, R11A, C15 and D11 dissipate the energy of the leakage inductance and suppress ringing on the SMPS transformer. Due to the resonant capacitor (MOSFET's drain source capacitance), the overshoot is relatively smaller than fixed frequency flyback converter. Thus the snubber resistor can be used with a larger one which will reduce the snubber loss.

4.4 Output stage

On the secondary side, 5V output, the PWM pulse is generated by synchronous rectification controller **UCC24610.** The synchronous rectification pulse drives the medium voltage power OptiMOS™, **BSC067N06LS3 -G** which is optimized for synchronous rectification such as the lowest $R_{DS(on)}$, the perfect switching behavior of fast switching, the smallest footprint and highest power density. The capacitors C22 provides energy buffering following with the LC filter FB21 and C24 to reduce the output ripple and prevent interference between SMPS switching frequency and line frequency considerably. Storage capacitor C22 is designed to have an internal resistance (ESR) as small as possible. This is to minimize the output voltage ripple caused by the triangular current.

4.5 Feedback loop

For feedback, the output is sensed by the voltage divider of R26 and R25 and compared to TL431 internal reference voltage. C25, C26 and R24 comprise the compensation network. The output voltage of TL431 is converted to the current signal via optocoupler IC12 and two resistors R22 and R23 for regulation control.

5 Circuit operation

5.1 Startup operation

Since there is a built-in startup cell in the **ICE2QS03G**, there is no need for external start up resistor, which can improve standby performance significantly. When V_{CC} reaches the turn on voltage threshold 18V, the IC begins with a soft start. The soft-start implemented in **ICE2QS03G** is a digital time-based function. The preset soft-start time is 12ms with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.32V to 1V finally. After IC turns on, the V_{CC} voltage is supplied by auxiliary windings of the transformer.

5.2 Normal mode operation

The secondary output voltage is built up after startup. The secondary regulation control is adopted with TL431 and optocoupler. The compensation network C25, C26 and R24 constitutes the external circuitry of the error amplifier of TL431. This circuitry allows the feedback to be precisely controlled with respect to dynamically varying load conditions, therefore providing stable control.

5.3 Primary side peak current control

The MOSFET drain source current is sensed via external resistor R14 and R14A. Since **ICE2QS03G** is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle.

5.4 Digital frequency reduction

During normal operation, the switching frequency for **ICE2QS03G** is digitally reduced with decreasing load. At light load, the CoolMOS™ **IPS65R1K0CE** will be turned on not at the first minimum drain-source voltage time, but on the n^{th}. The counter is in range of 1 to 7, which depends on feedback voltage in a time-base. The feedback voltage decreases when the output power requirement decreases, and vice versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

5.5 Burst mode operation

At light load condition, the SMPS enters into **Active Burst Mode**. At this stage, the controller is always active but the V_{CC} must be kept above the switch off threshold. During active burst mode, the efficiency increase significantly and at the same time it supports low ripple on V_{out} and fast response on load jump.

For determination of entering Active Burst Mode operation, three conditions apply:

1. The feedback voltage is lower than the threshold of V_{FBEB}(1.25V). Accordingly, the peak current sense voltage across the shunt resistor is 0.1667;

2. The up/down counter is 7;

3. And a certain blanking time (t_{BEB}=24ms).

Once all of these conditions are fulfilled, the Active Burst Mode flip-flop is set and the controller enters Active Burst Mode operation. This multi-condition determination for entering Active Burst Mode operation prevents mis-triggering of entering Active Burst Mode operation, so that the controller enters Active Burst Mode operation only when the output power is really low during the preset blanking time.

During active burst mode, the maximum current sense voltage is reduced from 1V to 0.34V so as to reduce the conduction loss and the audible noise. At the burst mode, the FB voltage is changing like a sawtooth between 3.0 and 3.6V.

The feedback voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 34% during Active Burst Mode a certain load is needed so that feedback voltage can exceed VLB (4.5V). After leaving active burst mode, maximum current can now be provided to stabilize V_O. In addition, the up/down counter will be set to 1 immediately after leaving Active Burst Mode. This is helpful to decrease the output voltage undershoot.

6 Protection features

6.1 V_{CC} over voltage and under voltage protection

During normal operation, the V_{CC} voltage is continuously monitored. When the V_{CC} voltage increases up to $V_{CC,OVP}$ or V_{CC} voltage falls below the under voltage lock out level $V_{CC,off}$, the IC will enter into autorestart mode.

6.2 Over load/Open loop protection

In case of open control loop, feedback voltage is pulled up with internally block. After a fixed blanking time, the IC enters into auto restart mode. In case of secondary short-circuit or overload, regulation voltage V_{FB} will also be pulled up, same protection is applied and IC will auto restart.

6.3 Auto restart for over temperature protection

The IC has a built-in over temperature protection function. When the controller's temperature reaches 140°C, the IC will shut down switch and enters into auto restart. This can protect power MOSFET from overheated.

6.4 Adjustable output overvoltage protection

During off-time of the power switch, the voltage at the zero-crossing pin ZC is monitored for output overvoltage detection. If the voltage is higher than the preset threshold 3.7V for a preset period 100µs, the IC is latched off.

6.5 Short winding protection

The source current of the MOSFET is sensed via external resistor R14 and R14A. If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} of 1.68V during the on-time of the power switch, the IC is latched off. This constitutes a short winding protection. To avoid an a$_{CC}$idental latch off, a spike blanking time of 190ns is integrated in the output of internal comparator.

6.6 Foldback point protection

For a quasi-resonant flyback converter, the maximum possible output power is increased when a constant current limit value is used for all the mains input voltage range. This is usually not desired as this will increase additional cost on transformer and output diode in case of output over power conditions.
The internal foldback protection is implemented to adjust the VCS voltage limit according to the bus voltage. Here, the input line voltage is sensed using the current flowing out of ZC pin, during the MOSFET on-time. As the result, the maximum current limit will be lower at high input voltage and the maximum output power can be well limited versus the input voltage.

7 Circuit diagram

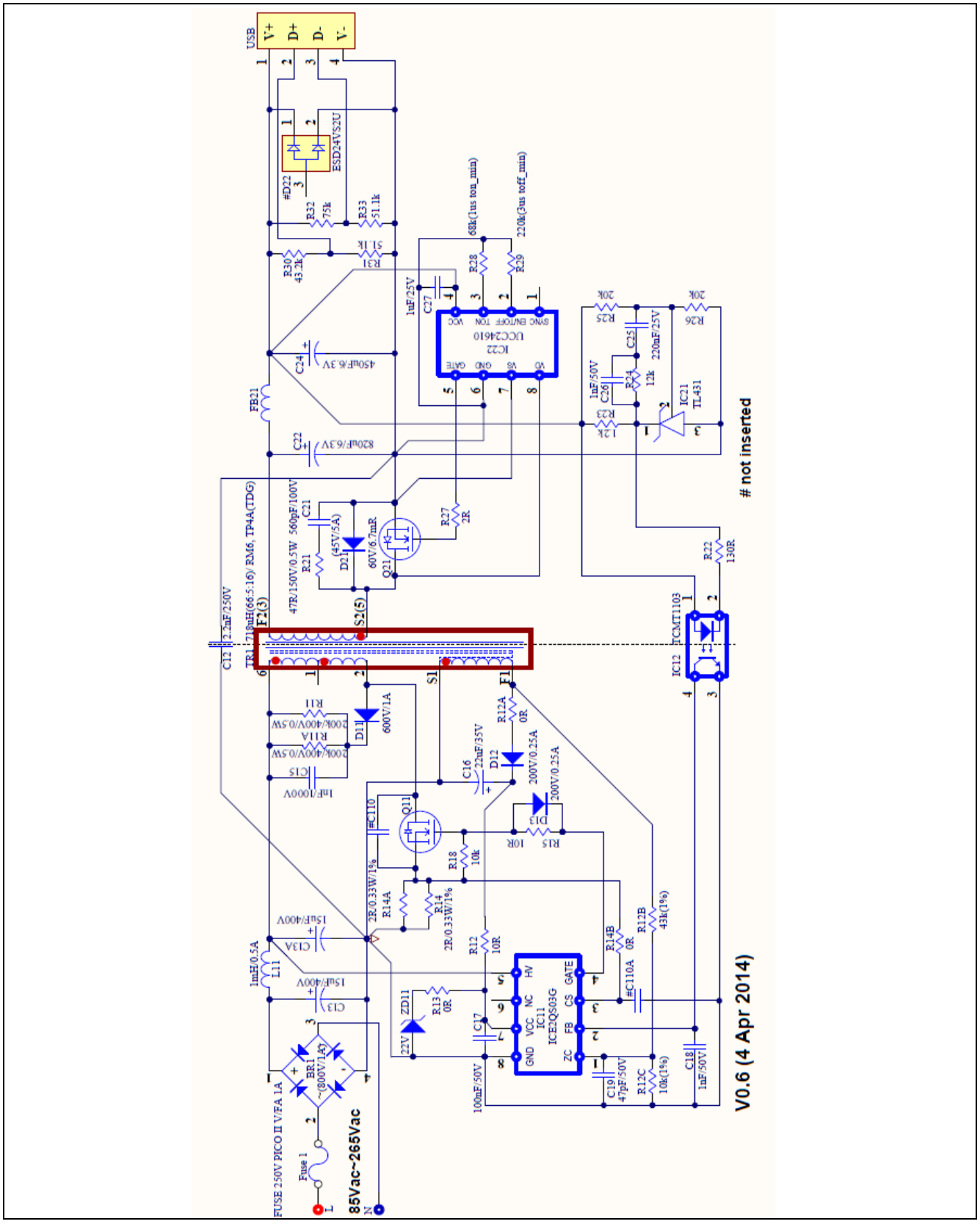


Figure 3 Schematic of REF-15W_CE1K0 ADAPTER

8 PCB layout

8.1 Top side

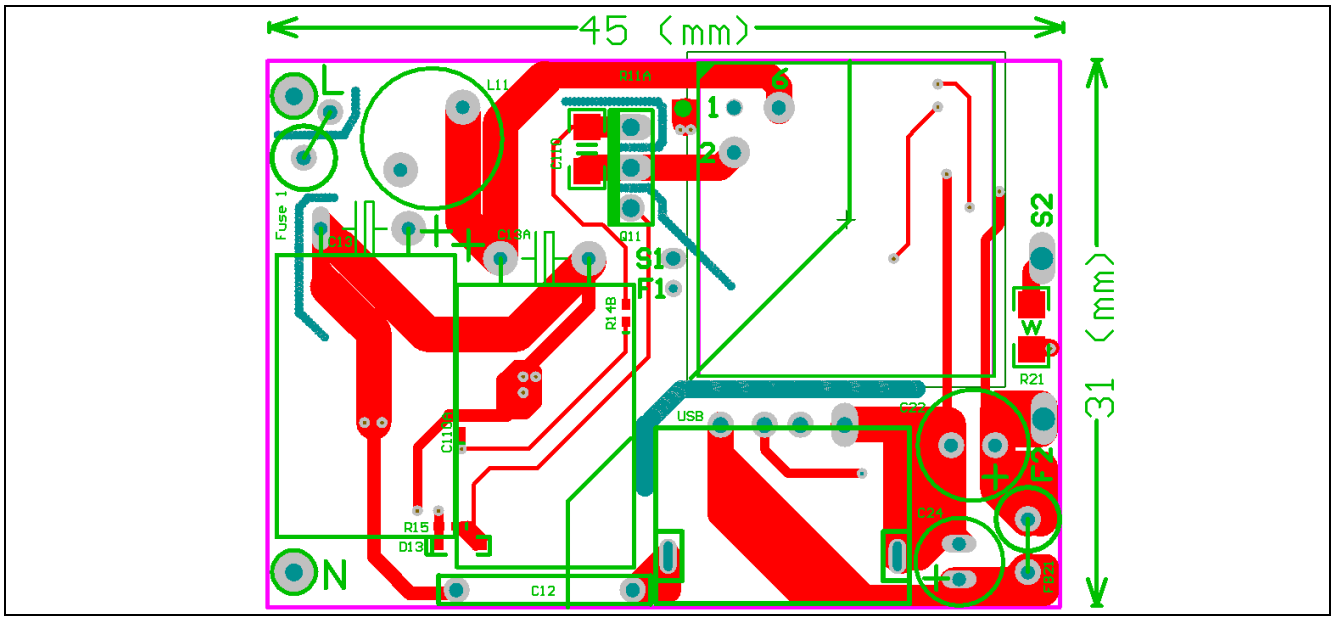


Figure 4 Top side copper and component legend

8.2 Bottom side

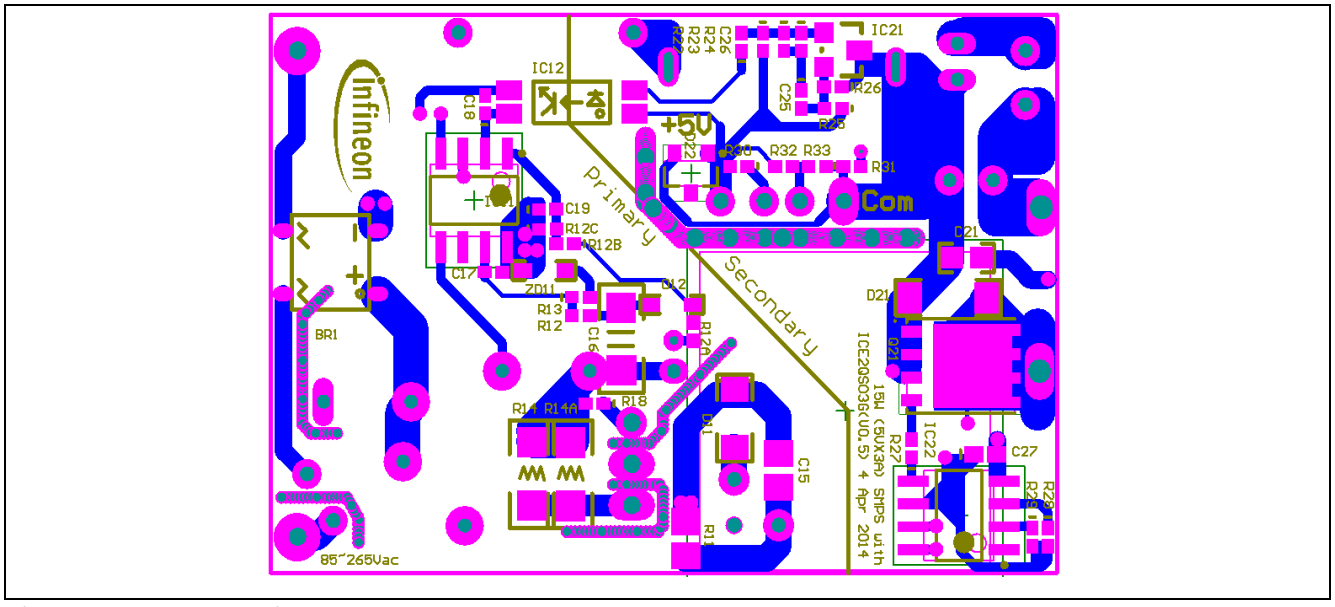


Figure 5 Bottom side copper and component legend

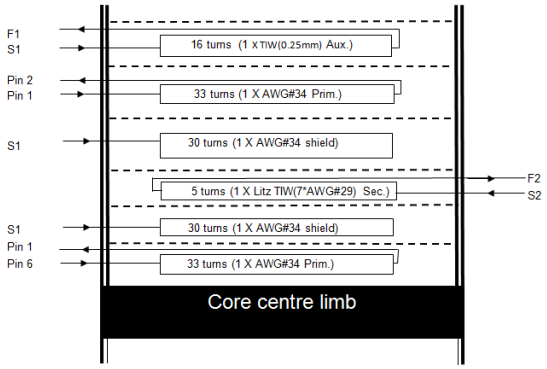
9 Bill of material (BOM)

Table 2 Bill of materials

No.	Designator	Description	Footprint	Part Number	Manufacturer	Quantity
1	BR1	(800V/1A)	SOP-4	D1UBA80	SHINDENGEN	1
2	C12	2.2nF/250V	MKT2/13/10_0M8	DE1E3KL222MC4BNA1S	MURATA	1
3	C13, C13A	15uF/400V	RB10H(10x16)	400AX15M10X16	RUBYCON	2
4	C15	1nF/1000V	0805	C0805X102KDRACTU		1
5	C16	22uF/35V	1206	C3216X5R1V226M		1
6	C17	100nF/50V	0402	GRM155R71H104KE14D	MURATA	1
7	C18, C26	1nF/50V	0402	GRM155R71H102KA01D	MURATA	2
8	C19	47pF/50V	0402	GRM1555C1H470JA01D	MURATA	1
9	C21	560pF/100V	0603	GRM1885C2A561JA01D	MURATA	1
10	C22	820uF/6.3V	RB6.3	MP6RL820MC8		1
11	C24	450uF/6.3V	RB5	MP6RL450MB8		1
12	C25	220nF/25V	0402	GRM155C81E224KE01D	MURATA	1
13	C27	1uF/25V	0402	GRM155R61E105KA12D	MURATA	1
14	D11	600V/1A	Sub SMA	ES1JL		1
15	D12,D13	200V/0.25A	SOD323	BAS21-03W	INFINEON	2
16	D21	45V/5A	DO-221AC (slimSMA)	VSSAF5L45		1
17	F1	250V/1A	AXIAL0.4_V 3mm	0263001.HAT1L		1
18	FB21	FAIR RITE	AXIAL0.4_V 3mm	2743002112		1
19	IC11	ICE2QS03G	SO-8	ICE2QS03G	INFINEON	1
20	IC12	TCMT1103	optocoupler half pitch mini flat package	TCMT1103		1
21	IC21	TL431	SOT-23	TL431BFDT		1
22	IC22	UCC24610	SO-8	UCC24610		1
23	L	connector	Connector	5000RED		1
24	L11	1mH/0.5A	CH8	768772102	WURTH ELECTRONICS	1
25	N	Connector N(2.5)	Connector(2.5)	5001BLACK		1
26	Q11	650V/1R	TO251(IPAK)	IPS65R1K0CE	INFINEON	1
27	Q21	60V/6.7mR	INF-PG-TDSON81	BSC067N06LS3 G	INFINEON	1
28	R11,R11A	200k/400V/0.5W	0805	ERJP06F2003V		2
29	R12, R15	10R	0402			2
30	R12A, R13, R14B	0R	0402			3
31	R12B	43k/1%	0402			1
32	R12C	10k/1%	0402			1
33	R14, R14A	2R/0.33W/1%	1206	ERJ8BQF2R0V		2
34	R18	10k	0402			1
35	R21	47R/0.5W	0805	ERJP6WF47R0V		1
36	R22	130R	0402			1
37	R23	1.2k	0402			1
38	R24	12k	0402			1
39	R25, R26	20k	0402			2
40	R27	2R	0402			1
41	R28	68k	0402			1
42	R29	220k	0402			1
43	R30	43.2k	0402			1
44	R31, R33	51.1k	0402			1
45	R32	75k	0402			1
46	TR1	718uH(66:5:16) RM6(TP4A)	TR_RM6_THT6Pin			1
47	USB Port	USBPORT	USB2 Short(Horizontal)	JL-CAF-001		1
48	ZD11	22V Zener	SOD323	UDZS22B		1

10 Transformer construction

Core and material: RM6 TP4A
Bobbin: RM6 with 3 pin
Primary Inductance, Lp=718 µH(±10%), measured between pin 2 and pin 6



Start	Stop	No. of turns	Wire size	Layer
6	1	33	1XAWG#34	1/2 Primary
S1(Flying wire)	floating	30	1XAWG#34	Shield
S2(5) Flying wire	F2(3) Flying wire	5	1XLitz TIW(7 X AWG#29)	Secondary
S1(Flying wire)	floating	30	1XAWG#34	Shield
1	2	33	1XAWG#34	1/2 Primary
S1(Flying wire)	F1 (Flying wire)	16	1XTIW(0.25mm)	Auxiliary

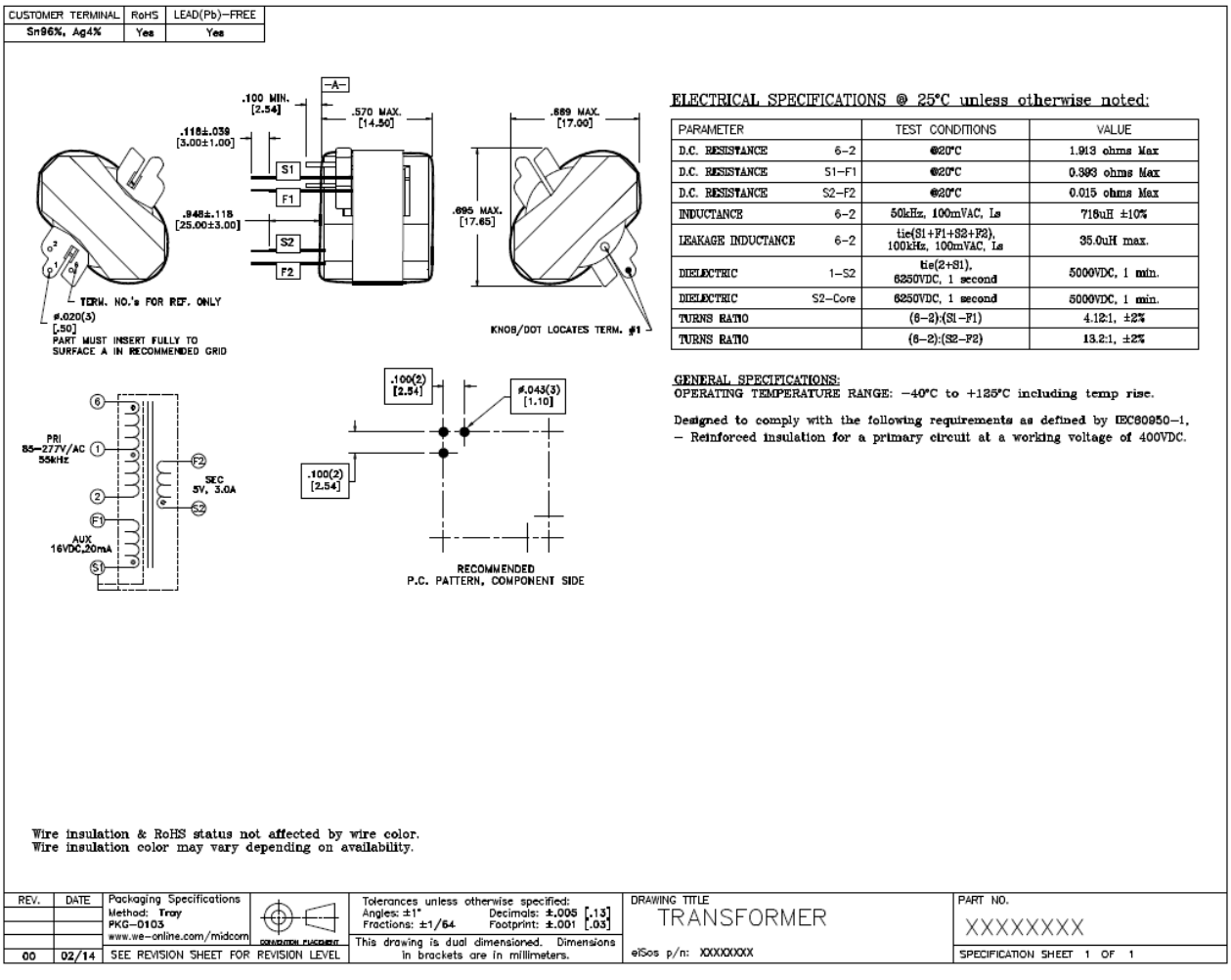


Figure 6 Transformer structure

11 Test results

11.1 Efficiency, regulation and output ripple

Table 3 Efficiency, regulation & output ripple

V_{in} (Vac)	P_{in} (W)	V_{out} (Vdc)	I_{out} (A)	$V_{out_ripple_pk_pk}$ (mV)	P_{out} (W)	η (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out} (A)
85	0.0322	5.02	0.00	59.70				20.00	3.42
	1.7400	5.02	0.30	57.40	1.51	86.55			
	4.2700	5.02	0.75	22.60	3.77	88.17	87.94		
	8.5100	5.02	1.50	32.10	7.53	88.48			
	12.7900	5.02	2.25	35.20	11.30	88.31			
	17.3500	5.02	3.00	49.70	15.06	86.80			
115	0.0326	5.02	0.00	64.90				19.85	3.48
	1.7500	5.02	0.30	59.90	1.51	86.06			
	4.2700	5.02	0.75	20.10	3.77	88.17	88.93		
	8.4400	5.02	1.50	29.80	7.53	89.22			
	12.6400	5.02	2.25	35.00	11.30	89.36			
	16.9300	5.02	3.00	40.30	15.06	88.95			
230	0.0339	5.02	0.00	70.20				20.44	3.61
	1.7700	5.02	0.30	81.30	1.51	85.08			
	4.4200	5.02	0.75	22.40	3.77	85.18	87.85		
	8.4900	5.02	1.50	33.50	7.53	88.69			
	12.6500	5.02	2.25	35.30	11.30	89.29			
	17.0700	5.02	3.00	37.00	15.06	88.22			
265	0.0347	5.02	0.00	76.00				21.45	3.76
	1.7800	5.02	0.30	77.90	1.51	84.61			
	4.4900	5.02	0.75	22.90	3.77	83.85	87.04		
	8.5400	5.02	1.50	33.70	7.53	88.17			
	12.7200	5.02	2.25	36.60	11.30	88.80			
	17.2400	5.02	3.00	38.80	15.06	87.35			

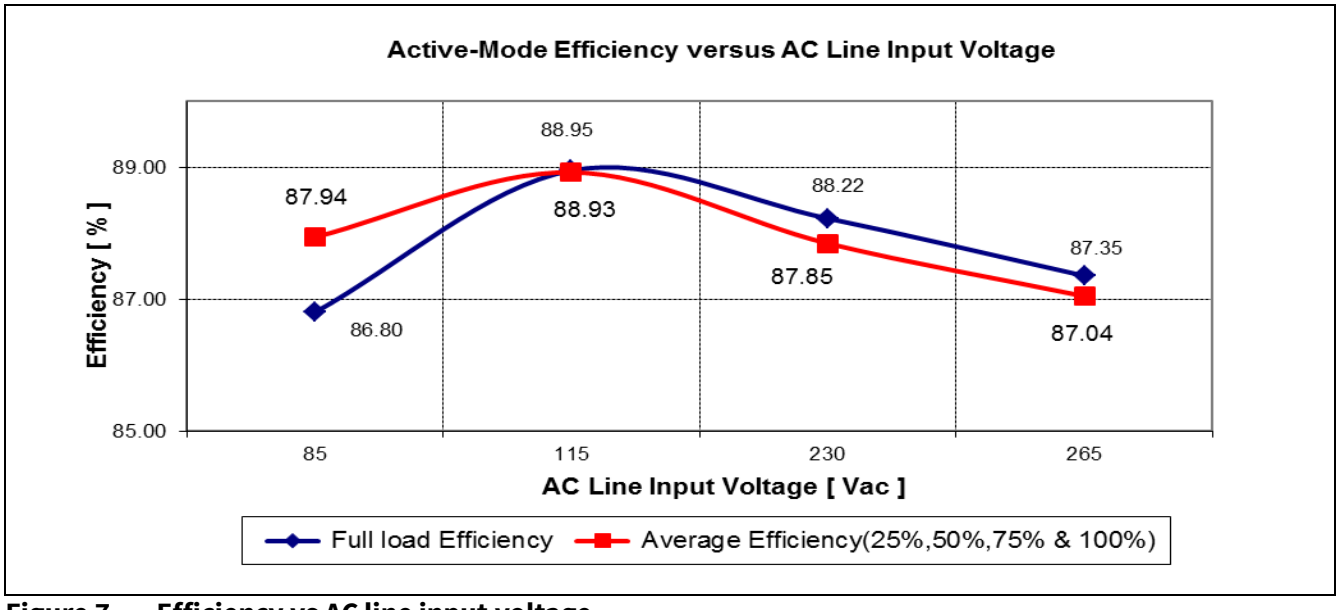


Figure 7 Efficiency vs AC line input voltage

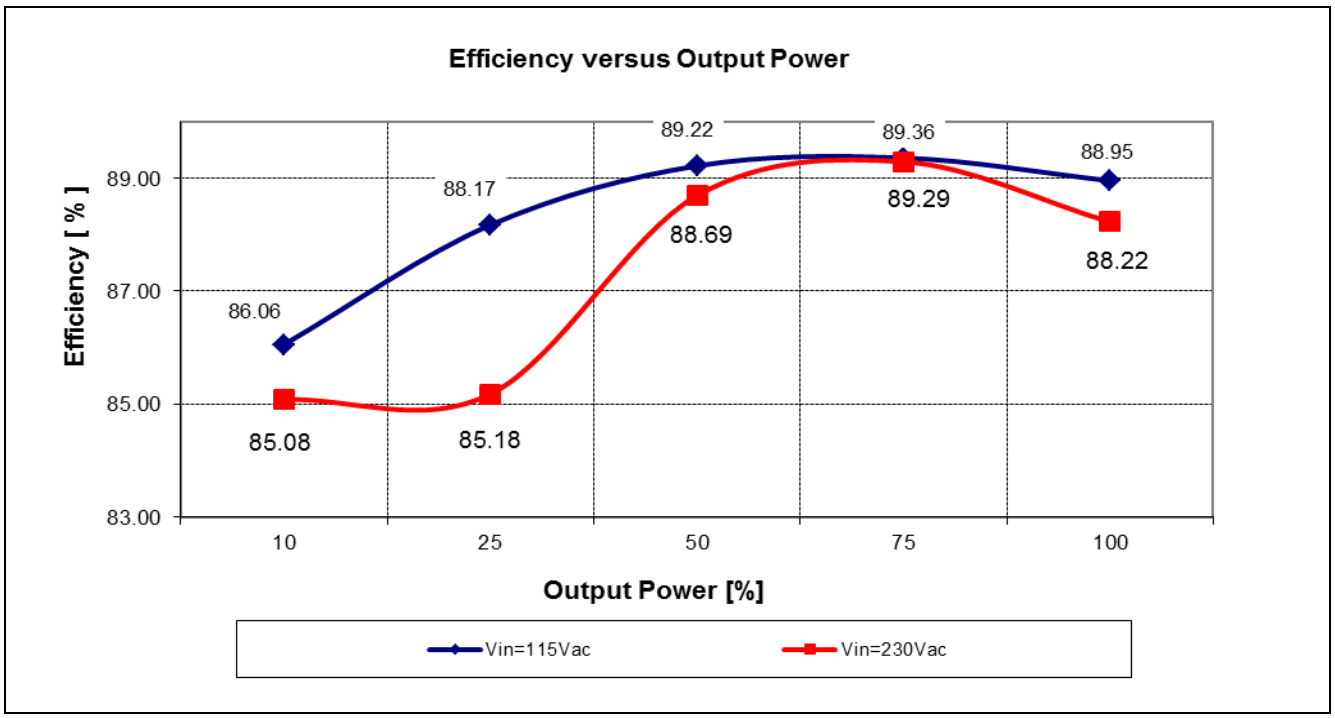


Figure 8 Efficiency vs output power @ 115Vac and 230V line

11.2 Standby power

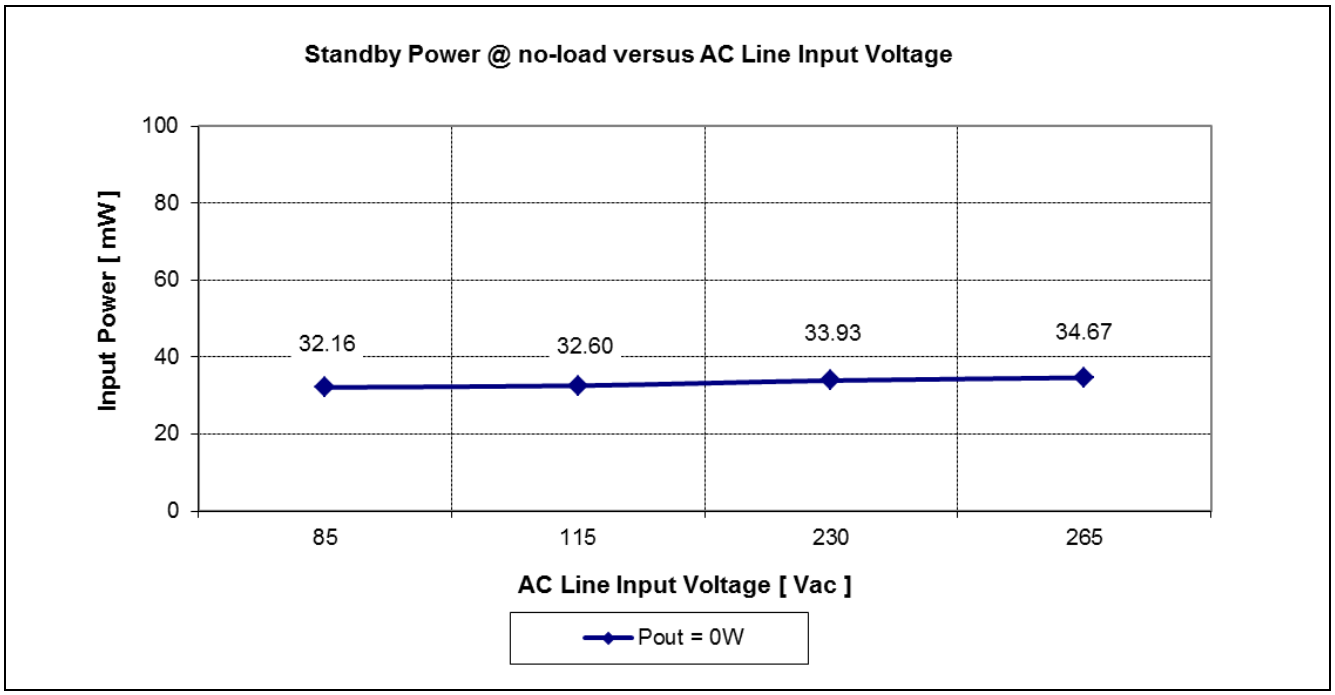


Figure 9 Standby power @ no load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

11.3 Line regulation

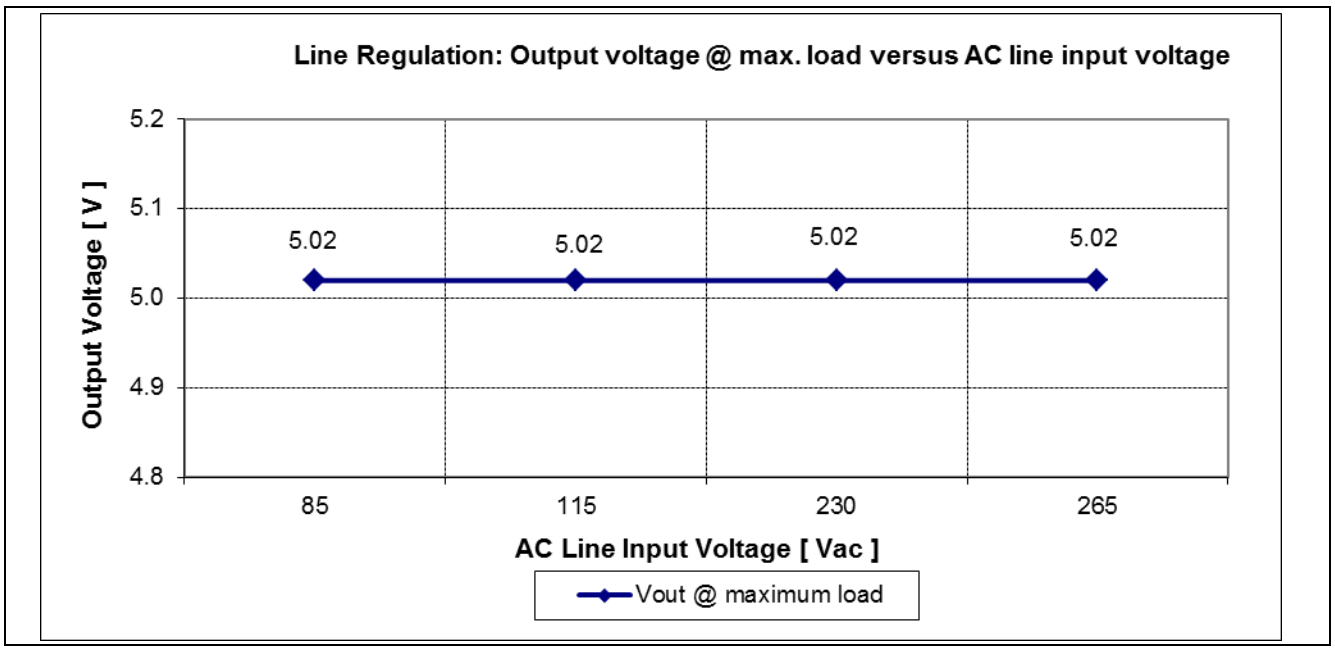


Figure 10 Line regulation V_{out} @ full load vs AC line input voltage

11.4 Load regulation

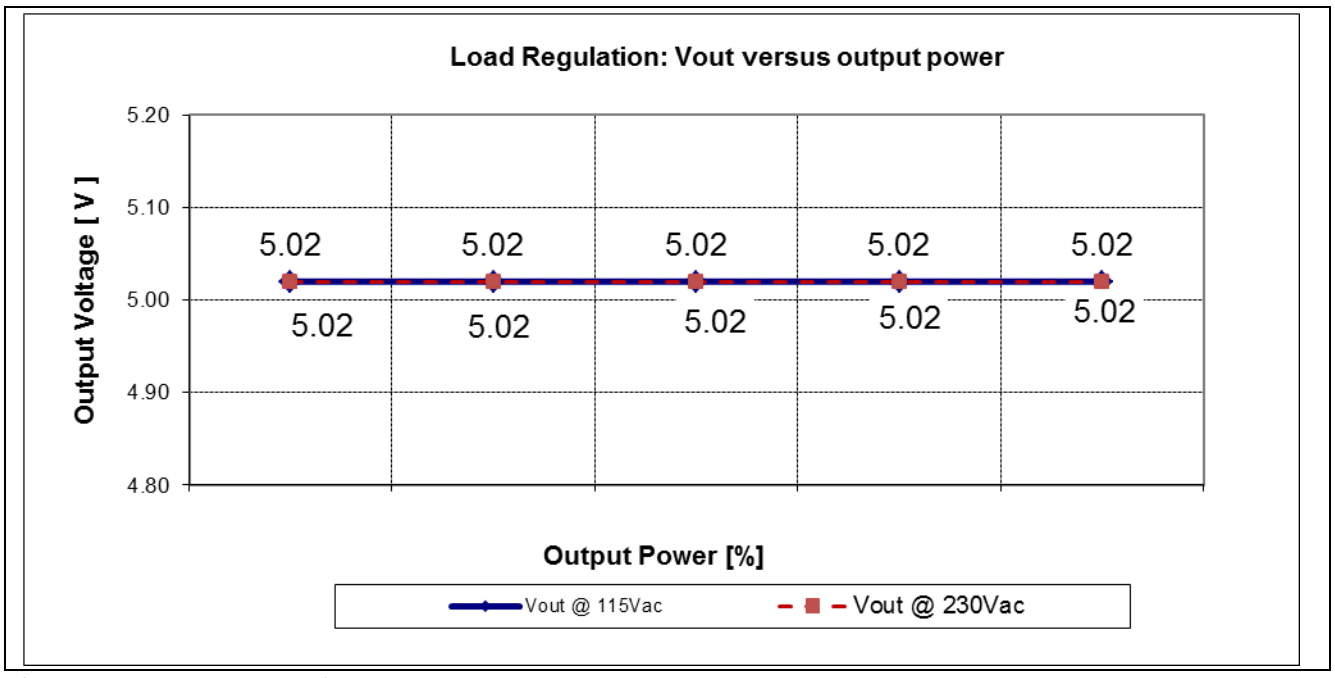


Figure 11 Load regulation V_{out} vs output power

11.5 Maximum power

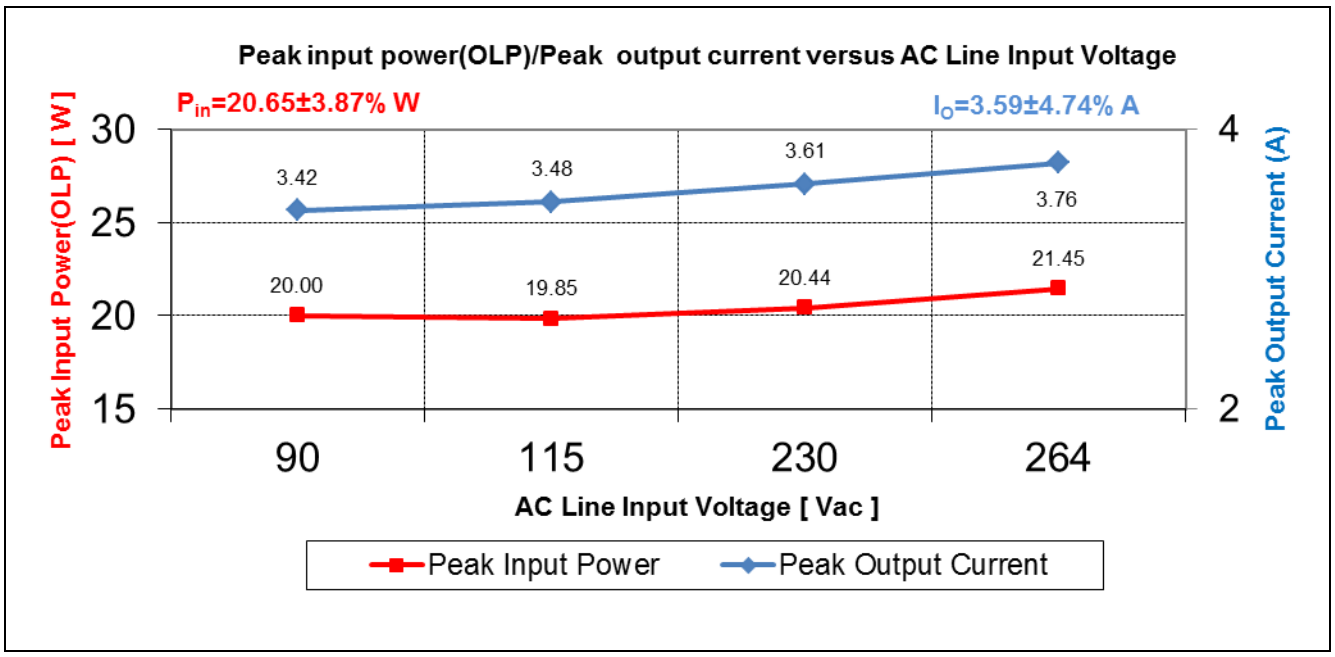


Figure 12 Maximum input power (before over-load protection) vs AC line input voltage

11.6 ESD immunity (EN61000-4-2)

Pass EN61000-4-2 level 3 (±6kV) contact discharge.

11.7 Surge immunity (EN61000-4-5)

Pass EN61000-4-5 Installation class 3 (2kV: common mode).

11.8 Conducted emissions (EN55022 class B)

The conducted EMI was measured by Schaffner (SMR25503) and followed the test standard of EN55022 (CISPR 22) class B. The demo board was set up at maximum load (15W) with input voltage of 115Vac and 230Vac.

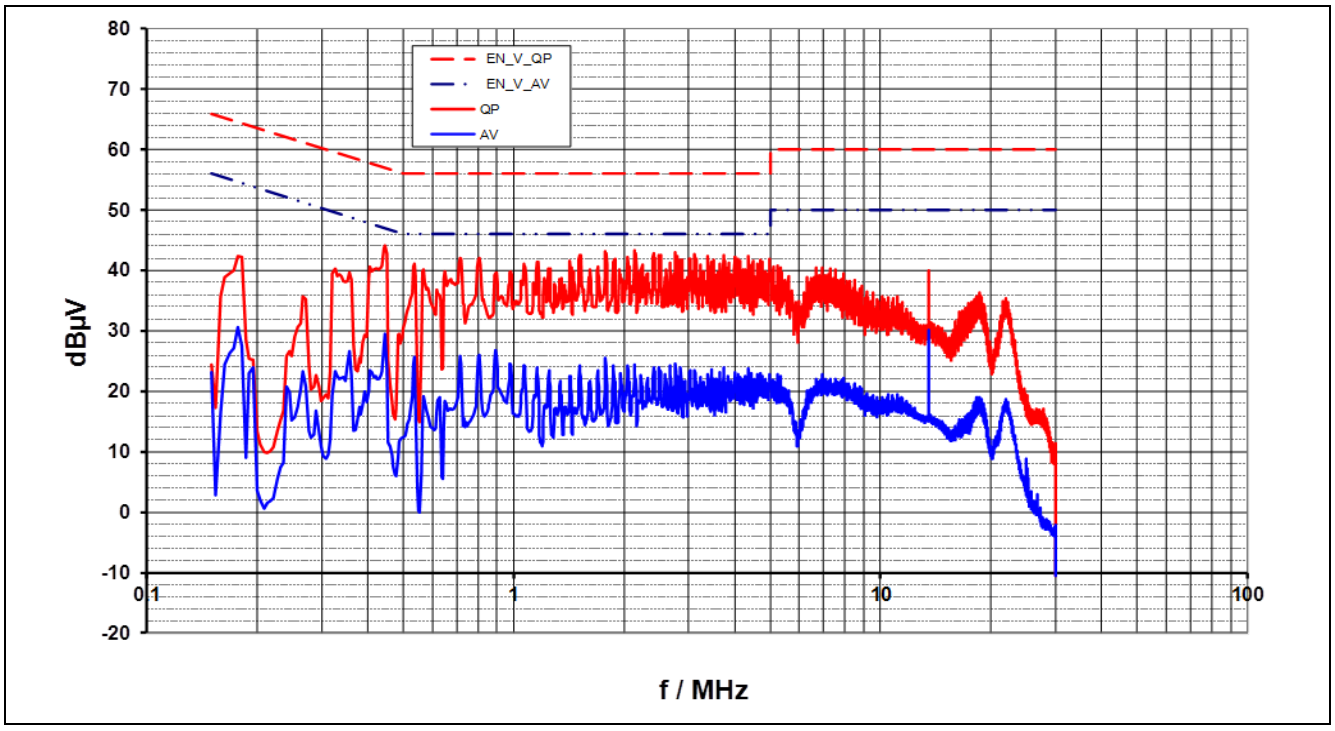


Figure 13 Conducted emissions(Line) at 115Vac and maximum Load

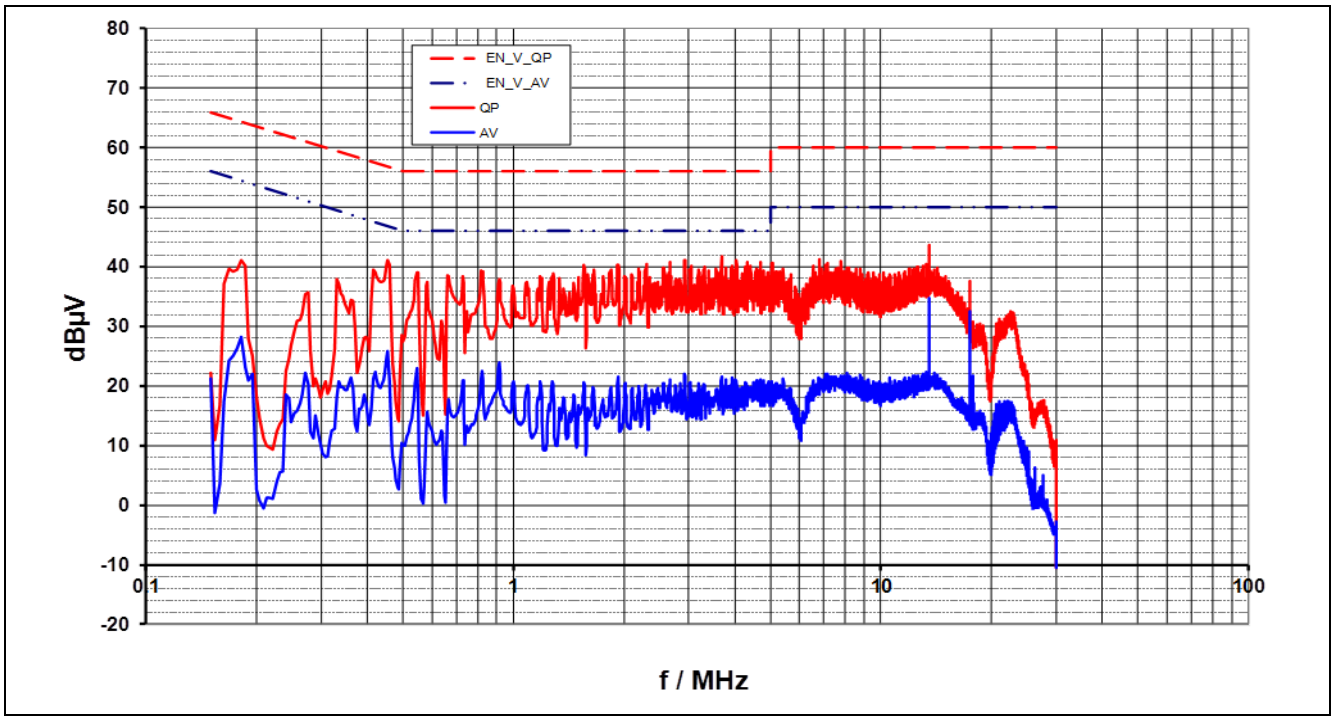


Figure 14 Conducted emissions(Neutral) at 115Vac and maximum Load

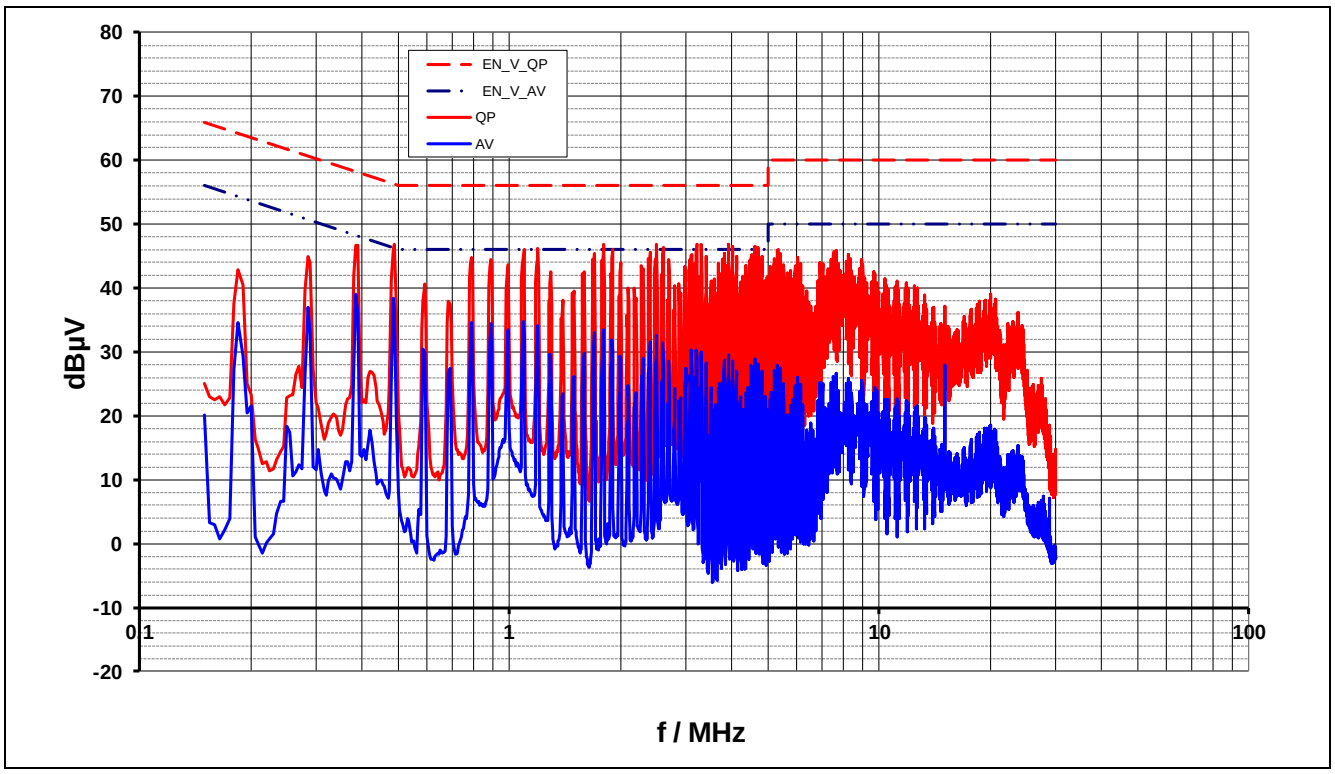


Figure 15 Conducted emissions(line) at 230Vac and maximum Load

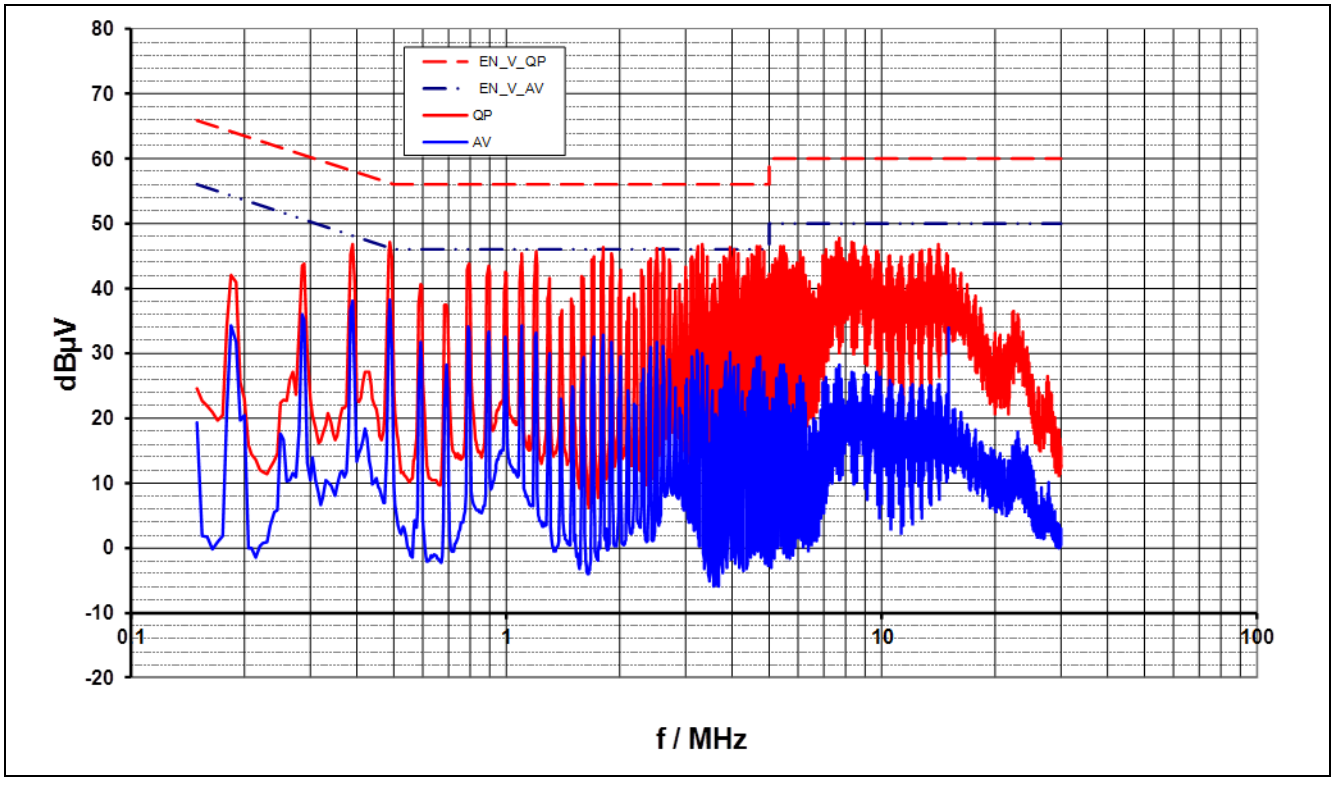
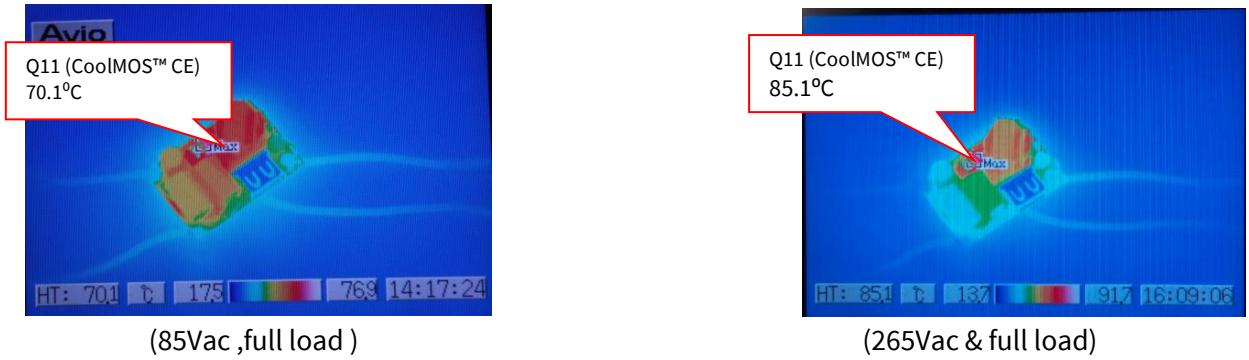


Figure 16 Conducted emissions(Neutral) at 230Vac and maximum Load

Pass conducted EMI EN55022 (CISPR 22) class B with > 8dB margin for QP.

11.9 Thermal measurement

The reference adapter's open frame thermal test was done by thermal infrared camera (TVS-500EX) at the ambient temperature 25°C. The thermal measures were taken after two hours running with full load and the highest temperature of Q11 (CoolMOS™ CE) is 70.1°C for low line and 85.1°C for high line.



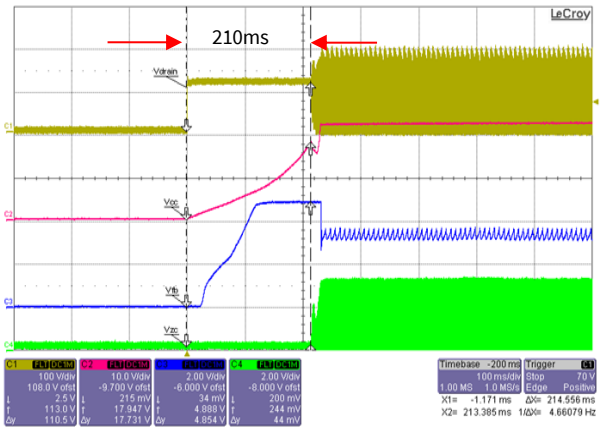
(85Vac ,full load) (265Vac & full load)

Figure 17 Infrared thermal image of REF-15W_CE1K0 ADAPTER

12 Waveforms and scope plots

All waveforms and scope plots were recorded with a LeCroy 6050 oscilloscope

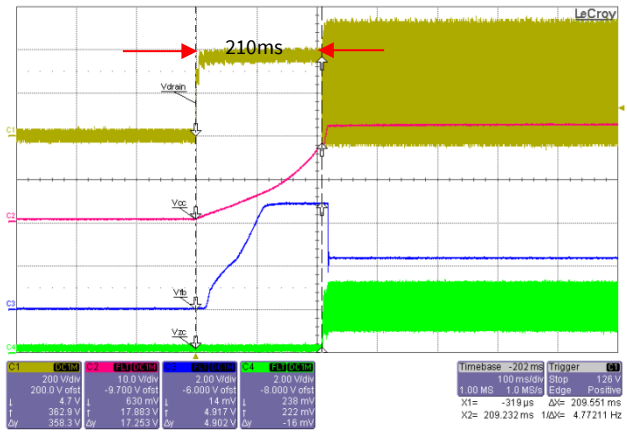
12.1 Start up at low/high AC line input voltage with maximum load



Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Startup time = 210ms

Figure 18 Startup @ 85Vac & max. load

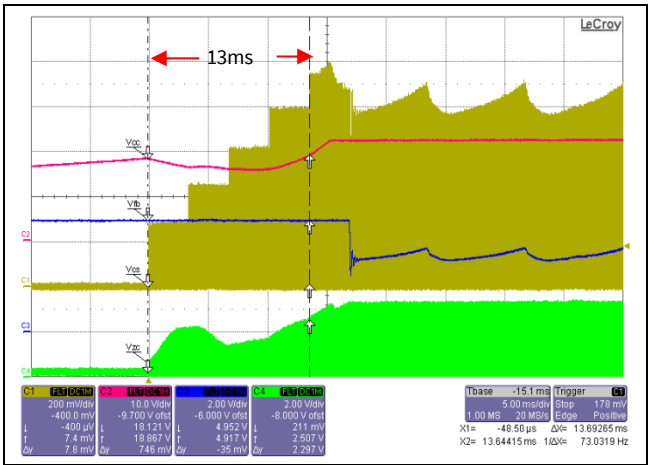


Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Startup time = 210ms

Figure 19 Startup @ 265Vac & max. load

12.2 Soft start

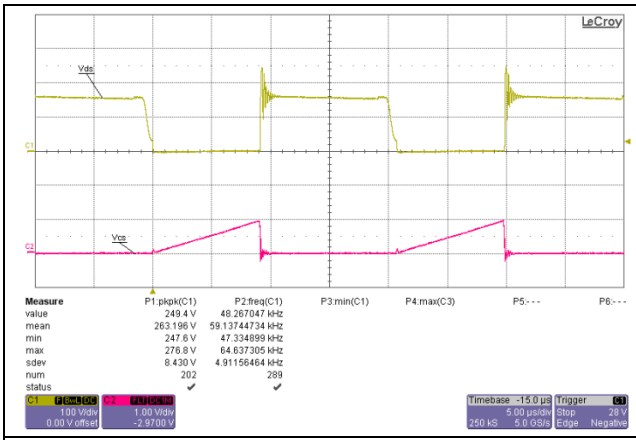


Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Soft Star time = 13ms

Figure 20 Soft Start @ 85Vac & max. load

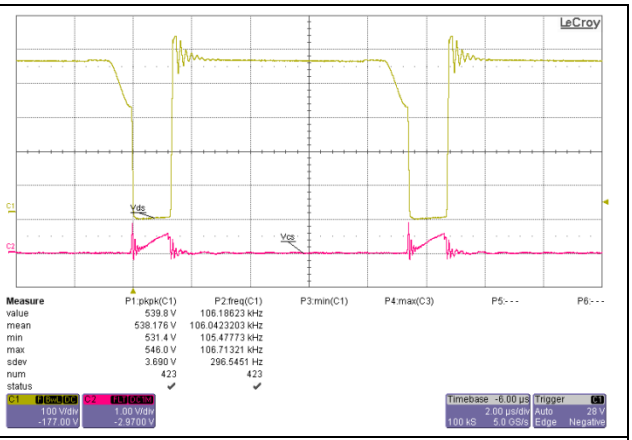
12.3 Drain voltage and current at maximum load



Channel 1; C1 : Drain-source voltage (V_{DS})
Channel 2; C2 : Current sense voltage (V_{CS})

V_{Drain_peak} = 276V

Figure 21 Operation @ 85Vac and max. load

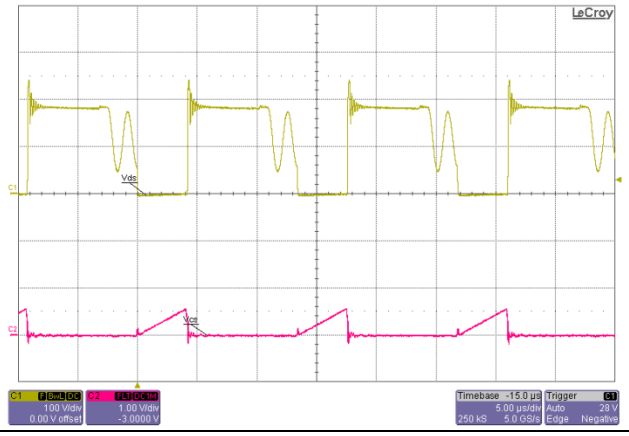


Channel 1; C1 : Drain-source voltage (V_{DS})
Channel 2; C2 : Current sense voltage (V_{CS})

V_{Drain_peak} = 546V

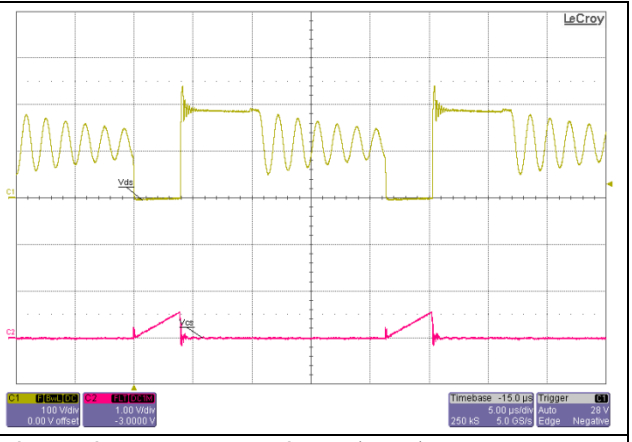
Figure 22 Operation @ 265Vac and max. load

12.4 Zero crossing point during normal operation



Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Current sense voltage (V_{CS})

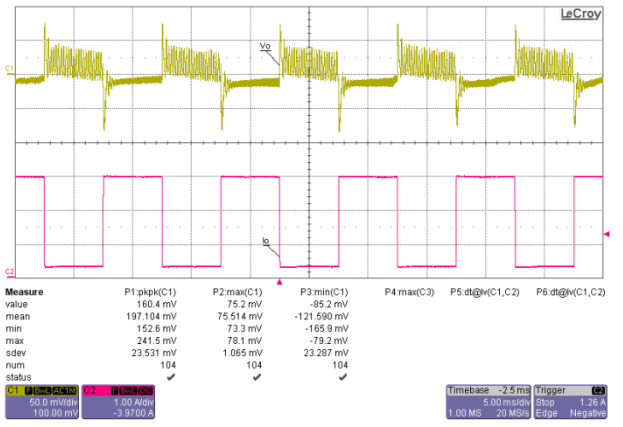
Figure 23 Operation @ 85Vac and 2nd zero crossing



Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Current sense voltage (V_{CS})

Figure 24 Operation @ 85Vac and 7th zero crossing

12.5 Load transient response (Dynamic load from 10% to 100%)

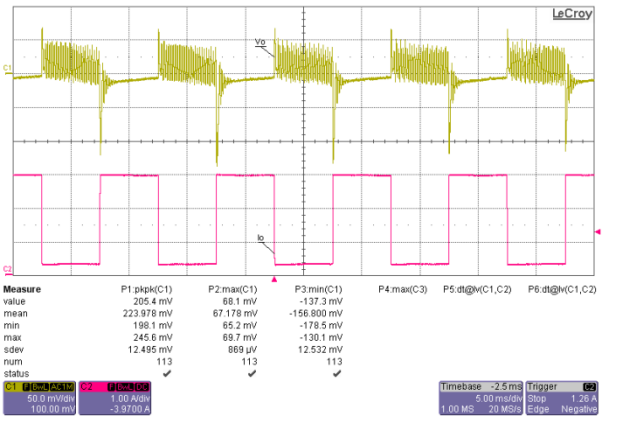


Channel 1; C1 : Output ripple voltage (V_{out})
Channel 2; C2 : Output current (I_{out})

$V_{ripple_pk_pk}$=241mV (Load change from10% to 100%,100Hz,0.4A/µS slew rate)

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 25 – Load transient response @ 85Vac



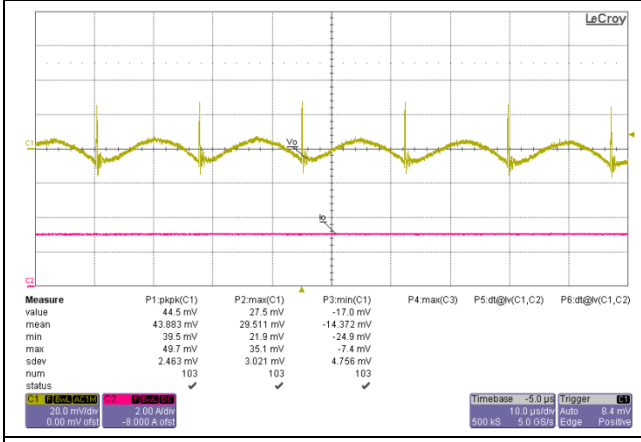
Channel 1; C1 : Output ripple voltage (V_{out})
Channel 2; C2 : Output current (I_{out})

$V_{ripple_pk_pk}$=245mV (Load change from10% to 100%,100Hz,0.4A/µS slew rate)

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 26 Load transient response @ 265Vac

12.6 Output ripple voltage at maximum load



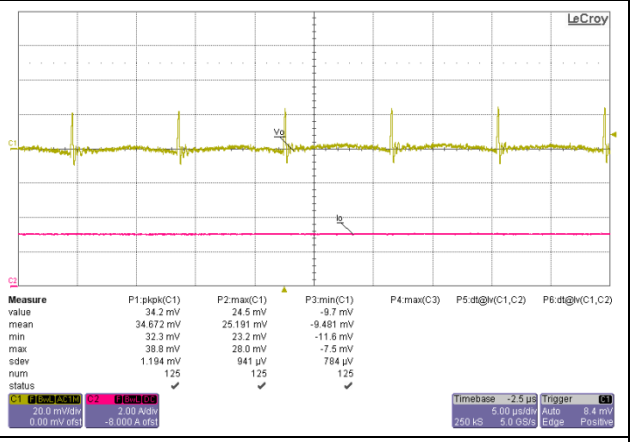
Channel 1; C1 : Output ripple voltage (V_{out})

Channel 2; C2 : Output current (I_{out})

$V_{ripple_pk_pk}$=49.7mV

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 27 AC output ripple @ 85Vac and max. load



Channel 1; C1 : Output ripple voltage (V_{out})

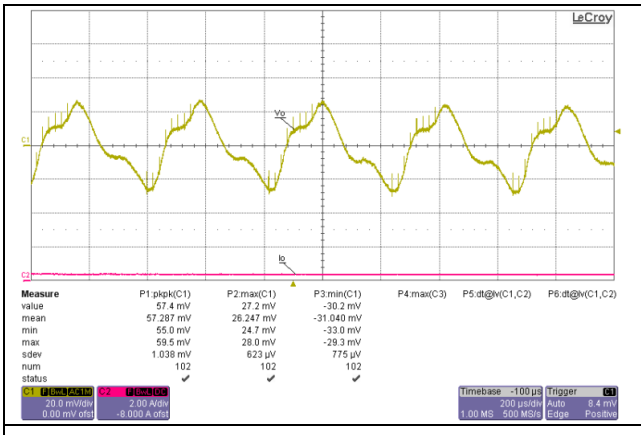
Channel 2; C2 : Output current (I_{out})

$V_{ripple_pk_pk}$ = 38.8mV

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 28 AC output ripple @ 265Vac and max. load

12.7 Output ripple voltage during burst mode at 1 W load



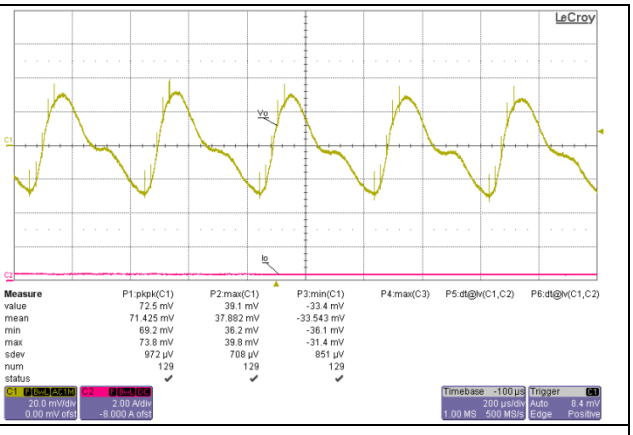
Channel 1; C1 : Output ripple voltage (V_{out})

Channel 2; C2 : Output current (I_{out})

$V_{ripple_pk_pk}$=59.5mV

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 29 AC output ripple @ 85Vac and 1W load



Channel 1; C1 : Output ripple voltage (V_{out})

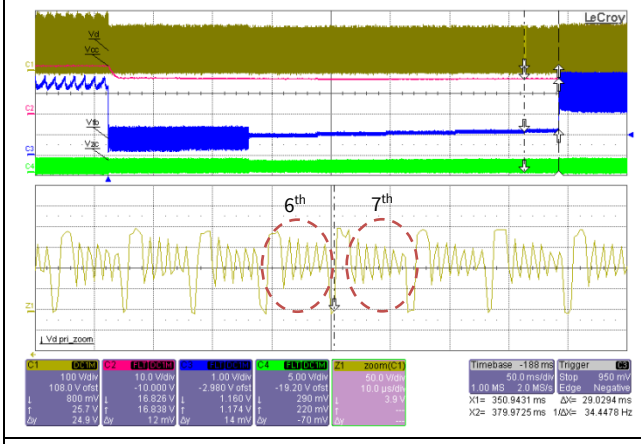
Channel 2; C2 : Output current (I_{out})

$V_{ripple_pk_pk}$ = 73.8mV

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 30 AC output ripple @ 265Vac and 1W load

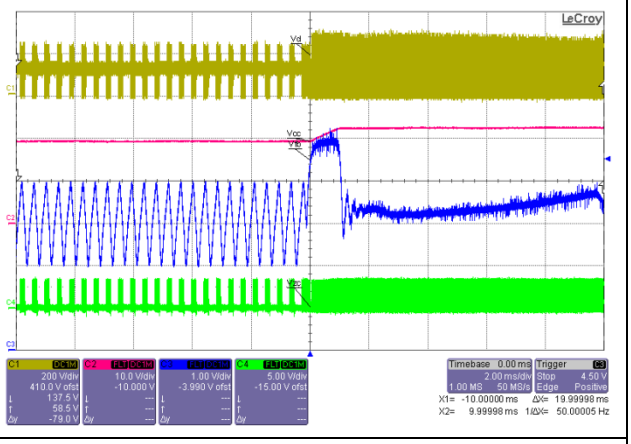
12.8 Active Burst mode operation



Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Condition: V_{FB}<1.2V, N_{ZC}=7 and $t_{blanking}$ =29ms
(load change form full load to 1W load)

Figure 31 Entering active burst mode @ 85Vac

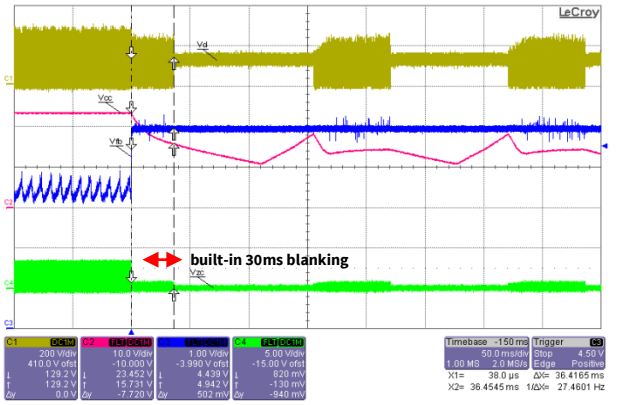


Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Condition: V_{FB}>4.5V
(load change from 1W to full load)

Figure 32 Leaving active burst mode @ 85Vac

12.9 Over load protection (Auto restart mode)

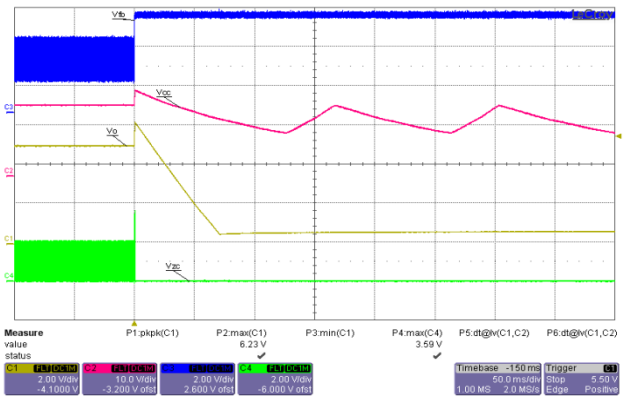


Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Condition: V_{FB}>4.5V & last for 30ms blanking time
(output load change from full load to short load)

Figure 33 Over load protection with extended blanking time @ 85Vac

12.10 Output overvoltage protection (Latched off mode)



Channel 1; C1 : Output voltage (V_{out})

Channel 2; C2 : Supply voltage (V_{CC})

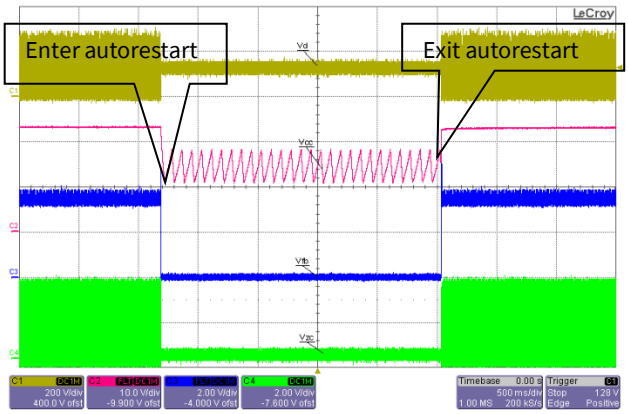
Channel 3; C3 : Feedback voltage (V_{FB})

Channel 4; C4 : Zero crossing voltage (V_{ZC})

Condition: V_O >5.5V (V_{ZC}>3.7V)(short R26 during while system operation at no load)

Figure 34 Output overvoltage protection @ 85Vac

12.11 V_{CC} under voltage/Short optocoupler protection (Auto restart mode)



Channel 1; C1 : Drain voltage (V_{Drain})

Channel 2; C2 : Supply voltage (V_{CC})

Channel 3; C3 : Feedback voltage (V_{FB})

Channel 4; C4 : Zero crossing voltage (V_{ZC})

V_{CC} under voltage/short optocoupler protection (short the transistor of optocoupler during system operating @ full load & release)

Figure 35 V_{CC} under voltage/short optocoupler protection @ 85Vac

13 References

[1] ICE2QS03G data sheet, Infineon Technologies AG

[2] IPS65R1K0CE data sheet, 650V CoolMOS™ CE Power Transistor, Infineon Technologies AG

[3] BSC067N06LS3 G data sheet, 60V OptiMOS™ 3 Power Transistor, Infineon Technologies AG

[4] BAS21-03W data sheet, Infineon Technologies AG

[5] Converter Design Using the Quasi-Resonant PWM Controller ICE2QS01, Infineon Technologies AG, 2006. [ANPS0003]

[6] Design tips for flyback converters using the Quasi-Resonant PWM controller ICE2QS01, Infineon Technologies, 2006. [ANPS0005]

[7] Determine the switching frequency of Quasi-Resonant flyback converters designed with ICE2QS01, Infineon Technologies, 2006. [ANPS0004]

[8] ICE2QS03G design guide. [ANPS0027]

[9] 36W Evaluation Board with Quasi-Resonant PWM Controller ICE2QS03G, 2011. [AN-PS0040]

Revision History

Major changes since the last revision

Page or Reference	Description of change
1,2,4,5,6,8,11,12,14,15,16,17,20,22, 23 & 25	Make consistent symbol

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