Active Energy Metering IC with di/dt Sensor Interface

ADE7759*

FEATURES

High Accuracy, Supports IEC 687/1036
On-Chip Digital Integrator Allows Direct Interface with Current Sensors with di/dt Output Such as Rogowski Coil
Less Than 0.1% Error over a Dynamic Range of 1000 to 1
On-Chip User-Programmable Threshold for Line Voltage SAG Detection and PSU Supervisory
Supplies Sampled Waveform Data and Active Energy (40 Bits)
Digital Power, Phase, and Input DC Offset Calibration
On-Chip Temperature Sensor (Typical 1 LSB/°C Resolution)
SPI Compatible Serial Interface
Pulse Output with Programmable Frequency
Interrupt Request Pin (IRQ) and IRQ Status Register
Proprietary ADCs and DSP provide High Accuracy over Large Variations in Environmental Conditions and Time
Reference 2.4 V ± 8% (20 ppm/°C Typical) with External Overdrive Capability
Single 5 V Supply, Low Power Consumption (25 mW Typical)

GENERAL DESCRIPTION

The ADE7759 is an accurate active power and energy measurement IC with a serial interface and a pulse output. The ADE7759 incorporates two second-order Σ-Δ ADCs, a digital integrator (on CH1), reference circuitry, temperature sensor, and all the signal processing required to perform active power and energy measurement.

An on-chip digital integrator allows direct interface to di/dt current sensors such as a Rogowski coil. The digital integrator eliminates the need for an external analog integrator and provides excellent long-term stability and precise phase matching between the current and the voltage channels. The integrator can be switched off if the ADE7759 is used with conventional current sensors.

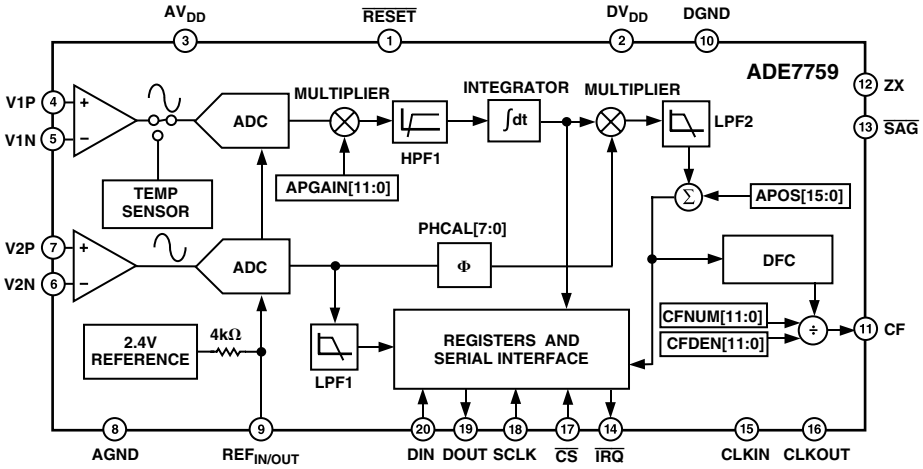
The ADE7759 contains a sampled waveform register and an active energy register capable of holding at least 11.53 seconds of accumulated power at full ac load. Data is read from the ADE7759 via the serial interface. The ADE7759 also provides a pulse output (CF) with frequency that is proportional to the active power.

In addition to active power information, the ADE7759 also provides various system calibration features, i.e., channel offset correction, phase calibration, and power offset correction. The part also incorporates a detection circuit for short duration voltage drop (SAG). The voltage threshold and the duration (in number of half-line cycles) of the drop are user programmable. An open-drain logic output ($\overline{SAG}$) goes active low when a sag event occurs.

A zero crossing output (ZX) produces an output that is synchronized to the zero crossing point of the line voltage. This output can be used to extract timing or frequency information from the line. The signal is also used internally to the chip in the line cycle energy accumulation mode; i.e., the number of half-line cycles in which the energy accumulation occurs can be controlled. Line cycle energy accumulation enables a faster and more precise energy accumulation and is especially useful during calibration. This signal is also useful for synchronization of relay switching with a voltage zero crossing.

The interrupt request output is an open drain, active low logic output. The interrupt status register indicates the nature of the interrupt, and the interrupt enable register controls which event produces an output on the $\overline{IRQ}$ pin. The ADE7759 is available in a 20-lead SSOP package.

FUNCTIONAL BLOCK DIAGRAM



*U.S. Patents 5,745,323; 5,760,617; 5,862,069;5,872,469.

REV. A

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TABLE OF CONTENTS

FEATURES 1
GENERAL DESCRIPTION 1
FUNCTIONAL BLOCK DIAGRAM 1
SPECIFICATIONS 3
TIMING CHARACTERISTICS 5
ABSOLUTE MAXIMUM RATINGS 6
ORDERING GUIDE 6
PIN CONFIGURATION 7
PIN FUNCTION DESCRIPTIONS 7
TERMINOLOGY 8
MEASUREMENT ERROR 8
PHASE ERROR BETWEEN CHANNELS 8
POWER SUPPLY REJECTION 8
ADC OFFSET ERROR 8
GAIN ERROR 8
GAIN ERROR MATCH 8
TYPICAL PERFORMANCE CHARACTERISTICS (TPC) . . 9
TEST CIRCUITS 11
ANALOG INPUTS 11
di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR 12
ZERO CROSSING DETECTION 13
LINE VOLTAGE SAG DETECTION 14
Sag Level Set 14
POWER SUPPLY MONITOR 14
INTERRUPTS 15
Using the ADE7759 Interrupts with an MCU 15
Interrupt Timing 15
TEMPERATURE MEASUREMENT 16
ANALOG-TO-DIGITAL CONVERSION 16
Antialias Filter 16
ADC Transfer Function 17
Reference Circuit 17
CHANNEL 1 ADC 17
Channel 1 ADC Gain Adjust 18
Channel 1 Sampling 18
CHANNEL 1 AND CHANNEL 2 WAVEFORM SAMPLING MODE 18
CHANNEL 2 ADC 19
Channel 2 Sampling 19
PHASE COMPENSATION 19
ACTIVE POWER CALCULATION 20
ENERGY CALCULATION 21
Integration Time under Steady Load 22
POWER OFFSET CALIBRATION 22
ENERGY-TO-FREQUENCY CONVERSION 22
LINE CYCLE ENERGY ACCUMULATION MODE . . . 24
CALIBRATING THE ENERGY METER 24
Calculating the Average Active Power 24
Calibrating the Frequency at CF 25
Energy Meter Display 25
CLKIN FREQUENCY 25
SUSPENDING THE ADE7759 FUNCTIONALITY 26
APPLICATION INFORMATION 26
SERIAL INTERFACE 26
Serial Write Operation 26
Serial Read Operation 27
CHECKSUM REGISTER 28
REGISTER DESCRIPTIONS 30
Communications Register 30
Mode Register (06H) 31
Interrupt Status Register (04H) 32
Reset Interrupt Status Register (05H) 32
CH1OS Register (08H) 33
OUTLINE DIMENSIONS 34
REVISION HISTORY 35

SPECIFICATIONS[1] (AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 3.579545 MHz XTAL, T_{MIN} to T_{MAX} = –40°C to +85°C, unless otherwise noted.)

Parameter	Spec	Unit	Test Conditions/Comments
ENERGY MEASUREMENT ACCURACY			
Measurement Bandwidth	14	kHz	CLKIN = 3.579545 MHz
Measurement Error[1] on Channel 1			Channel 2 = 300 mV rms/60 Hz, Gain = 1
Channel 1 Range = 0.5 V Full-Scale			
Gain = 1	0.1	% typ	Over a Dynamic Range 1000 to 1
Gain = 2	0.1	% typ	Over a Dynamic Range 1000 to 1
Gain = 4	0.1	% typ	Over a Dynamic Range 1000 to 1
Gain = 8	0.1	% typ	Over a Dynamic Range 1000 to 1
Gain = 16	0.2	% typ	Over a Dynamic Range 1000 to 1
Channel 1 Range = 0.25 V Full-Scale			
Gain = 1	0.1	% typ	Over a Dynamic Range 1000 to 1
Gain = 2	0.1	% typ	Over a Dynamic Range 1000 to 1
Gain = 4	0.1	% typ	Over a Dynamic Range 1000 to 1
Gain = 8	0.2	% typ	Over a Dynamic Range 1000 to 1
Gain = 16	0.2	% typ	Over a Dynamic Range 1000 to 1
Channel 1 Range = 0.125 V Full-Scale			
Gain = 1	0.1	% typ	Over a Dynamic Range 1000 to 1
Gain = 2	0.1	% typ	Over a Dynamic Range 1000 to 1
Gain = 4	0.2	% typ	Over a Dynamic Range 1000 to 1
Gain = 8	0.2	% typ	Over a Dynamic Range 1000 to 1
Gain = 16	0.4	% typ	Over a Dynamic Range 1000 to 1
Phase Error[1] between Channels	±0.05	° max	Line Frequency = 45 Hz to 65 Hz, HPF on
AC Power Supply Rejection[1]			AV_{DD} = DV_{DD} = 5 V + 175 mV rms/120 Hz
Output Frequency Variation (CF)	0.2	% typ	Channel 1 = 20 mV rms/60 Hz, Gain = 16, Range = 0.5 V Channel 2 = 300 mV rms/60 Hz, Gain = 1
DC Power Supply Rejection[1]			AV_{DD} = DV_{DD} = 5 V ± 250 mV dc
Output Frequency Variation (CF)	±0.3	% typ	Channel 1 = 20 mV rms/60 Hz, Gain = 16, Range = 0.5 V Channel 2 = 300 mV rms/60 Hz, Gain = 1
ANALOG INPUTS[3]			
Maximum Signal Levels	±0.5	V max	V1P, V1N, V2N, and V2P to AGND
Input Impedance (DC)	390	kΩ min	
Bandwidth	14	kHz	CLKIN/256, CLKIN = 3.579545 MHz
Gain Error[1, 3]			External 2.5 V Reference, Gain = 1 on Channels 1 and 2
Channel 1			
Range = 0.5 V Full-Scale	±4	% typ	V1 = 0.5 V dc
Range = 0.25 V Full-Scale	±4	% typ	V1 = 0.25 V dc
Range = 0.125 V Full-Scale	±4	% typ	V1 = 0.125 V dc
Channel 2	±4	% typ	V2 = 0.5 V dc
Gain Error Match[1]			External 2.5 V Reference
Channel 1			
Range = 0.5 V Full-Scale	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Range = 0.25 V Full-Scale	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Range = 0.125 V Full-Scale	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Channel 2	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Offset Error[1]			
Channel 1	±20	mV max	Gain = 1
Channel 2	±20	mV max	Gain = 1
WAVEFORM SAMPLING			Sampling CLKIN/128, 3.579545 MHz/128 = 27.9 kSPS
Channel 1			See Channel 1 Sampling
Signal-to-Noise plus Distortion	62	dB typ	150 mV rms/60 Hz, Range = 0.5 V, Gain = 2
Bandwidth (–3 dB)	14	kHz	CLKIN = 3.579545 MHz
Channel 2			See Channel 2 Sampling
Signal-to-Noise plus Distortion	52	dB typ	150 mV rms/60 Hz, Gain = 2
Bandwidth (–3 dB)	156	Hz	CLKIN = 3.579545 MHz

Parameter	Spec	Unit	Test Conditions/Comments
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.6	V max	2.4 V + 8%
	2.2	V min	2.4 V – 8%
Input Capacitance	10	pF max	
ON-CHIP REFERENCE			Nominal 2.4 V at $REF_{IN/OUT}$ Pin
Reference Error	±200	mV max	
Current Source	10	µA max	
Output Impedance	4	kΩ min	
Temperature Coefficient	20	ppm/°C typ	
CLKIN			Note All Specifications CLKIN of 3.579545 MHz
Input Clock Frequency	4	MHz max	
	1	MHz min	
LOGIC INPUTS			
$\overline{RESET}$, DIN, SCLK, CLKIN, and $\overline{CS}$			
Input High Voltage, V_{INH}	2.4	V min	DV_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	DV_{DD} = 5 V ± 5%
Input Current, I_{IN}	±3	µA max	Typically 10 nA, V_{IN} = 0 V to DV_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS			
$\overline{SAG}$ and $\overline{IRQ}$			Open Drain Outputs, 10 kΩ pull-up resistor
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
ZX and DOUT			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
CF			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	1	V max	I_{SINK} = 7 mA
POWER SUPPLY			For Specified Performance
AV_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
DV_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
AI_{DD}	3	mA max	Typically 2.0 mA
DI_{DD}	4	mA max	Typically 3.0 mA

NOTES
[1]See Terminology section for explanation of specifications.
[2]See plots in Typical Performance Characteristics.
[3]See Analog Inputs section.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 3.579545 MHz XTAL, T_{MIN} to T_{MAX} = –40°C to +85°C, unless otherwise noted.)

Parameter	A, B Versions	Unit	Test Conditions/Comments
Write Timing			
t_1	20	ns (min)	$\overline{CS}$ Falling Edge to First SCLK Falling Edge
t_2	150	ns (min)	SCLK Logic High Pulsewidth
t_3	150	ns (min)	SCLK Logic Low Pulsewidth
t_4	10	ns (min)	Valid Data Setup Time before Falling Edge of SCLK
t_5	5	ns (min)	Data Hold Time after SCLK Falling Edge
t_6	6.4	µs (min)	Minimum Time between the End of Data Byte Transfers
t_7	4	µs (min)	Minimum Time between Byte Transfers during a Serial Write
t_8	100	ns (min)	$\overline{CS}$ Hold Time after SCLK Falling Edge
Read Timing			
t_9	4	µs (min)	Minimum Time between Read Command (i.e., a Write to Communications Register) and Data Read
t_{10}	4	µs (min)	Minimum Time between Data Byte Transfers during a Multibyte Read
t_{11}[3]	30	ns (min)	Data Access Time after SCLK Rising Edge following a Write to the Communications Register
t_{12}[4]	100	ns (max)	Bus Relinquish Time after Falling Edge of SCLK
	10	ns (min)	
t_{13}[4]	100	ns (max)	Bus Relinquish Time after Rising Edge of $\overline{CS}$
	10	ns (min)	

NOTES
[1]Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5 ns (10% to 90%) and timed from a voltage level of 1.6 V.
[2]See Figures 2 and 3 and Serial Interface section of this data sheet.
[3]Measured with the load circuit in Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.
[4]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

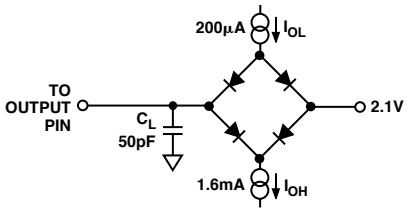


Figure 1. Load Circuit for Timing Specifications

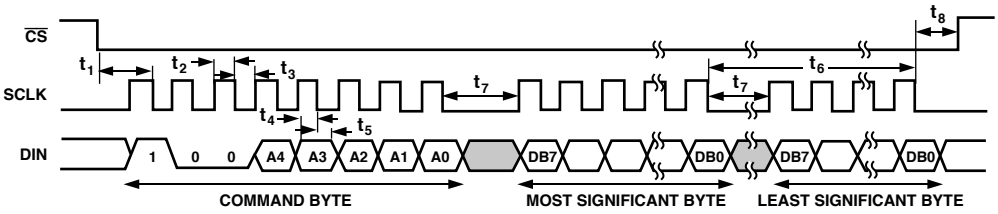


Figure 2. Serial Write Timing

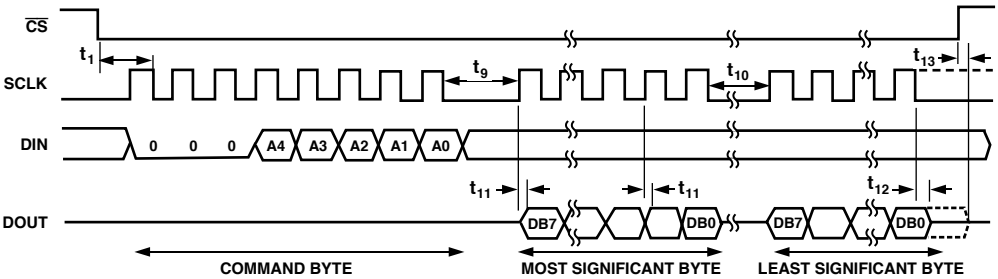


Figure 3. Serial Read Timing

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

AV_{DD} to AGND . . . . . –0.3 V to +7 V
DV_{DD} to DGND . . . . . –0.3 V to +7 V
DV_{DD} to AV_{DD} . . . . . –0.3 V to +0.3 V
Analog Input Voltage to AGND
V1P, V1N, V2P, and V2N . . . . . –6 V to +6 V
Reference Input Voltage to AGND . . –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND . . . –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Industrial (A, B Versions) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
20-Lead SSOP, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 112°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

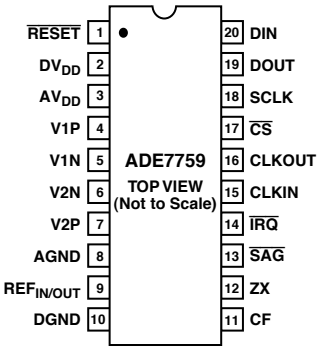
Model	Package Option*
ADE7759ARS	RS-20
ADE7759ARSRL	RS-20
EVAL-ADE7759EB	ADE7759 Evaluation Board

*RS = Shrink Small Outline Package in tubes; RSRL = Shrink Small Outline Package in reel.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADE7759 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Reset Pin for the ADE7759. A logic low on this pin will hold the ADCs and digital circuitry (including the serial interface) in a reset condition.
2	DV_{DD}	Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7759. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled to DGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
3	AV_{DD}	Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the ADE7759. The supply should be maintained at 5 V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling method. This pin should be decoupled to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
4, 5	V1P, V1N	Analog Inputs for Channel 1. This channel is intended for use with the di/dt current transducers such as Rogowski coil, or other current sensors such as shunt or current transformer (CT). These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5 V, ±0.25 V, and ±0.125 V, depending on the full-scale selection—see Analog Inputs section. Channel 1 also has a PGA with gain selections of 1, 2, 4, 8, or 16. The maximum signal level at these pins with respect to AGND is ±0.5 V. Both inputs have internal ESD protection circuitry. In addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
6, 7	V2N, V2P	Analog Inputs for Channel 2. This channel is intended for use with the voltage transducer. These inputs are fully differential voltage inputs with a maximum differential signal level of ±0.5 V. Channel 2 also has a PGA with gain selections of 1, 2, 4, 8, or 16. The maximum signal level at these pins with respect to AGND is ±0.5 V. Both inputs have internal ESD protection circuitry, and an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
8	AGND	This pin provides the ground reference for the analog circuitry in the ADE7759, i.e., ADCs and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, e.g., antialiasing filters, current and voltage transducers. To keep ground noise around the ADE7759 to a minimum, the quiet ground plane should be connected to the digital ground plane at only one point. It is acceptable to place the entire device on the analog ground plane—see Application Information section.
9	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.4 V ± 8% and a typical temperature coefficient of 20 ppm/°C. An external reference source may be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF capacitor in parallel with a 100 nF capacitor.
10	DGND	This provides the ground reference for the digital circuitry in the ADE7759, i.e., multiplier, filters, and frequency output (CF). Because the digital return currents in the ADE7759 are small, it is acceptable to connect this pin to the analog ground plane of the system—see Application Information section. However, high bus capacitance on the DOUT pin may result in noisy digital current that affects performance.
11	CF	Calibration Frequency Logic Output. The CF logic output gives Active Power information. This output is intended to be used for operational and calibration purposes. The full-scale output frequency can be adjusted by writing to the APGAIN, CFNUM, and CFDEN registers—see Energy to Frequency Conversion section.

PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Description
12	ZX	Voltage Waveform (Channel 2) Zero Crossing Output. This output toggles logic high and low at the zero crossing of the differential signal on Channel 2—see Zero Crossing Detection section.
13	$\overline{SAG}$	This open-drain logic output goes active low when either no zero crossings are detected or a low voltage threshold (Channel 2) is crossed for a specified duration—see Line Voltage Sag Detection section.
14	$\overline{IRQ}$	Interrupt Request Output. This is an active low open-drain logic output. Maskable interrupts include active energy register rollover, active energy register at half-full, zero crossing, $\overline{SAG}$, and arrivals of new waveform samples—see Interrupts section.
15	CLKIN	Master Clock for ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7759. The clock frequency for specified operation is 3.579545 MHz. Ceramic load capacitors of between 10 pF and 30 pF should be used with the gate oscillator circuit. Refer to crystal manufacturer's data sheet for load capacitance requirements.
16	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the ADE7759. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
17	$\overline{CS}$	Chip Select. Part of the 4-wire SPI serial interface. This active low logic input allows the ADE7759 to share the serial bus with several other devices—see Serial Interface section.
18	SCLK	Serial Clock Input for the Synchronous serial interface. All serial data transfers are synchronized to this clock—see Serial Interface section. The SCLK has a Schmitt-trigger input for use with a clock source that has a slow edge transition time, e.g., opto-isolator outputs.
19	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin on the rising edge of SCLK. This logic output is normally in a high impedance state unless it is driving data onto the serial data bus—see Serial Interface section.
20	DIN	Data Input for the Serial Interface. Data is shifted in at this pin on the falling edge of SCLK—see Serial Interface section.

TERMINOLOGY

MEASUREMENT ERROR

The error associated with the energy measurement made by the ADE7759 is defined by the following formula:

$$\textit{Percentage Error} = \frac{\textit{Energy registered by the ADE7759} - \textit{True Energy}}{\textit{True Energy}}$$

PHASE ERROR BETWEEN CHANNELS

The digital integrator and the HPF1 (High-Pass Filter) in Channel 1 have nonideal phase response. To offset this phase response and equalize the phase response between channels, two phase correction networks are placed in Channel 1: one for the digital integrator and the other for the HPF1. Each phase correction network corrects the phase response of the corresponding component and ensures a phase match between Channel 1 (current) and Channel 2 (voltage) to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range 40 Hz to 1 kHz.

POWER SUPPLY REJECTION

This quantifies the ADE7759 measurement error as a percentage of reading when the power supplies are varied.

For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when an ac (175 mV rms/120 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see Measurement Error definition above. For the dc PSR measurement a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±5%. Any error introduced is again expressed as a percentage of reading.

ADC OFFSET ERROR

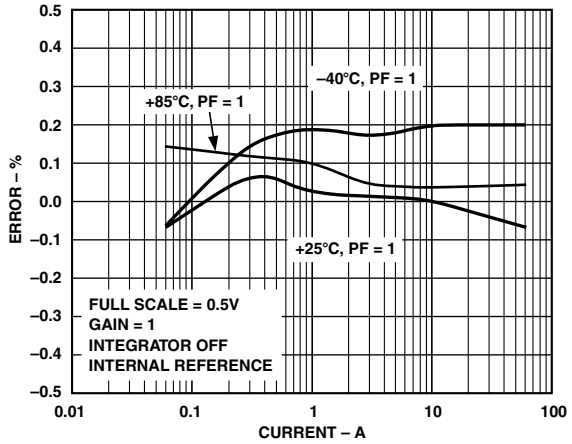
This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection—see Typical Performance Characteristics. However, when HPF1 is switched on, the offset is removed from Channel 1 (current) and the power calculation is not affected by this offset. The offsets may be removed by performing an offset calibration—see Analog Inputs section.

GAIN ERROR

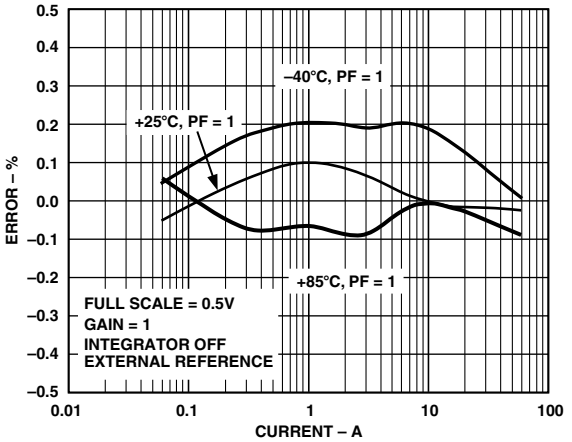
The gain error in the ADE7759 ADCs is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code—see Channel 1 ADC and Channel 2 ADC. It is measured for each of the input ranges on Channel 1 (0.5 V, 0.25 V, and 0.125 V). The difference is expressed as a percentage of the ideal code.

GAIN ERROR MATCH

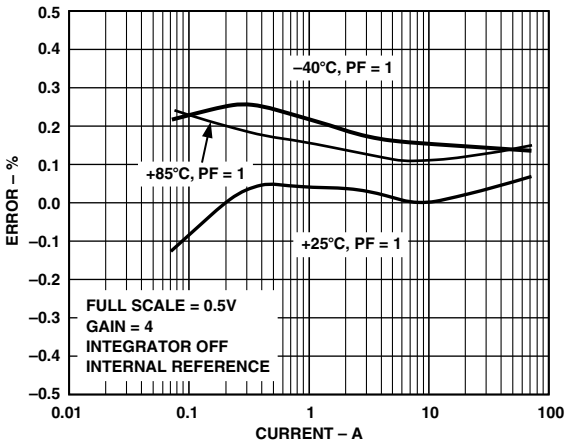
The Gain Error Match is defined as the gain error (minus the offset) obtained when switching between a gain of 1 (for each of the input ranges) and a gain of 2, 4, 8, or 16. It is expressed as a percentage of the output ADC code obtained under a gain of 1. This gives the gain error observed when the gain selection is changed from 1 to 2, 4, 8, or 16.



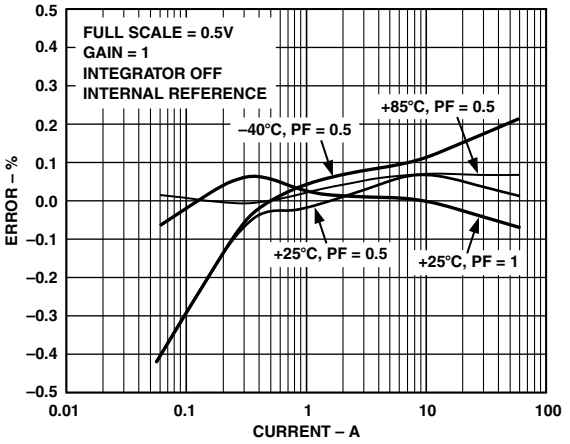
TPC 1. Error as a % of Reading



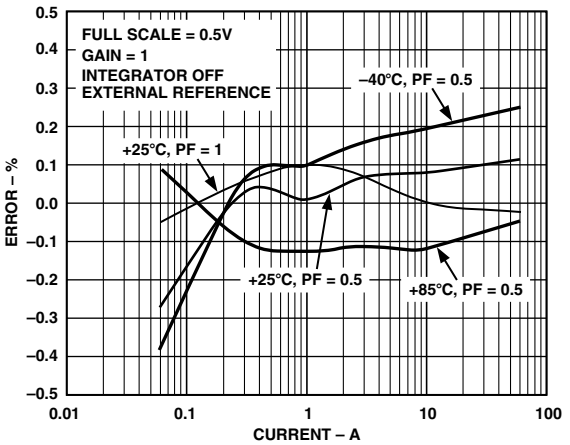
TPC 2. Error as a % of Reading



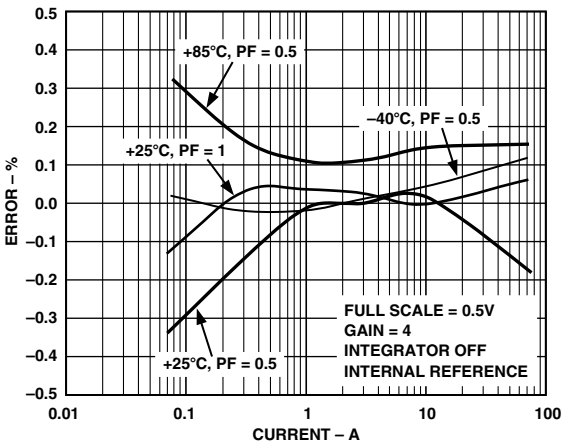
TPC 3. Error as a % of Reading



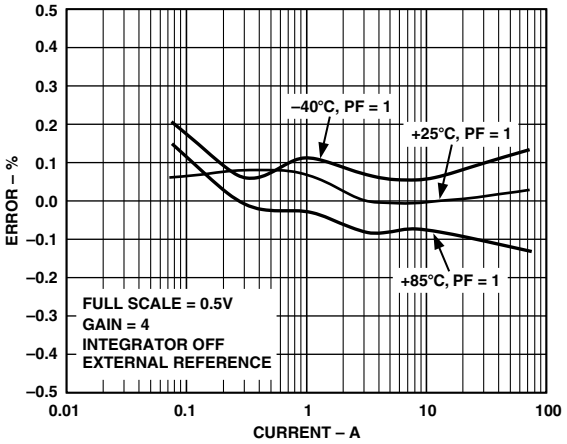
TPC 4. Error as a % of Reading



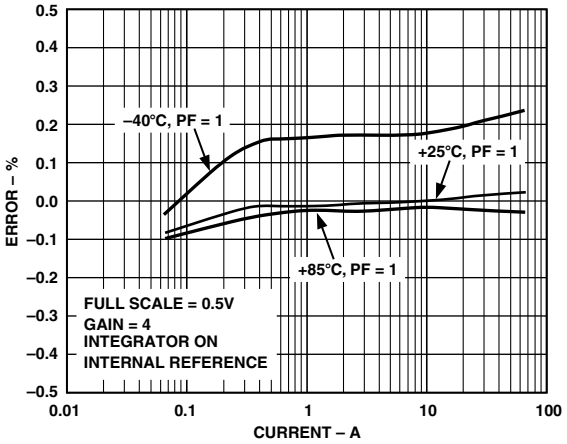
TPC 5. Error as a % of Reading



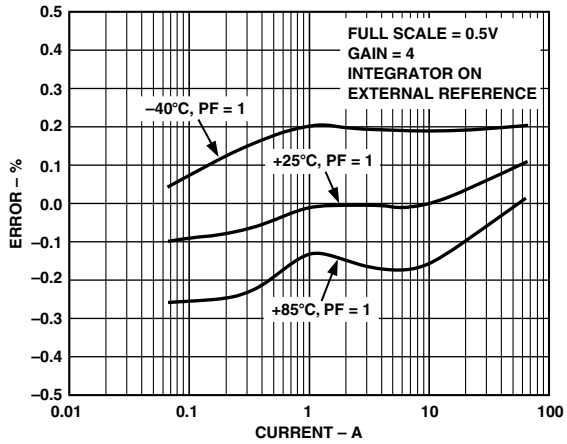
TPC 6. Error as a % of Reading



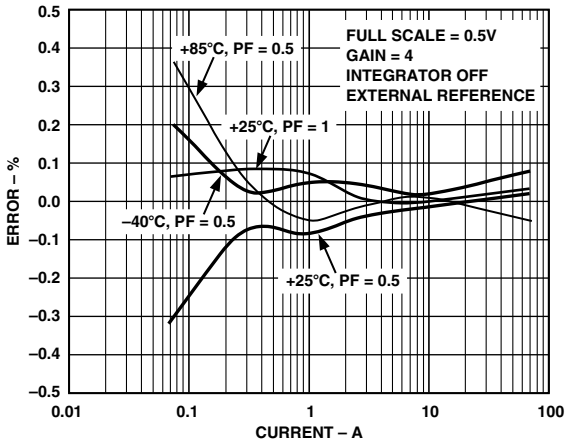
TPC 7. Error as a % of Reading



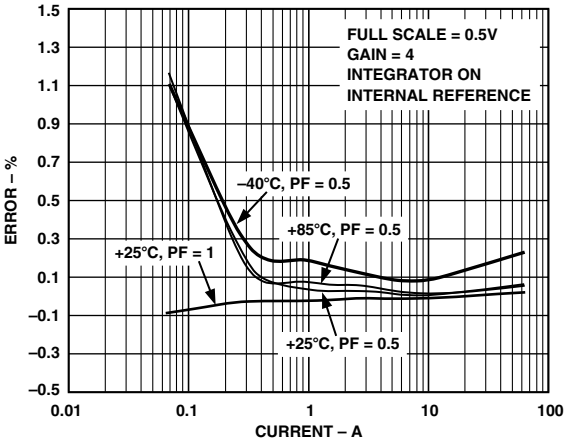
TPC 8. Error as a % of Reading



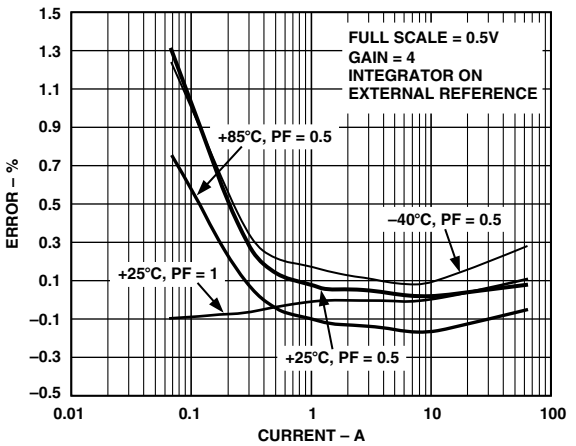
TPC 9. Error as a % of Reading



TPC 10. Error as a % of Reading

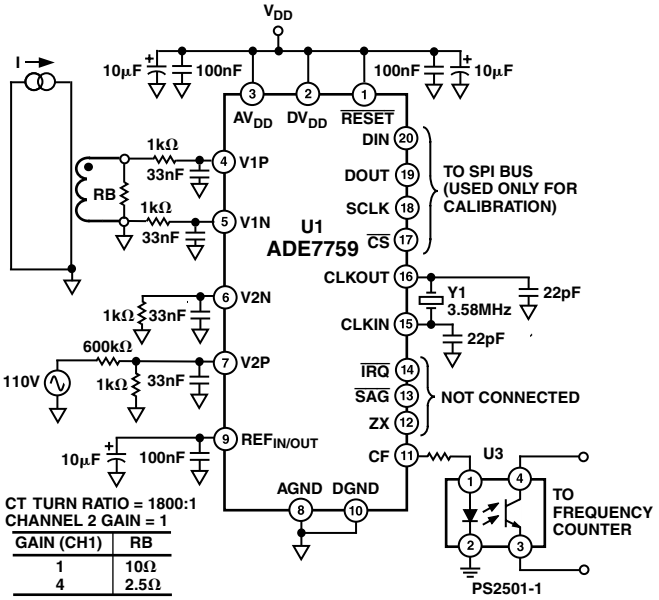


TPC 11. Error as a % of Reading

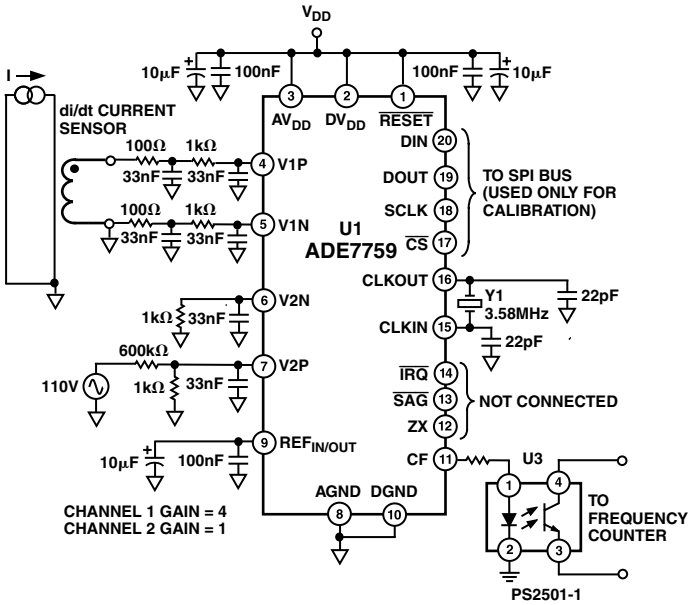


TPC 12. Error as a % of Reading

Test Circuits



Test Circuit 1. Performance Curve (Integrator OFF)



Test Circuit 2. Performance Curve (Integrator ON)

ANALOG INPUTS

The ADE7759 has two fully differential voltage input channels. The maximum differential input voltage for input pairs V1P/V1N and V2P/V2N are ±0.5 V. In addition, the maximum signal level on analog inputs for V1P/V1N and V2P/V2N are ±0.5 V with respect to AGND.

Each analog input channel has a PGA (Programmable Gain Amplifier) with possible gain selections of 1, 2, 4, 8, and 16. The gain selections are made by writing to the gain register—see Figure 5. Bits 0 to 2 select the gain for the PGA in Channel 1 and the gain selection for the PGA in Channel 2 is made via Bits 5 to 7. Figure 4 shows how a gain selection for Channel 1 is made using the gain register.

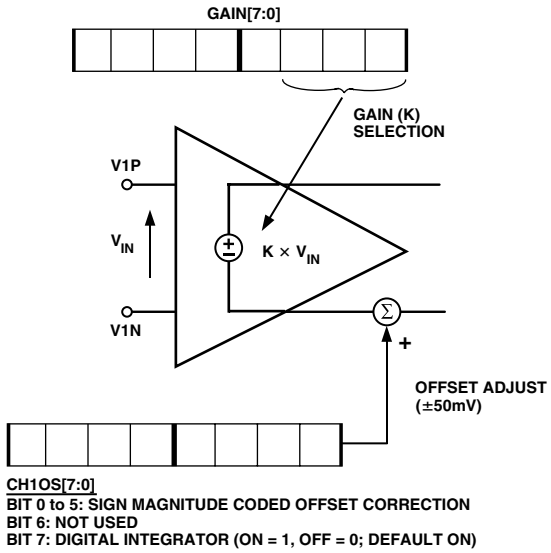


Figure 4. PGA in Channel 1

In addition to the PGA, Channel 1 also has a full-scale input range selection for the ADC. The ADC analog input range selection is also made using the gain register—see Figure 5. As mentioned previously the maximum differential input voltage is 0.5 V. However, by using Bits 3 and 4 in the gain register, the maximum ADC input voltage can be set to 0.5 V, 0.25 V, or 0.125 V. This is achieved by adjusting the ADC reference—see Reference Circuit section. Table I summarizes the maximum differential input signal level on Channel 1 for the various ADC range and gain selections.

Table I. Maximum Input Signal Levels for Channel 1

Max Signal Channel 1	ADC Input Range Selection 0.5 V	0.25 V	0.125 V
0.5 V	Gain = 1		
0.25 V	Gain = 2	Gain = 1	
0.125 V	Gain = 4	Gain = 2	Gain = 1
0.0625 V	Gain = 8	Gain = 4	Gain = 2
0.0313 V	Gain = 16	Gain = 8	Gain = 4
0.0156 V		Gain = 16	Gain = 8
0.00781 V			Gain = 16

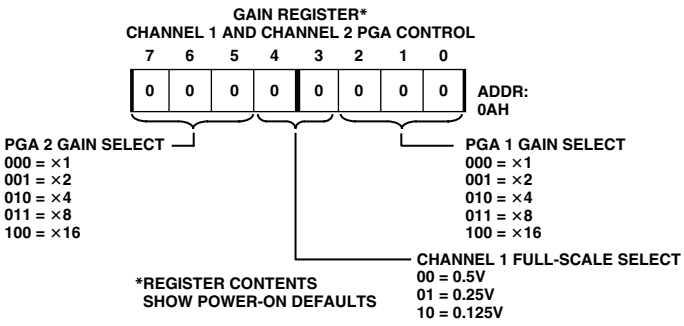


Figure 5. Analog Gain Register

It is also possible to adjust offset errors on Channel 1 and Channel 2 by writing to the offset correction registers (CH1OS and CH2OS, respectively). These registers allow channel offsets in the range ±24 mV to ±50 mV (depending on the gain setting) to be removed. Note that it is not necessary to perform an offset correction in an energy measurement application if HPF1 Channel 1 is switched on. Figure 6 shows the effect of offsets on the real power calculation; an offset on Channel 1 and Channel 2 will contribute a dc component after multiplication. Since this dc component is extracted by LPF2 to generate the active (real) power information, the offsets will have contributed an error to the active power calculation. This problem is easily avoided by enabling HPF1 in Channel 1. By removing the offset from at least one channel, no error component is generated at dc by the multiplication. Error terms at cos(ωt) are removed by LPF2 and by integration of the active power signal in the active energy register (AENERGY[39:0])—see Energy Calculation section.

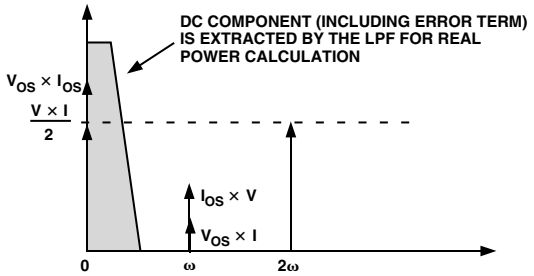


Figure 6. Effect of Channel Offsets on the Real Power Calculation

The contents of the offset correction registers are 6-bit, sign and magnitude coded. The weighting of the LSB size depends on the gain setting, i.e., 1, 2, 4, 8, or 16. Table II shows the correctable offset span for each of the gain settings and the LSB weight (mV) for the offset correction registers. The maximum value that can be written to the offset correction registers is ±31 decimal—see Figure 7.

Table II. Offset Correction Range

Gain	Correctable Span	LSB Size
1	±50 mV	1.61 mV/LSB
2	±37 mV	1.19 mV/LSB
4	±30 mV	0.97 mV/LSB
8	±26 mV	0.84 mV/LSB
16	±24 mV	0.77 mV/LSB

Figure 7 shows the relationship between the offset correction register contents and the offset (mV) on the analog inputs for a gain setting of one. To perform an offset adjustment, the analog inputs should be first connected to AGND, and there should be no signal on either Channel 1 or Channel 2. A read from Channel 1 or Channel 2 using the waveform register will give an indication of the offset in the channel. This offset can be canceled by writing an equal but opposite offset value to the relevant offset register. The offset correction can be confirmed by performing another read. Note that when adjusting the offset of Channel 1, the digital integrator and the HPF1 should be disabled.

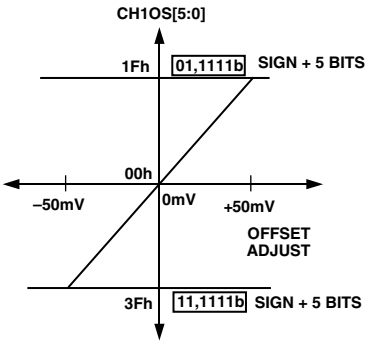


Figure 7. Channel Offset Correction Range (Gain = 1)

di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR

The di/dt sensor detects changes in magnetic field caused by ac current. Figure 8 shows the principle of a di/dt current sensor.

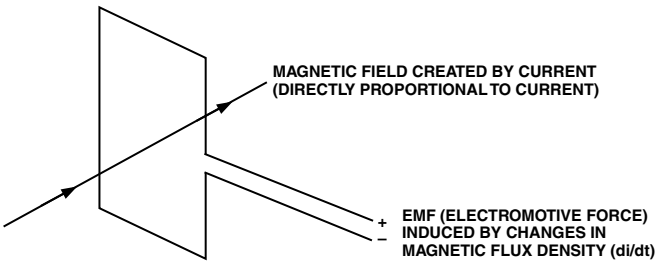


Figure 8. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal that is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current-carrying conductor and the di/dt sensor. Figure 9 shows that the mutual inductance produces a di/dt signal at the output of the sensor.

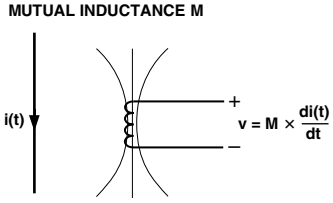


Figure 9. Mutual Inductance Between the di/dt Sensor and the Current Carrying Conductor

The current signal needs to be recovered from the di/dt signal before it can be used for active power calculation. An integrator is therefore necessary to restore the signal to its original form. The ADE7759 has a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator on Channel 1 is switched on by default when the ADE7759 is powered up. Setting the MSB of the CH1OS register to 0 will turn off the integrator. Figures 10 to 13 show the magnitude and phase response of the digital integrator.

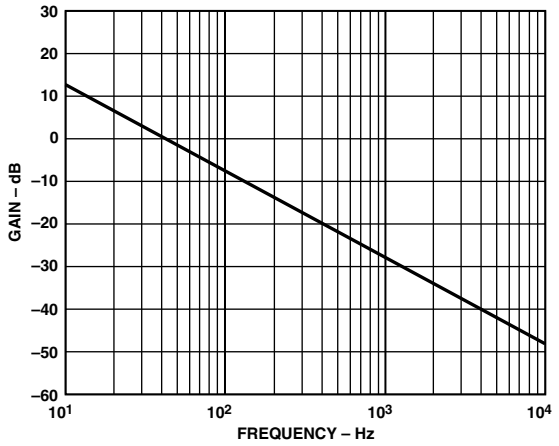


Figure 10. Gain Response of the Digital Integrator

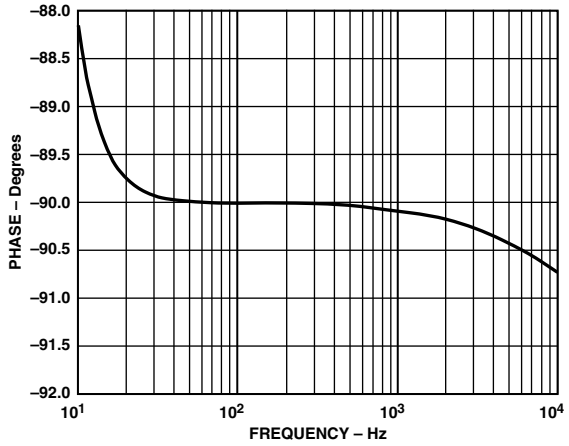


Figure 11. Phase Response of the Digital Integrator

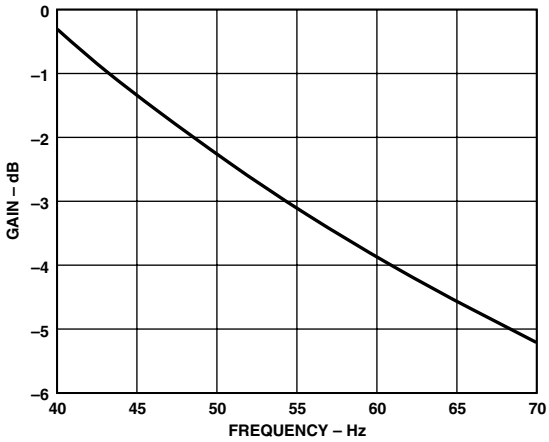


Figure 12. Gain Response of the Digital Integrator (40 Hz to 70 Hz)

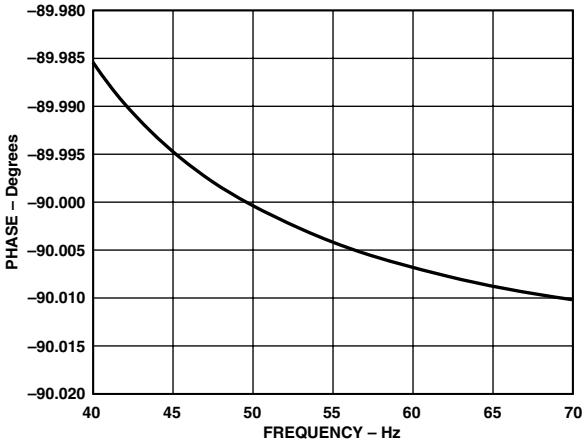


Figure 13. Phase Response of the Digital Integrator (40 Hz to 70 Hz)

Note that the integrator has a –20 dB/dec attenuation and approximately –90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. However, the di/dt sensor has a 20 dB/dec gain associated with it, and generates significant high frequency noise. A more effective antialiasing filter is needed to avoid noise due to aliasing—see Antialias Filter section.

When the digital integrator is switched off, the ADE7759 can be used directly with a conventional current sensor such as current transformer (CT) or a low resistance current shunt.

ZERO CROSSING DETECTION

The ADE7759 has a zero crossing detection circuit on Channel 2. This zero crossing is used to produce an external zero cross signal (ZX), and it is also used in the calibration mode—see Energy Calibration section. The zero crossing signal is also used to initiate a temperature measurement on the ADE7759—see Temperature Measurement section. Figure 14 shows how the zero cross signal is generated from the output of LPF1.

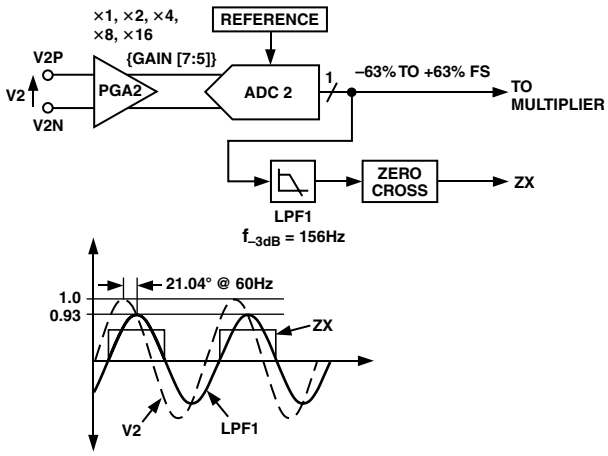


Figure 14. Zero Cross Detection on Channel 2

The ZX signal will go logic high on a positive going zero crossing and logic low on a negative going zero crossing on Channel 2. The zero crossing signal ZX is generated from the output of LPF1. LPF1 has a single pole at 156 Hz (CLKIN = 3.579545 MHz). As a result, there will be a phase lag between the analog input signal V2 and the output of LPF1. The phase response of this filter is shown in the Channel 2 Sampling section. The phase lag response of LPF1 results in a time delay of approximately 0.97 ms (@ 60 Hz) between the zero crossing on the analog inputs of Channel 2 and the rising or falling edge of ZX.

The zero crossing detection also has an associated timeout register, ZXTOUT. This unsigned, 12-bit register is decremented 1 LSB every 128/CLKIN seconds. The register is reset to its user-programmed full-scale value every time a zero crossing on Channel 2 is detected. The default power-on value in this register is FFFh. If the register decrements to zero before a zero crossing is detected and the DISSAG bit in the mode register is logic zero, the $\overline{\text{SAG}}$ pin will go active low. The absence of a zero crossing is also indicated on the $\overline{\text{IRQ}}$ output if the SAG Enable bit in the interrupt enable register is set to Logic 1. Irrespective of the enable bit setting, the SAG flag in the interrupt status register is always set when the ZXTOUT register is decremented to zero—see Interrupts section. The zero cross timeout register can be written/read by the user and has an address of 0Eh—see Serial Interface section. The resolution of the register is 128/CLKIN seconds per LSB. Thus the maximum delay for an interrupt is 0.15 second ($128/\text{CLKIN} \times 2^{12}$).

LINE VOLTAGE SAG DETECTION

In addition to the detection of the loss of the line voltage signal (zero crossing), the ADE7759 can also be programmed to detect when the absolute value of the line voltage drops below a certain peak value, for a number of half cycles. This condition is illustrated in Figure 15.

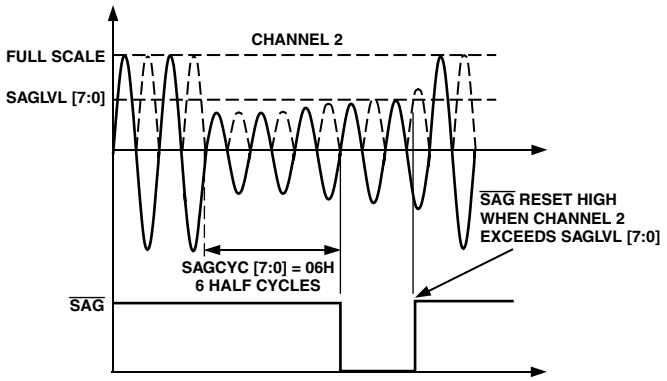


Figure 15. Sag Detection

Figure 15 shows the line voltage fall below a threshold that is set in the sag level register (SAGLVL[7:0]) for nine half cycles. Since the sag cycle register (SAGCYC[7:0]) contains 06h, the $\overline{\text{SAG}}$ pin will go active low at the end of the sixth half cycle for which the line voltage falls below the threshold, if the DISSAG bit in the mode register is Logic 0. As is the case when zero crossings are no longer detected, the sag event is also recorded by setting the SAG flag in the interrupt status register. If the SAG enable bit is set to Logic 1, the $\overline{\text{IRQ}}$ logic output will go active low—see Interrupts section.

The $\overline{\text{SAG}}$ pin will go logic high again when the absolute value of the signal on Channel 2 exceeds the sag level set in the Sag Level register. This is shown in Figure 15 when the $\overline{\text{SAG}}$ pin goes high during the tenth half cycle from the time when the signal on Channel 2 first dropped below the threshold level.

Sag Level Set

The contents of the sag level register (1 byte) are compared to the absolute value of the most significant byte output from LPF1, after it is shifted left by one bit. For example, the nominal maximum code from LPF1 with a full-scale signal on Channel 2 is 257F6h or (0010, 0101, 0111, 1111, 0110b)—see Channel 2 Sampling section. Shifting one bit left will give 0100, 1010, 1111, 1110, 1100b, or 4AFECh. Therefore, writing 4Ah to the sag level register will put the sag detection level at full scale. Writing 00h will put the sag detection level at zero. The sag level register is compared to the most significant byte of a waveform sample after the shift left, and detection is made when the contents of the sag level register are greater.

POWER SUPPLY MONITOR

The ADE7759 also contains an on-chip power supply monitor. The analog supply (AV_{DD}) is continuously monitored by the ADE7759. If the supply is less than 4 V ± 5%, the ADE7759 will go into an inactive state, i.e., no energy will be accumulated when the supply voltage is below 4 V. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

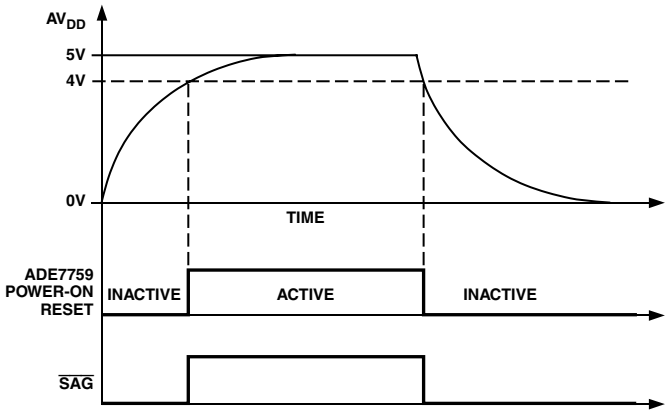


Figure 16. On-Chip Power Supply Monitor

As seen in Figure 16, the trigger level is nominally set at 4 V. The tolerance on this trigger level is about ±5%. The $\overline{\text{SAG}}$ pin can also be used as a power supply monitor input to the MCU. The $\overline{\text{SAG}}$ pin will go logic low when the ADE7759 is reset. The power supply and decoupling for the part should be such that the ripple at AV_{DD} does not exceed 5 V ± 5% as specified for normal operation.

Bit 6 of the interrupt status register (STATUS[7:0]) will be set to logic high upon power-up or every time the analog supply (AV_{DD}) dips below the power supply monitor threshold (4 V ± 5%) and recovers. However, no interrupt can be generated because the corresponding bit (Bit 6) in the interrupt enable register (IRQEN[7:0]) is not active—see Interrupts section.

INTERRUPTS

ADE7759 interrupts are managed through the interrupt status register (STATUS[7:0]) and the interrupt enable register (IRQEN[7:0]). When an interrupt event occurs in the ADE7759, the corresponding flag in the status register is set to a Logic 1—see Interrupt Status Register section. If the enable bit for this interrupt in the interrupt enable register is Logic 1, then the $\overline{IRQ}$ logic output goes active low. The flag bits in the status register are set irrespective of the state of the enable bits.

To determine the source of the interrupt, the system master (MCU) should perform a read from the status register with reset (RSTATUS[7:0]). This is achieved by carrying out a read from address 05h. The $\overline{IRQ}$ output will go logic high on completion of the interrupt status register read command—see Interrupt Timing section. When carrying out a read with reset, the ADE7759 is designed to ensure that no interrupt events are missed. If an interrupt event occurs just as the status register is being read, the event will not be lost and the $\overline{IRQ}$ logic output is guaranteed to go high for the duration of the interrupt status register data transfer before going logic low again to indicate the pending interrupt. See the following section for a more detailed description.

Using the ADE7759 Interrupts with an MCU

Figure 17 shows a timing diagram with a suggested implementation of ADE7759 interrupt management using an MCU. At time t_1, the $\overline{IRQ}$ line will go active low, indicating that one or more interrupt events have occurred in the ADE7759. The $\overline{IRQ}$ logic output should be tied to a negative edge-triggered external interrupt on the MCU. On detection of the negative edge, the MCU should be configured to start executing its Interrupt Service Routine (ISR). On entering the ISR, all interrupts should be disabled using the global interrupt enable bit. At this point, the MCU external interrupt flag can be cleared to capture interrupt events that occur during the current ISR.

When the MCU interrupt flag is cleared, a read from the status register with reset is carried out. This will cause the $\overline{IRQ}$ line to be reset logic high (t_2)—see Interrupt Timing section. The status register contents are used to determine the source of the interrupt(s), and thus the appropriate action will be taken. If a subsequent interrupt event occurs during the ISR, that event will be recorded by the MCU external interrupt flag being set again (t_3). On returning from the ISR, the global interrupt mask will be cleared (same instruction cycle) and the external interrupt flag will cause the MCU to jump to its ISR once again. This will ensure that the MCU does not miss any external interrupts.

Interrupt Timing

The Serial Interface section should be reviewed first, before the Interrupt Timing section. As previously described, when the $\overline{IRQ}$ output goes low, the MCU ISR must read the interrupt status register to determine the source of the interrupt. When reading the status register contents, the $\overline{IRQ}$ output is set high on the last falling edge of SCLK of the first byte transfer (read interrupt status register command). The $\overline{IRQ}$ output is held high until the last bit of the next 8-bit transfer is shifted out (interrupt status register contents)—see Figure 18. If an interrupt is pending at this time, the $\overline{IRQ}$ output will go low again. If no interrupt is pending, the $\overline{IRQ}$ output will stay high.

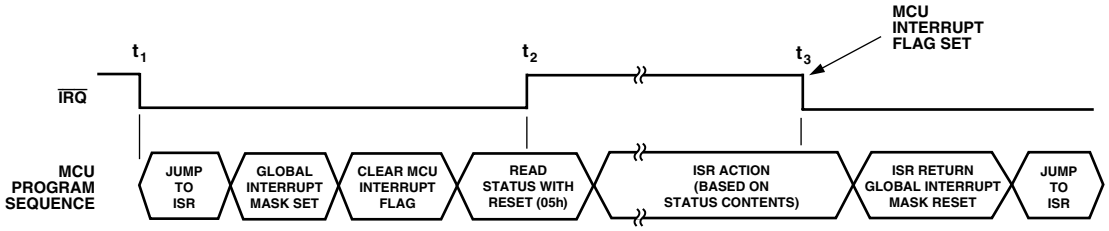


Figure 17. Interrupt Management

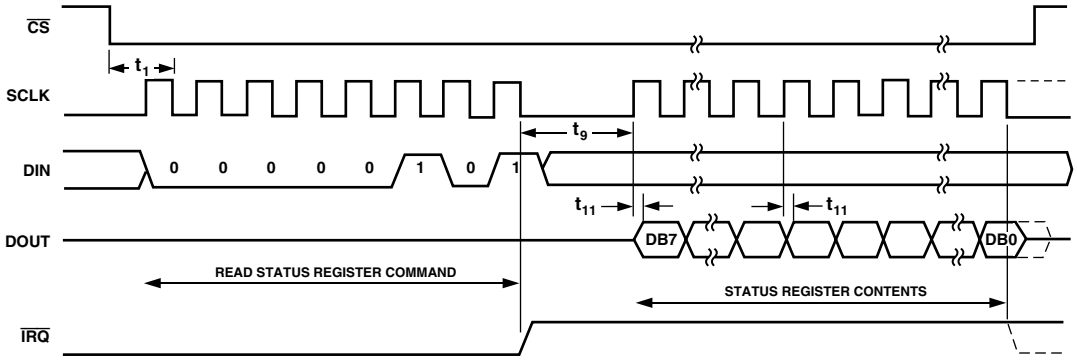


Figure 18. Interrupt Timing

TEMPERATURE MEASUREMENT

ADE7759 also includes an on-chip temperature sensor. A temperature measurement can be made by setting Bit 5 in the mode register. When Bit 5 is set logic high in the mode register, the ADE7759 will initiate a temperature measurement on the next zero crossing. When the zero crossing on Channel 2 is detected, the voltage output from the temperature sensing circuit is connected to ADC1 (Channel 1) for digitizing. The resultant code is processed and placed in the temperature register (TEMP[7:0]) approximately 26 µs later (24 CLKIN cycles). If enabled in the interrupt enable register (Bit 5), the $\overline{\text{IRQ}}$ output will go active low when the temperature conversion is finished. Note that temperature conversion will introduce a small amount of noise in the energy calculation. If temperature conversion is performed frequently (i.e., multiple times per second), a noticeable error will accumulate in the resulting energy calculation over time.

The contents of the temperature register are signed (twos complement) with a resolution of approximately 1 LSB/°C. The temperature register will produce a code of 00h when the ambient temperature is approximately 70°C. The temperature measurement is uncalibrated in the ADE7759 and has an offset tolerance that could be as high as ±20°C.

ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital conversion in the ADE7759 is carried out using two second-order sigma-delta ADCs. The block diagram in Figure 19 shows a first-order (for simplicity) sigma-delta ADC. The converter is made up of two parts, first the sigma-delta modulator and second the digital low-pass filter.

A sigma-delta modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7759, the sampling clock is equal to CLKIN/4. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) will approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged will a meaningful result be obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 20-bit datawords that are proportional to the input signal level.

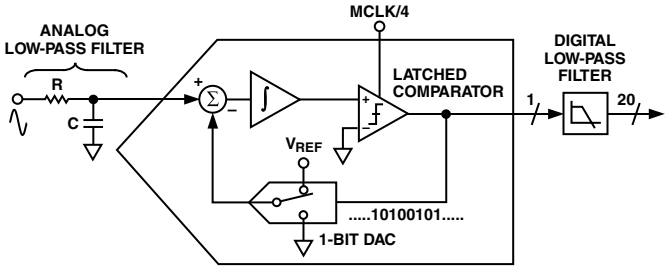


Figure 19. First Order Sigma-Delta (Σ-Δ) ADC

The sigma-delta converter uses two techniques to achieve high resolution from what is essentially a one-bit conversion technique. The first is oversampling. By oversampling we mean that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, the sampling rate in the ADE7759 is CLKIN/4 (894 kHz) and the band of interest is 40 Hz to 2 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered—see Figure 20. However, oversampling alone is not an efficient enough method to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required just to increase the SNR by only 6 dB (one bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. This is what happens in the sigma-delta modulator: the noise is shaped by the integrator, which has a high-pass type response for the quantization noise. The result is that most of the noise is at the higher frequencies, where it can be removed by the digital low-pass filter. This noise shaping is also shown in Figure 20.

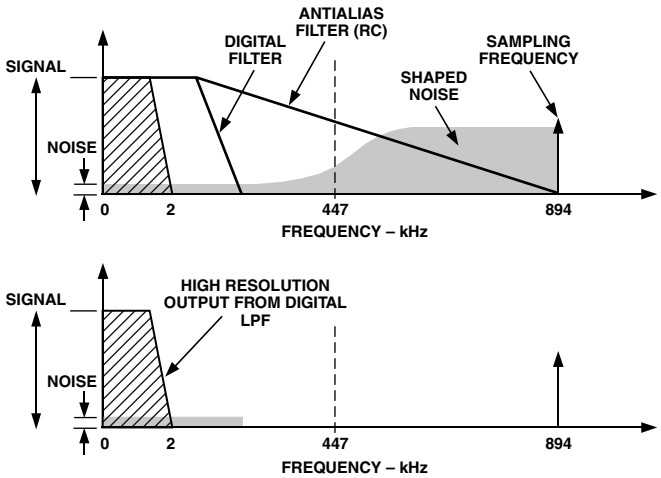


Figure 20. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Antialias Filter

Figure 19 also shows an analog low-pass filter (RC) on the input to the modulator. This filter is present to prevent aliasing. Aliasing is an artifact of all sampled systems. Basically, it means that frequency components in the input signal to the ADC that are higher than half the sampling rate of the ADC will appear in the sampled signal at a frequency below half the sampling rate. Figure 21 illustrates the effect. Frequency components above half the sampling frequency (also known as the Nyquist frequency, i.e., 447 kHz) get imaged or folded back down below 447 kHz. This will happen with all ADCs regardless of the architecture. In the example shown, it can be seen that only frequencies near the sampling frequency (894 kHz) will move into the band of interest for metering, i.e., 40 Hz–2 kHz. This allows us to use a very simple LPF (low-pass filter) to attenuate these high frequencies (near 900 kHz) and to prevent distortion in the band of interest. For a conventional current sensor, a simple RC filter (single pole) with a corner frequency of 10 kHz will produce an attenuation of approximately 40 dB at 894 kHz—see Figure 20. The 20 dB per decade attenuation is usually sufficient to eliminate the effects of aliasing for a conventional current sensor.

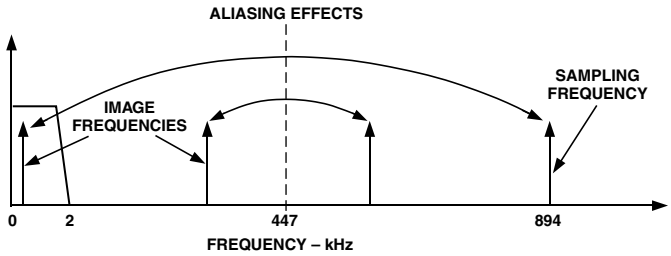


Figure 21. ADC and Signal Processing in Channel 1

For a di/dt sensor such as a Rogowski coil, however, the sensor has 20 dB per decade gain. This will neutralize the –20 dB per decade attenuation produced by this simple LPF and nullifies the antialias filter. Therefore, when using a di/dt sensor, measures should be taken to offset the 20 dB per decade gain coming from the di/dt sensor and produce sufficient attenuation to eliminate any aliasing effect. One simple approach is to cascade two RC filters to produce –40 dB per decade attenuation. The transfer function for a cascaded filter is the following:

$$H(s) = \frac{1}{1 + sR1C1 + sR2C2 + sR1C2 + s^2R1C1R2C2}$$

where $R1C1$ represents the RC used in the first stage of the cascade and $R2C2$ in that of the second stage. The s^2 term in the transfer function produces a –40 dB/decade attenuation. Note that to minimize the measurement error, especially at low power factor, it is important to match the phase angle between the voltage and the current channel. The small phase mismatch in the external antialias filter can be corrected using the phase calibration register (PHCAL[7:0])—see Phase Compensation section.

ADC Transfer Function

Below is an expression which relates the output of the LPF in the sigma-delta ADC to the analog input signal level. Both ADCs in the ADE7759 are designed to produce the same output code for the same input signal level.

$$Code(ADC) = 3.0492 \times \frac{V_{IN}}{V_{REF}} \times 262,144$$

Therefore, with a full-scale signal on the input of 0.5 V and an internal reference of 2.42 V, the ADC output code is nominally 165,151 or 2851Fh. The maximum code from the ADC is ±262,144, which is equivalent to an input signal level of ±0.794 V. However, for specified performance it is not recommended that the full-scale input signal level of 0.5 V be exceeded.

Reference Circuit

Shown in Figure 22 is a simplified version of the reference output circuitry. The nominal reference voltage at the $REF_{IN/OUT}$ pin is 2.42 V. This is the reference voltage used for the ADCs in the ADE7759. However, Channel 1 has three input range selections, which are selected by dividing down the reference value used for the ADC in Channel 1. The reference value used for Channel 1 is divided down to 1/2 and 1/4 of the nominal value by using an internal resistor divider, as shown in Figure 22.

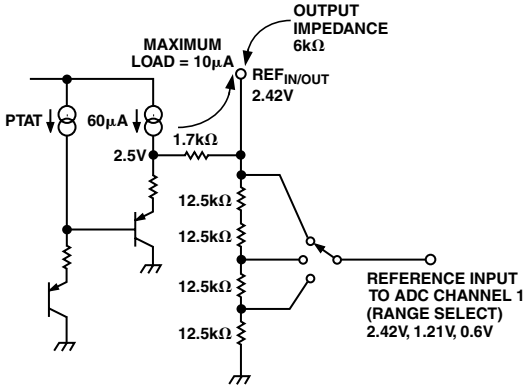


Figure 22. ADC and Reference Circuit Output

The $REF_{IN/OUT}$ pin can be overdriven by an external source, e.g., an external 2.5 V reference. Note that the nominal reference value supplied to the ADCs is now 2.5 V not 2.42 V. This has the effect of increasing the nominal analog input signal range by 2.5/2.42 × 100% = 3%, or from 0.5 V to 0.5165 V.

The internal voltage reference on the ADE7759 has a temperature drift associated with it—see ADE7759 Specifications section for the temperature coefficient specification (in ppm°C). The value of the temperature drift varies slightly from part to part. Since the reference is used for the ADCs in both Channel 1 and 2, any x% drift in the reference will result in 2x% deviation of the meter reading. The reference drift resulting from temperature changes is usually very small, and it is typically much smaller than the drift of other components on a meter. However, if guaranteed temperature performance is needed, one needs to use an external voltage reference. Alternatively, the meter can be calibrated at multiple temperatures. Real-time compensation can be achieved easily using the on-chip temperature sensor.

CHANNEL 1 ADC

Figure 23 shows the ADC and signal processing chain for Channel 1. In waveform sampling mode, the ADC outputs a signed twos complement 20-bit dataword at a maximum of 27.9 kSPS (CLKIN/128). The output of the ADC can be scaled by ±50% to perform an overall power calibration or to calibrate the ADC output. While the ADC outputs a 20-bit twos complement value, the maximum full-scale positive value from the ADC is limited to 40,000h (+262,144 decimal). The maximum full-scale negative value is limited to C0000h (–262,144 decimal). If the analog inputs are overranged, the ADC output code will clamp at these values. With the specified full-scale analog input signal of 0.5 V (or 0.25 V or 0.125 V—see Analog Inputs section), the ADC will produce an output code that is approximately 63% of its full-scale value. This is illustrated in Figure 23. The diagram in Figure 23 shows a full-scale voltage signal being applied to the differential inputs V1P and V1N. The ADC output swings between D7AE1h (–165,151) and 2851Fh (+165,151). This is approximately 63% of the full-scale value 40,000h (262,144). Overranging the analog inputs with more than 0.5 V differential (0.25 V or 0.125 V, depending on Channel 1 full-scale selection) will cause the ADC output to increase towards its full-scale value. However, for specified operation, the differential signal on the analog inputs should not exceed the recommended value of 0.5 V.

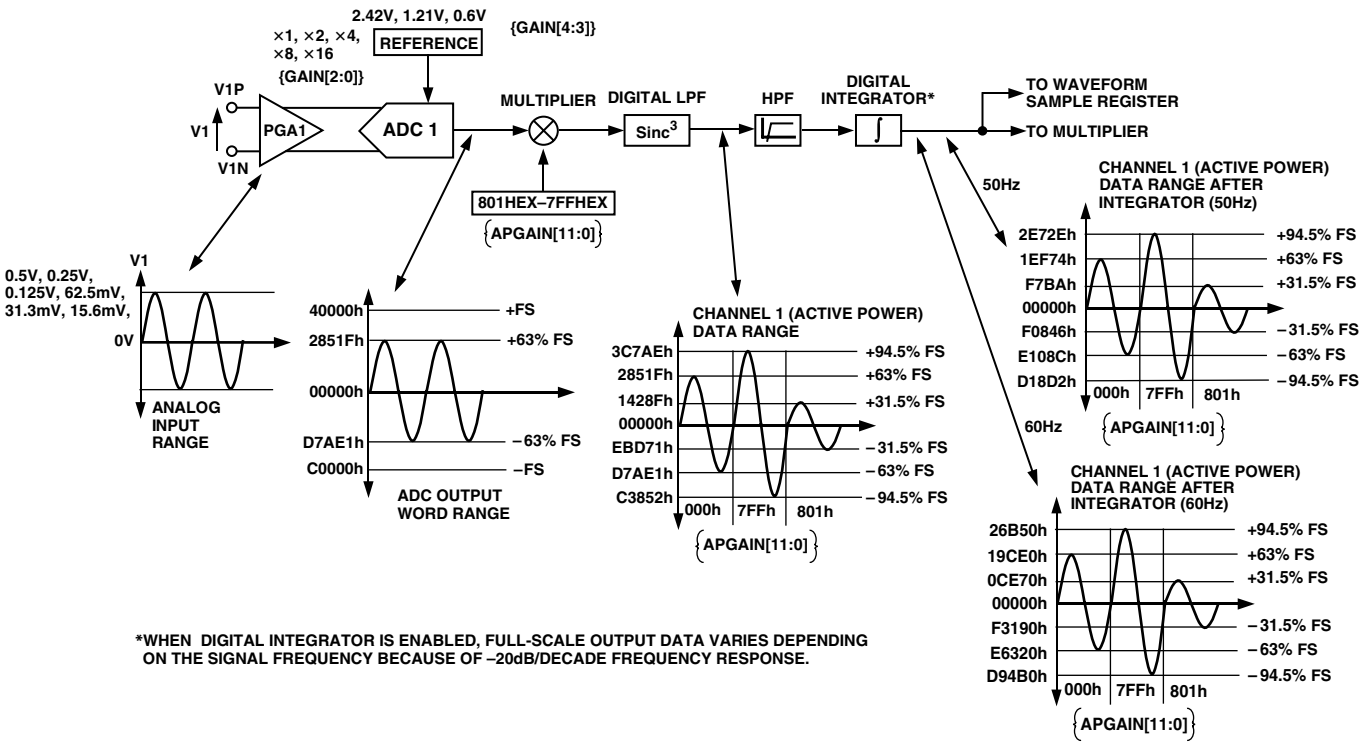


Figure 23. ADC and Signal Processing in Channel 1

Channel 1 ADC Gain Adjust

The ADC gain in Channel 1 can be adjusted by using the multiplier and active power gain register (APGAIN[11:0]). The gain of the ADC is adjusted by writing a twos complement 12-bit word to the active power gain register. Below is the expression that shows how the gain adjustment is related to the contents of the active power gain register.

$$Code = \left(ADC \times \left\{ 1 + \frac{APGAIN}{2^{12}} \right\} \right)$$

For example, when 7FFh is written to the active power gain register, the ADC output is scaled up by 50%. 7FFh = 2047 decimal, $2047/2^{12} = 0.5$. Similarly, 801h = 2047 decimal (signed twos complement) and ADC output is scaled by –50%. These two examples are illustrated in Figure 23.

Channel 1 Sampling

The waveform samples may also be routed to the waveform register (MODE[14:13] = 1, 0) to be read by the system master (MCU). In waveform sampling mode, the WSMP bit (Bit 3) in the interrupt enable register must also be set to Logic 1. The active power and energy calculation will remain uninterrupted during waveform sampling.

When in waveform sample mode, one of four output sample rates may be chosen by using Bits 11 and 12 of the mode register DTRT(1, 0). The output sample rate may be 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see Mode Register section. The interrupt request output $\overline{IRQ}$ signals a new sample availability by going active low. The timing is shown in Figure 24. The 20-bit wave form samples are transferred from the ADE7759 one byte (eight bits) at a time, with the most significant byte shifted out first. The 20-bit dataword is right justified and sign extended to 24 bits (three bytes)—see Serial Interface section.

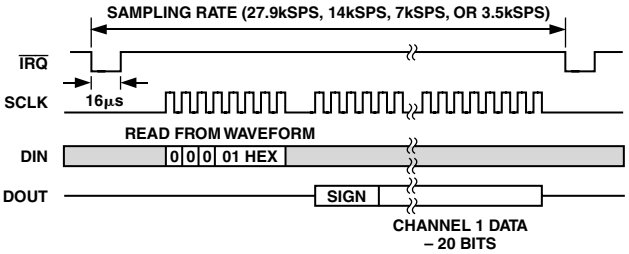


Figure 24. Waveform Sampling Channel 1

CHANNEL 1 AND CHANNEL 2 WAVEFORM SAMPLING MODE

In Channel 1 and Channel 2 waveform sampling mode (MODE[14:13] = 01), the output is a 40-bit waveform sample data that contains the waveform samples from both Channel 1 and Channel 2 ADCs. Figure 25 shows the format of the 40-bit waveform output.

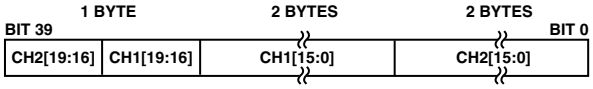


Figure 25. 40-Bit Combined Channel 1 and Channel 2 Waveform Sample Data Format

CHANNEL 2 ADC

Channel 2 Sampling

In Channel 2 waveform sampling mode (MODE[14:13] = 1, 1 and WSMP = 1), the ADC output code scaling for Channel 2 is the same as Channel 1, i.e., the output swings between D7AE1h (–165,151) and 2851Fh (+165,151)—see ADC Channel 1 section. However, before being passed to the waveform register, the ADC output is passed through a single-pole, low-pass filter with a cutoff frequency of 156 Hz. The plots in Figure 26 show the magnitude and phase response of this filter.

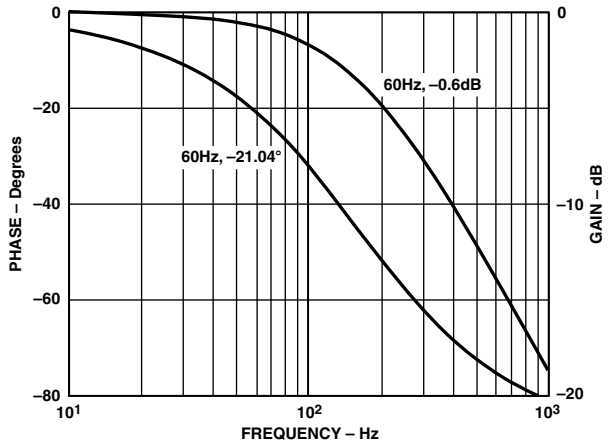


Figure 26. Magnitude and Phase Response of LPF1

The LPF1 has the effect of attenuating the signal. For example, if the line frequency is 60 Hz, the signal at the output of LPF1 will be attenuated by 7%.

$$\left|H(f)\right| = \frac{1}{\sqrt{1+\left(\frac{60\ Hz}{156\ Hz}\right)^2}} = 0.93 = -0.6\ dB$$

Note that LPF1 does not affect the power calculation. The signal processing chain in Channel 2 is illustrated in Figure 27. Unlike Channel 1, Channel 2 has only one analog input range (0.5 V differential). However, like Channel 1, Channel 2 does have a PGA with gain selections of 1, 2, 4, 8, and 16. For energy measurement, the output of the ADC is passed directly to the multiplier and is not filtered. An HPF is not required to remove any dc offset since it is only required to remove the offset from one channel to eliminate errors due to offsets in the power calculation. When in waveform sample mode, one of four output sample rates can be chosen by using Bits 11 and 12 of the mode register. The available output sample rates are 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see Mode Register section. The interrupt request output $\overline{IRQ}$ signals a new sample availability by going active low. The timing is the same as that for Channel 1 and is shown in Figure 24.

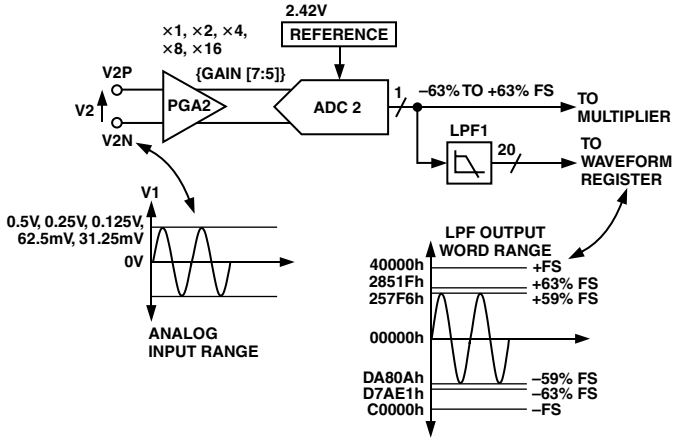


Figure 27. ADC and Signal Processing in Channel 2

PHASE COMPENSATION

When the HPF is disabled, the phase error between Channel 1 and Channel 2 is zero from dc to 3.5 kHz. When HPF1 is enabled, Channel 1 has a phase response illustrated in Figures 29 and 30. Also shown in Figure 31 is the magnitude response of the filter. As can be seen from the plots, the phase response is almost zero from 45 Hz to 1 kHz. This is all that is required in typical energy measurement applications.

However, despite being internally phase compensated, the ADE7759 must work with transducers that may have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a CT (Current Transformer). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7759 provides a means of digitally calibrating these small phase errors. The ADE7759 allows a small time delay or time advance to be introduced into the signal processing chain in order to compensate for small phase errors. Because the compensation is in time, this technique should only be used for small phase errors in the range of 0.1° to 0.5°. Correcting large phase errors using a time shift technique can introduce significant phase errors at higher harmonics.

The phase calibration register (PHCAL[7:0]) is a twos complement signed single-byte register that has values ranging from 9Eh (–98 in decimal) to 5Ch (92 in decimal). By changing the PHCAL register, the time delay in the Channel 2 signal path can change from –110 µs to +103 µs (CLKIN = 3.579545 MHz). One LSB is equivalent to 1.12 µs time delay or advance. With a line frequency of 60 Hz, this gives a phase resolution of 0.024° at the fundamental (i.e., 360° × 1.12 µs × 60 Hz). Figure 28 illustrates how the phase compensation is used to remove a 0.1° phase lead in Channel 1 due to the external transducer. To cancel the lead (0.1°) in Channel 1, a phase lead must also be introduced into Channel 2. The resolution of the phase adjustment allows the introduction of a phase lead in increments of 0.024°. The phase lead is achieved by introducing a time advance into Channel 2. A time advance of 4.48 µs is made by writing –4 (FCh) to the time delay block, thus reducing the amount of time delay by 4.48 µs, or equivalently, a phase lead of approximately 0.1° at line frequency of 60 Hz.

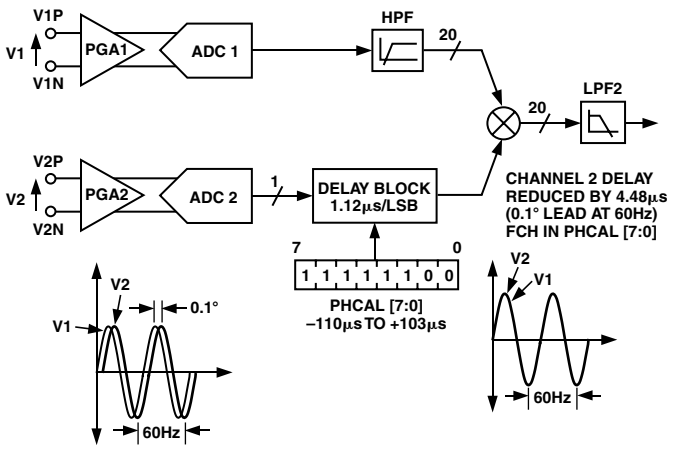


Figure 28. Phase Calibration

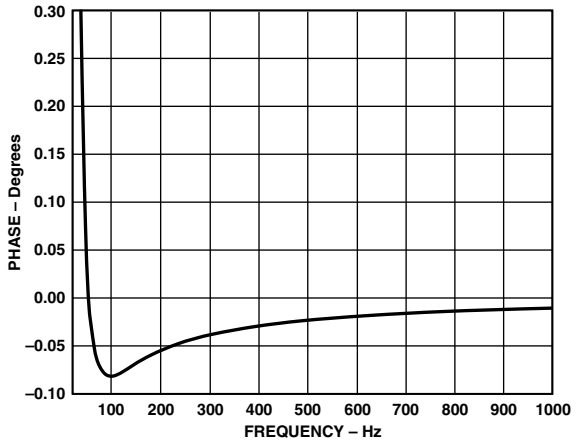


Figure 29. Combined Phase Response of the HPF and Phase Compensation (100 Hz to 1 kHz)

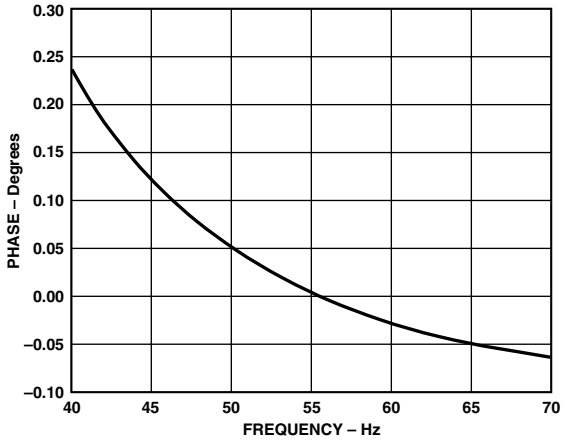


Figure 30. Combined Phase Response of the HPF and Phase Compensation (40 Hz to 70 Hz)

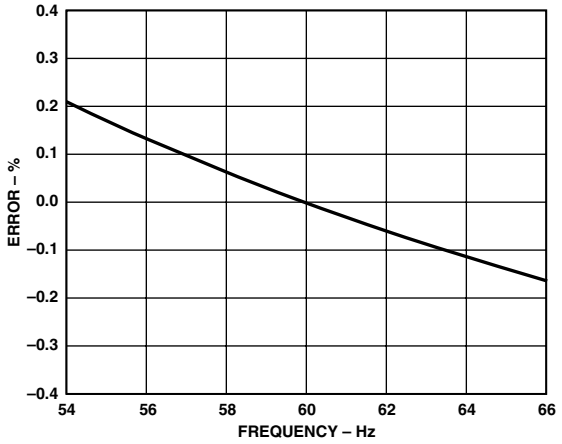


Figure 31. Combined Gain Response of the HPF and Phase Compensation (Deviation of Gain in % from Gain at 60 Hz)

ACTIVE POWER CALCULATION

Electrical power is defined as the rate of energy flow from source to load. It is given by the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal, and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/second. Equation 3 gives an expression for the instantaneous power signal in an ac system.

$$v(t) = \sqrt{2}\ V(\omega t) \tag{1}$$

$$i(t) = \sqrt{2}\ I\ \sin(\omega t) \tag{2}$$

where:
V = rms voltage
I = rms current

$$\begin{aligned} p(t) &= v(t) \times i(t) \\ p(t) &= VI - VI\cos(2\omega t) \end{aligned} \tag{3}$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 4.

$$P = \frac{1}{nT}\int_0^{nT} p\,(t)\,dt = VI \tag{4}$$

where T is the line cycle period. P is referred to as the active or real power. Note that the active power is equal to the dc component of the instantaneous power signal *p(t)* in Equation 3, i.e., *VI*. This is the relationship used to calculate active power in the ADE7759. The instantaneous power signal *p(t)* is generated by multiplying the current and voltage signals. The dc component of the instantaneous power signal is then extracted by LPF2 (low-pass filter) to obtain the active power information. This process is illustrated in Figure 32. Since LPF2 does not have an ideal "brick wall" frequency response (see Figure 33), the active power signal will have some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Since the ripple is sinusoidal in nature, it will be removed when the active power signal is integrated to calculate energy—see Energy Calculation section.

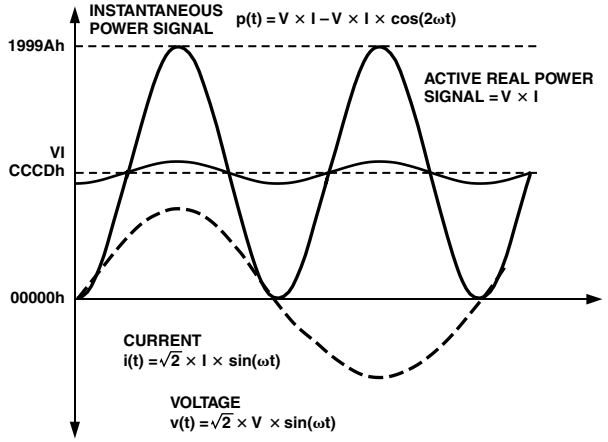


Figure 32. Active Power Calculation

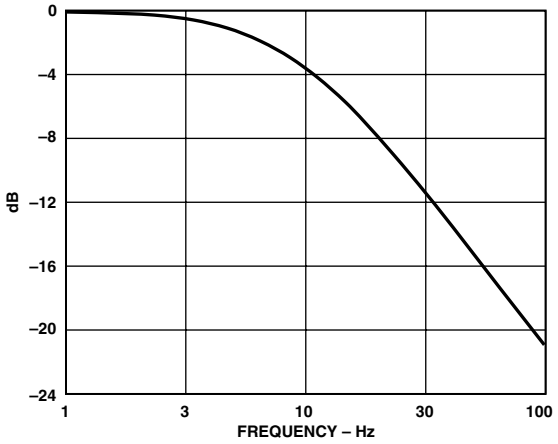


Figure 33. Frequency Response of LPF2

Figure 34 shows the signal processing chain for the active power calculation in the ADE7759. As explained, the active power is calculated by low pass filtering the instantaneous power signal.

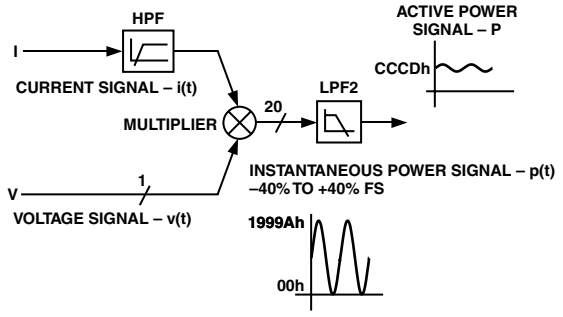


Figure 34. Active Power Signal Processing

Shown in Figure 35 is the maximum code (hexadecimal) output range for the active power signal (LPF2) when the digital integrator is disabled. Note that when the integrator is enabled, the output range changes depending on the input signal frequency. Furthermore, the output range can also be changed by the active power gain register—see Channel 1 ADC section. The minimum output range is given when the active power gain register contents are equal to 800h, and the maximum range is given by writing 7FFh to the active power gain register. This can be used to calibrate the active power (or energy) calculation in the ADE7759.

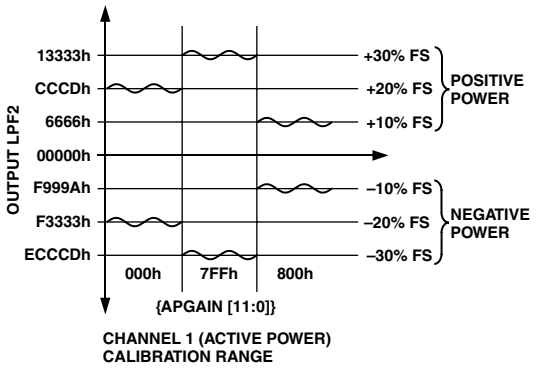


Figure 35. Active Power Calculation Output Range

ENERGY CALCULATION

As stated earlier, power is defined as the rate of energy flow. This relationship can be expressed mathematically as:

$$P = \frac{dE}{dt} \tag{5}$$

where P = power and E = energy.

Conversely, energy is given as the integral of power:

$$E = \int P dt \tag{6}$$

The AD7759 achieves the integration of the active power signal by continuously accumulating the active power signal in the 40-bit active energy register (ASENERGY[39:0]). This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 7 expresses this relationship:

$$E = \int P(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} p(nT) \times T \right\} \tag{7}$$

where n is the discrete time sample number and T is the sample period.

The discrete time sample period (T) for the accumulation register in the ADE7759 is 1.1 µs (4/CLKIN). As well as calculating the energy, this integration removes any sinusodial components which may be in the active power signal.

Figure 36 shows a graphical representation of this discrete time integration or accumulation. The active power signal in the waveform register is continuously added to the active energy register. This addition is a signed addition; therefore negative energy will be subtracted from the active energy contents.

As shown in Figure 36, the active power signal is accumulated in a 40-bit signed register (AENERGY[39:0]). The active power signal can be read from the waveform register by setting MODE[14:13] = 0, 0 and setting the WSMP bit (Bit 3) in the interrupt enable register to 1. Like Channel 1 and Channel 2 waveform sampling modes, the waveform data is available at sample rates of 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see Figure 24. Figure 37 shows this energy accumulation for full-scale signals (sinusodial) on analog inputs. The three curves displayed illustrate the minimum period of time it takes the energy register to roll over when the active power gain register contents are 7FFh, 000h, and 800h. The active power gain register is used to carry out power calibration in the ADE7759. As shown, the fastest integration time will occur when the active power gain register is set to maximum full scale, i.e., 7FFh.

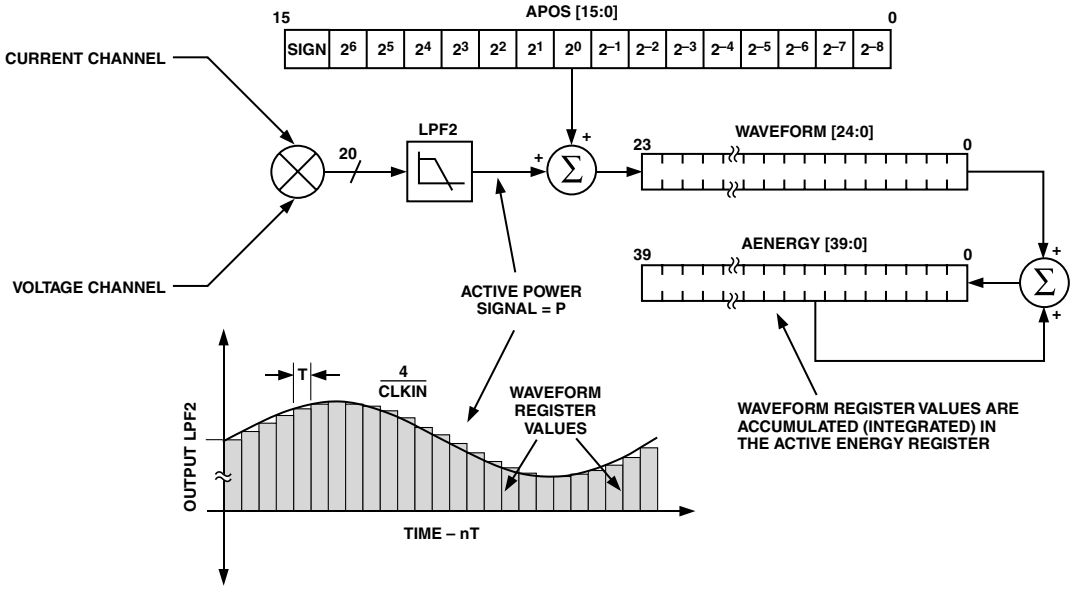


Figure 36. Energy Calculation

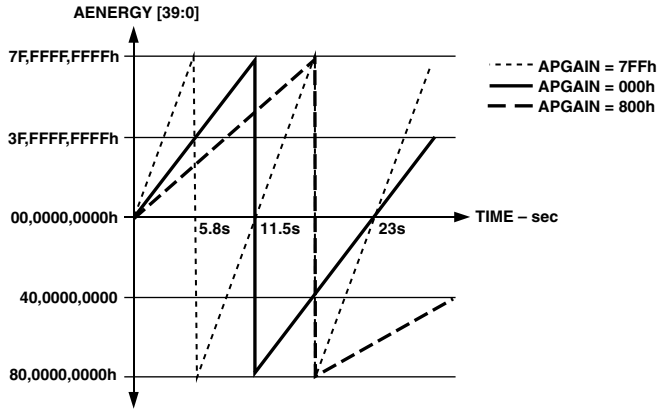


Figure 37. Energy Register Rollover Time for Full-Scale Power (Minimum and Maximum Power Gain)

Note that the energy register contents will roll over to full-scale negative (80,0000,0000h) and continue increasing in value when the power or energy flow is positive—see Figure 37. Conversely, if the power is negative, the energy register would underflow to full-scale positive (7F, FFFF, FFFFh) and continue decreasing in value. By using the interrupt enable register, the ADE7759 can be configured to issue an interrupt ($\overline{IRQ}$) when the active energy register is half-full (positive or negative) or when an over/underflow occurs.

Integration Time under Steady Load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 1.1 µs (4/CLKIN). With full-scale sinusoidal signals on the analog inputs, digital integrator turned off, and the active power gain register set to 000h, the average word value from LPF2 is CCCD—see Figures 34 and 35. The maximum value that can be stored in the active energy register before it overflows is 2^{39} or 7F,FFFF,FFFFh. Therefore, the integration time under these conditions is calculated as follows:

$$Time = \frac{7F, FFFF, FFFFh}{CCCDh} \times 1.1\,\mu s = 11.53\ seconds$$

POWER OFFSET CALIBRATION

The ADE7759 also incorporates an active power offset register (APOS[15:0]). This is a signed twos complement 16-bit register that can be used to remove offsets in the active power calculation—see Figure 36. An offset may exist in the power calculation due to crosstalk between channels on the PCB or in the IC itself. The offset calibration will allow the contents of the active power register to be maintained at zero when no power is being consumed.

The 256 LSBs (APOS = 0100h) written to the active power offset register are equivalent to 1 LSB in the waveform sample register, assuming the average value output from LPF2 to store in the waveform register is CCCDh (52,429 in decimal) when inputs on Channels 1 and 2 are both at full scale and the digital integrator is turned off. At –60 dB down on Channel 1 (1/1000 of the Channel 1 full-scale input), the average word value output from LPF2 is 52.429 (52,429/1,000). One LSB in the waveform register has a measurement error of 1/52.429 × 100% = 1.9% of the average value. The active power offset register has a resolution equal to 1/256 LSB of the waveform register, thus the power offset correction resolution is 0.007%/LSB (1.9%/256) at –60 dB. When the digital integrator is turned on, the resolution of the LSB varies slightly with the line frequency.

ENERGY-TO-FREQUENCY CONVERSION

ADE7759 also provides energy-to-frequency conversion for calibration purposes. After initial calibration at manufacturing, the manufacturer or end customer will often verify the energy meter calibration. One convenient way to verify the meter calibration is for the manufacturer to provide an output frequency that is proportional to the energy or active power under steady

load conditions. This output frequency can provide a simple, single-wire, optically isolated interface to external calibration equipment. Figure 38 illustrates the energy-to-frequency conversion in the ADE7759.

The energy-to-frequency conversion is accomplished by accumulating the active power signal in a 24-bit register. An output pulse is generated when there is a zero to one transition on the MSB (most significant bit) of the register. Under steady load conditions the output frequency is proportional to the active power. The output frequency at CF, with full-scale ac signals on Channel 1 and Channel 2 and CFDEN = 000h, CFNUM = 000h, and APGAIN = 000h, is approximately 5.593 kHz. This can be calculated as follows:

With the active power gain register set to 000h, the average value of the instantaneous power signal (output of LPF2) is CCCDh or 52,429 decimal. An output frequency is generated on CF when the MSB in the energy-to-frequency register (24 bits) toggles, i.e., when the register accumulates 2^{23}. This means the register is updated 2^{23}/CCCDh times (or 159.999 times). Since the update rate is 4/CLKIN or 1.1175 µs, the time between MSB toggles (CF pulses) is given as:

$$159.999 \cdot 1.1175\,\mu s = 1.78799 \cdot 10^{-4} s (5592.86\ Hz)$$

Equation 8 gives an expression for the output frequency at the Energy-to-Frequency (ETF) output with the contents of CFDEN and CFNUM registers are both zero.

$$ETF\ Output\ (Hz) = \frac{Average\ LPF2\ Output \times CLKIN}{2^{25}} \quad (8)$$

This output frequency is easily scaled by a pair of calibration frequency divider registers (CFDEN[11:0] and CFNUM[11:0]). These frequency scaling registers are 12-bit registers that can scale the output frequency by 1 to 2^{12}. The output frequency is given by the expression below:

$$CF(Hz) = ETF\ Output\ (Hz) \times \frac{CFNUM\ [11{:}0] + 1}{CFDEN\ [11{:}0] + 1} \quad (9)$$

For example, if the *CF* output frequency is 5.59286 kHz while the contents of *CFNUM* and *CFDEN* are zero, the CF output frequency can be set to 25 Hz by writing 8 BDh (2237 in decimal) to the CFDEN register and 00Ah (10 in decimal) to the CFNUM register. Note that the CFNUM and CFDEN registers are meant only to scale down the frequency from the ETF output. Therefore, the content of CFDEN should always be set no less than that of the CFNUM register, i.e., the maximum output frequency from CF pin will never exceed that of the ETF output. The power-up default value for CFDEN is 3Fh and CFNUM is 0h.

The output frequency will have a slight ripple at a frequency equal to twice the line frequency. This is due to imperfect filtering of the instantaneous power signal to generate the active power signal—see Active Power Calculation section. Equation 3 gives an expression for the instantaneous power signal. This is filtered by LPF2, which has a magnitude response given by Equation 10:

$$|H(f)| = \frac{1}{1 + f/8.9\ Hz} \quad (10)$$

The active power signal (output of LPF2) can be rewritten as:

$$p(t) = VI - \left\{\frac{VI}{1 + 2f_l/8.9\ Hz}\right\}\cos(4\pi f_l t) \quad (11)$$

where f_l is the line frequency (e.g., 60 Hz).

From Equation 6:

$$E(t) = VIt - \left\{\frac{VI}{4\pi f_l(1 + 2f_l/8.9\ Hz)}\right\}\sin(4\pi f_l t) \quad (12)$$

From Equation 12 it can be seen that there is a small ripple in the energy calculation due to a sin(2ωt) component. This is shown in Figure 39. The active energy calculation is shown by the dashed straight line and is equal to V × I × t. The sinusoidal ripple in the active energy calculation is also shown. Since the average value of a sinusoid is zero, this ripple will not contribute to the energy calculation over time. However, the ripple can be observed in the frequency output, especially at higher output frequencies. The ripple will get larger as a percentage of the frequency at larger loads and higher output frequencies. The reason is that at higher output frequencies the integration or averaging time in the energy-to-frequency conversion process is shorter. As a consequence, some of the sinusoidal ripple is observable in the frequency output. Choosing a lower output frequency at CF for calibration can significantly reduce the ripple. Also, averaging the output frequency by using a longer gate time for the counter will achieve the same results.

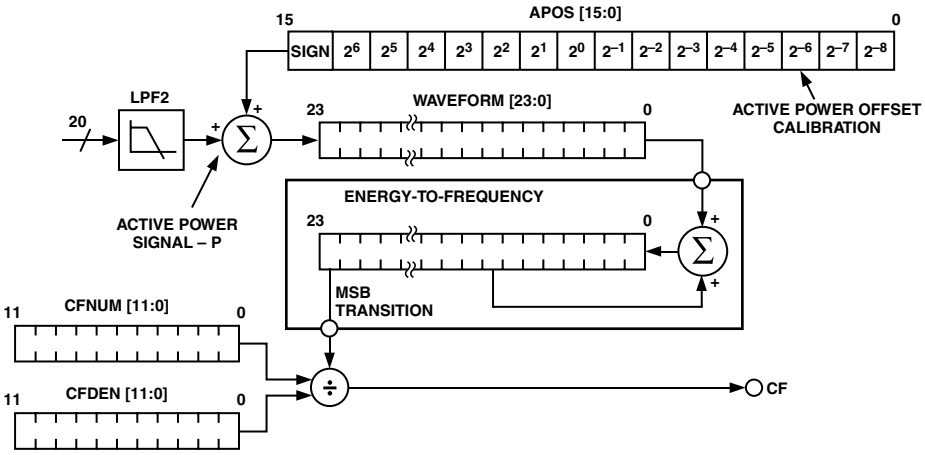


Figure 38. Energy-to-Frequency Conversion

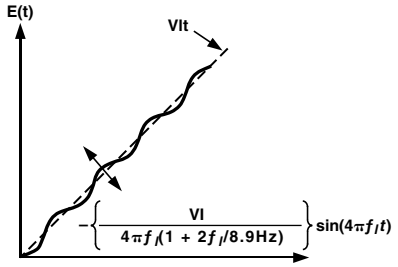


Figure 39. Output Frequency Ripple

LINE CYCLE ENERGY ACCUMULATION MODE

In line cycle energy accumulation mode, the energy accumulation of the ADE7759 can be synchronized to the Channel 2 zero crossing so that active energy can be accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of half-line cycles is that the sinusoidal component in the active energy is reduced to zero. This eliminates any ripple in the energy calculation. Energy is calculated more accurately and in a shorter time because the integration period can be shortened. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified and the time required to calibrate the meter can be significantly reduced. The ADE7759 is placed in line cycle energy accumulation mode by setting Bit 7 (CYCMODE) in the mode register. In line cycle energy accumulation mode the ADE7759 accumulates the active power signal in the LENERGY register (Address 14h) for an integral number of half cycles, as shown in Figure 40. The number of half-line cycles is specified in the LINECYC register (Address 14h). The ADE7759 can accumulate active power for up to 16,383 half cycles. Because the active power is integrated on an integral number of half-line cycles, at the end of a line cycle energy accumulation cycle, the CYCEND flag in the interrupt status register is set (Bit 2). If the CYCEND enable bit in the interrupt enable register is enabled, the $\overline{IRQ}$ output will also go active low. Thus the $\overline{IRQ}$ line can also be used to signal the completion of the line cycle energy accumulation. Another calibration cycle will start as long as the CYCMODE bit in the mode register is set. Note that the result of the first calibration is invalid and should be ignored. The result of all subsequent line cycle accumulation is correct.

From Equations 5 and 11:

$$E(t) = \int_0^{nT} VIdt - \left\{ \frac{VI}{4\,\pi f_l \left(1 + 2 f_l\,/\,8.9\,Hz\right)} \right\} \int_0^{nT} cos\,(2\,wt)\,dt \quad (13)$$

where n is an integer and T is the line cycle period.

Since the sinusoidal component is integrated over an integer number of line cycles, its value is always zero. Therefore:

$$E(t) = \int_0^{nT} VIdt + 0 \quad (14)$$

$$E(t) = VInT \quad (15)$$

Note that in this mode, the 14-bit LINECYC register can hold a maximum value of 16,383. In other words, the line cycle energy accumulation mode can be used to accumulate active energy for a maximum duration over 16,383 half-line cycles. At 60 Hz line frequency, it translates to a total duration of 16,383/120 Hz = 136.5 seconds. The 40-bit signed LENERGY register can overflow if large signals are present at the inputs. The LENERGY register can only hold up to 11.53 seconds of active energy when both its input channels are at ac full-scale—see Integration Time Under Steady Load section. Large LINECYC content is meant to be used only when the input signal is low and extensive averaging is required to reduce the noise.

CALIBRATING THE ENERGY METER

Calculating the Average Active Power

When calibrating the ADE7759, the first step is to calibrate the frequency on CF to some required meter constant, e.g., 3200 imp/kWh.

To determine the output frequency on CF, the average value of the active power signal (output of LPF2) must first be determined. One convenient way to do this is to use the line cycle energy accumulation mode. When the CYCMODE (Bit 7) bit in the mode register is set to a Logic 1, energy is accumulated over an integer number of half-line cycles as described in the last section. Since the line frequency is fixed at, say, 60 Hz, and the number of half cycles of integration is specified, the total integration time is given as:

$$\frac{1}{2 \times 60\ Hz} \times number\ of\ half\ cycles$$

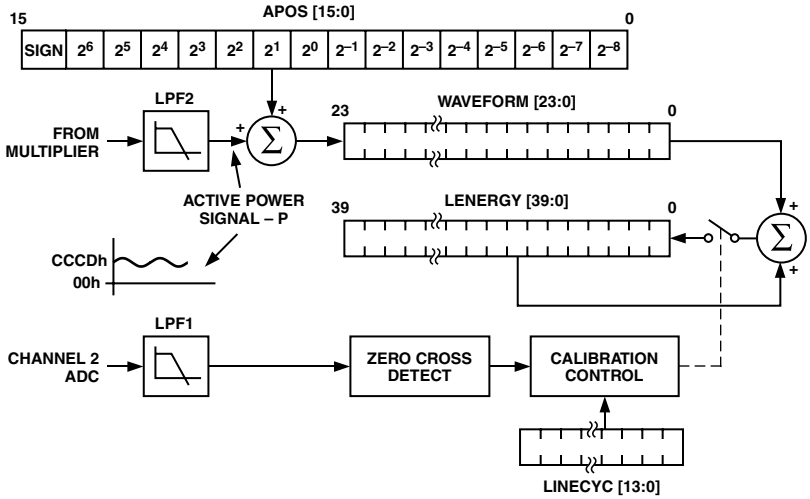


Figure 40. Energy Calculation in Line Cycle Energy Accumulation Mode

For 255 half cycles this would give a total integration time of 2.125 seconds. This would mean that the energy register was updated 2.125/1.1175 µs (4/CLKIN) times. The average output value of LPF2 is given as:

$$\frac{\textit{Contents of } LENERGY[39:0] \textit{ at the end}}{\textit{Number of times } LENERGY[39:0] \textit{ was updated}}$$

Or, equivalently, in terms of contents of various ADE7759 registers and CLKIN and line frequencies (f_l):

$$Average\ Word\ (LPF2) = \frac{LENERGY[39:0] \times 8 \times f_l}{LINECYC[13:0] \times CLKIN} \quad (16)$$

where f_l is the line frequency.

Calibrating the Frequency at CF

Once the average active power signal is calculated, it can be used to determine the frequency at CF before calibration. When the frequency before calibration is known, the pair of CF frequency divider registers (CFNUM and CFDEN) can be adjusted so as to produce the required frequency on CF. In this example, a meter constant of 3200 imp/kWh is chosen as an appropriate constant. This means that under a steady load of 1 kW, the output frequency on CF would be:

$$Frequency\ (CF) = \frac{3200\ imp/kWh}{60\ \text{min} \cdot 60\ \text{sec}} = \frac{3200}{3600} = 0.8888\ Hz$$

Assuming the meter is set up with a test current (basic current) of 20 A and a line voltage of 220 V for calibration, the load is calculated as 220 V × 20 A = 4.4 kW. Therefore, the expected output frequency on CF under this steady load condition would be 4.4 × 0.8888 Hz = 3.9111 Hz. Under these load conditions, the transducers on Channel 1 and Channel 2 should be selected such that the signal on the voltage channel should see approximately half scale and the signal on the current channel about 1/8 of full scale (assuming a maximum current of 80 A). The average value from LPF2 is calculated as 3,276.81 decimal using the calibration mode as described above. Then using Equation 8 (energy-to-frequency conversion), the frequency under this load is calculated as:

$$Frequency\ (CF) = \frac{3276.81 \times 3.579545\ MHz}{2^{25}} = 349.566\ Hz$$

This is the frequency with the contents of the CFNUM and CFDEN registers equal to 000h. The desired frequency out is 3.9111 Hz. Therefore, the CF frequency must be divided by 349.566/3.9111 Hz or 89.3779 decimal. This is achieved by loading the pair of CF divider registers with the closest rational number. In this case, the closest rational number is found to be 25/2234 (or 19h/8BAh). Therefore, 18h and 8B9h should be written to the CFNUM and CFDEN registers, respectively. Note that the CF frequency is divided by the contents of (CFNUM + 1)/(CFDEN + 1). With the CF divide registers contents equal to 18h/8B9h, the output frequency is given as 349.566 Hz/89.36 = 3.91188 Hz. Note that this setting has an error of +0.02%.

Calibrating CF is made easy by using the line cycle energy accumulation mode on the ADE7759, provided that the line frequency is accurately known during calibration. Using line cycle energy accumulation mode, the calibration time can be reduced by synchronizing energy accumulation to the zero crossing of the voltage channel—see the Line Cycle Energy Accumulation Mode section. However, this requires the line frequency to be precisely known. As shown in Equation 16, the average value of LPF2 is directly proportional to the line frequency. Any deviation from the nominal frequency will directly affect the calibration result. The line frequency could be measured using the ZX output of the ADE7759. Alternatively, the average value of LPF2 can be calculated from the output frequency from CF—see the Energy to Frequency Conversion section.

Note that besides CFNUM and CFDEN registers, changing APGAIN[11:0] register will also affect the output frequency from CF. The APGAIN register has a resolution of 0.0244%/LSB.

Energy Meter Display

Besides the pulse output, which is used to verify calibration, a solid state energy meter will very often require some form of display. The display should show the amount of energy consumed in kWh (kilowatthours). One convenient and simple way to interface the ADE7759 to a display or energy register (e.g., MCU with nonvolatile memory) is to use CF. For example, the CF frequency could be calibrated to 1,000 imp/kWhr. The MCU would count pulses from CF. Every pulse would be equivalent to 1 watt-hour. If more resolution is required, the CF frequency could be set to, say, 10,000 imp/kWh.

If more flexibility is required when monitoring energy usage, the active energy register (AENERGY) can be used to calculate energy. A full description of this register can be found in the Energy Calculation section. The AENERGY register gives the user both sign and magnitude information regarding energy consumption. On completion of the CF frequency output calibration, i.e., after the active power gain (APGAIN) register has been adjusted, a second calibration sequence can be initiated. The purpose of this second calibration routine is to determine a kWh/LSB coefficient for the AENERGY register. Once the coefficient has been calculated, the MCU can determine the energy consumption at any time by reading the AENERGY contents and multiplying by the coefficient to calculate kWh.

CLKIN FREQUENCY

In this data sheet, the characteristics of the ADE7759 are shown with the CLKIN frequency equal to 3.579545 MHz. However, the ADE7759 is designed to have the same accuracy at any CLKIN frequency within the specified range. If the CLKIN frequency is not 3.579545 MHz, various timing and filter characteristics will need to be redefined with the new CLKIN frequency. For example, the cutoff frequencies of all digital filters (LPF1, LPF2, HPF1, etc.) will shift in proportion to the change in CLKIN frequency according to the following equation:

$$New\ Frequency = Original\ Frequency \times \frac{CLKIN\ Frequency}{3.579545\ MHz} \quad (17)$$

The change of CLKIN frequency does not affect the timing characteristics of the serial interface because the data transfer is synchronized with serial clock signal (SCLK). But one needs to observe the read/write timing of the serial data transfer—see Timing Characteristics. Table III lists various timing changes that are affected by CLKIN frequency.

Table III. Frequency Dependencies of the ADE7759 Parameters

Parameter	CLKIN Dependency
Nyquist frequency for CH 1 and 2 ADCs	CLKIN/8
PHCAL resolution (seconds per LSB)	4/CLKIN
Active Energy register update rate (Hz)	CLKIN/4
Waveform sampling rate (Number of samples per second)	
WAVSEL 1, 0 = 0 0	CLKIN/128
0 1	CLKIN/256
1 0	CLKIN/512
1 1	CLKIN/1024
Maximum ZXTOUT period	524,288/CLKIN

SUSPENDING THE ADE7759 FUNCTIONALITY

The analog and the digital circuit can be suspended separately. The analog portion of the ADE7759 can be suspended by setting the ASUSPEND bit (Bit 4) of the mode register to logic high—see Mode Register section. In suspend mode, all waveform samples from the ADCs will be set to zeros. The digital circuitry can be halted by stopping the CLKIN input and maintaining a logic high or low on CLKIN pin. The ADE7759 can be reactivated by restoring the CLKIN input and setting the ASUSPEND bit to logic low.

APPLICATION INFORMATION

Application Note AN-564 contains detailed information on how to design an ANSI Class 100 watt-hour meter based on the ADE7756, a pin-to-pin compatible product with the ADE7759. Application Note AN-578 describes an algorithm on how to calculate the voltage and current rms values using an external MCU. It is available from the ADE7756 product homepage under the Application Note link on the energy metering homepage, www.analog.com/energymeter.

SERIAL INTERFACE

All ADE7759 functionality is accessible via several on-chip registers—see Figure 41. The contents of these registers can be updated or read using the on-chip serial interface. After power-on, or toggling the $\overline{\text{RESET}}$ pin low, or a falling edge on $\overline{\text{CS}}$, the ADE7759 is placed in communications mode. In communications mode the ADE7759 expects a write to its communications register. The data written to the communications register determines whether the next data transfer operation will be a read or a write and also which register is accessed. Therefore, all data transfer operations with the ADE7759, whether a read or a write, must begin with a write to the communications register.

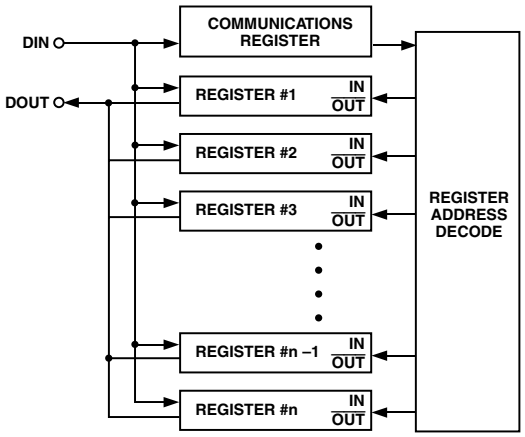


Figure 41. Addressing ADE7759 Registers via the Communications Register

The communications register is an 8-bit wide register. The MSB determines whether the next data transfer operation is a read or a write. The five LSBs contain the address of the register to be accessed. See Communications Register section for a more detailed description. Figures 42 and 43 show the data transfer sequences for a read and write operation, respectively.

On completion of a data transfer (read or write), the ADE7759 once again enters communications mode.

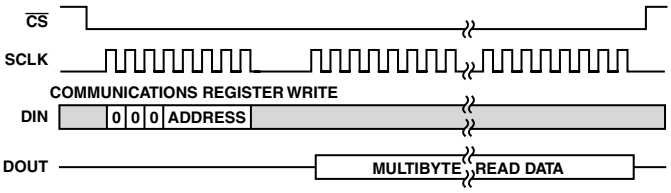


Figure 42. Reading Data from the ADE7759 via the Serial Interface

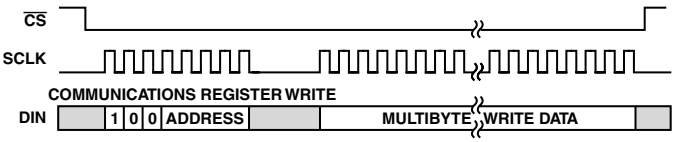


Figure 43. Writing Data to the ADE7759 via the Serial Interface

A data transfer is complete when the LSB of the ADE7759 register being addressed (for a write or a read) is transferred to or from the ADE7759.

The serial interface of the ADE7759 is made up of four signals: SCLK, DIN, DOUT, and $\overline{\text{CS}}$. The serial clock for a data transfer is applied at the SCLK logic input. This logic input has a Schmitt-trigger input structure, which allows slow rising (and falling) clock edges to be used. All data transfer operations are synchronized to the serial clock. Data is shifted into the ADE7759 at the DIN logic input on the falling edge of SCLK. Data is shifted out of the ADE7759 at the DOUT logic output on a rising edge of SCLK. The $\overline{\text{CS}}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. A falling edge on $\overline{\text{CS}}$ also resets the serial interface and places the ADE7759 into communications mode. The $\overline{\text{CS}}$ input should be driven low for the entire data transfer operation. Bringing $\overline{\text{CS}}$ high during a data transfer operation will abort the transfer and place the serial bus in a high impedance state. The $\overline{\text{CS}}$ logic input may be tied low if the ADE7759 is the only device on the serial bus. However, with $\overline{\text{CS}}$ tied low, all initiated data transfer operations must be fully completed, i.e., the LSB of each register must be transferred as there is no other way of bringing the ADE7759 back into communications mode without resetting the entire device, i.e., using $\overline{\text{RESET}}$.

Serial Write Operation

The serial write sequence takes place as follows. With the ADE7759 in communications mode (i.e., the $\overline{\text{CS}}$ input logic low), a write to the communications register first takes place. The MSB of this byte transfer is a 1, indicating that the data transfer operation is a write. The first five LSBs of this byte contain the address of the register to be written to. The ADE7759 starts shifting in the register data on the next falling edge of SCLK. All remaining bits of register data are shifted in on the falling edge of subsequent SCLK pulses—see Figure 44.

As explained earlier, the data write is initiated by a write to the communications register followed by the data. During a data write operation to the ADE7759, data is transferred to all on-chip registers one byte at a time. After a byte is transferred into the serial port, there is a finite time before it is transferred to one of the ADE7759 on-chip registers. Although another byte transfer to the serial port can start while the previous byte is being transferred to an on-chip register, this second byte transfer should not finish until at least 4 µs after the end of the previous byte transfer. This functionality is expressed in the timing specification t_6—see Figure 44. If a write operation is aborted during a byte transfer ($\overline{CS}$ brought high), then that byte will not be written to the destination register.

Destination registers may be up to 3 bytes wide—see the Register Description section. Therefore, the first byte shifted into the serial port at DIN is transferred to the MSB (Most Significant Byte) of the destination register. If the addressed register is 12 bits wide, for example, a two-byte data transfer must take place. The data is always assumed to be right justified: therefore, in this case, the four MSBs of the first byte would be ignored and the four LSBs of the first byte written to the ADE7759 would be the four MSBs of the 12-bit word. Figure 45 illustrates this example.

Serial Read Operation

During a data read operation from the ADE7759, data is shifted out at the DOUT logic output on the rising edge of SCLK. As was the case with the data write operation, a data read must be preceded by a write to the communications register.

With the ADE7759 in communications mode (i.e., $\overline{CS}$ logic low), an 8-bit write to the communications register first takes place. The MSB of this byte transfer is a 0, indicating that the next data transfer operation is a read. The first five LSBs of this byte contain the address of the register that is to be read. The ADE7759 starts shifting out of the register data on the next rising edge of SCLK—see Figure 46. At this point, the DOUT logic output leaves its high impedance state and starts driving the data bus. All remaining bits of register data are shifted out on subsequent SCLK rising edges. The serial interface also enters communications mode again as soon as the read has been completed. At this point, the DOUT logic output enters a high impedance state on the falling edge of the last SCLK pulse. The read operation may be aborted by bringing the $\overline{CS}$ logic input high before the data transfer is complete. The DOUT output enters a high impedance state on the rising edge of $\overline{CS}$.

When an ADE7759 register is addressed for a read operation, the entire contents of that register are transferred to the serial port. This allows the ADE7759 to modify its on-chip registers without the risk of corrupting data during a multibyte transfer. Note that when a read operation follows a write operation, the read command (i.e., write to communications register) should not happen for at least 4 µs after the end of the write operation. If the read command is sent within 4 µs of the write operation, the last byte of the write operation may be lost. This timing constraint is given as timing specification t_9.

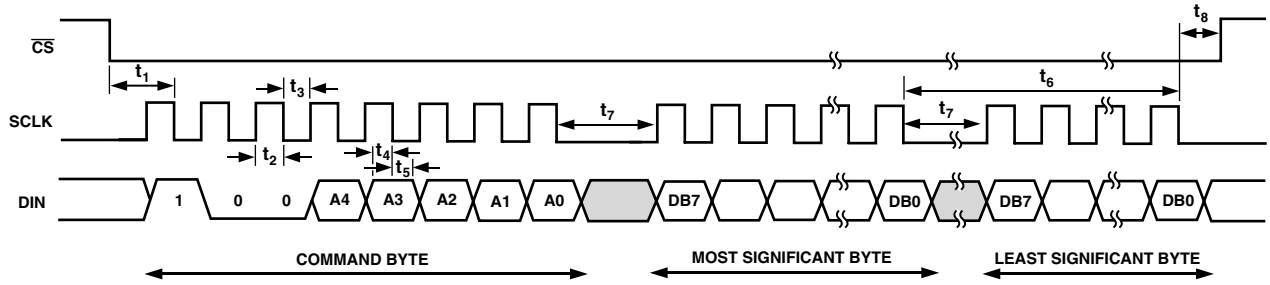


Figure 44. Serial Interface Write Timing Diagram

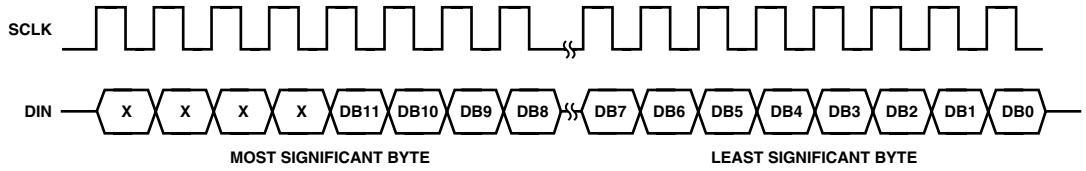


Figure 45. 12-Bit Serial Write Operation

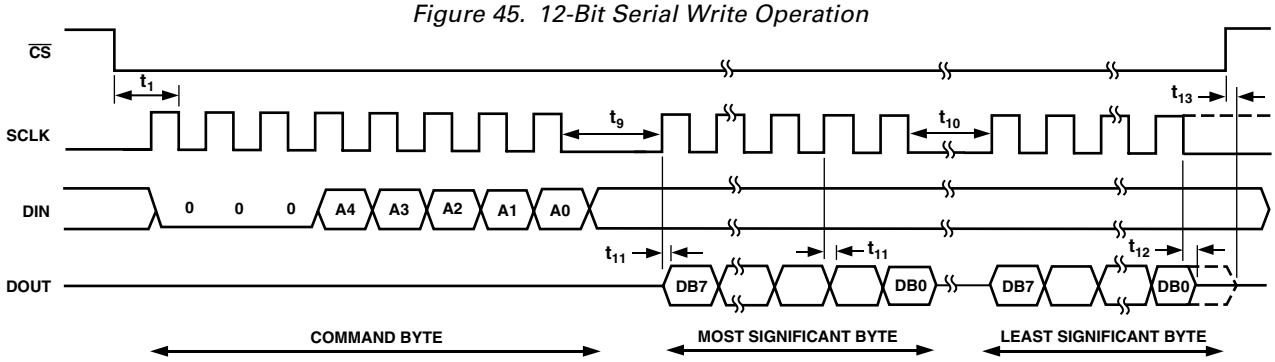


Figure 46. Serial Interface Read Timing Diagram

CHECKSUM REGISTER

The ADE7759 has a checksum register (CHKSUM[5:0]) to ensure that the data bits received in the last serial read operation are not corrupted. The 6-bit checksum register is reset before the first bit (MSB of the register to be read) is put on the DOUT pin. During a serial read operation, when each data bit becomes available on the rising edge of SCLK, the bit will be added to the checksum register. In the end of the serial read operation, the content of the checksum register will be the sum of all the ones contained in the register previously read. Using the checksum register, the user can determine if an error has occurred during the last read operation.

Note that a read to the CHKSUM register will also generate a checksum of the CHKSUM register itself.

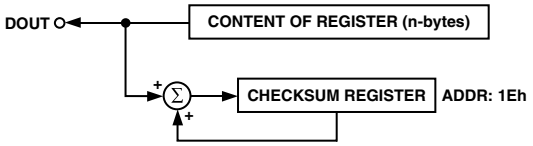


Figure 47. Checksum Register for Serial Interface Read

Table IV. Register List

Address	Name	R/W	No. of Bits	Default	Description
01h	WAVEFORM	R	24/40	0h	The Waveform Register is a read-only register. This register contains the sampled waveform data from Channel 1, Channel 2, or the active power signal. The data source and the length of the waveform registers are selected by data bits 14 and 13 in the mode register—see Channel 1 and 2 Sampling section.
02h	AENERGY	R	40	0h	Active Energy Register. Active power is accumulated (Integrated) over time in this 40-bit, read-only register. The energy register can hold a minimum of 11.53 seconds of active energy information with full-scale analog inputs before it overflows—see Energy Calculation section.
03h	RSTENERGY	R	40	0h	Same as the active energy register except that the register is reset to 0 following a read operation.
04h	STATUS	R	8	40h	Interrupt Status Register. This is an 8-bit read-only register. The status register contains information regarding the source of ADE7759 interrupts—see Interrupts section.
05h	RSTSTATUS	R	8	0h	Same as the interrupt status register except that the register contents are reset to 0 (all flags cleared) after a read operation.
06h	MODE	R/W	16	000Ch	Mode Register. This is a 16-bit register through which most of the ADE7759 functionality is accessed. Signal sample rates, filter enabling, and calibration modes are selected by writing to this register. The contents may be read at any time—see Mode Register section.
07h	CFDEN	R/W	12	3Fh	CF Frequency Divider Denominator Register. The output frequency on the CF pin is adjusted by writing to this 12-bit read/write register—see Energy-to-Frequency Conversion section.
08h	CH1OS	R/W	8	80h	Channel 1 Offset Adjust. The MSB is used to enable the digital integrator. Bit 6 is not used. Writing to Bits 0 to 5 allows offsets on Channel 1 to be removed—see Analog Inputs section and CH1OS Register section.
09h	CH2OS	R/W	6	0h	Channel 2 Offset Adjust. Writing to this 6-bit register allows any offsets on Channel 2 to be removed—see Analog Inputs section.
0Ah	GAIN	R/W	8	0h	PGA Gain Adjust. This 8-bit register is used to adjust the gain selection for the PGA in Channel 1 and 2—see Analog Inputs section.

Address	Name	R/W	No. of Bits	Default	Description
0Bh	APGAIN	R/W	12	0h	Active Power Gain Adjust. This is a 12-bit register. The active power calculation can be calibrated by writing to this register. The calibration range is ±50% of the nominal full-scale active power. The resolution of the gain adjust is 0.0244%/LSB—see Channel 1 ADC Gain Adjust section.
0Ch	PHCAL	R/W	8	0h	Phase Calibration Register. The phase relationship between Channel 1 and Channel 2 can be adjusted by writing to this 8-bit register. The valid content of this twos complement register is between 9Eh and 5Ch, which is a phase difference of –2.365° to +2.221° at 60 Hz in 0.0241° steps—see Phase Compensation section.
0Dh	APOS	R/W	16	0h	Active Power Offset Correction. This 16-bit register allows small offsets in the Active Power calculation to be removed—see Active Power Calculation section.
0Eh	ZXTOUT	R/W	12	FFFh	Zero Cross Timeout. If no zero crossings are detected on Channel 2 within a time period specified by this 12-bit register, the interrupt request line ($\overline{IRQ}$) will be activated. The maximum timeout period is 0.15 seconds—see Zero Crossing Detection section.
0Fh	SAGCYC	R/W	8	FFh	Sag Line Cycle Register. This 8-bit register specifies the number of consecutive half-line cycles the signal on Channel 2 must be below SAGLVL before the $\overline{SAG}$ output is activated—see Voltage Sag Detection section.
10h	IRQEN	R/W	8	40h	Interrupt Enable Register. ADE7759 interrupts may be deactivated at any time by setting the corresponding bit in this 8-bit enable register to Logic 0. The status register will continue to register an interrupt event even if disabled. However, the $\overline{IRQ}$ output will not be activated—see Interrupts section.
11h	SAGLVL	R/W	8	0h	Sag Voltage Level. An 8-bit write to this register determines at what peak signal level on Channel 2 the $\overline{SAG}$ pin will become active. The signal must remain low for the number of cycles specified in the SAGCYC register before the $\overline{SAG}$ pin is activated—see Line Voltage Sag Detection section.
12h	TEMP	R	8	0h	Temperature Register. This is an 8-bit register which contains the result of the latest temperature conversion—see Temperature Measurement section.
13h	LINECYC	R/W	4	3FFFh	Line Cycle Energy Accumulation Mode Half-Cycle Register. This 14-bit register is used during line cycle energy accumulation mode to set the number of half-line cycles active energy is accumulated—see Line Cycle Energy Accumulation Mode section.
14h	LENERGY	R	40	0h	Line Cycle Energy Accumulation Mode Active Energy Register. This 40-bit register accumulates active energy during line cycle energy accumulation mode. The number of half-line cycles is set by the LINECYC register—see Line Cycle Energy Accumulation Mode section.
15h	CFNUM	R/W	2	0h	CF Frequency Divider Numerator Register. The output frequency on the CF pin is adjusted by writing to this 12-bit read/write register—see Energy to Frequency Conversion section.
1Eh	CHKSUM	R	6	0h	Checksum Register. This 6-bit read-only register is equal to the sum of all the ones in the previous read—see Serial Read Operation section.
1Fh	DIEREV	R	8	01h	Die Revision Register. This 8-bit read-only register contains the revision number of the silicon.

REGISTER DESCRIPTIONS

All ADE7759 functionality is accessed via the on-chip registers. Each register is accessed by first writing to the communications register and then transferring the register data. A full description of the serial interface protocol is given in the Serial Interface section.

Communications Register

The communications register is an 8-bit, write-only register that controls the serial data transfer between the ADE7759 and the host processor. All data transfer operations must begin with a write to the communications register. The data written to the communications register determines whether the next operation is a read or a write and which register is being accessed. Table V outlines the bit designations for the communications register.

Table V. Communications Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W/$\overline{R}$	**0**	**0**	**A4**	**A3**	**A2**	**A1**	**A0**

Bit Location	Bit Mnemonic	Description
0 to 4	A0 to A4	The five LSBs of the communications register specify the register for the data transfer operation. Table III lists the address of each ADE7759 on-chip register.
5 to 6	RESERVED	These bits are unused and should be set to zero.
7	W/$\overline{R}$	When this bit is a Logic 1, the data transfer operation immediately following the write to the Communications register will be interpreted as a write to the ADE7759. When this bit is a Logic 0, the data transfer operation immediately following the write to the communications register will be interpreted as a read operation.

Mode Register (06H)

The ADE7759 functionality is configured by writing to the mode register—see Figure 45. Table VI summarizes the functionality of each bit in the mode register.

Table VI. Mode Register

Bit Location	Bit Mnemonic	Description
0	DISHPF	The HFP (high-pass filter) in Channel 1 is disabled when this bit is set.
1	DISLPF2	The LPF (low-pass filter) after the multiplier (LPF2) is disabled when this bit is set.
2	DISCF	The frequency output CF is disabled when this bit is set.
3	DISSAG	The line voltage sag detection is disabled when this bit is set.
4	ASUSPEND	By setting this bit to Logic 1, both ADE7759s' A/D converters can be turned off. In normal operation, this bit should be left at Logic 0. All digital functionality can be stopped by suspending the clock signal at CLKIN pin.
5	TEMPSEL	The temperature conversion starts when this bit is set to 1. This bit is automatically reset to 0 when the temperature conversion is finished.
6	SWRST	Software Chip Reset. A data transfer should not take place to the ADE7759 for at least 18 µs after a software reset.
7	CYCMODE	Setting this bit to Logic 1 places the chip in line cycle energy accumulation mode.
8	DISCH1	ADC 1 (Channel 1) inputs are internally shorted together.
9	DISCH2	ADC 2 (Channel 2) inputs are internally shorted together.
10	SWAP	By setting this bit to Logic 1 the analog inputs V2P and V2N are connected to ADC 1 and the analog inputs V1P and V1N are connected to ADC 2.
12, 11	DTRT1, 0	These bits are used to select the waveform register update rate. DTRT1 DTRT0 Update Rate 0 0 27.9 kSPS (CLKIN/128) 0 1 14 kSPS (CLKIN/256) 1 0 7 kSPS (CLKIN/512) 1 1 3.5 kSPS (CLKIN/1024)
14, 13	WAVSEL1, 0	These bits are used to select the source of the sampled data for the waveform register. WAVSEL1, 0 Length Source 0 0 24 bits Active Power Signal (output of LPF2) 0 1 40 bits Channel 1 and Channel 2 1 0 24 bits Channel 1 1 1 24 bits Channel 2
15	TEST1	Writing a Logic 1 to this bit position places the ADE7759 in test mode. This is intended for factory testing only and should be left at 0.

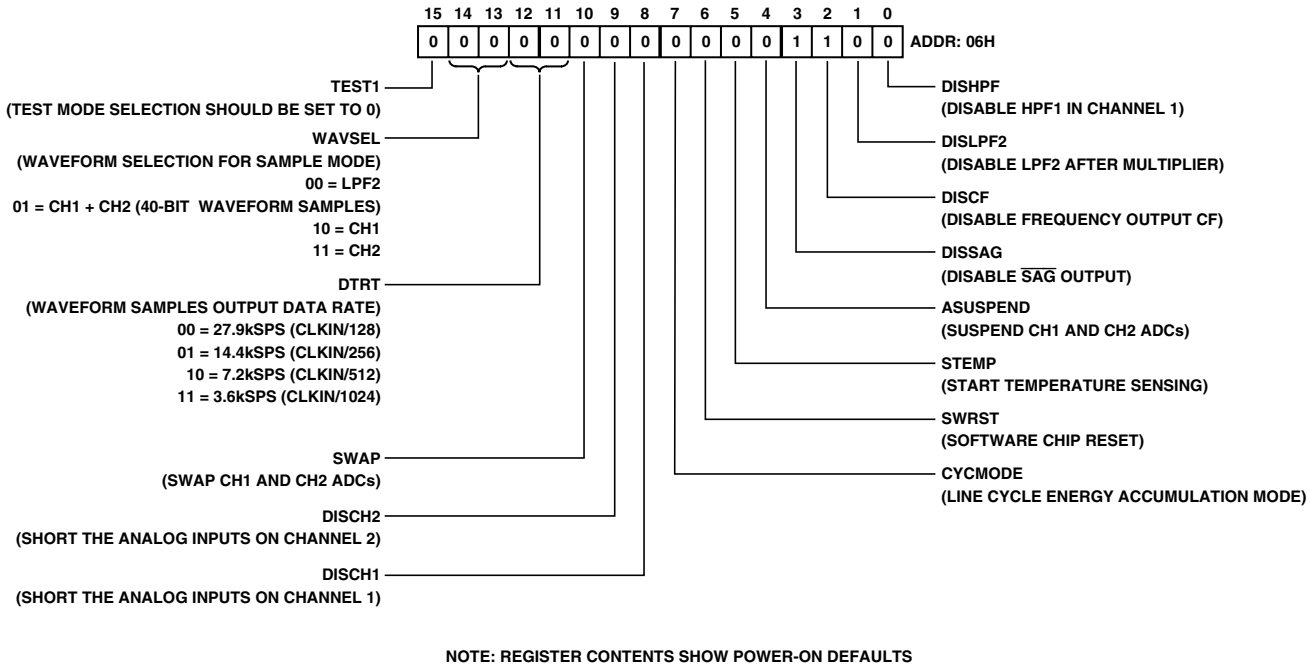


Figure 48. Mode Register

Interrupt Status Register (04H)/Reset Interrupt Status Register (05H)

The status register is used by the MCU to determine the source of an interrupt request ($\overline{IRQ}$). When an interrupt event occurs in the ADE7759, the corresponding flag in the interrupt status register is set logic high. If the enable bit for this flag is Logic 1 in the interrupt enable register, the $\overline{IRQ}$ logic output goes active low. When the MCU services the interrupt, it must first carry out a read from the interrupt status register to determine the source of the interrupt.

Table VII. Interrupt Status Register, Reset Interrupt Status Register, and Interrupt Enable Register

Bit Location	Interrupt Flag	Description
0	AEHF	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the active energy register.
1	SAG	Indicates that an interrupt was caused by a SAG on the line voltage or no zero crossings were detected.
2	CYCEND	Indicates the end of energy accumulation over an integer number of half line cycles as defined by the content of the LINECYC register—see Line Cycle Energy Accumulation Mode section.
3	WSMP	Indicates that new data is present in the waveform register.
4	ZX	This status bit reflects the status of the ZX logic output—see Zero Crossing Detection section.
5	TEMP	Indicates that a temperature conversion result is available in the temperature register.
6	RESET	Indicates the end of a reset (for both software or hardware reset). The corresponding enable bit has no function in the interrupt enable register, i.e., this status bit is set at the end of a reset, but it cannot be enabled to cause an interrupt.
7	AEOF	Indicates that the active energy register has overflowed.

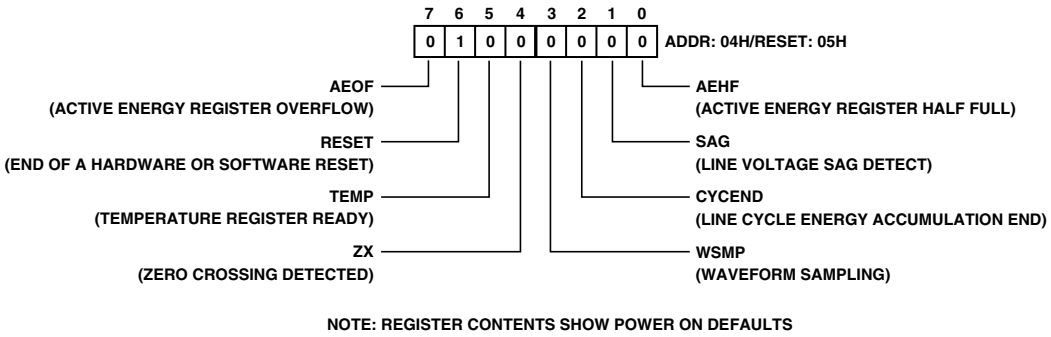


Figure 49. Interrupt Status Register

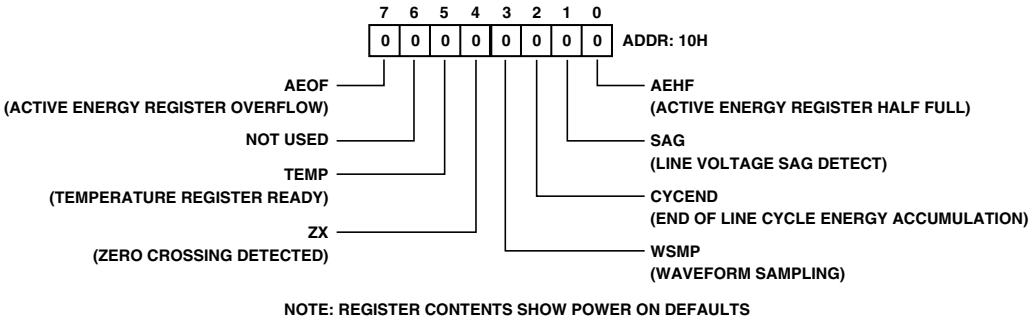


Figure 50. Interrupt Enable Register

CH1OS Register (08H)

The CH1OS register is an 8-bit, read/write enabled register. The MSB of this register is used to switch on/off the digital integrator in Channel 1, and Bits 0 to 5 indicate the amount of the offset correction in Channel 1. Table VIII summarizes the function of this register.

Table VIII. CH1OS Register

Bit Location	Bit Mnemonic	Description
0 to 5	OFFSET	The six LSBs of the CH1OS register control the amount of dc offset correction in Channel 1 ADC. The 6-bit offset correction is sign and magnitude coded. Bits 0 to 4 indicate the magnitude of the offset correction. Bit 5 shows the sign of the offset correction. A 0 in Bit 5 means the offset correction is positive and a 1 indicates the offset correction is negative.
6	Not Used	This bit is unused.
7	INTEGRATOR	This bit is used to activate the digital integrator on Channel 1. The digital integrator is switched on by setting this bit. This bit is set to be 1 on default.

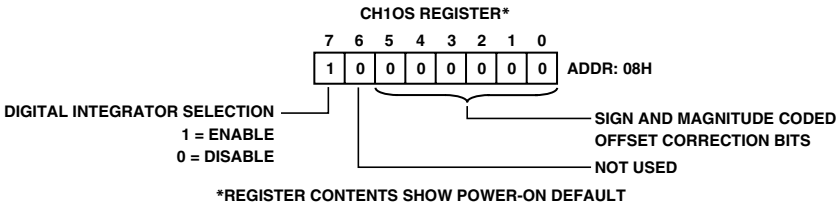
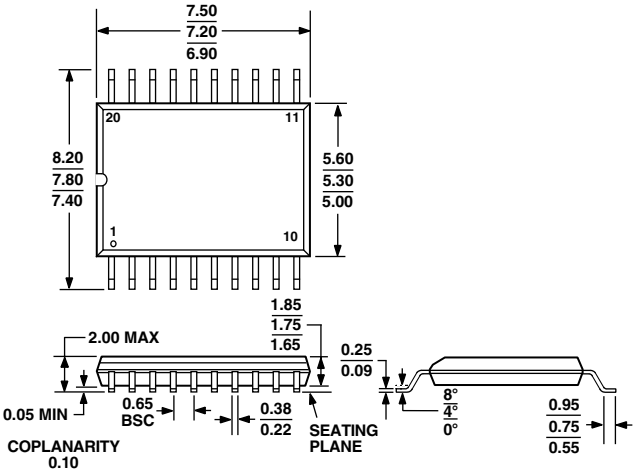


Figure 51. CH1OS Register

OUTLINE DIMENSIONS

20-Lead Shrink Small Outline Package [SSOP] (RS-20)

Dimensions shown in millimeters



Revision History

Location	Page
12/02—Data Sheet changed from REV. 0 to REV. A.	
Changes to SPECIFICATIONS	3
Changes to ORDERING GUIDE	6
Changes to Figure 23	18
Updated OUTLINE DIMENSIONS	34

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