

Inverter Grade Thyristors (Stud Version), 105 A



TO-209AC (TO-94)

FEATURES

- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- Guaranteed high dI/dt
- High surge current capability
- Low thermal impedance
- High speed performance
- Compression bonding
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRODUCT SUMMARY

Package	TO-209AC (TO-94)
Diode variation	Single SCR
$I_{T(AV)}$	105 A
V_{DRM}/V_{RRM}	400 V, 800 V
V_{TM}	1.73 V
I_{TSM} at 50 Hz	3000 A
I_{TSM} at 60 Hz	3150 A
I_{GT}	200 mA
T_C/T_{hs}	85 °C

TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		105	A
	T_C	85	°C
$I_{T(RMS)}$		165	A
I_{TSM}	50 Hz	3000	
	60 Hz	3150	
I^2t	50 Hz	45	kA ² s
	60 Hz	41	
V_{DRM}/V_{RRM}		400 to 800	V
t_q	Range	10 to 25	μs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST103S	04	400	500	30
	08	800	900	

**CURRENT CARRYING CAPABILITY**

FREQUENCY							UNITS
50 Hz	280	180	440	330	4730	3630	A
400 Hz	310	200	470	300	2500	1850	
1000 Hz	320	200	480	310	1530	1090	
2500 Hz	340	210	490	320	840	580	
Recovery voltage V_r	50		50		50		V
Voltage before turn-on V_d	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current di/dt	50		-		-		A/μs
Case temperature	60	85	60	85	60	85	°C
Equivalent values for RC circuit	22/0.15		22/0.15		22/0.15		Ω/μF

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS	
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			105	A	
					85	°C	
Maximum RMS on-state current	I _{T(RMS)}	DC at 76 °C case temperature			165	A	
Maximum peak, one half cycle, non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	3000		
		t = 8.3 ms			3150		
		t = 10 ms	100 % V _{RRM} reapplied		2530		
		t = 8.3 ms			2650		
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		45	kA ² s	
		t = 8.3 ms			41		
		t = 10 ms	100 % V _{RRM} reapplied		32		
		t = 8.3 ms			29		
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied			450	kA ² √s	
Maximum peak on-state voltage	V _{TM}	I _{TM} = 300 A, T _J = T _J maximum, t _p = 10 ms sine wave pulse			1.73	V	
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			1.32		
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.35		
Low level value of forward slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			1.40	mΩ	
High level value of forward slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.30		
Maximum holding current	I _H	T _J = 25 °C, I _T > 30 A			600	mA	
Typical latching current	I _L	T _J = 25 °C, V _A = 12 V, R _a = 6 Ω, I _G = 1 A			1000		

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned on current	di/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$, $I_{TM} = 2 \times di/dt$	1000	A/μs
Typical delay time	t_d	$T_J = 25$ °C, $V_{DM} = \text{Rated } V_{DRM}$, $I_{TM} = 50$ A DC, $t_p = 1$ μs Resistive load, gate pulse: 10 V, 5 Ω source	0.80	μs
Maximum turn-off time	minimum	$T_J = T_J$ maximum, $I_{TM} = 100$ A, commutating $di/dt = 10$ A/μs $V_R = 50$ V, $t_p = 200$ μs, dV/dt : See table in device code	10	
	maximum		25	

**BLOCKING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM} , higher value available on request	500	V/ μ s
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	40	W
Maximum average gate power	$P_{G(AV)}$		5	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	5	A
Maximum peak positive gate voltage	$+V_{GM}$		20	V
Maximum peak negative gate voltage	$-V_{GM}$		5	
Maximum DC gate current required to trigger	I_{GT}	$T_J = 25$ °C, $V_A = 12$ V, $R_a = 6$ Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{Stg}		-40 to 150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.195	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.08	
Mounting torque, ± 10 %		Non-lubricated threads	15.5 (137)	N · m (lbf · in)
		Lubricated threads	14 (120)	
Approximate weight			130	g
Case style		See dimensions - link at the end of datasheet	TO-209AC (TO-94)	

 ΔR_{thJC} CONDUCTION

CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.034	0.025	$T_J = T_J$ maximum	K/W
120°	0.040	0.042		
90°	0.052	0.056		
60°	0.076	0.079		
30°	0.126	0.127		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

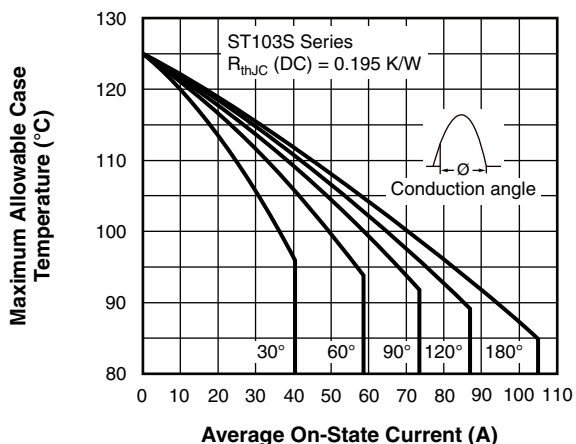


Fig. 1 - Current Ratings Characteristics

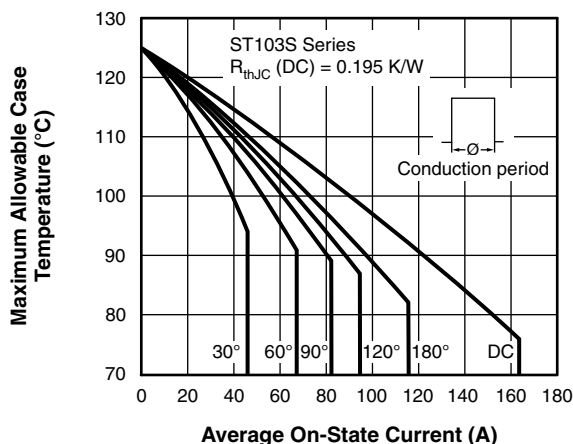


Fig. 2 - Current Ratings Characteristics

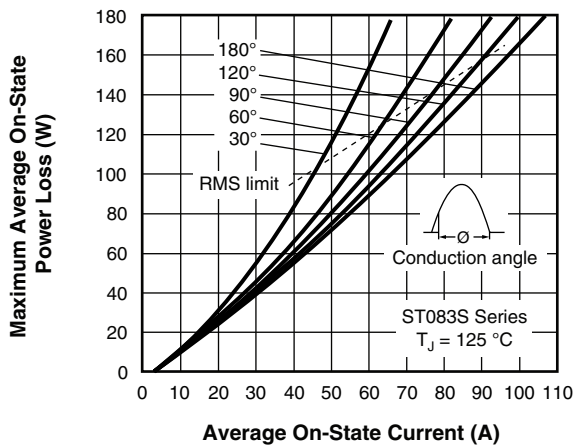


Fig. 3 - On-State Power Loss Characteristics

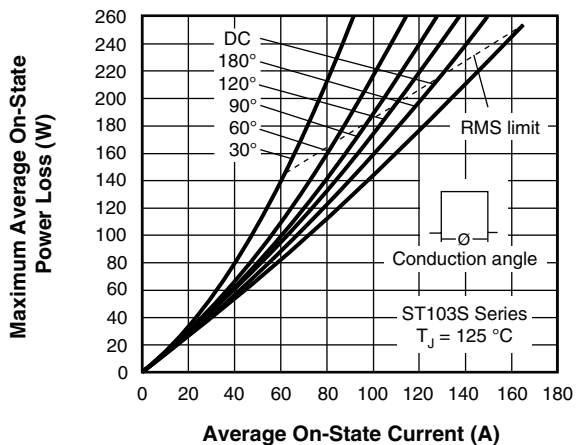
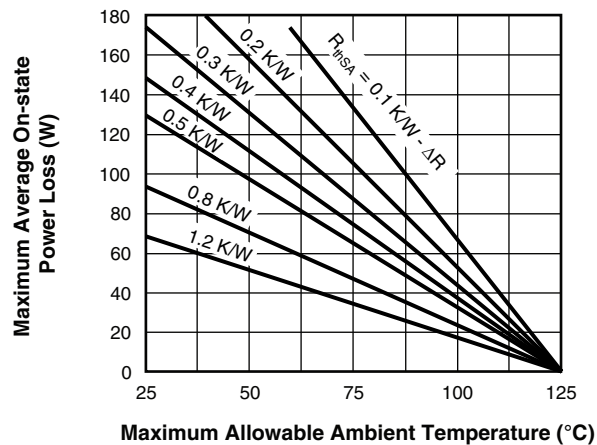
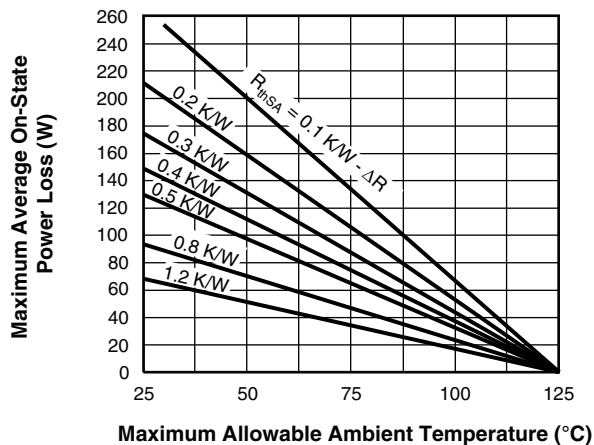


Fig. 4 - On-State Power Loss Characteristics



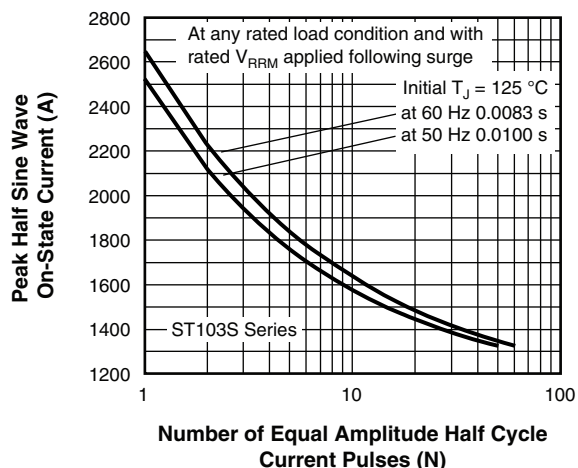


Fig. 5 - Maximum Non-Repetitive Surge Current

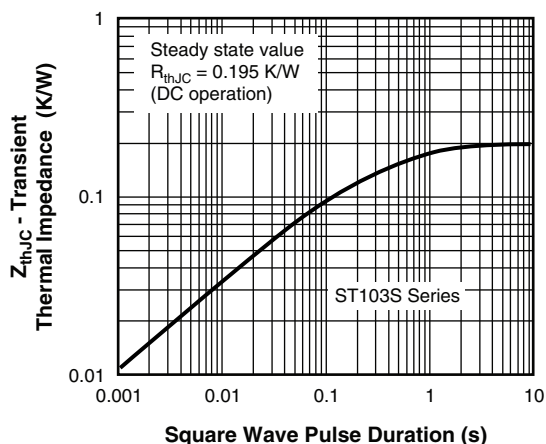
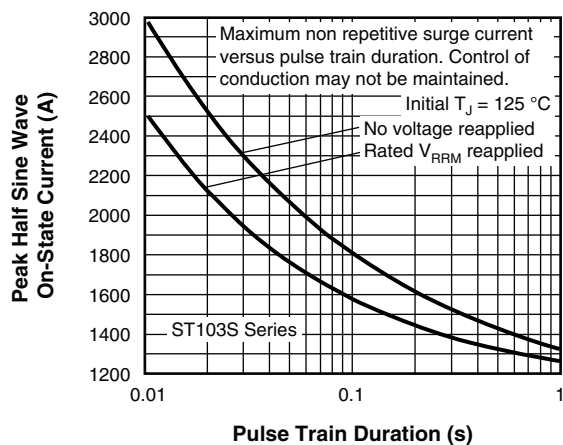

Fig. 8 - Thermal Impedance Z_{thJC} Characteristic


Fig. 6 - Maximum Non-Repetitive Surge Current

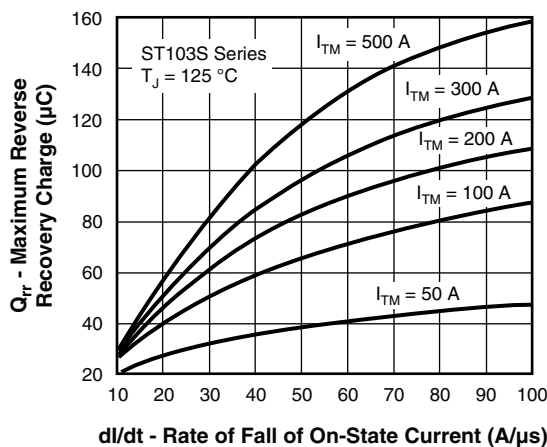


Fig. 9 - Reverse Recovered Charge Characteristics

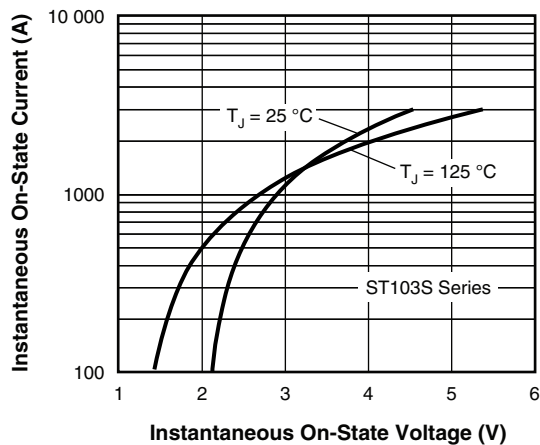


Fig. 7 - On-State Voltage Drop Characteristics

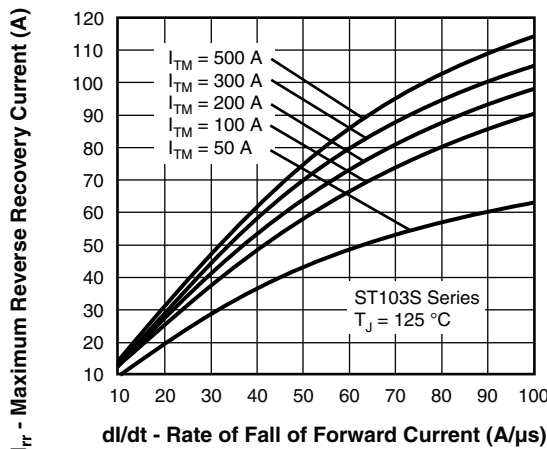


Fig. 10 - Reverse Recovery Current Characteristics

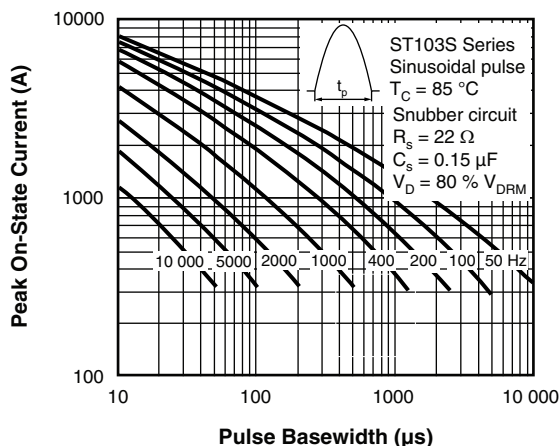
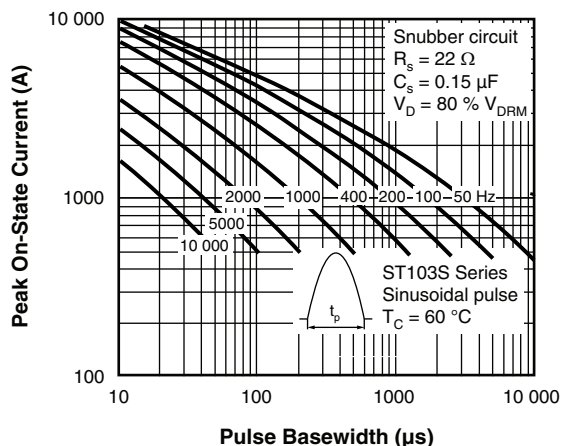


Fig. 11 - Frequency Characteristics

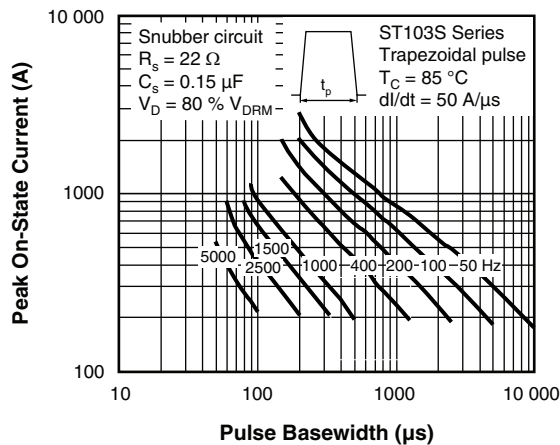
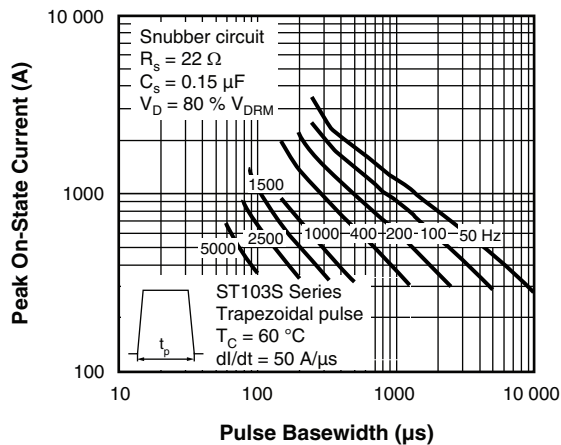


Fig. 12 - Frequency Characteristics

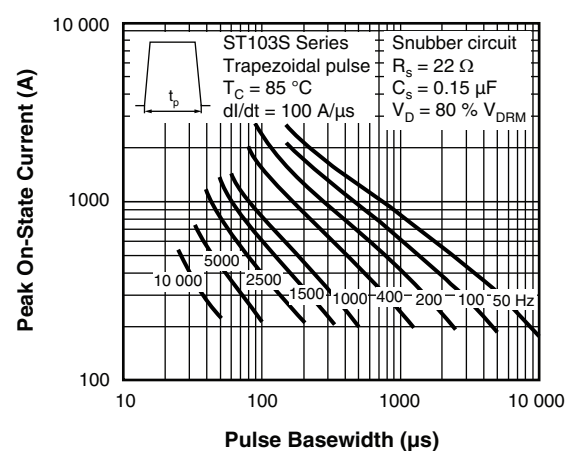
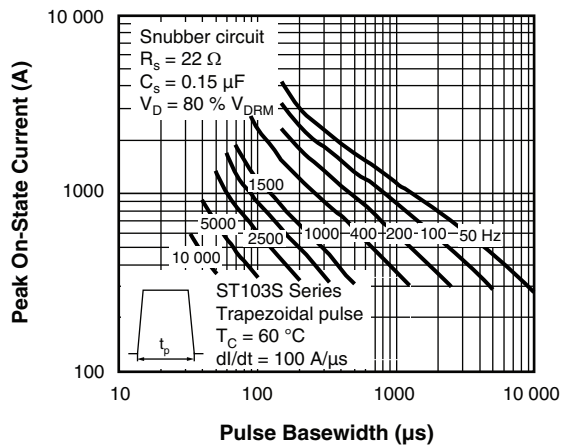


Fig. 13 - Frequency Characteristics

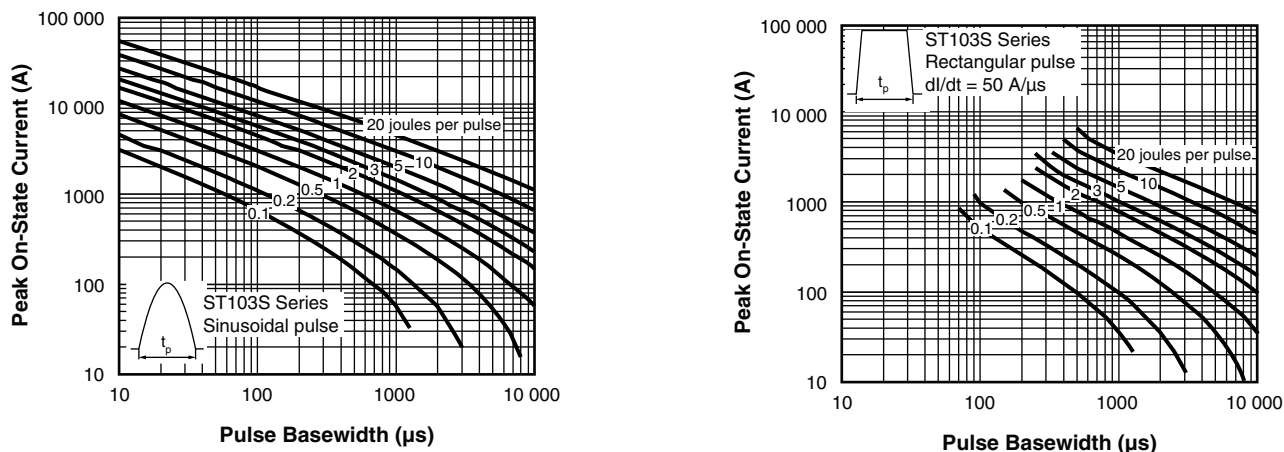


Fig. 14 - Maximum On-State Energy Power Loss Characteristics

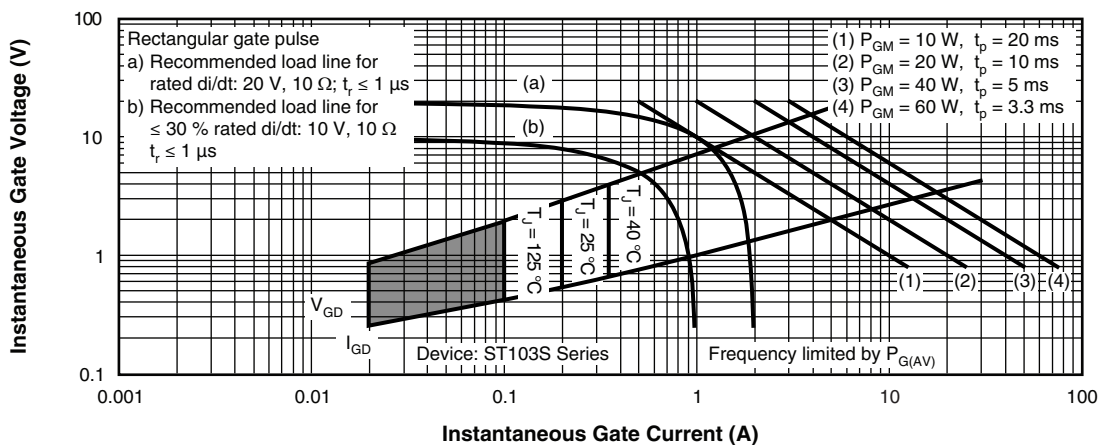


Fig. 15 - Gate Characteristics

**ORDERING INFORMATION TABLE**

Device code	VS-	ST	10	3	S	08	P	F	N	0	P
	1	2	3	4	5	6	7	8	9	10	11

- 1** - Vishay Semiconductors product
- 2** - Thyristor
- 3** - Essential part number
- 4** - 3 = Fast turn-off
- 5** - S = Compression bonding stud
- 6** - Voltage code x 100 = V_{RRM} (see Voltage ratings table)
- 7** - P = Stud base 1/2"-20UNF-2A
- 8** - Reapplied dV/dt code (for t_q test conditions)
- 9** - t_q code
- 10** - 0 = Eyelet terminals
(gate and aux. cathode leads)
1 = Fast-on terminals
(gate and aux. cathode leads)
- 11** - None = Standard production
P = Lead (Pb)-free

dV/dt - t_q combinations available					
dV/dt (V/ μ s)	20	50	100	200	400
10	CN	DN	EN	FN*	-
12	CM	DM	EM	FM	HM
15	CL	DL	EL	FL*	HL
18	CP	DP	EP	FP	HP
20	CK	DK	EK	FK	HK
25	-	-	-	-	HJ

* Standard part number.

All other types available only on request.

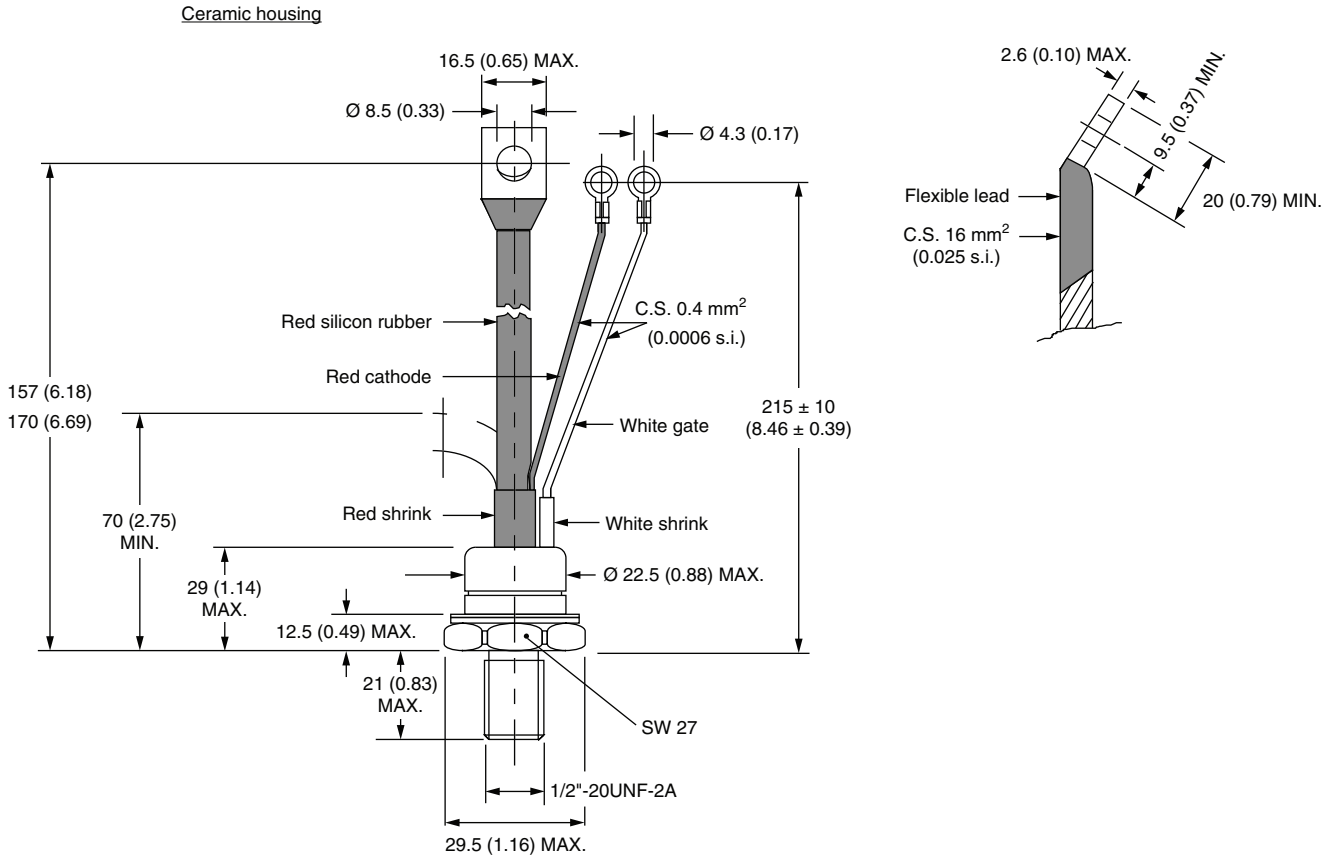
LINKS TO RELATED DOCUMENTS

Dimensions

www.vishay.com/doc?95003

TO-209AC (TO-94) for ST083S and ST103S Series

DIMENSIONS in millimeters (inches)





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