

■ Features, Benefits and Applications

- The world's only VCMO with programmable pull range: ± 60 PPM, ± 120 PPM, ± 240 PPM
- Typical pull range linearity of 0.06%
- 1-110 MHz frequency range
- LVCMOS/LVTTL compatible output
- Typical power consumption of 6.1 mA in active mode
- Typical VCMO tuning voltage: 0 V to 1.85 V for all Vdds
- Four industry-standard 4-pin packages: 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm
- All-silicon timing device with outstanding reliability of 2 FIT (10x improvement over quartz-based devices), enhancing system MTBF
- Ultra short lead time
- Ideal for Set-top Box, DTV, DVD-R, instrumentation, low bandwidth analog PLL, networking and communications

■ Specifications

Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-----------------------------|--------|----------------------------|------|------|------|---|
| Output Frequency Range | f | 1 | – | 110 | MHz | |
| Frequency Stability | F_stab | -20 | – | +20 | PPM | Inclusive of: Initial stability, operating temperature, rated power, supply voltage change, load change. ± 20 PPM is available for extended commercial temperature only. |
| | | -25 | – | +25 | PPM | |
| | | -30 | – | +30 | PPM | |
| | | -50 | – | +50 | PPM | |
| Pull Range ^[1,2] | PR | $\pm 60, \pm 120, \pm 240$ | | | PPM | |
| Upper Control Voltage | VC_U | 1.55 | – | 1.85 | V | All Vdds. Voltage at which maximum deviation (+60, +120, +240 PPM) is guaranteed. |
| Lower Control Voltage | VC_L | 0 | – | 0.1 | V | All Vdds. Voltage at which maximum deviation (-60, -120, -240 PPM) is guaranteed. |
| Linearity | Lin | – | 0.06 | 0.25 | % | |
| Frequency Change Polarity | – | Positive slope | | | – | |
| Operating Temperature Range | T_use | -20 | – | +70 | °C | Extended Commercial |
| | | -40 | – | +85 | °C | Industrial |
| Supply Voltage | Vdd | 1.71 | 1.8 | 1.89 | V | |
| | | 2.25 | 2.5 | 2.75 | V | |
| | | 2.52 | 2.8 | 3.08 | V | |
| | | 2.97 | 3.3 | 3.63 | V | |
| Current Consumption | Idd | – | 6.7 | 7.5 | mA | No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V |
| | | – | 6.1 | 6.7 | mA | No load condition, f = 20 MHz, Vdd = 1.8 V |
| Duty Cycle | DC | 45 | – | 55 | % | All Vdds. f \leq 75 MHz |
| | | 40 | – | 60 | % | All Vdds. f > 75 MHz |
| Rise/Fall Time | Tr, Tf | – | 1 | 2.0 | ns | Vdd = 2.5, 2.8 or 3.3 V, 20% - 80% Vdd level |
| | | – | 1 | 2.5 | ns | Vdd = 1.8 V, 20% - 80% Vdd level |
| Output Voltage High | VOH | 90 | – | – | %Vdd | IOH = -4 mA (Vdd = 3.3 V) IOH = -3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA (Vdd = 1.8 V) |
| Output Voltage Low | VOL | – | – | 10 | %Vdd | IOL = 4 mA (Vdd = 3.3 V) IOL = 3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOL = 2 mA (Vdd = 1.8 V) |
| Output Load | Ld | – | – | 15 | pF | Maximum frequency and supply voltage Contact SiTime for higher output load |
| Start-up Time | T_osc | – | – | 10 | ms | Time @ minimum supply voltage to be zero |
| RMS Period Jitter | T_jitt | – | – | 6 | ps | f = 75 MHz, Vdd = 1.8 V |
| | | – | – | 4 | ps | f = 75 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V |
| RMS Phase Jitter (random) | T_phj | – | 0.6 | – | ps | f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz, VDD = 2.5 V, 2.8 V, or 3.3 V |
| | | – | 0.8 | – | ps | f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz, VDD = 1.8 V |

Notes:

1. Absolute Pull Range (APR) is defined as the guaranteed pull range over temperature and voltage.
2. APR = pull range (PR) - frequency stability (F_stab).

■ Specifications (Cont.)

Pin Description Tables

| Pin #1 Functionality |
|---|
| VIN |
| 0 - 1.85 V: produces voltage dependent frequency change |

| Pin Map | |
|---------|------------|
| Pin | Connection |
| 1 | VIN |
| 2 | GND |
| 3 | CLK |
| 4 | VDD |

Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|--|--------|------|-------|
| Storage Temperature | -65 | 150 | °C |
| VDD | -0.5 | 4 | V |
| Electrostatic Discharge | – | 6000 | V |
| Theta JA (with copper plane on VDD and GND) | – | 75 | °C/W |
| Theta JC (with PCB traces of 0.010 inch to all pins) | – | 24 | °C/W |
| Soldering Temperature (follow standard Pb free soldering guidelines) | – | 260 | °C |
| Number of Program Writes | – | 1 | NA |
| Program Retention over -40 to 125 °C, Process, VDD (0 to 3.65 V) | 1,000+ | – | years |

Environmental Compliance

| Parameter | Condition/Test Method |
|----------------------------|---------------------------------|
| Mechanical Shock | MIL-STD-883F, Method 2002; 50kG |
| Mechanical Vibration | MIL-STD-883F, Method 2007; 70G |
| Temperature Cycle | JESD22, Method A104 |
| Solderability | MIL-STD-883F, Method 2003 |
| Moisture Sensibility Level | MSL1 @ 260 °C |

■ Dimensions and Land Patterns

| Package Size – Dimensions (Unit: mm) ^[3] | Recommended Land Pattern (Unit: mm) ^[4] |
|---|---|
| <p>2.5 x 2.0 x 0.75 mm</p> <p>Top view dimensions: 2.5 ± 0.10 mm (width), 2.0 ± 0.10 mm (height). Pin locations: #1, #2, #3, #4. Manufacturing origin 'Y' and lot number 'XXXX' are marked. Bottom view shows a 0.75 ± 0.05 mm thick package.</p> | <p>Land pattern dimensions: 1.9 mm (width between pads), 1.5 mm (height between pads), 1.1 mm (width of pads), 1.0 mm (height of pads).</p> |
| <p>3.2 x 2.5 x 0.75 mm</p> <p>Top view dimensions: 3.2 ± 0.15 mm (width), 2.5 ± 0.15 mm (height). Pin locations: #1, #2, #3, #4. Manufacturing origin 'Y' and lot number 'XXXX' are marked. Bottom view shows a 0.75 ± 0.05 mm thick package.</p> | <p>Land pattern dimensions: 2.2 mm (width between pads), 1.9 mm (height between pads), 1.4 mm (width of pads), 1.2 mm (height of pads).</p> |
| <p>5.0 x 3.2 x 0.75 mm</p> <p>Top view dimensions: 5.0 ± 0.15 mm (width), 3.2 ± 0.15 mm (height). Pin locations: #1, #2, #3, #4. Manufacturing origin 'Y' and lot number 'XXXX' are marked. Bottom view shows a 0.75 ± 0.05 mm thick package.</p> | <p>Land pattern dimensions: 2.54 mm (width between pads), 2.2 mm (height between pads), 1.6 mm (height of pads), 1.5 mm (width of pads).</p> |
| <p>7.0 x 5.0 x 0.90 mm</p> <p>Top view dimensions: 7.0 ± 0.15 mm (width), 5.0 ± 0.15 mm (height). Pin locations: #1, #2, #3, #4. Manufacturing origin 'Y' and lot number 'XXXX' are marked. Bottom view shows a 0.90 ± 0.10 mm thick package. A 'No Connect' pad is indicated.</p> | <p>Land pattern dimensions: 5.08 mm (width between pads), 3.81 mm (height between pads), 2.2 mm (width of pads), 2.0 mm (height of pads).</p> |

Notes:

- Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
- A capacitor of value 0.1 μF between Vdd and GND is recommended.
- The 7050 package with part number designation "-8" has NO center pad.

■ Part No. Guide - How to Order

The Part No. Guide is for reference only. For real-time customization and exact part number, use the SiTime [Part Number Generator](#).

SiT3701AC-14-18F - 105.12345T



Notes:

- 6. Contact SiTime for different drive strength options for driving higher loads or reducing EMI.
- 7. Without Center Pad.

Frequency Stability vs. Temperature Range Options

| Frequency Stability (PPM) | Temperature Range | Supply Voltage | | | |
|---------------------------|-------------------|----------------|-------|-------|-------|
| | | 1.8 V | 2.5 V | 2.8 V | 3.3 V |
| ±20 | C (-20 to +70 °C) | ✓ | ✓ | ✓ | ✓ |
| | I (-40 to +85 °C) | - | - | - | - |
| ±25 | C (-20 to +70 °C) | ✓ | ✓ | ✓ | ✓ |
| | I (-40 to +85 °C) | ✓ | ✓ | ✓ | ✓ |
| ±30 | C (-20 to +70 °C) | ✓ | ✓ | ✓ | ✓ |
| | I (-40 to +85 °C) | ✓ | ✓ | ✓ | ✓ |
| ±50 | C (-20 to +70 °C) | ✓ | ✓ | ✓ | ✓ |
| | I (-40 to +85 °C) | ✓ | ✓ | ✓ | ✓ |

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