150V Low I_Q Step-Down DC/DC Controller with 100% Duty Cycle Capability

FEATURES

- **Wide Operating V_{IN} Range: 4.5V to 150V**
- **Wide V_{OUT} Range: 0.8V to 60V**
- **9µA I_Q when Regulating 48V_{IN} to 3.3V_{OUT}**
- **16µA I_Q when Regulating 12V_{IN} to 3.3V_{OUT}**
- **Very Low Dropout Operation: 100% Duty Cycle**
- **Adjustable Input Overvoltage Lockout**
- **Programmable PGOOD Undervoltage Monitor**
- **R_{SENSE} or Inductor DCR Current Sensing**
- Selectable High Efficiency Burst Mode® Operation or Pulse-Skipping Mode at Light Loads
- Programmable Fixed Frequency: 50kHz to 850kHz
- Phase-Lockable Frequency: 75kHz to 800kHz
- Internal Fixed Soft-Start and External Programmable Soft-Start or Voltage Tracking
- Strong MOSFET Gate Driver with Selectable Undervoltage Lockout Thresholds
- Optional External NMOS for Gate Driver Bias in High Power Applications

APPLICATIONS

- Automotive and Industrial Power Systems
- Telecommunication Power Systems
- Distributed Power Systems

DESCRIPTION

The LTC®3894 is a high voltage step-down DC/DC switching regulator controller. It drives a P-channel power MOSFET switch allowing 100% duty cycle operation. It enables a low part count, simple, and robust solution for high reliability, high voltage applications.

The LTC3894 operates over a wide input voltage range from 4.5V to 150V and can regulate output voltages from 0.8V to 60V. It offers excellent light load efficiency, drawing only 9µA quiescent current while regulating the output voltage with no load. Its peak current mode, constant frequency architecture provides for good control of switching frequency and output current limit. The switching frequency can be programmed from 50kHz to 850kHz with an external resistor and can be synchronized to an external clock from 75kHz to 800kHz.

The LTC3894 offers programmable output voltage soft-start or tracking. Safety features include overvoltage, overcurrent and overtemperature protection with a power good output monitor with adjustable threshold.

The LTC3894 is available in a thermally enhanced 20-Pin TSSOP package with leads removed to accommodate high voltage creepage and clearance requirements.

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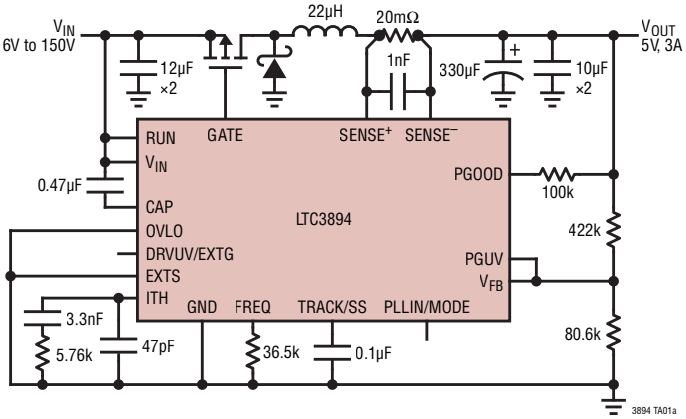
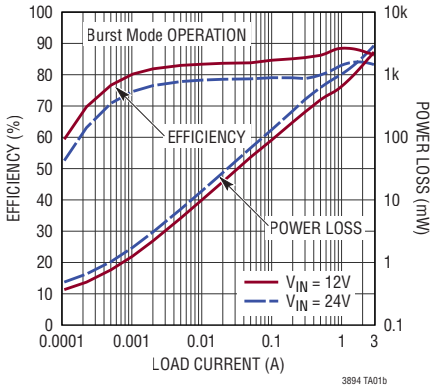
TYPICAL APPLICATION

High Efficiency 150V to 5V Step-Down Regulator



Efficiency and Power Loss vs Load Current



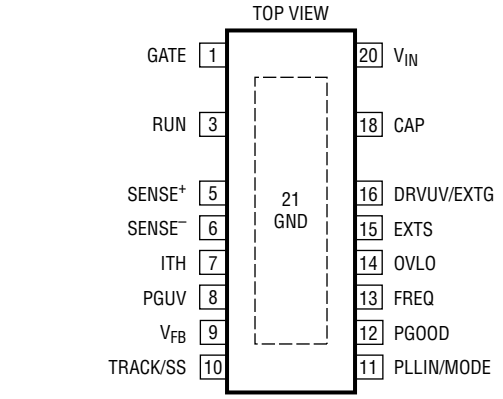
Rev. A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}), RUN ..... –0.3V to 150V
SENSE+, SENSE–, PGOOD Voltage ..... –0.3V to 65V
V_{IN}-V_{CAP} Voltage ..... –0.3V to 10V
V_{FB}, PLLIN/MODE, PGUV, OVLO,
EXTS Voltages ..... –0.3V to 6V
TRACK/SS Voltage (Note 11) ..... –0.3V to 2.8V
ITH, FREQ Voltage ..... –0.3V to 5V
DRVUV/EXTG Voltage ..... –0.3V to 9V
Operating Junction Temperature Range (Notes 2, 3)
LTC3894E, LTC3894I ..... –40°C to 125°C
LTC3894H ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



FE PACKAGE
20(16)-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB FOR RATED ELECTRICAL AND THERMAL CHARACTERISTICS

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3894EFE#PBF	LTC3894EFE#TRPBF	LTC3894FE	20(16)-Lead Plastic TSSOP	–40°C to 125°C
LTC3894IFE#PBF	LTC3894IFE#TRPBF	LTC3894FE	20(16)-Lead Plastic TSSOP	–40°C to 125°C
LTC3894HFE#PBF	LTC3894HFE#TRPBF	LTC3894FE	20(16)-Lead Plastic TSSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{IN}	Input Voltage Operating Range	(Note 4) DRVUV = 0V		4.5		150	V
V_{OUT}	Regulated Output Voltage Set Point			0.8		60	V
I_Q	No Load DC Supply Current (Note 5)						
	Shutdown V_{IN} Pin Current	RUN = 0V			7	11	µA
	Sleep Mode V_{IN} Pin Current	V_{SENSE}^- = 2.5V, V_{FB} = 0.83V			27	40	µA
		V_{SENSE}^- ≥ 3.2V, V_{FB} = 0.83V			7	10	µA
	Sleep Mode $SENSE^-$ Pin Current (Note 6)	V_{SENSE}^- ≥ 3.2V, V_{FB} = 0.83V			21	30	µA
	Pulse-Skipping Mode V_{IN} Pin Current	V_{FB} = 0.83V V_{SENSE}^- = 0V V_{SENSE}^- = 3.3V V_{SENSE}^- = 5V			 1.8 1.5 0.8		 mA mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{Q(VINR)}$	Total Input Supply Current in Regulation at No Load in Burst Mode (Note 7)	V_{IN} = 12V Figure 14 Circuit, V_{OUT} = 3.3V Figure 12 Circuit, V_{OUT} = 5V			 16 22		 µA µA
		V_{IN} = 48V Figure 14 Circuit, V_{OUT} = 3.3V Figure 12 Circuit, V_{OUT} = 5V			 9 11		 µA µA
Output Sensing							
V_{FB}	Regulated Feedback Voltage	V_{ITH} = 1.2V (Note 8)	●	0.788	0.800	0.812	V
	Feedback Voltage Line Regulation	V_{IN} = 4.5V to 150V (Note 8)			±0.002	0.015	%/V
	Feedback Voltage Load Regulation	V_{ITH} = 0.6V to 1.8V (Note 8)			0.03	0.15	%
$g_{m(EA)}$	Error Amplifier Transconductance	V_{ITH} = 1.2V, ΔI_{ITH} = ±5µA (Note 8)			2		mS
I_{FB}	Feedback Input Bias Current				–10	±50	nA
Current Sensing							
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold ($V_{SENSE}^+ - V_{SENSE}^-$)	V_{FB} = 0.7V, V_{SENSE}^- = 3.3V	●	88	100	112	mV
I_{SENSE}^+	SENSE+ Pin Input Current	V_{SENSE}^+ = 3.3V			0.1	1	µA
I_{SENSE}^-	SENSE– Pin Input Current in Non-Sleep Mode (Note 6)	V_{SENSE}^- = 3.3V V_{SENSE}^- = 5V			200 880	300 1260	µA µA
Start-Up and Shutdown							
V_{RUN}	RUN Pin Enable Threshold	V_{RUN} Rising	●	1.14	1.24	1.34	V
V_{RUNHYS}	RUN Pin Hysteresis				125		mV
I_{SS}	Soft-Start Pin Charging Current	V_{SS} = 0V or 0V to 0.8V		8	11	14	µA
V_{OVLO}	Overvoltage Lockout Threshold	V_{OVLO} Rising Up Hysteresis	●	0.77	0.8 30	0.82	V mV
Gate Driver and V_{IN}-Cap LDO							
V_{UVLO}	Undervoltage Lockout	DRVUV = 0 (V_{IN}-V_{CAP}) Ramping Up Threshold (V_{IN}-V_{CAP}) Ramping Down Threshold Hysteresis	 ● ●	 3.4 3.25	 3.75 3.50 0.25	 4.3 3.75	 V V V
		DRVUV = Floating (V_{IN}-V_{CAP}) Ramping Up Threshold (V_{IN}-V_{CAP}) Ramping Down Threshold Hysteresis	 ● ●	 5.5 5.2	 6.0 5.55 0.45	 6.55 5.85	 V V V
V_{CAP}	Gate Bias LDO Output Voltage (V_{IN}-V_{CAP})	I_{CAP} = 0mA, 9V ≤ V_{IN} ≤ 150V (Note 9)	●	7.5	8.0	8.5	V
$V_{CAPDROP}$	Gate Bias LDO Dropout Voltage (V_{IN}-V_{CAP})	V_{IN} = 5V, I_{CAP} = 15mA (Note 9)		4.1	4.4		V
$\Delta V_{CAP(LOAD)}$	Gate Bias LDO Load Regulation	I_{CAP} = 0mA to 20mA		–2.8	–1.3		%
R_{UP}	Gate Pull-Up Resistance	Gate High			2		Ω
R_{DN}	Gate Pull-Down Resistance	Gate Low			0.9		Ω
$t_{ON(MIN)}$	Gate Minimum On-Time	(Note 10)			125		ns
Switching Frequency and Clock Synchronization							
f	Programmable Switching Frequency	R_{FREQ} = 25kΩ R_{FREQ} = 64.9kΩ R_{FREQ} = 105kΩ		 375	100 440 810	 505	kHz kHz kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{LO}	Low Switching Frequency	FREQ = 0V		320	350	380	kHz
f_{HI}	High Switching Frequency	FREQ = Open		470	530	590	kHz
f_{SYNC}	Synchronization Frequency		●	75		800	kHz
$V_{CLK(HI)}$	Clock Input High Level into PLLIN/MODE		●	2			V
$V_{CLK(LO)}$	Clock Input Low Level into PLLIN/MODE		●			0.5	V
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.2	0.35	V
I_{PG}	PGOOD Leakage Current	V_{PGOOD} = 65V				1	µA
V_{PGOV}	PGOOD Overvoltage Trip Threshold 	V_{FB} Ramping Positive with Respect to Set Regulated Voltage Hysteresis		7	10 2.5	13	% %
V_{PGUV}	PGOOD Undervoltage Trip Threshold	V_{PGUV} Ramping Negative Hysteresis		700	720 2.5	740	mV %
t_{PGDL}	PGOOD Delay	PGOOD High to Low PGOOD Low to High			100 100		µs µs
V_{FBOV}	V_{FB} Overvoltage Lockout Threshold	V_{FB} Ramping Positive with Respect to Set Regulated Voltage Hysteresis			10 2.5		% %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3894 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3894E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3894I is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC3894H is guaranteed over the –40°C to 150°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. High temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125ºC. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 38°C/W for the TSSOP package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The minimum input supply operating range is dependent on the UVLO thresholds as determined by the DRVUV/EXTG pin setting.

Note 5: The DC supply current is measured when the LTC3894 is not switching. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 6: SENSE1$^-$ bias current is reflected to the input supply by the formula

$$I_{VIN} = I_{SENSE1^-} \bullet V_{OUT}/(V_{IN} \bullet \eta)$$, where η is the efficiency.

Note 7: The total input supply current in Burst Mode is the total current drawn from input supply as measured in the Typical Application circuit on page 1 and Figure 14 on page 32 with no load current. The specification is not tested in production.

Note 8: The LTC3894 is tested in a feedback loop that servos the error amplifier output voltage (on ITH pin) to a specified voltage and measures the resultant V_{FB} voltage.

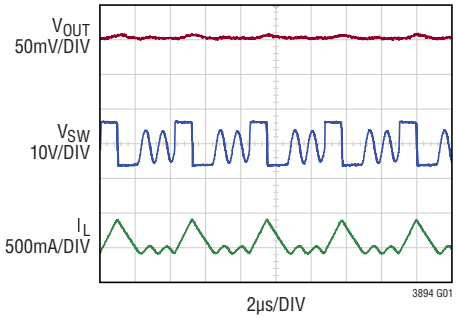
Note 9: Positive I_{CAP} current flows into the CAP pin and discharges the capacitor between the V_{IN} and CAP pins.

Note 10: The minimum on-time condition is specified for an inductor peak-to-peak ripple current > 40% of I_{MAX}.

Note 11: The absolute maximum rating for TRACK/SS pin is 2.8V when the pin is driven externally. When the pin is not driven, it may be pulled higher by the IC, typically to 4.7V.

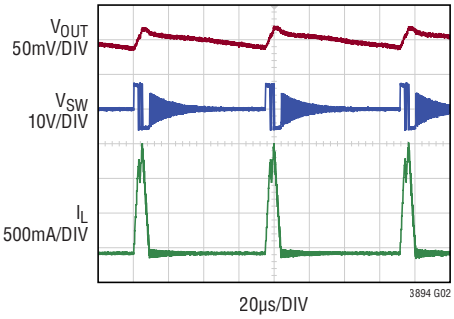
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Pulse-Skipping Mode Operation Waveforms



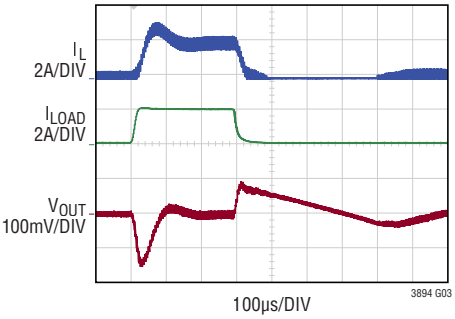
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 100mA
FIGURE 11 CIRCUIT

Burst Mode Operation Waveforms



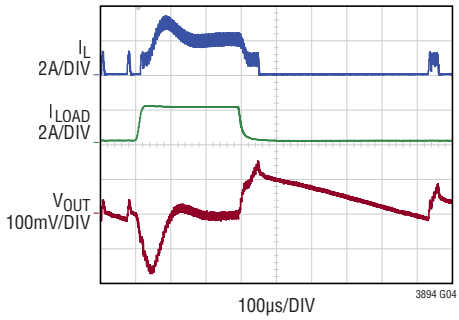
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 100mA
FIGURE 11 CIRCUIT

Transient Response: Pulse-Skipping Mode Operation



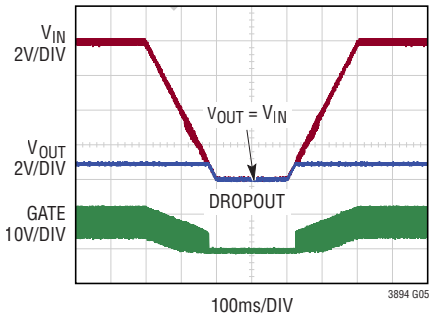
V_{IN} = 12V
V_{OUT} = 5V
LOAD STEP = 100mA TO 2A
FIGURE 11 CIRCUIT

Transient Response: Burst Mode Operation



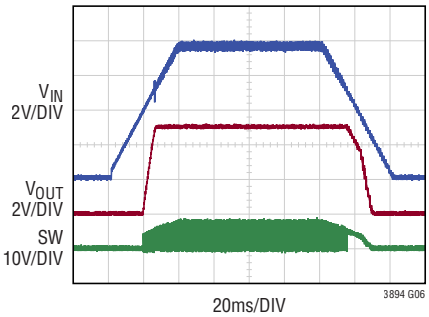
V_{IN} = 12V
V_{OUT} = 5V
LOAD STEP = 100mA TO 2A
FIGURE 11 CIRCUIT

Dropout Behavior (100% Duty Cycle)



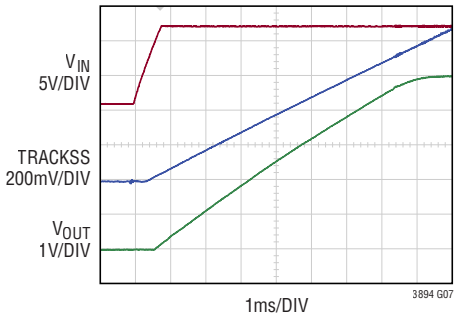
V_{IN} TRANSIENT 12V TO 4V
AND BACK TO 12V
V_{OUT} = 12V, I_{LOAD} = 100mA
FIGURE 14 CIRCUIT

Low V_{IN} Operation



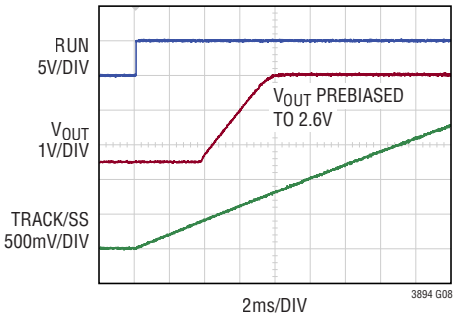
V_{IN} = 0V TO 7.8V
AND BACK TO 0V
V_{OUT} = 5V, I_{LOAD} = 100mA
FIGURE 11 CIRCUIT

Normal Soft Start-Up



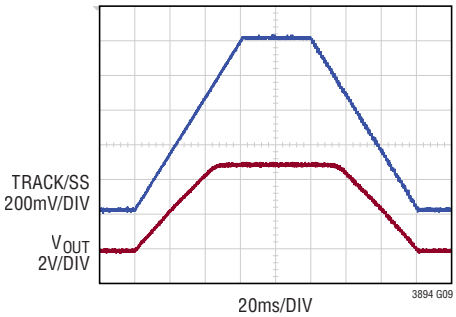
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 100mA
FIGURE 11 CIRCUIT

Soft Start-Up into a Prebiased Output



V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 500mA
FIGURE 11 CIRCUIT

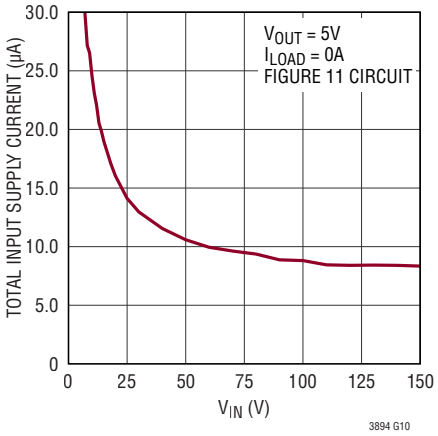
Output Tracking



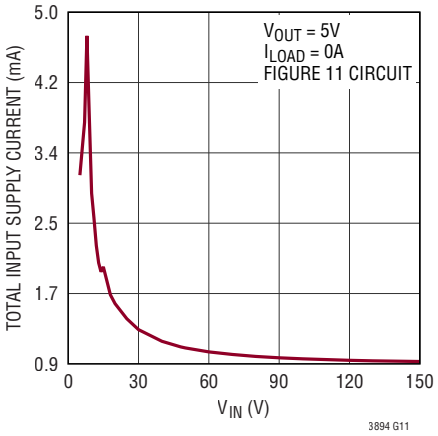
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 500mA
FIGURE 11 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

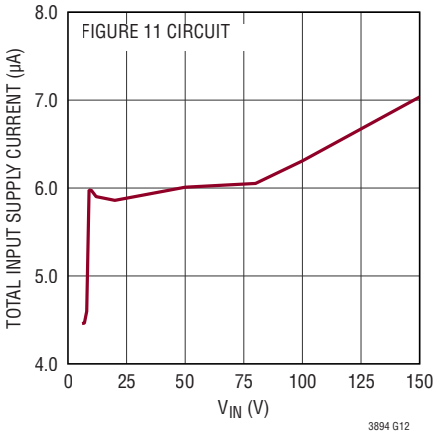
Burst Mode Input Current Over Input Voltage (No Load)



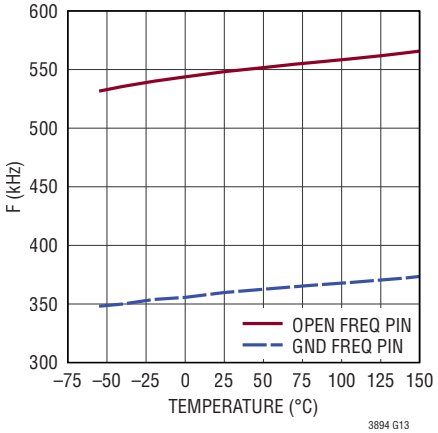
Pulse-Skipping Mode Input Current vs Input Voltage



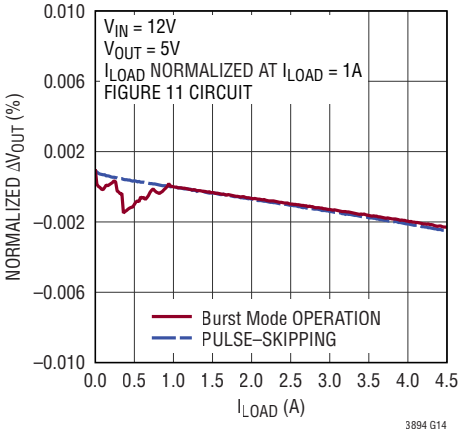
Shutdown Input Current vs Input Voltage



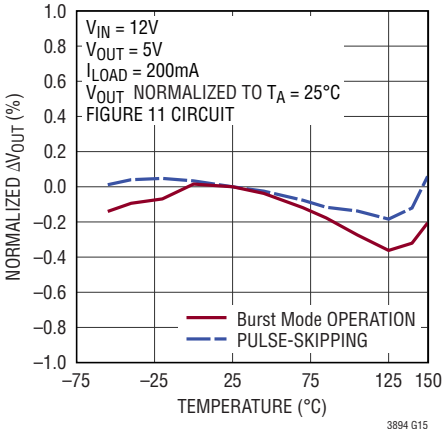
Free Running Frequency Over Temperature



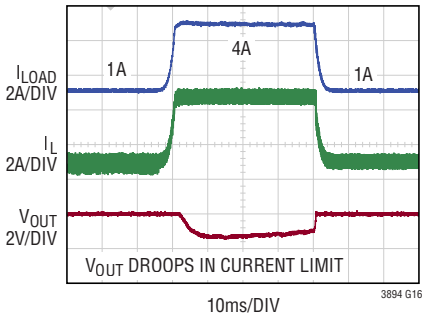
Output Regulation vs Load Current



Output Regulation vs Temperature

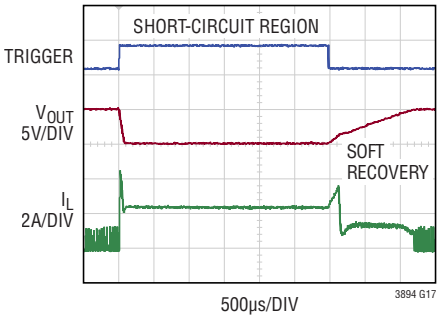


Overcurrent Protection



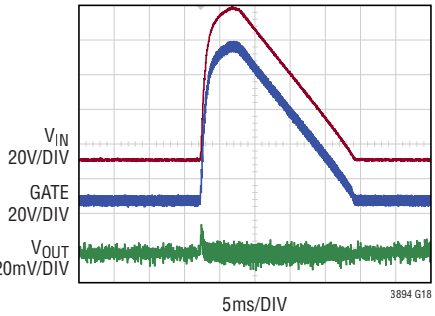
V_{IN} = 12V
V_{OUT} = 5V
FIGURE 11 CIRCUIT

Short-Circuit Protection



V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 500mA
FIGURE 11 CIRCUIT

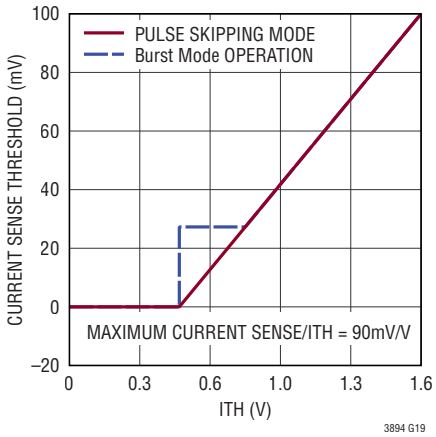
V_{IN} Line Transient Behavior



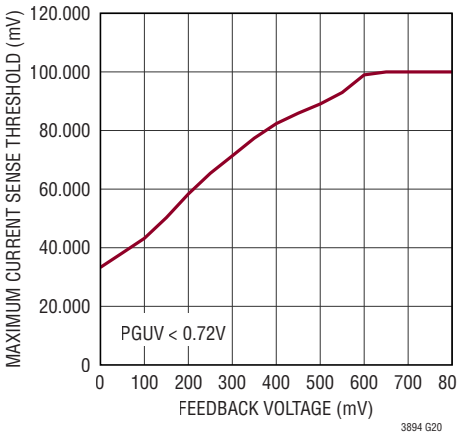
V_{IN} = 12V, SURGE TO 100V
V_{OUT} = 5V
I_{LOAD} = 2A
FIGURE 11 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

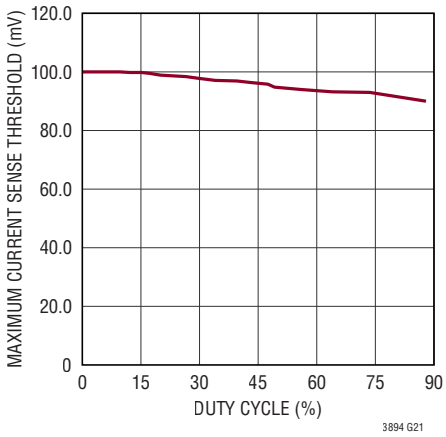
Maximum Current Sense Threshold vs ITH Voltage



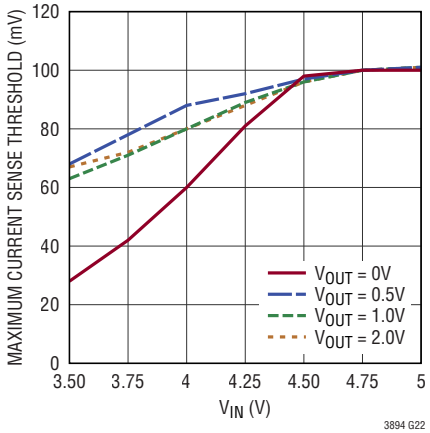
Buck Foldback Current Limit



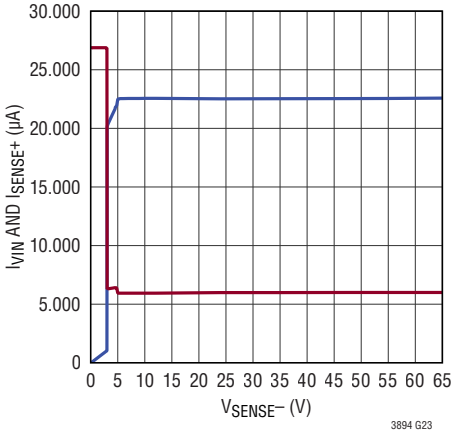
Maximum Current Sense Threshold vs Duty Cycle



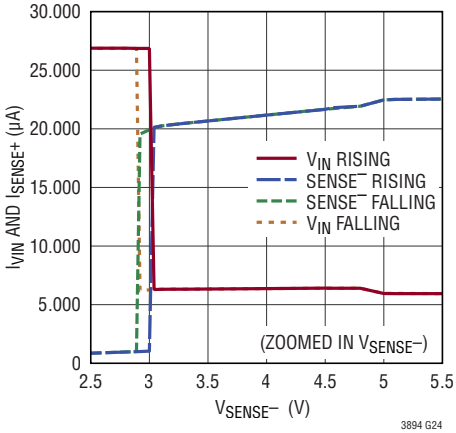
CLC vs V_{IN} at 150°C



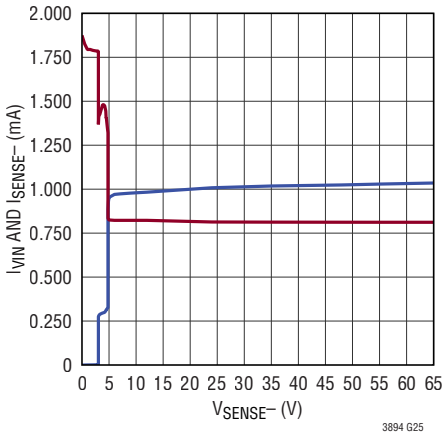
I_{VIN} and I_{SENSE^-} vs V_{SENSE^-} (Burst Mode Operation)



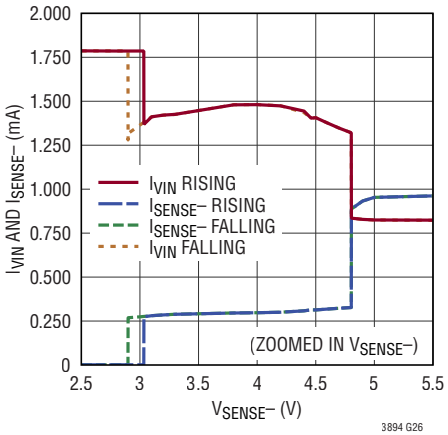
I_{VIN} and I_{SENSE^-} vs V_{SENSE^-} (Burst Mode Operation)



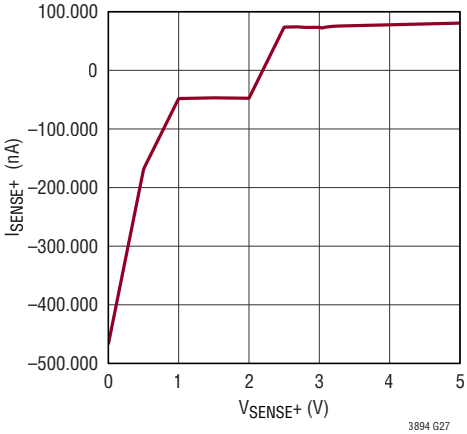
I_{VIN} and I_{SENSE^-} vs V_{SENSE^-} (Pulse-Skipping Mode)



I_{VIN} and I_{SENSE^-} vs V_{SENSE^-} (Pulse-Skipping Mode)



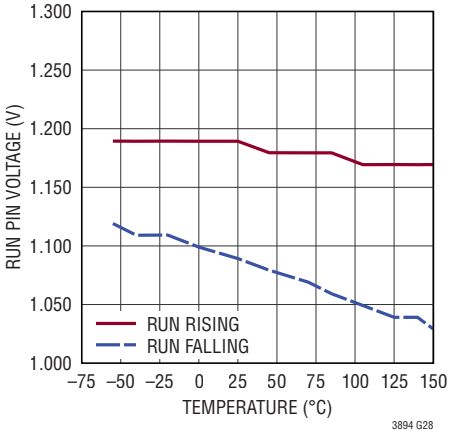
I_{SENSE^+} vs V_{SENSE^+}



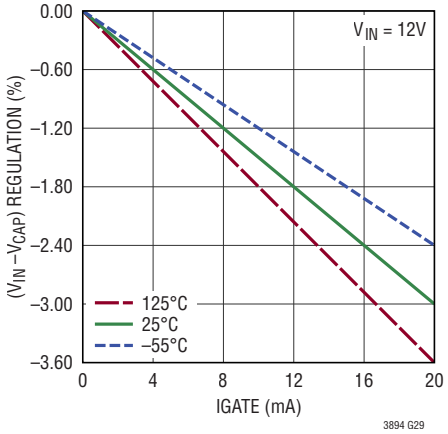
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

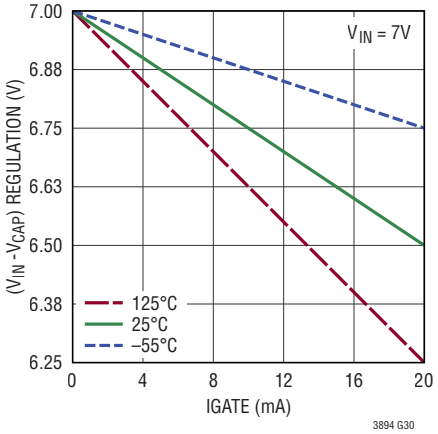
Shutdown (RUN) Threshold vs Temperature



GATE Bias LDO (V_{IN} - V_{CAP}) Load Regulation



GATE Bias LDO (V_{IN} - V_{CAP}) Dropout Regulation



PIN FUNCTIONS

GATE (Pin 1): Gate Drive Output for External P-Channel MOSFET. The voltage swing on this pin is between CAP and V_{IN}. The GATE driver output is held low at V_{CAP} to turn on the P-channel MOSFET and held high at V_{IN} to turn off the MOSFET. The gate driver output is held high when (V_{IN}-V_{CAP}) is less than V_{UVLO}.

RUN (Pin 3): Run Control High Impedance Input. A RUN voltage above the 1.26V threshold enables normal operation, while forcing this pin below 1.12V shuts down the controller. Forcing this pin below 0.7V shuts down the entire LTC3894, reducing quiescent current to approximately 7µA. This pin can be tied to V_{IN} directly or pulled up by a resistor. Do not float this pin.

SENSE$^+$ (Pin 5): Differential Current Sensing (+) Input. For R_{SENSE} current sensing, Kelvin (4-wire) connect SENSE$^+$ and SENSE$^-$ pins across the sense resistor. For DCR sensing, Kelvin connect SENSE$^+$ and SENSE$^-$ pins across the sense filter capacitor.

SENSE$^-$ (Pin 6): Differential Current Sensing (–) Input. For R_{SENSE} current sensing, Kelvin (4-wire) connect SENSE$^+$ and SENSE$^-$ pins across the sense resistor. For DCR sensing, Kelvin connect SENSE$^+$ and SENSE$^-$ pins across the filter capacitor. When SENSE$^-$ is greater than 3.2V, the SENSE$^-$ pin supplies power to internal circuitry. To reduce sensing errors, minimize the impedance in series with the SENSE$^-$ pin.

ITH (Pin 7): Error Amplifier Output and Switching Regulator Compensation Point. The voltage on this pin sets the current sense threshold.

PGUV (Pin 8): Pgood Undervoltage (UV) Comparator High Impedance Input. Connect the PGUV pin to the output through a resistor feedback divider or connect directly to V_{FB} pin to program the output PGOOD UV threshold. When the P_{GUV} pin voltage falls below 0.72V (0.8V – 10%) or lower, the PGOOD pin is asserted low after a 100µs blanking period.

V_{FB} (Pin 9): Output Feedback Sense Input. A resistor divider from the output to this pin sets the regulated output voltage. The LTC3894 will nominally regulate V_{FB} to the internal reference value of 0.8V.

PIN FUNCTIONS

TRACK/SS (Pin 10): Soft-Start and External Tracking Input. The LTC3894 regulates the V_{FB} voltage to the smaller of 0.8V or the voltage on the SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. Alternatively, another voltage supply connected through a resistor divider to this pin allows the output to track the other supply during start-up.

PLLIN/MODE (Pin 11): External Reference Clock Input and Burst Mode Enable/Disable. When an external clock is applied to this pin, the internal phase-locked loop will synchronize the turn-on edge of the gate drive signal with the rising edge of the external clock. When no external clock is applied, this input determines the mode of operation during light loading. Floating this pin selects low I_Q Burst Mode operation. Pulling to ground selects pulse-skipping mode operation.

PGOOD (Pin 12): Power Good Monitor Output. This open drain logic output is pulled to ground when the V_{FB} pin is 10% above its regulation point (OV) or when the PGUV pin voltage is below the PGOOD undervoltage (UV) threshold V_{PGUV}. There is a 100µs delay before PGOOD changes state in response to either an OV or a UV event.

FREQ (Pin 13): Switching Frequency Setpoint Input. The switching frequency is programmed between 75kHz and 850 kHz by an external setpoint resistor R_{FREQ} connected between the FREQ pin and SGND. An internal 20µA current source creates a voltage across the external setpoint resistor to set the internal oscillator frequency. Alternatively, this pin can be driven directly by a DC voltage to set the oscillator frequency. Grounding selects a fixed operating frequency of 350kHz. Floating selects a fixed operating frequency of 535kHz.

OVLO (Pin 14): Overvoltage Lockout High Impedance Input. For an adjustable V_{IN} overvoltage protection, connect this pin through a resistor divider to V_{IN}. When the voltage on this pin is greater than the 0.8V lockout threshold, ,the external P-channel MOSFET is turned off immediately and the TRACK/SS pin is discharged to GND to ensure a graceful recovery. Connect this pin to GND when the OVLO function is not used.

EXTS (Pin 15): Source Terminal Connection for the Optional External N-Channel MOSFET. When an optional external N-channel MOSFET is used to provide bias to the gate driver, connect this pin to the MOSFET source terminal and connect a 0.1µF bypass capacitor next to the the pin to ensure stable operation (see Applications Information section on page 21). When not in use, connect this pin to ground. Do not float this pin.

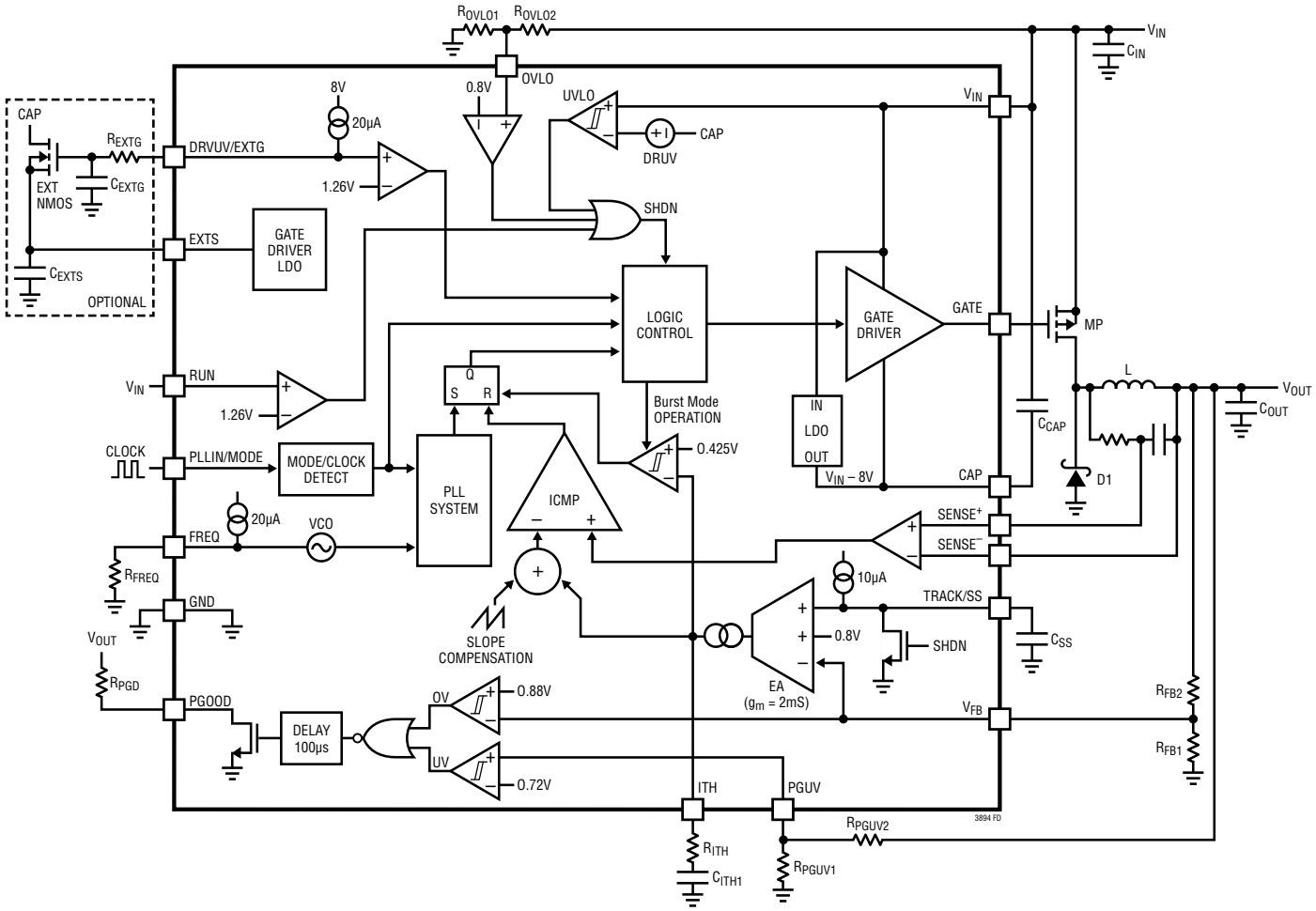
DRVUV/EXTG (Pin 16): Driver Undervoltage Lockout (UVLO) Select Pin and External N-Channel Gate Connection. This is a dual function pin. Grounding this pin selects a UVLO threshold of 3.75V between V_{IN} and CAP. Floating or connecting it to a voltage greater than 400mV selects a UVLO threshold of 6V. When an external N-channel MOSFET is used for the gate driver bias, connect its gate terminal to the pin through a 1k resistor. This selects the 6V UVLO threshold by default.

CAP (Pin 18): Lower Supply Rail for Gate Driver Bias. V_{IN} is the higher supply rail. The gate driver bias supply voltage (V_{IN}-V_{CAP}) is regulated to 8V when V_{IN} is greater than 8V. A low ESR ceramic bypass capacitor of at least 0.47µF is required from V_{IN} to CAP pin to maintain stable voltage regulation. The capacitor value needs to increase to a minimum of 2.2µF if an external N-channel MOSFET is used for gate driver bias. To ensure stable low noise operation, the bypass capacitor should be placed adjacent to the V_{IN} and CAP pins and connected using the same PCB metal layer.

V_{IN} (Pin 20): Chip Power Supply. A minimum bypass capacitor of 1µF is required from the V_{IN} pin to GND. For best performance use a low ESR ceramic capacitor and place the capacitor near the V_{IN} pin and GND pin to minimize the size of the high current loop.

GND (Exposed Pad Pin 21): Chip Ground. The exposed pad must be soldered to the circuit board for electrical contact and for rated electrical and thermal performance of the package.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop (Refer to Functional Diagram)

The LTC3894 uses a constant frequency peak current-mode control architecture to regulate the output voltage in an nonsynchronous step-down DC/DC switching regulator. The V_{FB} input is compared to an internal reference by a transconductance error amplifier (EA). The internal reference can be either a fixed 0.8V reference V_{REF} or the voltage input on the TRACK/SS pin. In normal operation V_{FB} regulates to the internal 0.8V reference voltage. In soft-start or tracking mode, when the TRACK/SS pin voltage is less than the internal 0.8V reference voltage, V_{FB} will regulate to the TRACK/SS pin voltage. The error amplifier output connects to the ITH pin. The voltage level on the ITH pin is then summed with a slope compensation ramp to create the peak inductor current set point.

The peak inductor current is measured through a sense resistor R_{SENSE} placed across the $SENSE^+$ and $SENSE^-$ pins. The resultant differential voltage from $SENSE^+$ to $SENSE^-$ is proportional to the inductor current and is compared to the peak inductor current set point. During normal operation the P-channel power MOSFET is turned on when the clock leading edge sets the SR latch through the S input. The P-channel MOSFET is turned off through the SR latch R input when the differential voltage of $V_{SENSE}^+ - V_{SENSE}^-$ is greater than the peak inductor current set point and the current comparator, I_{CMP}, trips high. After the MOSFET is turned off, an external Schottky diode carries inductor current until it reaches zero or the beginning of the next clock cycle.

Gate Driver Bias(V_{IN}–CAP) and Undervoltage Lockout (UVLO)

Power for the P-channel MOSFET gate driver is derived from the V_{IN} and CAP pins. The CAP pin is regulated to 8V below V_{IN} by an internal low dropout linear regulator(LDO).A minimum capacitance of 0.47µF (low ESR ceramic) is required between V_{IN} and CAP to assure stability. The internal V_{IN}-CAP LDO can generate significant on-chip heat when using a P-channel MOSFET with large gate capacitance at high V_{IN} and high switching frequency. An external N-channel MOSFET bias path can be used to move the heat off chip and its connections are shown on page 10. When the external N-channel MOSFET is used, a minimum capacitance of 2.2µF (low ESR ceramic) is recommended between V_{IN} and CAP.

For $V_{IN} \leq 8V$, the LDO will be in dropout and the CAP voltage will be near ground (the V_{IN}-CAP differential voltage will nearly equal V_{IN}). If V_{IN}-CAP is less than V_{UVLO}, the LTC3894 enters a UVLO state where the external P-channel MOSFET is turned off and most internal circuitry is shut down. In order to exit UVLO, the V_{IN}-CAP voltage must exceed either 3.75V or 6V depending on the DRVUV /EXTG voltage setting. When an external N-channel MOSFET bias path is used, a UVLO threshold of 6V is selected by default.

Shutdown and Soft-Start

When the RUN pin is below 0.7V, the controller and most internal circuits are disabled. In this micropower shutdown state, the LTC3894 draws only 7µA. The RUN pin voltage must rise above 1.24V to enable the controller. The RUN pin can be tied to or pulled up to an external supply of up to 150V or it can be driven directly by a logic gate.

The start-up of the output voltage V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.8V internal reference, the V_{FB} pin is regulated to the voltage on the TRACK/SS pin. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to signal ground. An internal 10µA pull-up current charges this capacitor, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises from 0V to 0.8V, the output voltage V_{OUT} rises smoothly from zero to its final value.

Alternatively, the TRACK/SS pin can be used to cause the startup of V_{OUT} to track that of another supply. Typically, this requires connecting the TRACK/SS pin to an external resistor divider from the other supply to ground. (See Applications Information section.) During a shutdown, input overvoltage, and input undervoltage, or overtemperature event, the TRACK/SS pin is discharged to ground to ensure smooth restart.

If the slew rate of the TRACK/SS pin is greater than 0.6V/ms, the output will track an internal soft-start ramp instead of the TRACK/SS pin. The internal soft-start offers

OPERATION

a smooth start-up of the output in the case of a short-circuit recovery where the output voltage will recover from near ground.

Light Load Current Operation (Burst Mode Operation or Pulse-Skipping Mode)

At light loads, the LTC3894 operates in either pulse-skipping mode or high efficiency Burst mode. To select pulse-skipping operation, tie the PLLIN/MODE pin to ground. To select Burst Mode operation, float the PLLIN/MODE pin.

In Burst Mode operation, if the V_{FB} is higher than the reference voltage, the error amplifier will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high, enabling sleep mode.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current the LTC3894 draws to 30µA. When the $SENSE^-$ pin voltage is greater than 3.2V, the majority of this current (25µA) is drawn by $SENSE^-$ and only 6µA is drawn by the V_{IN} pin. For output voltages greater than 3.2V, this dramatically reduces the total quiescent current drawn from the input supply in sleep mode. When referred back to the input supply, the quiescent current is reduced by the DC/DC voltage conversion ratio and the incremental efficiency from V_{OUT} to V_{IN}.

Therefore, for the typical application on the first page with Burst Mode selected, the total input supply current at no load in regulation can be estimated using:

$$I_{Q(VINR)} = 6\mu A + \frac{V_{OUT}}{0.9 \bullet V_{IN}} = \left(\frac{0.8V}{R_{FB1}} + 22\mu A \right)$$

where R_{FB1} is the lower feedback divider resistor.

As the output voltage and hence the feedback voltage decreases, the error amplifier's output will rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the error amplifier, and the controller resumes normal operation by turning on the external P-channel MOSFET on the next cycle of the internal oscillator.

In Burst Mode operation, the peak inductor current has to reach at least 25% of current limit for the current comparator, ICMP, to trip and turn the P-MOSFET back off, even though the ITH voltage may indicate a lower current setpoint value.

When the PLLIN/MODE pin is connected to ground for pulse-skipping mode, the LTC3894 will skip pulses during light loads. In this mode, ICMP may remain tripped for several cycles and force the external P-channel MOSFET to stay off, thereby skipping pulses. This mode offers the benefits of smaller output ripple, lower audible noise, and reduced RF interference, at the expense of lower efficiency when compared to Burst Mode operation.

Frequency Selection and Clock Synchronization

The switching frequency of the LTC3894 can be selected using the FREQ pin. If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to signal ground, floated, or programmed through an external resistor. Tying the FREQ pin to signal ground selects 350kHz, while floating selects 535kHz. Placing a resistor between the FREQ pin and signal ground allows the frequency to be programmed between 50kHz and 850kHz.

The phase-locked loop (PLL) on the LTC3894 will synchronize the internal oscillator to an external clock source when connected to the PLLIN/MODE pin. The PLL forces the turn-on edge of the external P-channel MOSFET to be aligned with the rising edge of the synchronizing signal.

The oscillator's default frequency is based on the operating frequency set by the FREQ pin. If the oscillator's default frequency is near the external clock frequency, only slight adjustments are needed for the PLL to synchronize the external P-channel MOSFET's turn-on edge to the rising edge of the external clock. This allows the PLL to lock rapidly without deviating far from the desired frequency. The PLL is guaranteed from 75kHz to 750kHz. The clock input levels should be greater than 2V for logic high and less than 0.5V for logic low.

Power Good

The PGOOD pin connects to the open-drain output of an internal N-channel MOSFET. The MOSFET pulls the PGOOD pin low when either the V_{FB} pin voltage is overvoltage at 10% or more above or the PGUV pin is undervoltage

OPERATION

at 10% or more below the 0.8V internal voltage reference. The PGOOD pin is also pulled low during an overtemperature, RUN pin shutdown, V_{IN} overvoltage or V_{IN} undervoltage lockout event. When the V_{FB} pin voltage is less than 0.88V (0.8V + 10%) and PGUV is above 0.72V (0.8V – 10%), the internal N-channel MOSFET is turned off and the PGOOD pin is allowed to be pulled up by an external resistor to V_{OUT} or another source no greater than 60V. The PGOOD open-drain output has a 100µs delay before it can transition states.

When the V_{FB} voltage is higher than 0.88V (0.8V + 10%) nominal, this is considered an overvoltage condition and the external P-MOSFET is immediately turned off and remains turned off until V_{FB} falls below 0.88V with built-in hysteresis of 20mV.

Current Limit Foldback

In the event of an output short-circuit or overcurrent condition that causes the output voltage to fall to less than 72% of its nominal regulated level and the PGUV pin voltage is less than 0.72V, current limit foldback is activated, progressively lowering the peak current limit in proportion to the drop of V_{OUT} until reaching a minimum current limit of about 36% of full current limit. Current limit foldback reduces the power dissipation in the Schottky diode and assures robust operation during a continuous short-circuit fault. Current limit foldback is disabled during soft-start (as long as the V_{FB} voltage is keeping up with the TRACK/SS voltage). Note that the LTC3894 continuously monitors the inductor current and prevents current runaway under all conditions.

LTC3894 has an internal overtemperature protection circuit that shuts off the controller and the external P-channel MOSFET when internal die temperature exceeds 180°C. The circuit also discharges the TRACK/SS pin to GND to ensure a smooth restart.

Input Supply Overvoltage Lockout (OVLO Pin)

The LTC3894 implements a protection feature that inhibits switching when the input voltage rises above a programmable operating range. By using a resistor divider from the input supply to ground, the OVLO pin serves as a precise input supply voltage monitor. Switching is disabled when the OVLO pin rises above 0.8V, which can be configured to limit switching to a specific range of input supply voltage. An input supply overvoltage event triggers a TRACK/SS reset, which results in a graceful recovery from an input supply transient.

APPLICATIONS INFORMATION

The LTC3894 is a current mode, constant frequency nonsynchronous step-down DC/DC controller with a P-channel power MOSFET acting as the main switch and a Schottky power diode acting as the commutating (catch) diode. The input range extends from 4.5V to 150V. The output range can be programmed from 0.8V to 60V. The LTC3894 can transition from regulation to 100% duty cycle when the input voltage drops below the programmed output voltage. Additionally, the LTC3894 offers Burst Mode operation with a very low quiescent current, delivering outstanding efficiency in light load operation not typically found in a controller. The LTC3894 is a low pin-count, robust and easy to use solution in applications which require high efficiency and operate with widely varying high voltage inputs.

The typical application on the front page is a basic LTC3894 application circuit where the inductor current is sensed using a low value sense resistor, R_{SENSE}, placed between the power inductor and V_{OUT}. Once the required output voltage and operating frequency have been determined, external component selection is driven by load requirements, and begins with the selection of inductor and R_{SENSE}. Next, the power MOSFET and catch diode are selected. Finally, input and output capacitors are selected.

Output Voltage Programming

The output voltage is programmed by connecting a feedback resistor divider from the output to the V_{FB} pin as shown in Figure 1. The output voltage in steady state

APPLICATIONS INFORMATION

operation is set by the feedback resistors according to the equation:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_{FB2}}{R_{FB1}}\right)$$

To improve the transient response, a feedforward capacitor C_{FF} may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the GATE signal that drives the external P-MOSFET.

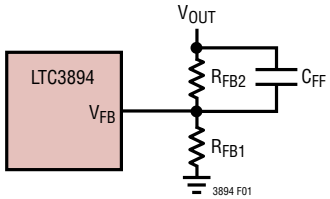


Figure 1. Setting the Output Voltage

Switching Frequency and Clock Synchronization

The choice of operating frequency is a trade-off between efficiency and component size. Lowering the operating frequency improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. Conversely, raising the operating frequency degrades efficiency but reduces component size.

The LTC3894 can free run at a user programmed switching frequency, or it can synchronize to an external clock. When a clock signal is applied to the PLLIN/MODE pin, the turn-on of the external P-channel MOSFET is coincidental with the rising edge of the applied clock. The switching frequency of the LTC3894 is programmed with the FREQ pin, and the external clock is applied at the PLLIN/MODE pin. Table 1 highlights the different states in which the FREQ pin can be used in conjunction with the PLLIN/MODE pin.

Table 1

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
Floating	DC Voltage	535kHz
Resistor to GND	DC Voltage	50kHz to 850kHz
Any of the Above	External Clock	Phase Locked to External Clock

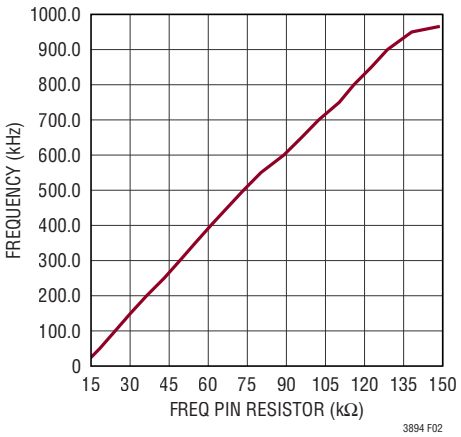


Figure 2. Switching Frequency vs Resistor on FREQ Pin

The free-running switching frequency can be programmed from 50kHz to 850kHz by connecting a resistor from FREQ pin to signal ground. The resulting switching frequency as a function of resistance on FREQ pin is shown in Figure 2.

Set the free-running frequency to the desired synchronization frequency using the FREQ pin so that the internal oscillator is prebiased to approximately the synchronization frequency. While it is not required that the free-running frequency be near the external clock frequency, doing so will minimize synchronization time.

Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge and transition losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L, decreases with higher inductance or higher frequency and increases with higher V_{IN}.

Given the desired input and output voltages, the inductor value and operation frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

APPLICATIONS INFORMATION

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and results in lower output ripple. The highest efficiency operation can be obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency, and operating frequency.

A reasonable starting point for ripple current is 40% of $I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current does not exceed a specified maximum, the inductance should be chosen according to:

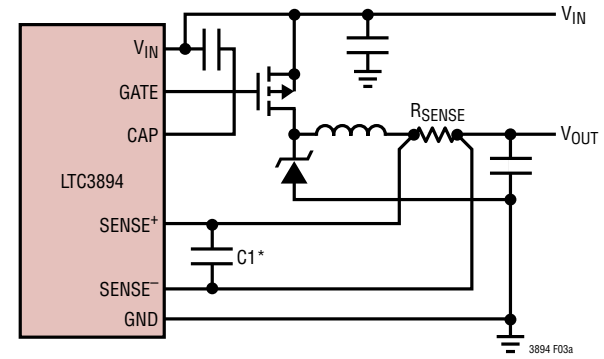
$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

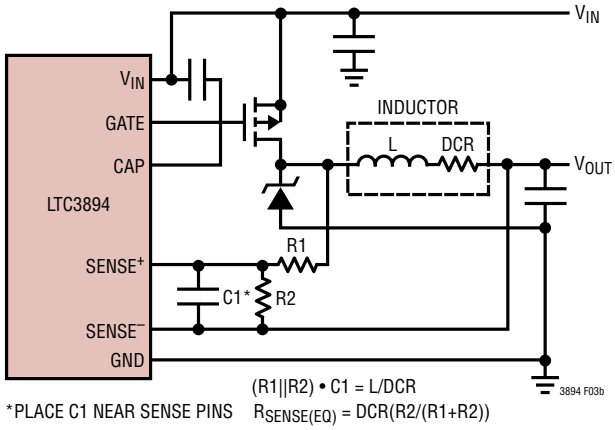
Inductor Core Selection

Once the inductance value has been determined, the type of inductor must be selected. Core loss is independent of core size for a given inductor value, but it is very dependent on the inductance selected. As inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!



(3a) Using a Resistor to Sense Current



(3b) Using the Inductor DCR to Sense Current

Figure 3. Current Sensing Methods

Inductor Current Sensing

LTC3894 can be configured to use either low value series resistor sensing (Figure 3a) or DCR (inductor resistance) sensing (Figure 3b). The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the differential current comparator. The common mode voltage range on these pins is 0V to 65V (absolute maximum), enabling the LTC3894 to regulate an output voltage up

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to a nominal 60V (allowing margin for tolerances and transients). The SENSE+ pin is high impedance. This high impedance allows the current comparators to be used in inductor DCR sensing.

The impedance of the SENSE– pin changes depending on the common mode voltage. When SENSE– is less than 2.9V, it is high impedance, drawing less than 1µA. When SENSE– is above 3.2V, pin current increases considerably and can be as high as 1.2mA.

Any voltage drop caused by the current along the SENSE– PCB board trace directly translates into errors in current sensing. The impedance of the SENSE– board layout trace need to be minimized to maintain high sensing accuracy.

Optional filter component C1, mutual to the sense lines, should be placed close to the LTC3894, and the sense lines should run close together to a 4-wire Kelvin connection underneath the current sense element (shown in Figure 4). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 3b), R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

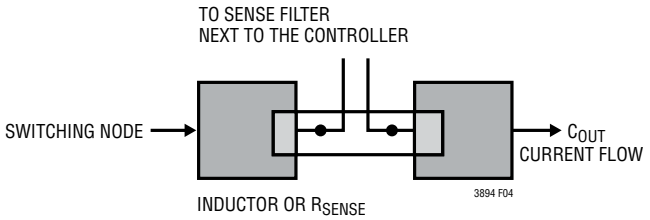

Figure 4. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 3a. R_{SENSE} is chosen based on the required output current. The voltage across the resistor, V_{SENSE}, is proportional to inductor current. The LTC3894 current comparator has a fixed maximum current sense threshold $V_{SENSE(MAX)}$ of 100mV (typical).

The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, $I_{OUT(MAX)}$, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{OUT(MAX)} + \frac{\Delta I_L}{2}}$$

Choose a sense resistor with low parasitic inductance to improve sensing accuracy.

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value (88mV) for the $V_{SENSE(MAX)}$ threshold in the Electrical Characteristics table and take into account inductance tolerance as listed in inductor manufacturer's data sheet (typically ±20%).

When using the controller in high duty cycle conditions, the maximum output current level will be reduced due to the internal compensation required to meet the stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current depending upon the operating duty factor. (See Maximum Current Sense Threshold vs Duty Cycle curve on page 7).

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3894 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 3b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter

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components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{OUT(MAX)} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value (88mV) for the $V_{SENSE(MAX)}$ threshold in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio R_D:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX}\ at\ T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current.

The equivalent resistance R1||R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR\ at\ 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\quad R2 = \frac{R1 \bullet R_D}{1-R_D} = \frac{R1||R2}{1-R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Power MOSFET Selection

The LTC3894 drives a P-channel power MOSFET that serves as the main switch for the asynchronous step-down converter. Important P-channel power MOSFET parameters include drain-to-source breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, gate charge Q_G, and the MOSFET's thermal resistance $\theta_{JC(MOSFET)}$ and $\theta_{JA(MOSFET)}$.

A partial list of P-channel MOSFET devices suitable for a 150V high current LTC3894 application includes FDMS86263P (Fairchild), SIR873DP (Vishay), IRF6218S (Infineon), FDMC86259P (Fairchild), and Si7439DP (Vishay).

The gate driver bias voltage V_{IN}-V_{CAP} is set by an internal LDO regulator. In normal operation, the CAP pin will be regulated to 8V below V_{IN}. A minimum 0.47µF capacitor is required between the V_{IN} and CAP pins to ensure LDO stability. If required, additional capacitance can be added to accommodate higher gate currents. The capacitance should be increased to a minimum of 2.2µF when the external N-channel MOSFET is used. In shutdown and Burst Mode operation, the CAP LDO is turned off. In the event of CAP leakage to ground, the CAP voltage is limited to 9V by a weak internal clamp from V_{IN} to CAP. As a result, a minimum 10V V_{GS} rated MOSFET is required.

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The power dissipated by the P-channel MOSFET when the LTC3894 is in continuous conduction mode is given by:

$$P_{MOSFET} \cong D \bullet I_{OUT}{}^2 \bullet \rho_\tau \bullet R_{DS(ON)} + V_{IN}{}^2 \bullet \left(\frac{I_{OUT}}{2}\right) \bullet (C_{MILLER}) \bullet \left[\frac{R_{DN}}{(V_{IN} - V_{CAP}) - V_{MILLER}} + \frac{R_{UP}}{V_{MILLER}}\right] \bullet f$$

where D is duty factor, $R_{DS(ON)}$ is on-resistance of P-MOSFET, ρ_τ is temperature coefficient of on-resistance, R_{DN} is the pull-down driver resistance specified at 0.9Ω typical and R_{UP} is the pull-up driver resistance specified at 2Ω typical. V_{MILLER} is the Miller effective V_{GS} voltage and is taken graphically from the power MOSFET data sheet.

The power MOSFET input capacitance C_{MILLER} is the most important selection criteria for determining the transition loss term in the P-channel MOSFET but is not directly specified on MOSFET data sheets. C_{MILLER} is a combination of several components, but it can be derived from the typical gate charge curve included on most data sheets (Figure 5). The curve is generated by forcing a constant current out of the gate of a common-source connected P-MOSFET that is loaded with a resistor, and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and gate-to-drain capacitances. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain voltage rises across the resistor load. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{SD} test voltage, but can be adjusted for different V_{SD} voltages by multiplying by the ratio of the adjusted V_{SD} to the curve specified V_{SD} value. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b (or the parameter Q_{GD} on a manufacturer's data sheet) and dividing it by the specified V_{SD} test voltage, $V_{SD(TEST)}$.

$$C_{MILLER} \cong \frac{Q_{GD}}{V_{SD(TEST)}}$$

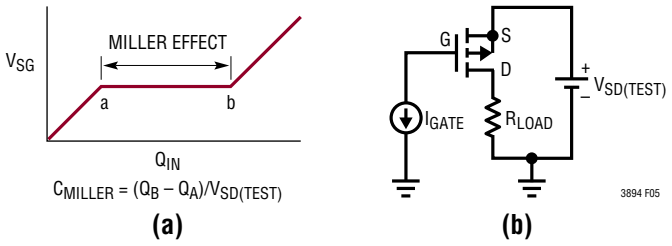

Figure 5. (a) Typical P-MOSFET Gate Charge Characteristics and (b) Test Set-Up to Generate Gate Charge Curve

The term with C_{MILLER} accounts for transition loss, which is highest at high input voltages. For V_{IN} < 20V, the high-current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. When an application is intended for use at low V_{IN}, care must be taken to select a P-channel MOSFET with threshold voltage $V_{GS(TH)}$ low enough to operate at low V_{IN}.

Schottky Diode Selection

When the P-MOSFET is turned off, a power Schottky diode is required to function as a commutating diode to carry the inductor current. The average diode current is therefore dependent on the P-MOSFET's duty factor. The worst case condition for diode conduction is a short-circuit condition where the Schottky must handle the maximum current as its duty factor approaches 100% (and the P-channel MOSFET's duty factor approaches 0%). The diode therefore must be chosen carefully to meet worst case voltage and current requirements. The equation below describes the continuous or average forward diode current rating required, where D is the regulator duty factor.

$$I_{F(AVG)} \cong I_{OUT(MAX)} \bullet (1 - D)$$

Once the average forward diode current is calculated, the power dissipation can be determined. Refer to the Schottky diode data sheet for the power dissipation P_{DIODE} as a function of average forward current $I_{F(AVG)}$. P_{DIODE} can also be iteratively determined by the two equations below, where $V_{F(IOUT,TJ)}$ is a function of both $I_{F(AVG)}$ and junction temperature T_J. Note that the thermal

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resistance $\theta_{JA(DIODE)}$ given in the data sheet is typical and can be highly layout dependent. It is therefore important to make sure that the Schottky diode has adequate heat sinking.

$$T_J \cong P_{DIODE} \bullet \theta_{JA(DIODE)} + T_A$$

$$P_{DIODE} \cong I_{F(AVG)} \bullet V_{F(IOUT,TJ)}$$

The Schottky diode forward voltage is a function of both I_{OUT} and T_J, so several iterations may be required to satisfy both equations. The Schottky forward voltage V_F should be taken from the Schottky diode data sheet curve showing Instantaneous Forward Voltage. The forward voltage will decrease as a function of T_J and increase as a function of I_F. The nominal forward voltage will also tend to increase as the reverse breakdown voltage increases. It is therefore advantageous to select a Schottky diode appropriate to the input voltage requirements.

C_{IN} and C_{OUT} Selection

The input capacitance C_{IN} is required to filter the square wave current through the P-channel MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

$$I_{CIN(RMS)} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{CIN(RMS)} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to derate the capacitor.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, specialty polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Specialty polymer capacitors offer very low ESR but have lower specific capacitance than other types. Tantalum capacitors have the highest specific capacitance, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects.

The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switch and controller. To dampen input voltage transients, add a small 5µF to 40µF aluminum electrolytic capacitor with an ESR in the range of 0.5Ω to 2Ω. High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of lead inductance.

Discontinuous and Continuous Operation

The LTC3894 operates in discontinuous conduction (DCM) until the load current is high enough for the inductor current to be positive at the end of the switching cycle. The output load current at the continuous/discontinuous boundary $I_{OUT(CDB)}$ is given by the following equation:

$$I_{OUT(CDB)} \cong \frac{(V_{IN} - V_{OUT})(V_{OUT} + V_F)}{2 \bullet L \bullet f \bullet (V_{IN} + V_F)}$$

The continuous/discontinuous boundary is inversely proportional to the inductor value. Therefore, if required, $I_{OUT(CDB)}$ can be reduced by increasing the inductor value.

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RUN Pin and V_{IN} Overvoltage/Undervoltage Lockout

The LTC3894 is enabled using the RUN pin. It has a rising threshold of 1.24V with 100mV of hysteresis. Pulling the RUN pin below 1.12V shuts down the main control loop. Pulling it below 0.8V disables the controller and most internal circuits. In this state the LTC3894 draws only 7µA of quiescent current.

The RUN pin is high impedance and must be externally pulled up/down or driven directly by logic. The RUN pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down.

The RUN and OVLO pins can alternatively be configured as adjustable undervoltage (UVLO) and overvoltage (OVLO) lockouts on the V_{IN} supply with a resistor divider from V_{IN} to ground. A simple resistor divider can be used as shown in Figure 6 to meet specific V_{IN} voltage requirements.

The current that flows through the R3-R4-R5 divider will directly add to the shutdown, sleep, and active current of the LTC3894, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the megaohm range may be required to keep the impact on quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R3 + R4 + R5 (R_{TOTAL}) should be chosen first based on the allowable DC current that can be drawn from V_{IN}.

The individual values of R3, R4 and R5 can be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \frac{0.8V}{\text{RISING } V_{IN} \text{ OVLO THRESHOLD}}$$

$$R4 = R_{TOTAL} \bullet \frac{1.24V}{\text{RISING } V_{IN} \text{ UVLO THRESHOLD}} - R5$$

$$R3 = R_{TOTAL} - R5 - R4$$

For applications that do not require an OVLO, the OVLO pin can be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the previous equations with R5 = 0Ω.

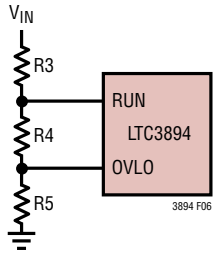

Figure 6. Adjustable UV and OV Lockout

Similarly, for applications that do not require an adjustable UVLO, the RUN pin can be tied to V_{IN}. In this configuration, the UVLO threshold is limited to the internal V_{IN}-CAP UVLO thresholds (V_{UVLO}) as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the previous equations with R3 = 0Ω.

PGOOD Programming in Dropout Applications (PGUV Pin)

The PGUV or Power Good Undervoltage pin is included to give greater flexibility in defining a normal range of operating V_{OUT} for the LTC3894. In a conventional DC/DC controller, the OV and UV comparators monitor the V_{FB} pin and define a fixed ± power good window about a regulation point for V_{OUT}. In the LTC3894, the OV comparator monitors the V_{FB} pin and the UV comparator monitors the PGUV pin. For a typical application that does not operate in dropout, the PGUV pin can be tied to the V_{FB} pin to establish a conventional ±10% PGOOD window around the regulation point, outside of which V_{OUT} enters UV and OV condition respectively. Because the LTC3894 is a 100% duty cycle controller, it can be used in applications where dropout or operating V_{OUT} below regulation is part of normal operation. For those applications, the PGUV pin can be used to establish a lower limit for PGOOD independent of the V_{FB} pin.

A good example of defining power good in both regulation and dropout is a 12V battery output preregulator with a wide ranging V_{IN} and V_{OUT} regulation point set at 12V. If the defined operating output range is 12V to 9V a conventional power good cannot be used because 9V is under the V_{FB} UV threshold (12V – 10% or 10.8V). In this example, the PGOOD window is defined between 10% above 12V

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and 10% below 9V. The Output Voltage OV (V_{OUTOV}) is 13.2V and Output Voltage UV (V_{OUTUV}) is 8.1V.

To set PGUV to trigger at 9V minus 10% or 8.1V use a resistor divider as seen in Figure 7. The resistors R_{UV1} and R_{UV2} set the divided output to the PGUV pin. V_{OUTUV} is defined as the voltage where the divided output on the

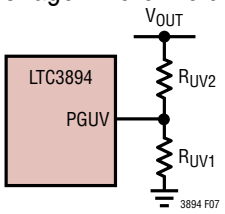

Figure 7. Programmable Power Good UV

PGUV pin is 0.72V (0.8V – 10%). The resistor divider may be calculated as follows:

$R_{UV(1,2)}$ is chosen based on I_Q current requirements.

$$R_{UV(1,2)} = R_{UV1} + R_{UV2} = \text{Assume } 500k$$

$$R_{UV1} = R_{UV(1,2)} \bullet \frac{0.72V}{V_{OUTUV}}$$

$$R_{UV1} = 500k \bullet \frac{0.72V}{8.1} = 44k$$

$$R_{UV2} = R_{UV(1,2)} - R_{UV1} = 500k - 44k = 456k, \text{ use } 453k$$

To reduce I_Q and component counts, the above resistor divider can be combined with the feedback resistors as shown here and in Figure 13.

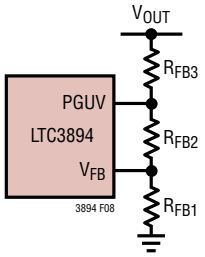

Figure 8.

With the following design specifications:

$V_{OUT(REGULATION)}$ = 60V, V_{OUTUV} = 42V and choose R_{FB3} = 1MΩ,

R_{FB1} and R_{FB2} can be calculated as follows:

$$R_{FB1} = \frac{0.8V \bullet V_{OUTUV} \bullet R_{FB3}}{V_{OUT(REGULATION)} \bullet (V_{OUTUV} - 0.72V)} = 13.6k$$

Select R_{FB1} to be the 1% standard value of 13.7k.

$$R_{FB2} = \frac{0.72V \bullet R_{FB3}}{V_{OUTUV} - 0.72V} - R_{FB1} = 3.8k, \text{ use } 3.74k$$

The final selection of R_{FB3} = 1MΩ, R_{FB2} = 13.7k and R_{FB1} = 3.74k results in $V_{OUT(REGULATION)}$ = 59.4V and V_{OUTUV} = 42V.

External N-Channel MOSFET Bias Path for the Gate Driver (DRVUV/EXTG Pin and EXTS Pin)

The LTC3894 has an internal LDO to regulate the gate driver bias voltage (V_{IN}-CAP) to a nominal 8V and provide the gate drive current. The amount of the gate current depends on the external P-channel MOSFET gate capacitance and switching frequency. Charging and discharging the gate of the external P-channel MOSFET will result in an effective gate drive current and power loss inside the chip.

For applications where a large gate drive current and high V_{IN} generate excessively high internal power dissipation, the LTC3894 offers an option to bypass the internal LDO with an external N-channel MOSFET. This option will move the power dissipation off chip and lower the internal chip temperature. To effectively keep the chip and board temperature low, sufficient heat sink is required for the N-channel MOSFET. The connections for the N-channel MOSFET are shown in the Functional Diagram on page 10. Connecting the N-channel MOSFET automatically select the UVLO threshold of 6V. External buffer resistor R_{EXTG} (1k) and ceramic bypass capacitors C_{EXTS} and C_{EXTG} (0.1µF each, 20V rated) are required and need to be placed as close as practical to the N-channel MOSFET source terminal and EXTG pin respectively to ensure stable operation.

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External N-Channel MOSFET Selection

When selecting an external NMOS device for the external gate driver charge path, threshold $V_{GS(TH)}$,maximum V_{DS} rating, and maximum power rating need to be considered for the maximum V_{IN} used in an application . A NMOS with $V_{GS(TH)}$ less than 5V should be used. During operation, the maximum continuous voltage drop across the external N-channel MOSFET V_{DS} can be calculated as:

$$V_{DS(EXT.NMOS)} = V_{IN} – 8V$$

The average current flowing through the NMOS can be calculated as:

$$I_{AVG_NMOS} = Q_{G(ext.\ PFET)} \bullet f$$

where $Q_{G(ext.\ PFET)}$ is the total Gate charge needed to turn on the external PFET in a switching cycle, f is the switching frequency.

Total power dissipation in the N-channel MOSFET is:

$$P_{NMOS} = V_{DS(EXT.NMOS)} \bullet I_{AVG_NMOS} = (V_{IN} – 8V) \bullet Q_{G(ext.\ PFET)} \bullet f$$

As it can be seen, the maximum power dissipation occurs at maximum V_{IN} of 150V.

For example , in an application where V_{IN} = 150V, $Q_{G(ext.\ PFET)}$ = 30nC, f = 350kHz, P_{NMOS} = 142V • 30nC • 350kHz = 142V • 10.5mA = 1.49W

Sufficient heat sink is needed to remove the heat generated.

External Soft-Start and Output Tracking

Start-up characteristics are controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal 0.8V reference, the LTC3894 regulates the V_{FB} pin voltage to the voltage on the TRACK/SS pin. When the TRACK/SS pin is greater than the internal 0.8V reference, the V_{FB} pin voltage regulates to the 0.8V internal reference. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by connecting a capacitor from the TRACK/SS pin to ground. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin that causes V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{10\mu A}$$

When the LTC3894 is configured to track another supply, a voltage divider can be used from the tracking supply to the TRACK/SS pin to scale the ramp rate appropriately. Two common implementations of tracking as shown in Figure 9a are coincident and ratiometric. For coincident tracking, make the divider ratio from the external supply the same as the divider ratio for the feedback voltage. Ratiometric tracking could be achieved by using a different ratio than the feedback (Figure 9b).

Note that the constant TRACK/SS pin current produces a small offset error to the resistive divider tracking. Account for the error or minimize it by selecting small tracking resistor values.

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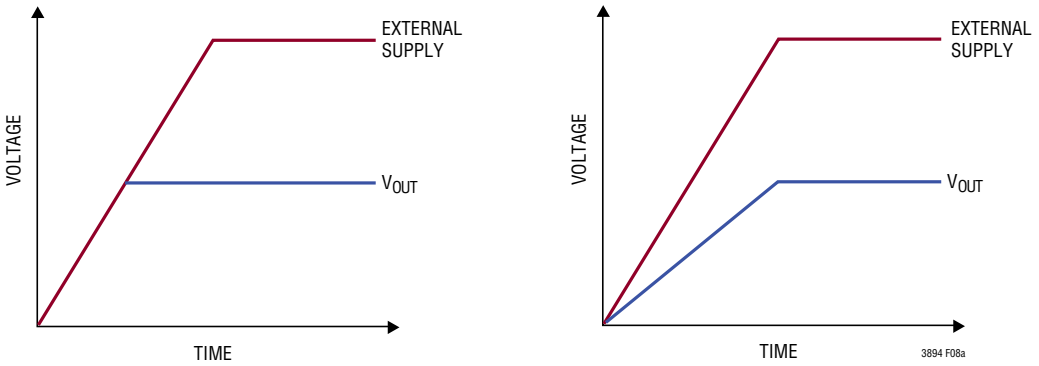

Figure 9(a). Two Different Modes of Output Tracking

Figure 9(b): Setup for Ratiometric and Coincident Tracking

Short-Circuit Faults: Current Limit and Foldback

In the LTC3894, the maximum inductor current is inherently limited by the current mode controller by the maximum current sense threshold voltage $V_{SENSE(MAX)}$.

LTC3894 also includes current foldback to help limit load current when the output is shorted to ground. When the output feedback V_{FB} voltage is less than 72% of the 0.8V internal reference (560mV), and PGUV is less than 0.72V, current limiting foldback is activated. The current limit will continue to drop as V_{FB} drops until reaching a minimum foldback current of about 36% of the the full operational current limit.

Under short-circuit conditions with very low duty cycles, cycle skipping will begin in order to limit the short-circuit current, thus preventing current limit runaway. In this situation, the power Schottky diode will be dissipating most of the power that is considerably reduced by the current limit foldback. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \left(\frac{V_{IN}}{L} \right)$$

The resulting average short-circuit current is:

$$I_{SC} = 45\% \bullet I_{LIM(MAX)} - \frac{1}{2} \Delta I_{L(SC)}$$

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Short-Circuit Recovery and Internal Soft-Start

An internal soft-start feature guarantees a maximum positive output voltage slew rate in all operational cases. In a short-circuit recovery condition for example, the output recovery rate is limited by the internal soft-start so that output voltage overshoot and excessive inductor current buildup is prevented.

The internal soft-start voltage and the external TRACK/SS pin operate independently. The output will track the lower of the two voltages. The slew rate of the internal soft-start voltage is roughly 0.6V/ms, which translates to a total soft-start time of 1.3ms. If the slew rate of the TRACK/SS pin is greater than 0.6V/ms the output will track the internal soft-start ramp. To assure robust fault recovery, the internal soft-start feature is active in all operational cases.

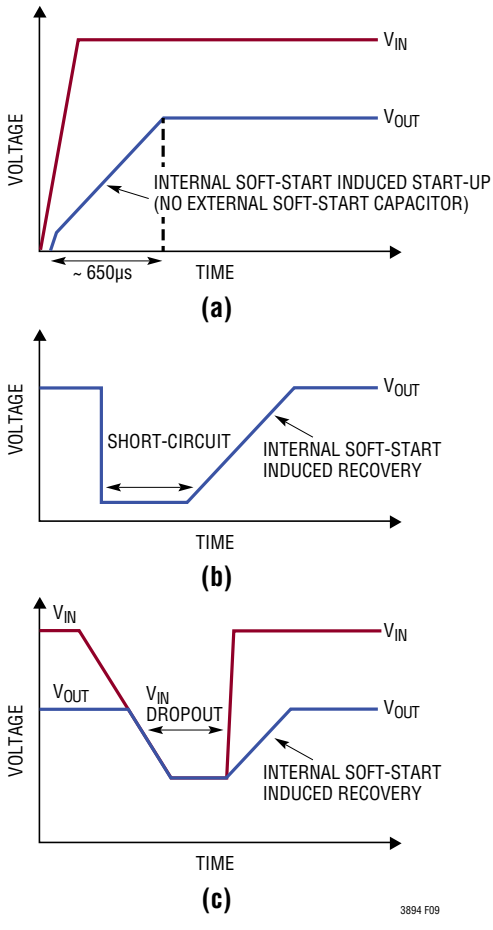

Figure 10. Internal Soft-Start (a) Allows Soft Start-Up without an External Soft-Start Capacitor and Allows Soft Recovery from (b) a Short-Circuit or (c) a V_{IN} Dropout

If a short-circuit condition occurs which causes the output to drop significantly, the internal soft-start will assure a soft recovery when the fault condition is removed.

The internal soft-start assures a clean soft ramp-up from any fault condition that causes the output to droop, guaranteeing a maximum ramp rate in soft-start, short-circuit fault release, or output recovery from drop out. Figure 10 illustrates how internal soft-start controls the output ramp-up rate under varying scenarios.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on chip, the overtemperature shutdown circuitry will shut down the LTC3894. When the junction temperature exceeds approximately 180°C, the overtemperature circuitry shuts down most of the LTC3894 chip including the external P-channel MOSFET and discharges TRACK/SS to ground. Once the junction temperature drops back to the approximately 165°C, the chip turns back on and restarts with a soft-start ramp. Long term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

UVLO Selection (DRVUV/EXTG Pin)

The DRVUV/EXTG pin can be used to select one of the two Undervoltage Lockout thresholds (UVLO) for the Gate drive bias voltage(VIN-CAP). When the pin is grounded, the gate drive UVLO threshold is set to 3.75V. When DRVUV/EXTG is floated, the UVLO is set to 6V.

Table 2 summarizes the values of UVLO threshold selected for different EXTG and EXTS pin configurations. Note that when the external N-channel MOSFET is used, the 6V UVLO is selected by default.

Table 2

TYPICAL UVLO RISING THRESHOLD	EXT NMOS	DRVUV/EXTG	EXTS
3.75V	No	GND	GND
6V	No	FLOAT	GND
6V	Yes*	Connected to External N-Channel MOSFET GATE	Connected to External N-Channel MOSFET SOURCE

*(Connect the external N-channel MOSFET drain to the CAP pin.)

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V_{IN} Undervoltage Lockout (UVLO)

With the user selectable UVLO threshold, The LTC3894 is designed to accommodate applications requiring widely varying input voltages from 4.5V to 150V.

There is a built-in hysteresis between UVLO rising and UVLO falling thresholds and its implication must be carefully considered in low V_{IN} operation. When DRVUV/EXTG pin is grounded, the nominal UVLO threshold with V_{IN} rising is 3.75V and the nominal UVLO falling is 3.5V. For the low UVLO threshold selection, the operating input voltage range of the LTC3894 is guaranteed to be 3.75V to 150V over temperature, but the initial V_{IN} ramp must exceed 3.75V to guarantee a start-up. When the DRVUV/EXTG pin is greater than 300mV, the nominal UVLO threshold rising is 6V and nominal UVLO falling is 5.55V. For this high UVLO threshold selection, the operating input voltage range of the LTC3894 is guaranteed to be 5.55V to 150V over temperature, but the initial V_{IN} ramp must exceed 6V to guarantee a start-up.

An automotive battery droops during a cold crank condition. The typical automotive battery voltage is 12V to 14.4V, which has more than enough headroom for the LTC3894 to start up. Onboard electronics which are powered by a DC/DC regulator require a minimum supply voltage for seamless operation during the cold crank condition, and the battery may droop close to these minimum supply requirements during a cold crank. The DC/DC regulator should not exacerbate the situation by having excessive voltage drop between the already suppressed battery voltage input and the output of the regulator which powers these electronics. As seen in Figure 11, the LTC3894's 100% duty cycle capability allows low dropout from the battery to the output. The drop from V_{IN} to V_{OUT} is determined by the output Load current multiplied by the total series resistance in dropout mode. The guaranteed UVLO falling thresholds of 3.5V and 5.55V assure sufficient margin for continuous, uninterrupted operation in extreme cold crank battery drooping conditions. However, additional input capacitance or slower soft-start time may be required at low V_{IN} in order to limit V_{IN} droop caused by inrush currents, especially if the input source has a sufficiently large output impedance.

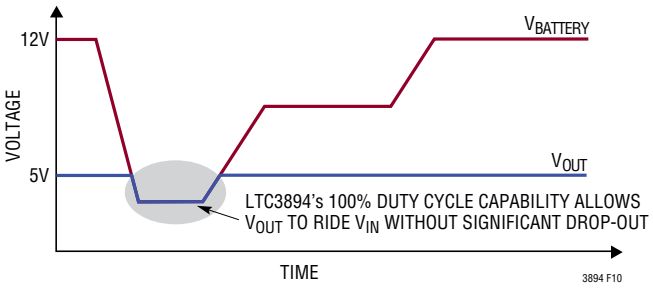

Figure 11. Typical Automotive Cold Crank

Minimum On-Time Considerations

The minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3894 is capable of turning on an external P-channel MOSFET, and is typically 125ns. It is determined by internal timing delays and the gate charge required to turn on the MOSFET. Low-duty-cycle applications may approach this minimum on-time limit, so care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN(MAX)} \bullet f}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will skip cycles. However, the output voltage will continue to regulate, but the voltage and current ripple will increase.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine the dominant contributors and therefore where efficiency improvements can be made. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, L3, etc., are the individual losses as a percentage of input power.

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Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3894 application circuits.

1. I^2R Loss: I^2R losses result from the P-channel MOSFET resistance, inductor resistance, the current sense resistor, and input and output capacitor ESR. In continuous mode operation the average output current flows through L but is chopped between the P-channel MOSFET and the bottom side Schottky diode. The following equation may be used to determine the total I^2R loss:

$$P_{L^2R} \approx \left(\frac{I^2_{OUT} + \Delta I^2_L}{12}\right) \bullet \left[\begin{matrix} R_{DCR} + R_{SENSE} + D \bullet \\ \left(R_{DS(ON)} + R_{ESR(CIN)}\right) \end{matrix}\right] + \frac{\Delta I^2_L}{12} \bullet R_{ESR(COUT)}$$

2. Transition Loss: Transition loss of the P-channel MOSFET becomes significant only when operating at high input voltages (typically 20V or greater.) The P-channel transition losses ($P_{PMOSTRL}$) can be determined from the following equation:

$$P_{PMOSTRL} = V_{IN}{}^2 \bullet \left(\frac{I_{OUT}}{2}\right) \bullet (C_{MILLER}) \bullet \left[\frac{R_{DN}}{(V_{IN} - V_{CAP}) - V_{MILLER}} + \frac{R_{UP}}{V_{MILLER}}\right] \bullet f$$

3. Gate Charging Loss: Charging and discharging the gate of the MOSFET will result in an effective gate charging current. Each time the P-channel MOSFET gate is switched from low to high and low again, a packet of charge dQ moves from the capacitor across V_{IN}-V_{CAP} and is then replenished from V_{IN} by the internal V_{CAP} regulator. The resulting dQ/dt current is a current out of V_{IN} flowing to ground. The total power loss in the controller including gate charging loss is determined by the following equation:

$$P_{CNTRL} = V_{IN} \bullet (I_Q + f \bullet Q_{G(PMOSFET)})$$

4. Schottky Loss: The Schottky diode loss is most significant at low duty factors (high step down ratios). The critical component is the Schottky forward voltage as a function of junction temperature and current. The Schottky power loss is given by the following equation.

$$P_{DIODE} \cong (1-D) \bullet I_{OUT} \bullet V_{F(IOUT, TJ)}$$

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If changes cause the input current to decrease, then the efficiency has increased. If there is no change in input current, there is no change in efficiency.

OPTI-LOOP® Compensation

OPTI-LOOP compensation, through the availability of the ITH pin, allows the transient response to be optimized for a wide range of loads and output capacitors. The ITH pin not only allows optimization of the control loop behavior but also provides a test point for the step-down regulator's DC-coupled and AC-filtered closed-loop response. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at this pin.

The ITH series R_{ITH}-C_{ITH1} filter sets the dominant pole-zero loop compensation. Additionally, a small capacitor placed from the ITH pin to signal ground, C_{ITH2}, may be required to attenuate high frequency noise. The values can be modified to optimize transient response once the final PCB layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The general goal of OPTI-LOOP compensation is to realize a fast but stable ITH response with minimal output

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droop due to the load step. For a detailed explanation of OPTI-LOOP compensation, refer to Application Note 76.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Connecting a resistive load in series with a power MOSFET, then placing the two directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load-step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated feedback loop response.

The gain of the loop increases with R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH1}. If R_{ITH} is increased by the same factor that C_{ITH1} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feedforward capacitor, C_{FF}, can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R_{FB2} which improves the phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate overall performance of the step-down regulator.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) input capacitors. If the switch connecting the load has low resistance and is driven quickly, then the discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem. The solution is to limit the turn-on speed of the load switch driver. A hot swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft starting.

Design Example

Consider a step-down regulator with the following specifications (Figure 12):

V_{IN} = 6V to 150V, V_{OUT} = 5V, $I_{OUT(MAX)}$ = 3A, and f = 200kHz

The output voltage is programmed according to:

$$R_{FB2} = R_{FB1} \bullet \left(\frac{V_{OUT}}{0.8V} \bullet -1 \right)$$

Select a 1% standard value resistor R_{FB1} = 80.6k, then calculate and choose R_{FB2} = 422k.

A 36.5kΩ between the FREQ pin and signal ground programs the switching frequency to 200kHz. The smallest on-time Ton occurs at 150V V_{IN} and can be calculated as:

$$T_{ON} = \frac{5V}{200kHz \bullet 150V} \approx 182ns$$

This on-time T_{ON} is larger than LTC3894's minimum on-time of 125ns with sufficient margin to prevent cycle skipping.

Next, set the inductor value to give 37% worst case ripple at maximum V_{IN} = 150V:

$$L = \frac{5V}{0.37 \bullet 3A \bullet 200kHz} \left(1 - \frac{5V}{150V} \right) \approx 21.7\mu H$$

Select a standard inductor of 22µH.

The resulting maximum inductor ripple current is:

$$\Delta I_L = \frac{5V}{22\mu H \bullet 200kHz} \left(1 - \frac{5V}{150V} \right) \approx 1.1A$$

Next, set the R_{SENSE} resistor value to ensure that the converter can deliver the maximum load current of 3A with sufficient margin to account for component variations and worst-case operating conditions. Using a 20% margin

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factor and the minimum value for the maximum current sense threshold (88mV), R_{SENSE} can be calculated to be:

$$R_{SENSE} = \frac{88mV}{1.2 \bullet \left(3A + \frac{1.1A}{2}\right)} = 20.6m\Omega$$

Select R_{SENSE} to be the standard value of 20mΩ with sufficient power rating.

The maximum value of the peak inductor current limit can be calculated using the maximum value for the maximum current sense threshold (112mV):

$$I_{L(PEAK)} = \frac{112mV}{20m\Omega} = 5.6A$$

Choose an inductor that has rated saturation current higher than 5.6A with sufficient margin.

The nominal output current limit can be calculated as:

$$I_{LIMIT} = \frac{100mV}{20m\Omega} - \frac{1.1A}{2} = 4.45A$$

Next choose a P-channel MOSFET with the appropriate BV_{DSS} and I_D rating. In this example, a good choice is the FAIRCHILD FDMS86263P (BV_{DSS} = 150V, I_D = –4.4A, $R_{DS(ON)}$ = 45mΩ, θ_{JA} = 50°C/W, ρ_T = 1.4 at 75°C). The power dissipation on the P-MOSFET can be estimated for V_{IN} of 150V with T (estimated) = 75°C as follows:

$$\begin{aligned} P_{PMOS} &= \frac{5V}{150V} \bullet (3A)^2 \bullet 1.4 \bullet 4.5m\Omega + (150V)^2 \bullet \frac{3A}{2} \\ &\quad \bullet \left(\frac{0.9\Omega}{8V - 3.9V} + \frac{2\Omega}{3.9V}\right) \bullet 90pF \bullet 200kHz \\ &\approx 18.9mW + 445mW \\ &= 464mW \end{aligned}$$

Next choose an appropriate Schottky diode that will handle the power requirements. The Diodes Inc. PDS4150 Schottky diode is selected ($V_{F(4A,125°C)}$ = 0.57V, V_R = 150V, θ_{JA} = 90°C/W) for this application. The power dissipation at full load = 3A can be calculated as:

$$P_{DIODE} = 3A \bullet \left(1 - \frac{5V}{150V}\right) \bullet 0.57V = 1.65W$$

These power dissipation calculations show that careful attention to heat sinking will be necessary.

An output short-circuit to ground will result in an output current limit foldback of:

$$I_{SC} = \frac{36mV}{20mV} - \frac{1}{2}\left(\frac{125ns - 150V}{22\mu H}\right) = 1.37A$$

The resulting power dissipated in the Schottky diode is:

$$P_{DIODE} \approx 1.37A \bullet 0.57V = 0.78W$$

The power dissipated in Schottky diode in short circuit foldback is less than when under full-load conditions. Choose low ESR ceramic capacitors as the input bypass capacitors that can handle the maximum RMS current of 1.5A over temperature. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR} \bullet \Delta I_L = 0.02\Omega \bullet 1.1A = 22mV_{P-P}$$

A soft-start time of 8ms can be programmed through a 0.1µF capacitor on the SS pin:

$$C_{SS} = \frac{8ms \bullet 10\mu A}{0.8V} = 0.1\mu F$$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3894.

1. Multilayer boards with dedicated ground layers are preferable for reduced noise and for heat sinking purposes. Use wide rails and/or entire planes for V_{IN}, V_{OUT} and GND for good filtering and minimal copper loss. If a ground layer is used, then it should be immediately below (and/or above) the routing layer for the power train components which consist of C_{IN}, sense resistor, P-MOSFET, Schottky diode, inductor, and C_{OUT}. Flood unused areas of all layers with copper for better heat sinking.

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2. Keep signal and power grounds separate except at the point where they are shorted together. Short signal and power ground together only at a single point with a narrow PCB trace (or single via in a multilayer board). All power train components should be referenced to power ground and all small signal components (e.g., C_{ITH1}, R_{FB1}, R_{FB2}, R_{FREQ}, C_{SS} etc.) should be referenced to signal ground.

3. Place C_{IN}, C_{CAP}, the Schottky diode, the P-channel MOSFET, inductor, and primary C_{OUT} capacitors close together in one compact area. The junction connecting the drain of P-MOSFET, cathode of Schottky, and (+) terminal of inductor (this junction is commonly referred to as the switch or phase node) should be compact but large enough to handle the inductor currents without large copper losses. Place the source of P-channel MOSFET as close as possible to the (+) plate of C_{IN} capacitor(s) that provides the bulk of the AC current (these are normally the ceramic capacitors), and connect the anode of the Schottky diode as close as possible to the (–) terminal of the same C_{IN} capacitor(s). The high dI/dt loop formed by C_{IN}, the MOSFET, and the Schottky diode should have short leads and PCB trace lengths to minimize high frequency EMI and voltage stress from inductive ringing. The (–) terminal of the primary C_{OUT} capacitor(s) which filters the bulk of the inductor ripple current (these are normally the ceramic capacitors) should also be connected close to the (–) terminal of C_{IN}.

4. Keep high dV/dt signals on the GATE and the switch nodes away from sensitive small signal traces and components. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC3894 and occupy minimum PC trace area.

5. The $SENSE^-$ and $SENSE^+$ leads should be routed together as a differential pair with minimum PC trace spacing. The optional filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor. DCR sensing resistor R1 should be placed close to the switch node. Current through the $SENSE^-$ trace can be 1mA or higher and IR drop along the trace can adversely affect current sensing accuracy. Care must be taken to reduce $SENSE^-$ board trace impedance.

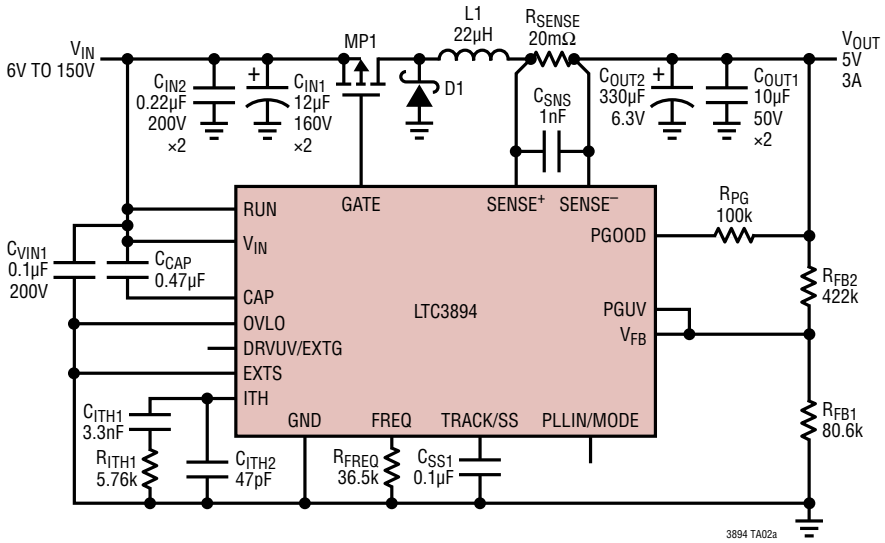
6. Place the resistive feedback divider $R_{FB1/2}$ as close as possible to the V_{FB} pin and connect it between the (+) terminal of C_{OUT} or the output regulation point and signal ground. The divider shall not share a common path with $SENSE^-$ connection and should be away from any noisy power train path and components.

7. Place the ceramic C_{CAP} capacitor as close as possible to V_{IN} and CAP pins. This capacitor provides the gate charging current for the power P-channel MOSFET.

8. Place small signal components as close to their respective pins as possible. This minimizes the possibility of PCB noise coupling into these pins. Give priority to V_{FB}, ITH, and FREQ pins. Use sufficient isolation when routing a clock signal into PLLIN /MODE pin so that the clock does not couple into sensitive small signal pins.

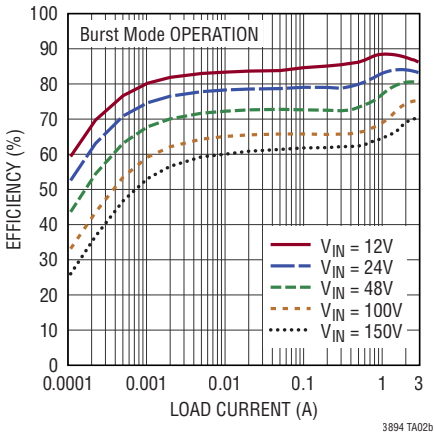
9. Minimize the length of board connection between the Gate pin and gate terminal of the external P-channel MOSFET and the connection between the CAP pin and the drain terminal of the external N-channel MOSFET when it is used.

TYPICAL APPLICATIONS



C_{VIN1}: 0.1µF 200V MURATA GRM31CR72D104KW03L
C_{CAP}: 0.47µF 16V MURATA GCM188R71C474KA55L
C_{IN1}:12µF 160V ILLINOIS CAPACTOR 126AVG160MGBJ
C_{IN2}: 0.22µF 200V MURATA GRM32DR72D224KW01
R_{SENSE} : 20mΩ SUSUMU KRL3216E-M-R020-F-T1
L1: 22µH WURTH ELEKTRONIK 7447709220 OR 7447704220
MP1: FAIRCHILD FDMS86263P
D1: DIODES PDS4150
C_{OUT2}: 330µF 6.3V AVS TPSD337M006R0050
C_{OUT1}: 10µF 50V MURATA GRM31CR61H106MA12L

Efficiency vs Load Current



Power Loss vs Load Current

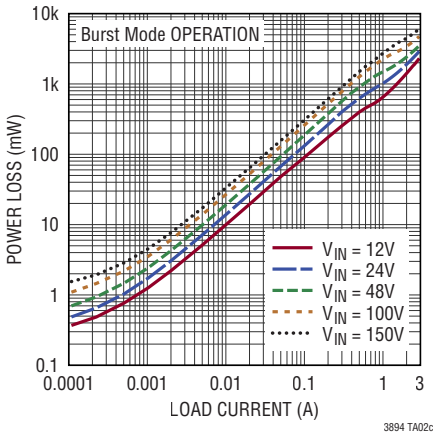
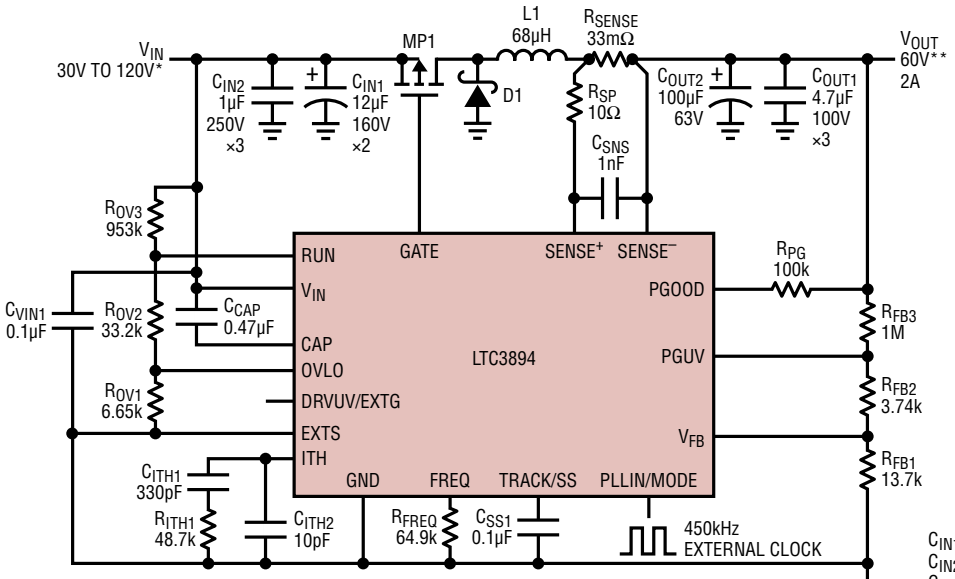


Figure 12. High Efficiency 150V to 5V/3A, 200kHz Step-Down Regulator

TYPICAL APPLICATIONS



* SURGES TO 150V, OVLO STOPS SWITCHING WHEN V_{IN} > 120V.
REGULATOR SHUTS DOWN WHEN V_{IN} < 30V.

** V_{OUT} FOLLOWS V_{IN} WHEN V_{IN} < 60V.
PGOOD UNDERVOLTAGE = 42V

C_{IN1}: 12µF 160V ILLINOIS CAP 126AVG160MGBJ
C_{IN2}: 1µF 250V TDK CGA8P3X7T2E105KS
C_{OUT1}: 4.7µF 100V TDK CGA6M3X7S2A475K
C_{OUT2}: 100µF 63V UNITED CHEMI-CON EMVH630ARA101MK
L1: 60µH WURTH ELEKTRONIK 7447709680
MP1: FAIRCHILD FDMC86259P
D1: ST MICRO STPS10150CG

Efficiency and Power Loss vs Load Current

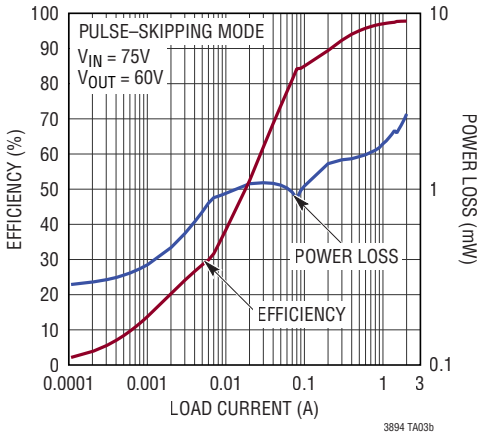
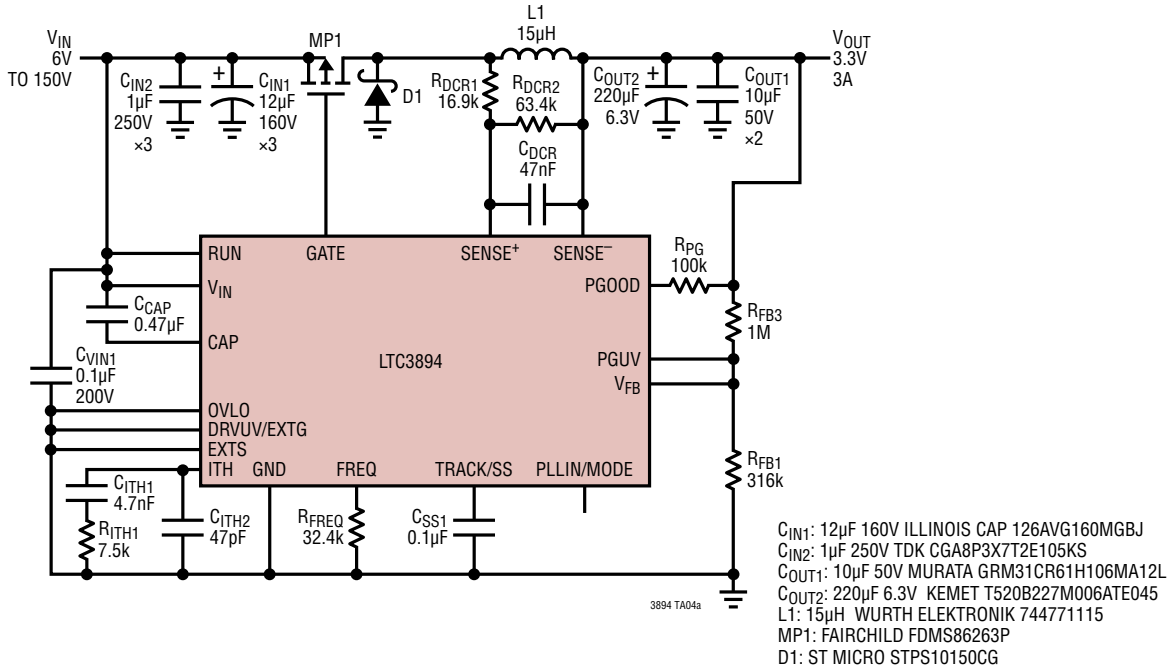


Figure 13. High Efficiency 120V Input to 60V Step-Down Regulator with Surge Protection to 150V

TYPICAL APPLICATIONS



C_{IN1}: 12µF 160V ILLINOIS CAP 126AVG160MGBJ
C_{IN2}: 1µF 250V TDK CGA8P3X7T2E105KS
C_{OUT1}: 10µF 50V MURATA GRM31CR61H106MA12L
C_{OUT2}: 220µF 6.3V KEMET T520B227M006ATE045
L1: 15µH WURTH ELEKTRONIK 744771115
MP1: FAIRCHILD FDMS86263P
D1: ST MICRO STPS10150CG

Efficiency and Power Loss vs Load Current

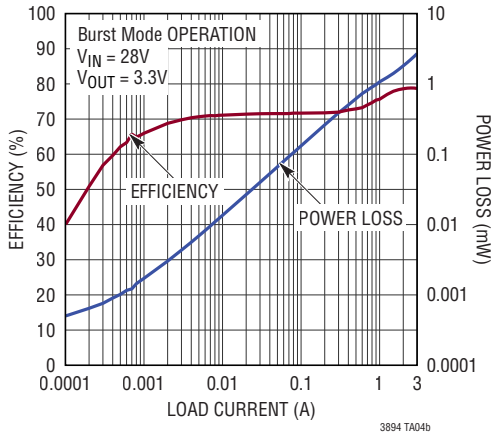
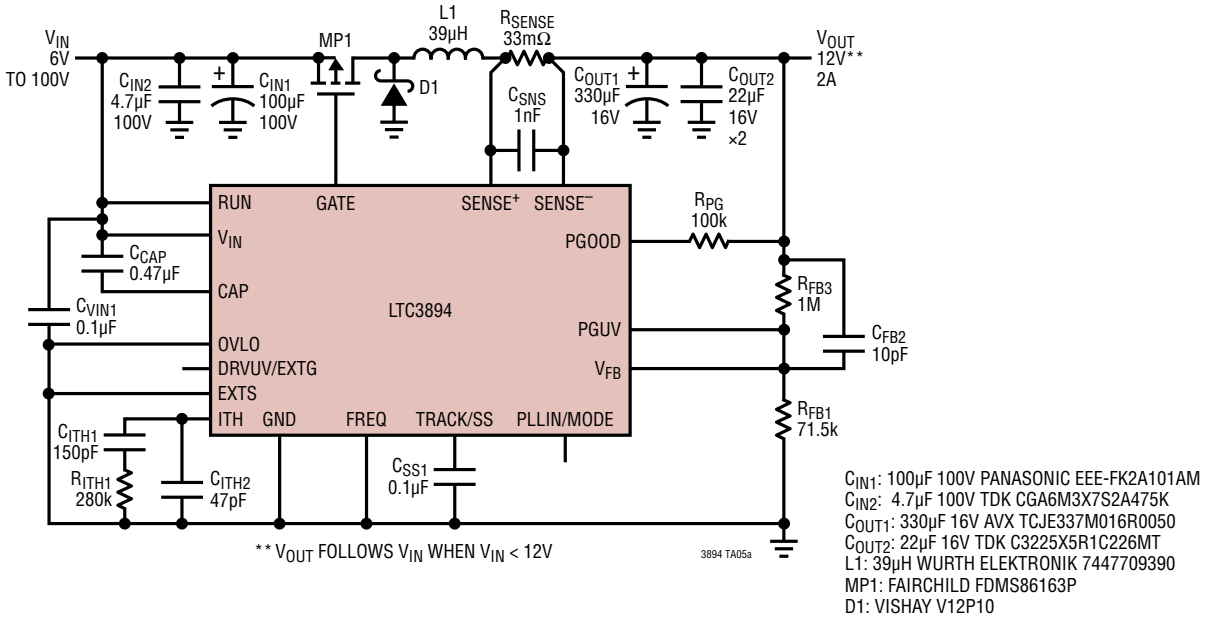


Figure 14. 6V to 150V Input, 3.3V/3A Output, 175kHz Step-Down Regulator

TYPICAL APPLICATIONS



C_{IN1}: 100µF 100V PANASONIC EEE-FK2A101AM
C_{IN2}: 4.7µF 100V TDK CGA6M3X7S2A475K
C_{OUT1}: 330µF 16V AVX TCJE337M016R0050
C_{OUT2}: 22µF 16V TDK C3225X5R1C226MT
L1: 39µH WURTH ELEKTRONIK 7447709390
MP1: FAIRCHILD FDMS86163P
D1: VISHAY V12P10

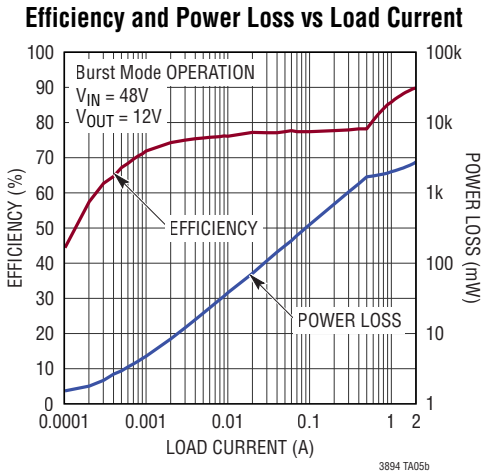
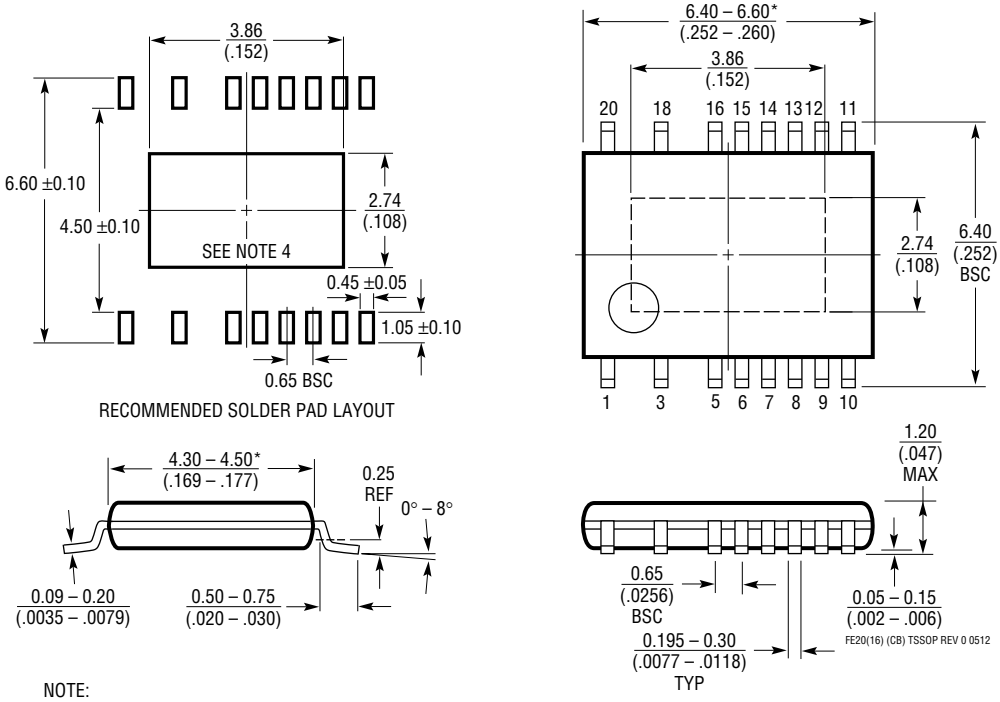


Figure 15. 6V to 100V Input, 12V/2A Output, 350kHz Step-Down Regulator

PACKAGE DESCRIPTION

FE Package
Variation: FE20(16)
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1924 Rev Ø)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/18	Added H-grade information	1–4

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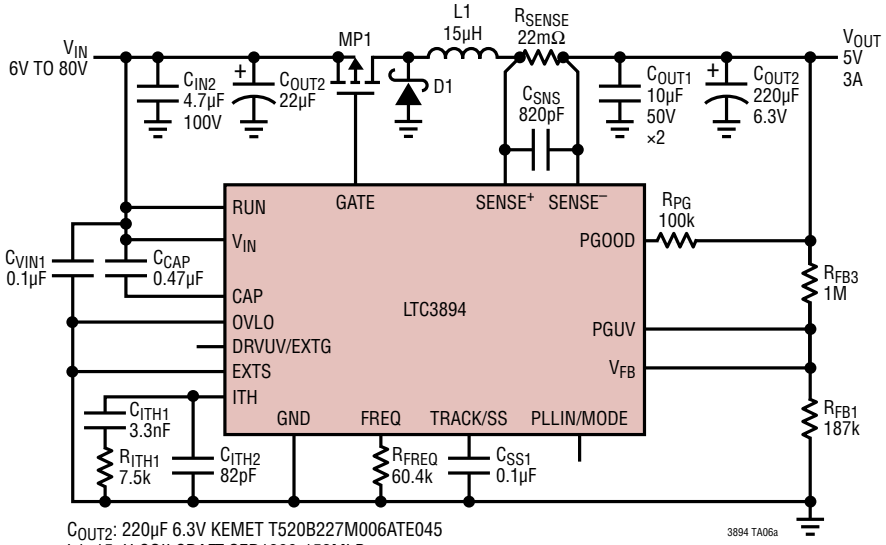
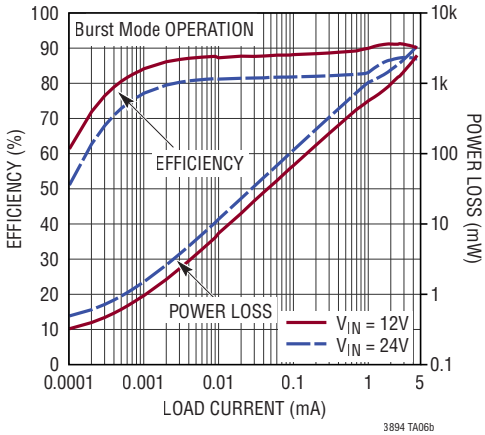
TYPICAL APPLICATION

High Efficiency 6V to 80V Input, 5V/3A Output, Step-Down Regulator



C_{OUT2}: 220µF 6.3V KEMET T520B227M006ATE045
L1: 15µH COILCRAFT SER1390-153MLB
MP1: FAIRCHILD FDMS86163P
D1: DIODES INC SBR3U100LP7

Efficiency and Power Loss vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3895/ LTC7801	150V Low I_Q, Synchronous Step-Down DC/DC Controller with 100% Duty Cycle	$4V \le V_{IN} \le 140V$, 150V Abs Max, PLL Fixed Frequency 50kHz to 900kHz, $0.8V \le V_{OUT} \le 60V$, Adjustable 5V to 10V Gate Drive, I_Q = 40µA, 4mm × 5mm QFN-24, TSSOP-24, TSSOP-38(31)
LTC3871	Bidirectional PolyPhase® Synchronous Buck or Boost Controller	V_{HIGH} Up to 100V, V_{LOW} Up to 30V, High Power Buck or Boost on Demand
LTC3639	High Efficiency, 150V 100mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, $4V \le V_{IN} \le 150V$, $0.8V \le V_{OUT} \le V_{IN}$, I_Q = 12µA, MSOP-16(12)
LTC3638	High Efficiency, 140V 250mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, $4V \le V_{IN} \le 140V$, $0.8V \le V_{OUT} \le V_{IN}$, I_Q = 12µA, MSOP-16(12)
LTC7138	High Efficiency, 140V 400mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, $4V \le V_{IN} \le 140V$, $0.8V \le V_{OUT} \le V_{IN}$, I_Q = 12µA, MSOP-16(12)
LTC7860	High Efficiency Switching Surge Stopper	$3.5V \le V_{IN} \le 60V$, Expandable to 200V+, Adjustable V_{OUT} Clamp and Current Limit, Power Inductor Improves EMI, MSOP-12
LT8631	100V, 1A Synchronous Micropower Step-Down Regulator	Integrated Power MOSFETs, $3V \le V_{IN} \le 100V$, $0.8V \le V_{OUT} \le 60V$, I_Q = 7µA, TSSOP-20(16)
LTC3896	150V Low I_Q, Synchronous Inverting DC/DC Controller	$4V \le V_{IN} \le 140V$, $150V_{P-P}$, $–60V \le V_{OUT} \le –0.8V$, Ground Reference Interface Pins, Adjustable 5V to 10V Gate Drive, I_Q = 40µA
LTC7103	105V, 2.3A Low EMI Synchronous Step-Down Regulator	$4.4V \le V_{IN} \le 105V$, $1V \le V_{OUT} \le V_{IN}$, I_Q = 2µA Fixed Frequency 200kHz to 2MHz, 5mm × 6mm QFN
LTC7810	150V, Low IQ, Dual, 2-Phase Synchronous Step-Down DC/DC Controller	$4.5V \le V_{IN} \le 150V$, $1V \le V_{OUT} \le 60V$, Low 16µA I_Q, Adjustable Gate Drive, Spread Spectrum, 7mm × 7mm EQFP

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Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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http://moschip.ru/get-element

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9