

# MC74HC73A

## Dual J-K Flip-Flop with Reset

### High-Performance Silicon-Gate CMOS

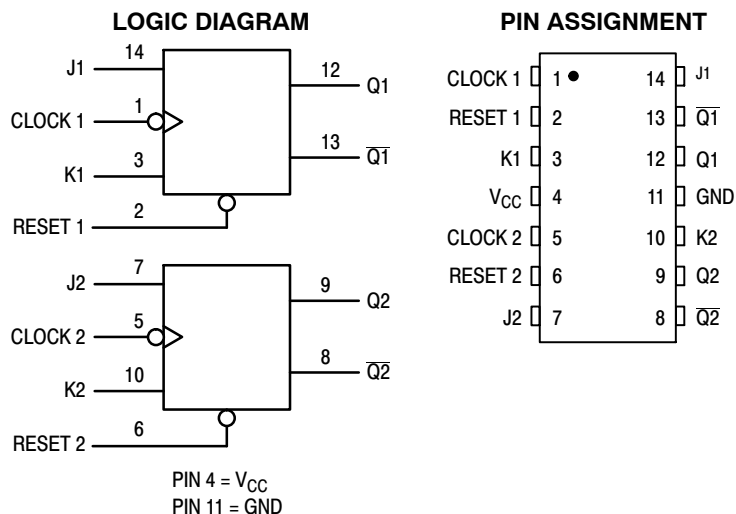
The MC74HC73A is identical in pinout to the LS73. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has an active-low asynchronous reset.

The MC74HC73A is identical in function to the HC107, but has a different pinout.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 92 FETs or 23 Equivalent Gates
- These are Pb-Free Devices



#### FUNCTION TABLE

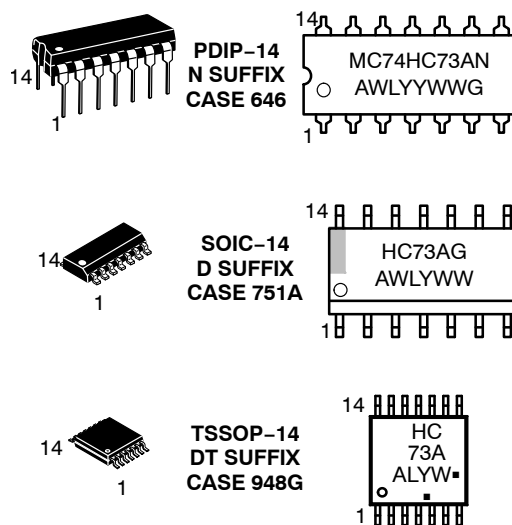
| Inputs |        |   |   | Outputs   |           |
|--------|--------|---|---|-----------|-----------|
| Reset  | Clock  | J | K | Q         | $\bar{Q}$ |
| L      | X      | X | X | L         | H         |
| H      | $\sim$ | L | L | No Change |           |
| H      | $\sim$ | L | H | L         | H         |
| H      | $\sim$ | H | L | H         | L         |
| H      | $\sim$ | H | H | Toggle    |           |
| H      | L      | X | X | No Change |           |
| H      | H      | X | X | No Change |           |
| H      | $\sim$ | X | X | No Change |           |



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#### MARKING DIAGRAMS



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package  
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC74HC73A

## MAXIMUM RATINGS\*

| Symbol    | Parameter                                                                        | Value                   | Unit |
|-----------|----------------------------------------------------------------------------------|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                            | – 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                             | – 1.5 to $V_{CC} + 1.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                            | – 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin                                                        | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin                                                       | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                         | $\pm 50$                | mA   |
| $P_D$     | Power Dissipation in Still Air<br>Plastic DIP†<br>SOIC Package†                  | 750<br>500              | mW   |
| $T_{stg}$ | Storage Temperature                                                              | – 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package) | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C

SOIC Package: – 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol                             | Parameter                                            | Min                     | Max             | Unit |    |
|------------------------------------|------------------------------------------------------|-------------------------|-----------------|------|----|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)                | 2.0                     | 6.0             | V    |    |
| V <sub>in</sub> , V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND) | 0                       | V <sub>CC</sub> | V    |    |
| T <sub>A</sub>                     | Operating Temperature, All Package Types             | − 55                    | + 125           | °C   |    |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise and Fall Time                             | V <sub>CC</sub> = 2.0 V | 0               | 1000 | ns |
|                                    | (Figure 1)                                           | V <sub>CC</sub> = 4.5 V | 0               | 500  |    |
|                                    |                                                      | V <sub>CC</sub> = 6.0 V | 0               | 400  |    |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol   | Parameter                                      | Test Conditions                                                                                         | $V_{CC}$<br>V     | Guaranteed Limit   |                    |                    | Unit          |
|----------|------------------------------------------------|---------------------------------------------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|---------------|
|          |                                                |                                                                                                         |                   | – 55 to<br>25°C    | ≤ 85°C             | ≤ 125°C            |               |
| $V_{IH}$ | Minimum High-Level Input Voltage               | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$                 | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V             |
| $V_{IL}$ | Maximum Low-Level Input Voltage                | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$                 | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V             |
| $V_{OH}$ | Minimum High-Level Output Voltage              | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$                                 | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V             |
|          |                                                | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$<br>$ I_{out}  \leq 5.2 \text{ mA}$ | 4.5<br>6.0        | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       |               |
| $V_{OL}$ | Maximum Low-Level Output Voltage               | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$                                 | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V             |
|          |                                                | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$<br>$ I_{out}  \leq 5.2 \text{ mA}$ | 4.5<br>6.0        | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |               |
| $I_{in}$ | Maximum Input Leakage Current                  | $V_{in} = V_{CC} \text{ or GND}$                                                                        | 6.0               | $\pm 0.1$          | $\pm 1.0$          | $\pm 1.0$          | $\mu\text{A}$ |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC} \text{ or GND}$<br>$I_{out} = 0 \mu\text{A}$                                           | 6.0               | 4                  | 40                 | 80                 | $\mu\text{A}$ |

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## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

| Symbol                                 | Parameter                                                               | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|----------------------------------------|-------------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|                                        |                                                                         |                      | – 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 1 and 4)           | 2.0                  | 6.0              | 4.8    | 4.0     | MHz  |
|                                        |                                                                         | 4.5                  | 30               | 24     | 20      |      |
|                                        |                                                                         | 6.0                  | 35               | 28     | 24      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock to Q or $\bar{Q}$<br>(Figures 1 and 4) | 2.0                  | 125              | 155    | 190     | ns   |
|                                        |                                                                         | 4.5                  | 25               | 31     | 38      |      |
|                                        |                                                                         | 6.0                  | 21               | 26     | 32      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Reset to Q or $\bar{Q}$<br>(Figures 2 and 4) | 2.0                  | 155              | 195    | 235     | ns   |
|                                        |                                                                         | 4.5                  | 31               | 39     | 47      |      |
|                                        |                                                                         | 6.0                  | 26               | 33     | 40      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 4)         | 2.0                  | 75               | 95     | 110     | ns   |
|                                        |                                                                         | 4.5                  | 15               | 19     | 22      |      |
|                                        |                                                                         | 6.0                  | 13               | 16     | 19      |      |
| C <sub>in</sub>                        | Maximum Input Capacitance                                               | —                    | 10               | 10     | 10      | pF   |

|                 |                                                |                                         |    |
|-----------------|------------------------------------------------|-----------------------------------------|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Per Flip-Flop)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|                 |                                                | 35                                      |    |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## TIMING REQUIREMENTS (Input $t_r = t_f = 6 \text{ ns}$ )

| Symbol                          | Parameter                                                    | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|---------------------------------|--------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|                                 |                                                              |                      | – 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| t <sub>su</sub>                 | Minimum Setup Time, J or K to Clock<br>(Figure 3)            | 2.0                  | 100              | 125    | 150     | ns   |
|                                 |                                                              | 4.5                  | 20               | 25     | 30      |      |
|                                 |                                                              | 6.0                  | 17               | 21     | 26      |      |
| t <sub>h</sub>                  | Minimum Hold Time, Clock to J or K<br>(Figure 3)             | 2.0                  | 3                | 3      | 3       | ns   |
|                                 |                                                              | 4.5                  | 3                | 3      | 3       |      |
|                                 |                                                              | 6.0                  | 3                | 3      | 3       |      |
| t <sub>rec</sub>                | Minimum Recovery Time, Reset Inactive to Clock<br>(Figure 2) | 2.0                  | 100              | 125    | 150     | ns   |
|                                 |                                                              | 4.5                  | 20               | 25     | 30      |      |
|                                 |                                                              | 6.0                  | 17               | 21     | 26      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Clock<br>(Figure 1)                     | 2.0                  | 80               | 100    | 120     | ns   |
|                                 |                                                              | 4.5                  | 16               | 20     | 24      |      |
|                                 |                                                              | 6.0                  | 14               | 17     | 20      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Reset<br>(Figure 2)                     | 2.0                  | 80               | 100    | 120     | ns   |
|                                 |                                                              | 4.5                  | 16               | 20     | 24      |      |
|                                 |                                                              | 6.0                  | 14               | 17     | 20      |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 1)              | 2.0                  | 1000             | 1000   | 1000    | ns   |
|                                 |                                                              | 4.5                  | 500              | 500    | 500     |      |
|                                 |                                                              | 6.0                  | 400              | 400    | 400     |      |

# MC74HC73A

## SWITCHING WAVEFORMS

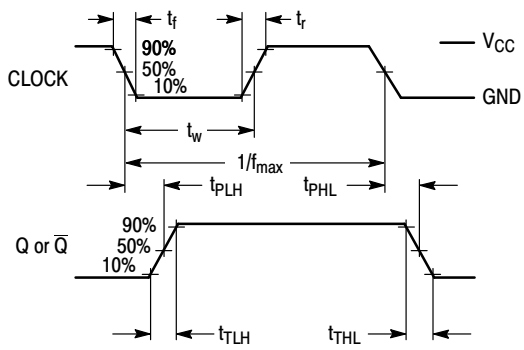


Figure 1.

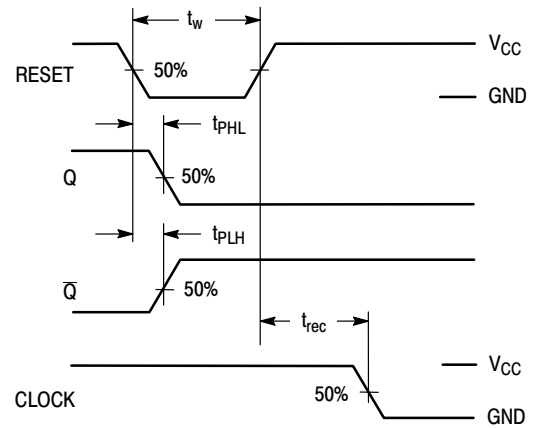


Figure 2.

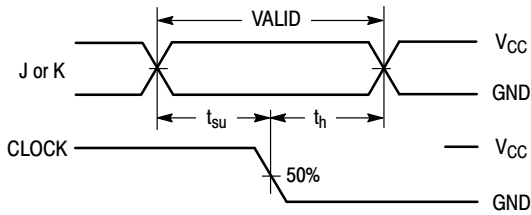
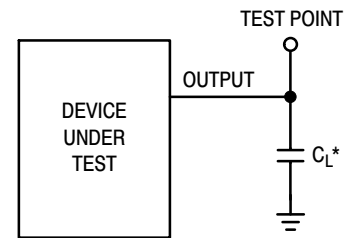


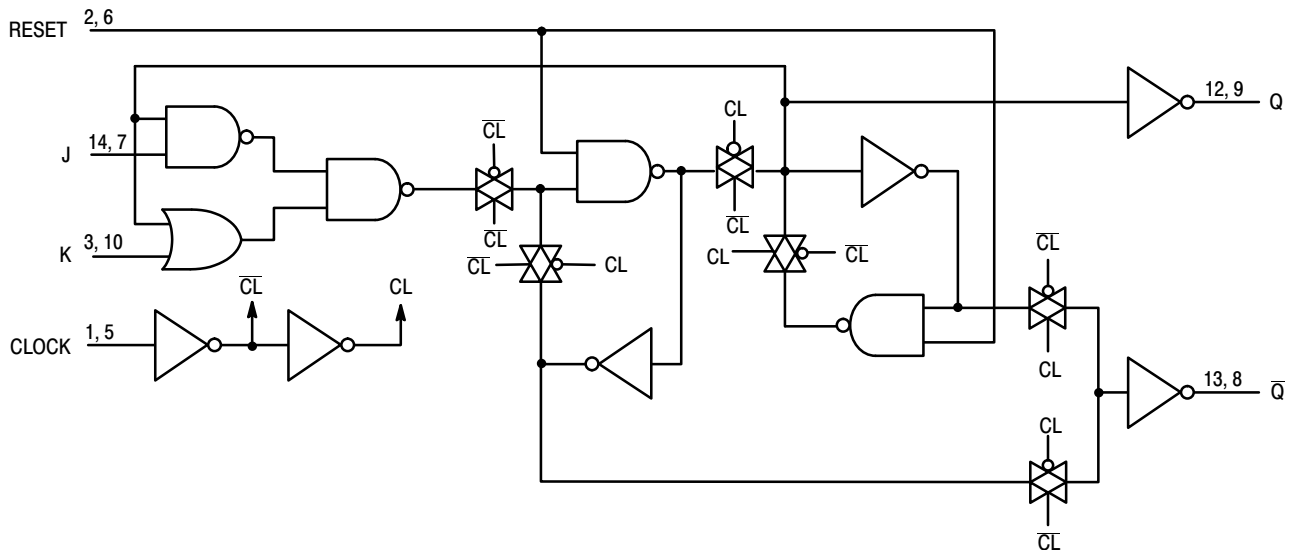
Figure 3.



\*Includes all probe and jig capacitance

Figure 4.

## EXPANDED LOGIC DIAGRAM



## MC74HC73A

### ORDERING INFORMATION

| Device         | Package              | Shipping <sup>†</sup> |
|----------------|----------------------|-----------------------|
| MC74HC73ANG    | PDIP-14<br>(Pb-Free) | 25 Units / Rail       |
| MC74HC73ADG    | SOIC-14<br>(Pb-Free) | 55 Units / Rail       |
| MC74HC73ADR2G  | SOIC-14<br>(Pb-Free) | 2500 / Tape & Reel    |
| MC74HC73ADTR2G | TSSOP-14*            |                       |

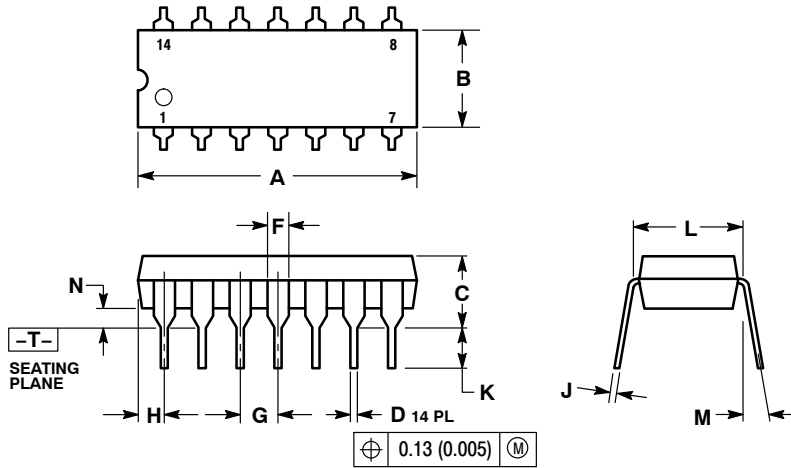
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74HC73A

## PACKAGE DIMENSIONS

**PDIP-14**  
CASE 646-06  
ISSUE P



### NOTES:

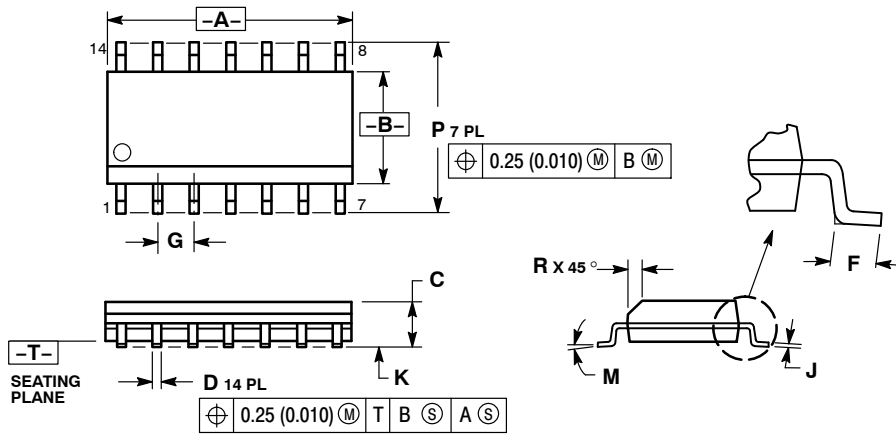
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.715     | 0.770 | 18.16       | 19.56 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.145     | 0.185 | 3.69        | 4.69  |
| D   | 0.015     | 0.021 | 0.38        | 0.53  |
| F   | 0.040     | 0.070 | 1.02        | 1.78  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.052     | 0.095 | 1.32        | 2.41  |
| J   | 0.008     | 0.015 | 0.20        | 0.38  |
| K   | 0.115     | 0.135 | 2.92        | 3.43  |
| L   | 0.290     | 0.310 | 7.37        | 7.87  |
| M   | 10 °      |       | 10 °        |       |
| N   | 0.015     | 0.039 | 0.38        | 1.01  |

# MC74HC73A

## PACKAGE DIMENSIONS

SOIC-14  
CASE 751A-03  
ISSUE H

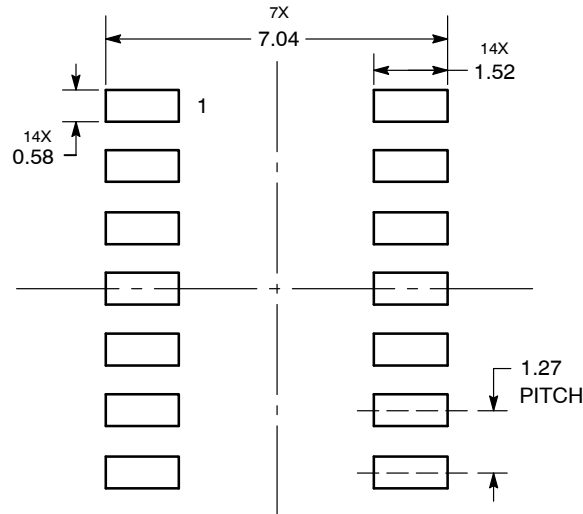


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 8.55        | 8.75 | 0.337     | 0.344 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.054     | 0.068 |
| D   | 0.35        | 0.49 | 0.014     | 0.019 |
| F   | 0.40        | 1.25 | 0.016     | 0.049 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| J   | 0.19        | 0.25 | 0.008     | 0.009 |
| K   | 0.10        | 0.25 | 0.004     | 0.009 |
| M   | 0°          | 7°   | 0°        | 7°    |
| P   | 5.80        | 6.20 | 0.228     | 0.244 |
| R   | 0.25        | 0.50 | 0.010     | 0.019 |

### SOLDERING FOOTPRINT\*



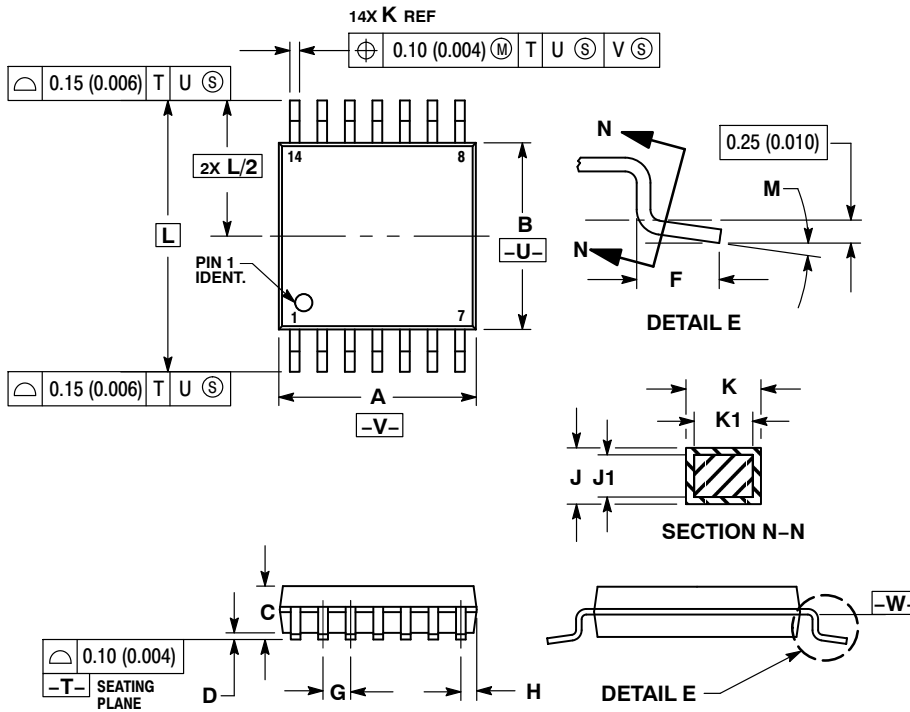
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC73A

## PACKAGE DIMENSIONS

TSSOP-14  
CASE 948G-01  
ISSUE B

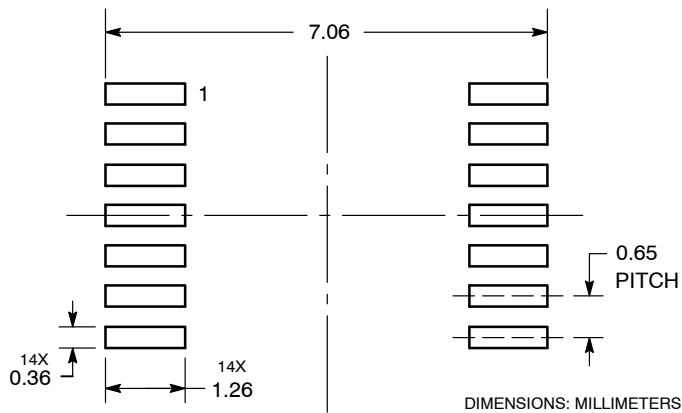


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES |       |
|-----|-------------|------|--------|-------|
|     | MIN         | MAX  | MIN    | MAX   |
| A   | 4.90        | 5.10 | 0.193  | 0.200 |
| B   | 4.30        | 4.50 | 0.169  | 0.177 |
| C   | ---         | 1.20 | ---    | 0.047 |
| D   | 0.05        | 0.15 | 0.002  | 0.006 |
| F   | 0.50        | 0.75 | 0.020  | 0.030 |
| G   | 0.65        | BSC  | 0.026  | BSC   |
| H   | 0.50        | 0.60 | 0.020  | 0.024 |
| J   | 0.09        | 0.20 | 0.004  | 0.008 |
| J1  | 0.09        | 0.16 | 0.004  | 0.006 |
| K   | 0.19        | 0.30 | 0.007  | 0.012 |
| K1  | 0.19        | 0.25 | 0.007  | 0.010 |
| L   | 6.40        | BSC  | 0.252  | BSC   |
| M   | 0°          | 8°   | 0°     | 8°    |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9