

# MC14541B

## Programmable Timer

The MC14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified  $V_{DD}$  range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency ( $f_{osc}$ ) with the  $n^{th}$  stage frequency being  $f_{osc}/2^n$ .

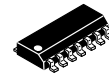
### Features

- Available Outputs  $2^8$ ,  $2^{10}$ ,  $2^{13}$  or  $2^{16}$
- Increments on Positive Edge Clock Transitions
- Built-in Low Power RC Oscillator ( $\pm 2\%$  accuracy over temperature range and  $\pm 20\%$  supply and  $\pm 3\%$  over processing at  $< 10$  kHz)
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as  $2^n$  Frequency Divider or Single Transition Timer
- $Q/\bar{Q}$  Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Automatic Reset Initializes All Counters On Power Up
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disabled (Pin 5 =  $V_{DD}$ )  
= 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 =  $V_{SS}$ )
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

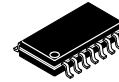


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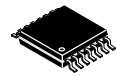
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SOIC-14  
D SUFFIX  
CASE 751A

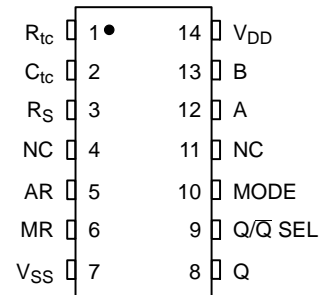


SOEIAJ-14  
F SUFFIX  
CASE 965



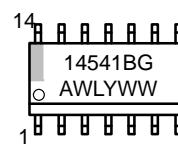
TSSOP-14  
DT SUFFIX  
CASE 948G

### PIN ASSIGNMENT

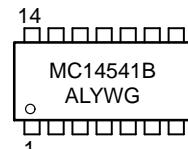


NC = NO CONNECTION

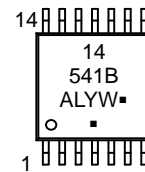
### MARKING DIAGRAMS



SOIC-14



SOEIAJ-14



TSSOP-14

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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## MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range, (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient)	$\pm 10$ (per Pin)	mA
$I_{out}$	Output Current (DC or Transient)	$\pm 45$ (per Pin)	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature, (8-Second Soldering)	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages:  $-7.0 \text{ mW}/^{\circ}\text{C}$  From  $65^{\circ}\text{C}$  To  $125^{\circ}\text{C}$

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC14541BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14541BDG*	SOIC-14 (Pb-Free)	55 Units / Rail
MC14541BDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14541BDR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC14541BDTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV14541BDTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
MC14541BFELG	SOEIAJ-14 (Pb-Free)	2000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55° C		25° C			125° C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level	V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
			10	-	0.05	-	0	0.05	-	0.05	
			15	-	0.05	-	0	0.05	-	0.05	
	"1" Level	V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level	V <sub>IL</sub>	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
			10	-	3.0	-	4.50	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
	"1" Level	V <sub>IH</sub>	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11	-	11	8.25	-	11	-	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	-4.19	-	-3.38	-6.75	-	-2.37	-	mAdc
			10	-7.96	-	-6.42	-12.83	-	-4.49	-	
			15	-16.3	-	-13.2	-26.33	-	-9.24	-	
	Sink	I <sub>OL</sub>	5.0	1.93	-	1.56	3.12	-	1.09	-	mAdc
			10	4.96	-	4.0	8.0	-	2.8	-	
			15	19.3	-	15.6	31.2	-	10.9	-	
Input Current	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	µAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Pin 5 is High) Auto Reset Disabled	I <sub>DD</sub>	5.0	-	5.0	-	0.005	5.0	-	150	µAdc	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Auto Reset Quiescent Current (Pin 5 is low)	I <sub>DDR</sub>	10	-	250	-	30	250	-	1500	µAdc	
		15	-	500	-	82	500	-	2000		
Supply Current (Notes 3 & 4) (Dynamic plus Quiescent)	I <sub>D</sub>	5.0	I <sub>D</sub> = (0.4 µA/kHz) f + I <sub>DD</sub>							µAdc	
		10	I <sub>D</sub> = (0.8 µA/kHz) f + I <sub>DD</sub>								
		15	I <sub>D</sub> = (1.2 µA/kHz) f + I <sub>DD</sub>								

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. When using the on chip oscillator the total supply current (in µAdc) becomes: I<sub>T</sub> = I<sub>D</sub> + 2 C<sub>tc</sub> V<sub>DD</sub> f × 10<sup>-3</sup> where I<sub>D</sub> is in µA, C<sub>tc</sub> is in pF, V<sub>DD</sub> in Volts DC, and f in kHz. (see Fig. 3) Dissipation during power-on with automatic reset enabled is typically 50 µA @ V<sub>DD</sub> = 10 Vdc.

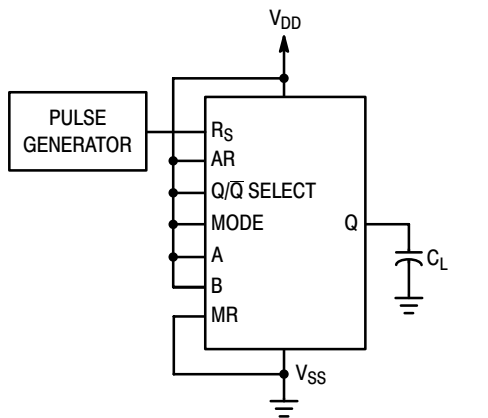
# MC14541B

## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay, Clock to Q ( $2^8$ Output) $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 3415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 1217 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 875 \text{ ns}$	$t_{PLH}$ $t_{PHL}$	5.0 10 15	– – –	3.5 1.25 0.9	10.5 3.8 2.9	$\mu\text{s}$
Propagation Delay, Clock to Q ( $2^{16}$ Output) $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 5915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 3467 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 2475 \text{ ns}$	$t_{PHL}$ $t_{PLH}$	5.0 10 15	– – –	6.0 3.5 2.5	18 10 7.5	$\mu\text{s}$
Clock Pulse Width	$t_{WH(cl)}$	5.0 10 15	900 300 225	300 100 85	– – –	ns
Clock Pulse Frequency (50% Duty Cycle)	$f_{cl}$	5.0 10 15	– – –	1.5 4.0 6.0	0.75 2.0 3.0	MHz
MR Pulse Width	$t_{WH(R)}$	5.0 10 15	900 300 225	300 100 85	– – –	ns
Master Reset Removal Time	$t_{rem}$	5.0 10 15	420 200 200	210 100 100	– – –	ns

5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



( $R_{tc}$  AND  $C_{tc}$  OUTPUTS ARE LEFT OPEN)

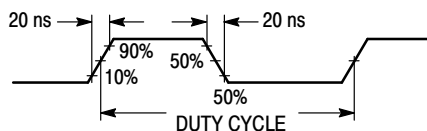


Figure 1. Power Dissipation Test Circuit and Waveform

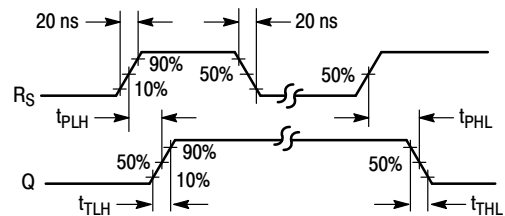
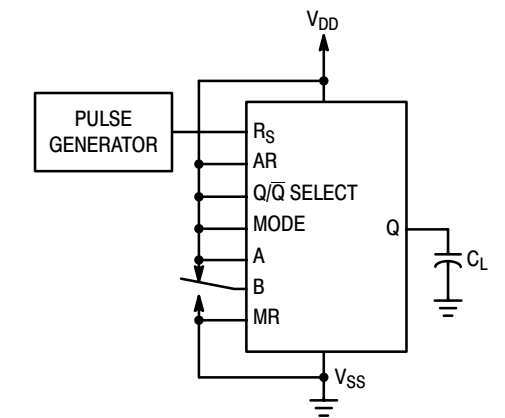
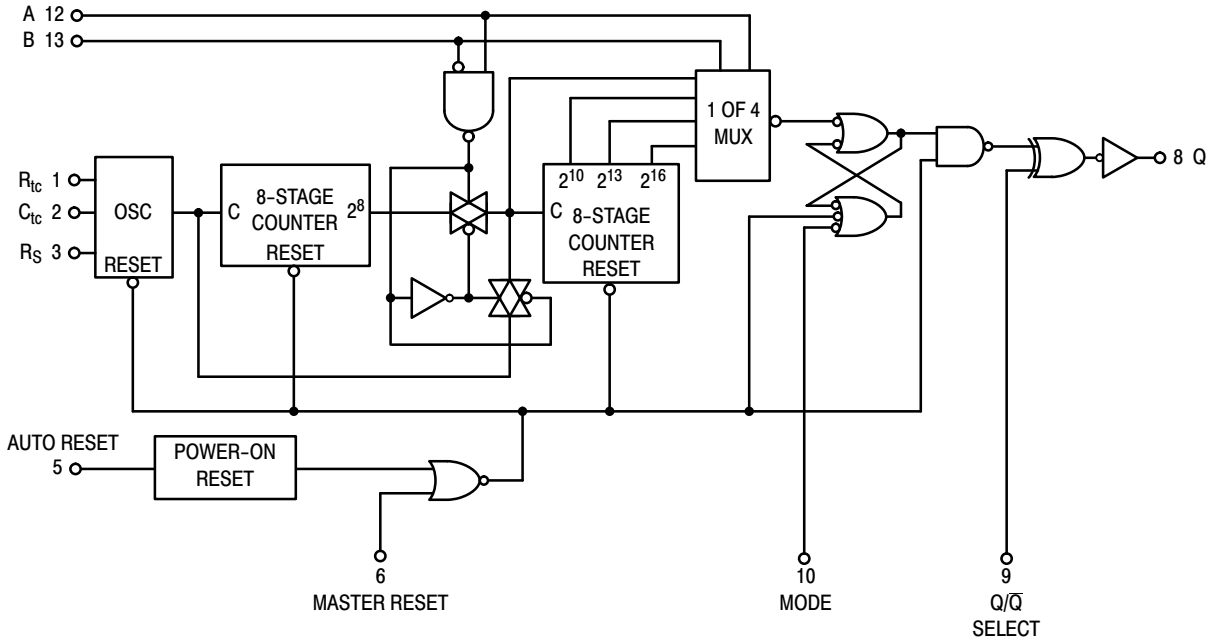


Figure 2. Switching Time Test Circuit and Waveforms

# MC14541B

## EXPANDED BLOCK DIAGRAM



$V_{DD}$  = PIN 14  
 $V_{SS}$  = PIN 7

### FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count $2^n$
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

### TRUTH TABLE

Pin	State	
	0	1
Auto Reset, 5	Auto Reset Operating	Auto Reset Disabled
Master Reset, 6	Timer Operational	Master Reset On
$Q/\bar{Q}$ , 9	Output Initially Low After Reset	Output Initially High After Reset
Mode, 10	Single Cycle Mode	Recycle Mode

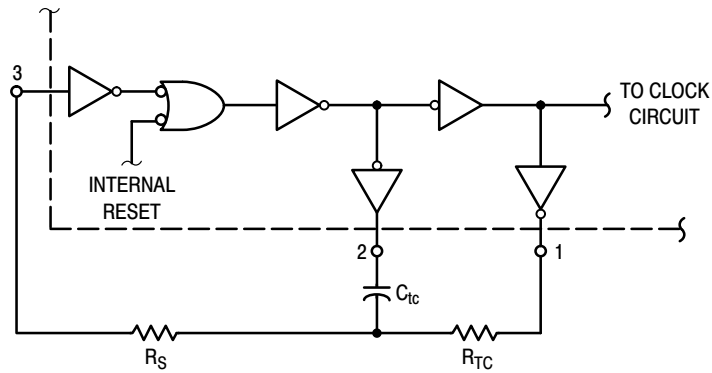


Figure 3. Oscillator Circuit Using RC Configuration

TYPICAL RC OSCILLATOR CHARACTERISTICS

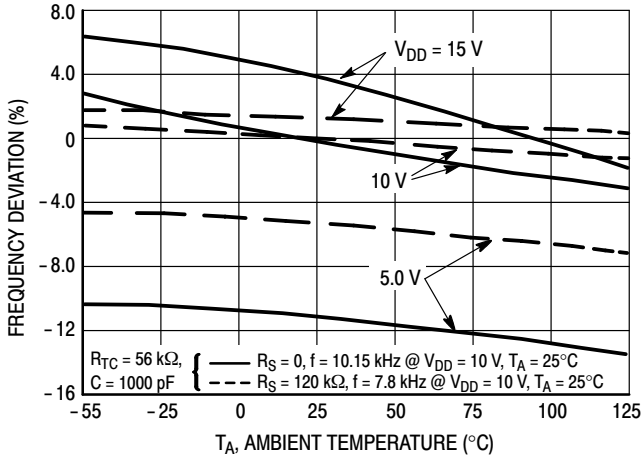


Figure 4. RC Oscillator Stability

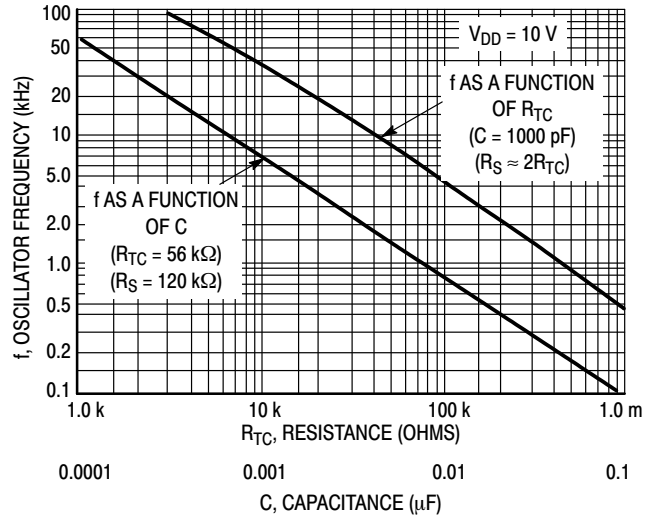


Figure 5. RC Oscillator Frequency as a Function of  $R_{tc}$  and  $C_{tc}$

OPERATING CHARACTERISTICS

With Auto Reset pin set to a “0” the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a “1”. Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a “1” provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3 R_{tc} C_{tc}} \quad \text{if } (1 \text{ kHz} \leq f \leq 100 \text{ kHz})$$

and  $R_S \approx 2 R_{tc}$  where  $R_S \geq 10 \text{ k}\Omega$

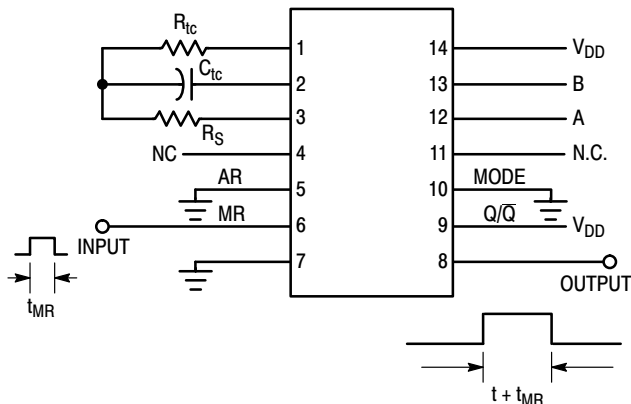
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages ( $2^8$ ,  $2^{10}$ ,  $2^{13}$  and  $2^{16}$ ). The  $2^n$  counts as shown in the Frequency Selection Table represents the Q output of the  $N^{\text{th}}$  stage of the counter. When A is “1”,  $2^{16}$  is selected for both states of B. However,

when B is “0”, normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting  $2^8$ ).

The  $Q/\bar{Q}$  select output control pin provides for a choice of output level. When the counter is in a reset condition and  $Q/\bar{Q}$  select pin is set to a “0” the Q output is a “0”, correspondingly when  $Q/\bar{Q}$  select pin is set to a “1” the Q output is a “1”.

When the mode control pin is set to a “1”, the selected count is continually transmitted to the output. But, with mode pin “0” and after a reset condition the  $R_S$  flip-flop (see Expanded Block Diagram) resets, counting commences, and after  $2^{n-1}$  counts the  $R_S$  flip-flop sets which causes the output to change state. Hence, after another  $2^{n-1}$  counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

DIGITAL TIMER APPLICATION



When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

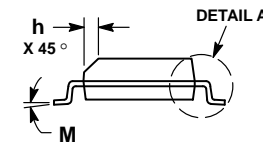
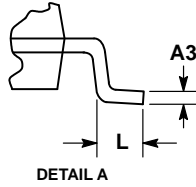
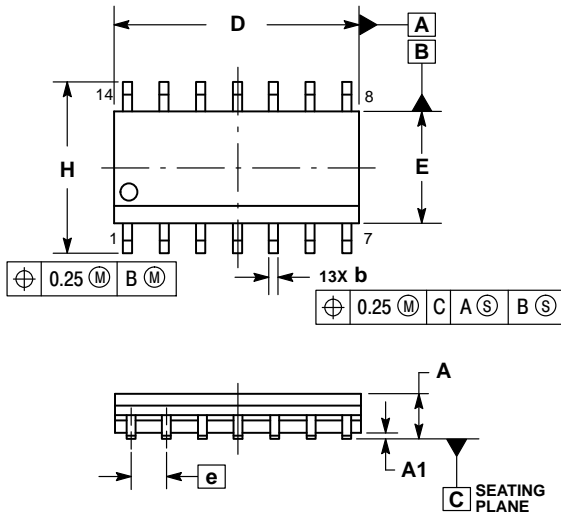
This “one shot” is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

# MC14541B

## PACKAGE DIMENSIONS

SOIC-14 NB  
CASE 751A-03  
ISSUE K

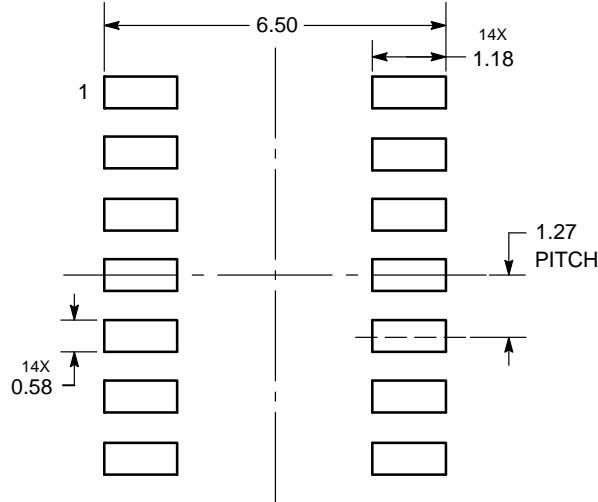


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



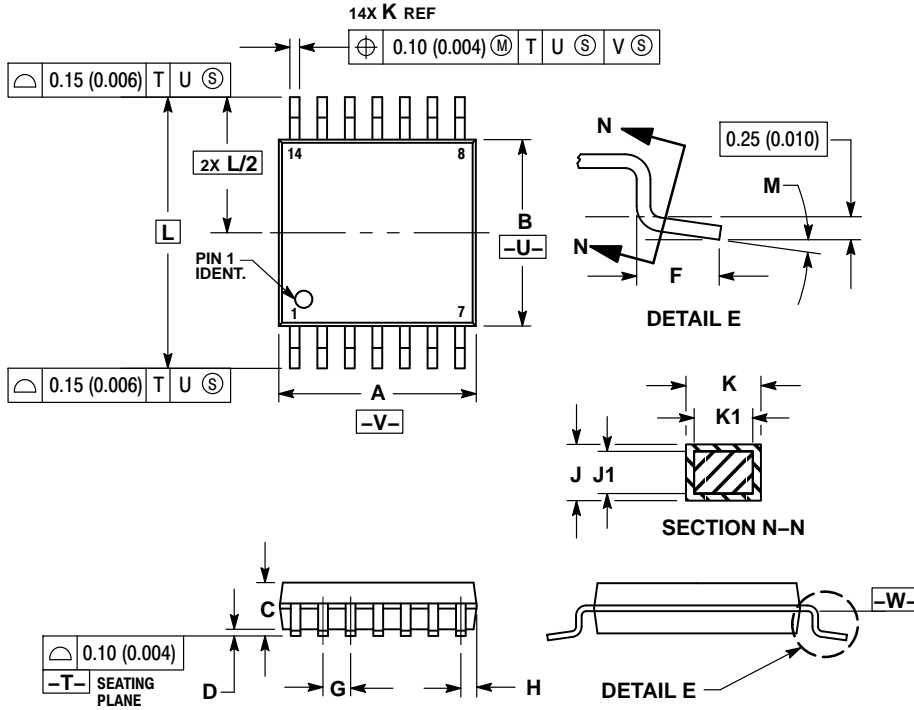
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC14541B

## PACKAGE DIMENSIONS

TSSOP-14  
CASE 948G  
ISSUE B

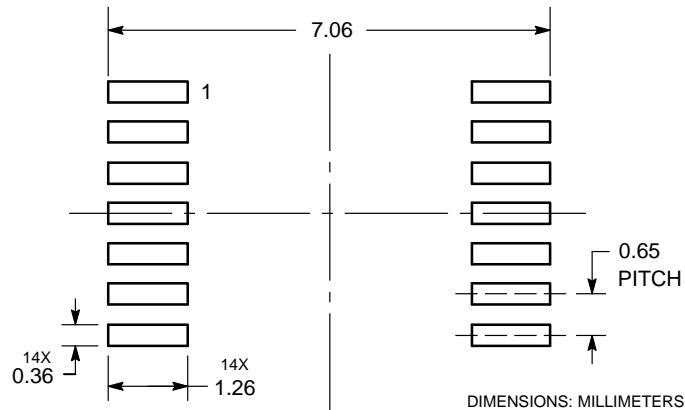


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

### SOLDERING FOOTPRINT\*



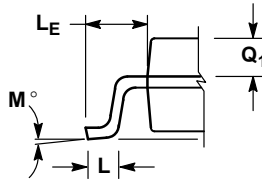
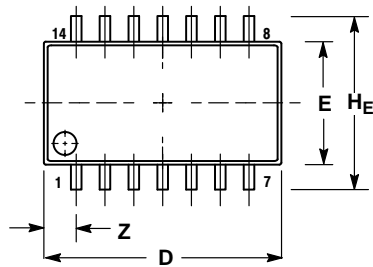
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



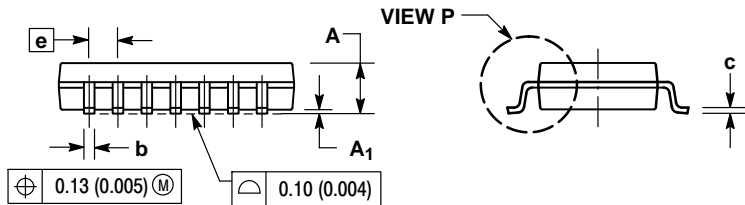
# MC14541B

## PACKAGE DIMENSIONS

SOEIAJ-14  
CASE 965  
ISSUE B




DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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