



*PRODUCT SPECIFICATION*

# **Z86C93**

CMOS Z8®  
MULTIPLY/DIVIDE  
MICROCONTROLLER



## Z86C93

### CMOS Z8® MULTIPLY/DIVIDE MICROCONTROLLER

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#### FEATURES

- Complete microcontroller, up to 24 I/O lines, and up to 64 Kbytes of addressable external space each for program and data memory.
- 16-bit x 16-bit hardwired multiplier with 32-bit product in 17 clock cycles.
- 32-bit x 16-bit hardwired divider with 16-bit quotient and 16-bit remainder in 20 clock cycles.
- 256-byte register file, including 236 general-purpose registers, up to three I/O port registers and 16 status and control registers.
- 17-byte Expanded Register File, including two general-purpose registers and 15 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Two 16-bit counter timers with 6-bit prescalers.
- Third 16-bit counter/timer with 4-bit prescaler, one capture register and a fast decrement mode.
- Register Pointer for short, fast instructions that can access any one of the sixteen working register groups.
- Additional emulation signals SCLK, IACK, and /SYNC are made available.
- Two low power standby modes, STOP and HALT
- Full-duplex UART
- $3.3 \pm 10\%$  volt operation at 25 MHz
- $5.0 \pm 10\%$  volt operation at 20, 25 and 33 MHz

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#### GENERAL DESCRIPTION

The Z86C93 is a CMOS ROMless Z8 microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier and 32-bit/16-bit divider and three 16-bit counter timers (Figure 1). A capture register and a fast decrement mode is also provided. It is offered in 40-pin PDIP, 44-pin PLCC, 44-pin QFP and 48-pin VQFP (Figures 2, 3, 4, 5 and 6). Besides the four additional signals (SCLK, IACK, /SYNC and /WAIT), the Z86C93 is compatible with the Z86C91, yet it offers a much more powerful mathematical capability.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

# GENERAL DESCRIPTION (Continued)

There are 256 registers located on-chip and organized as 236 general-purpose registers, 16 control and status registers, and four I/O port registers. The register file can be divided into sixteen groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. There are an additional 17 registers implemented in the Expanded Register File in Banks D and E. Two of the registers may be used as general-purpose registers, while 15 registers supply the data and control functions for the Multiply/Divide Unit and Counter/Timer blocks.

**Notes:**  
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection   | Circuit                | Device                             |
|--------------|------------------------|------------------------------------|
| Power Ground | V <sub>CC</sub><br>GND | V <sub>DD</sub><br>V <sub>SS</sub> |

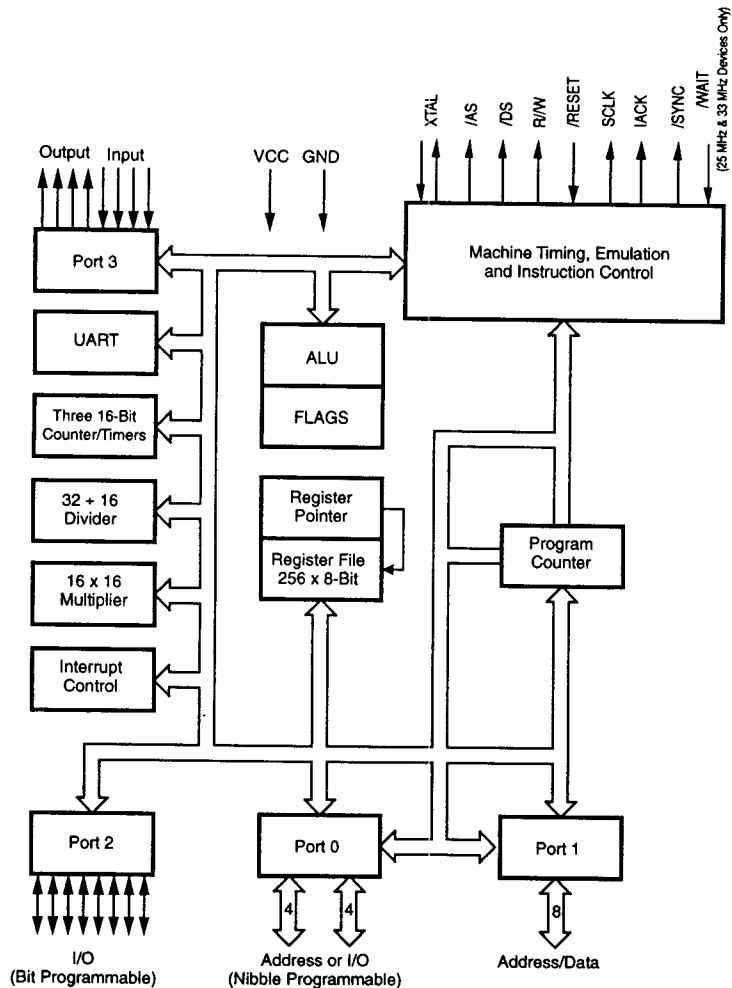


Figure 1. Functional Block Diagram

## PIN DESCRIPTION

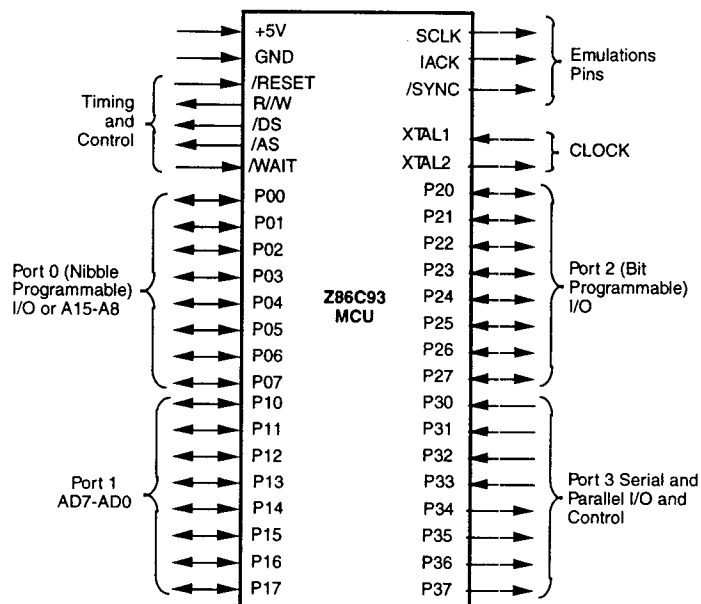


Figure 2. Pin Functions

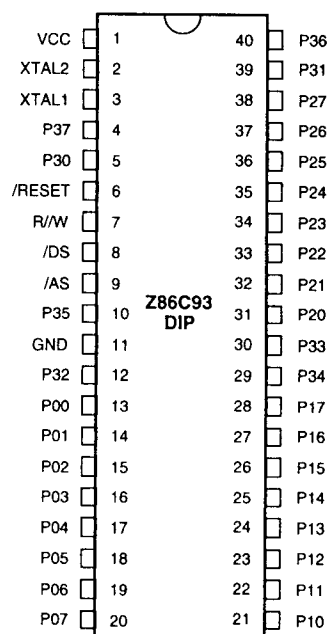
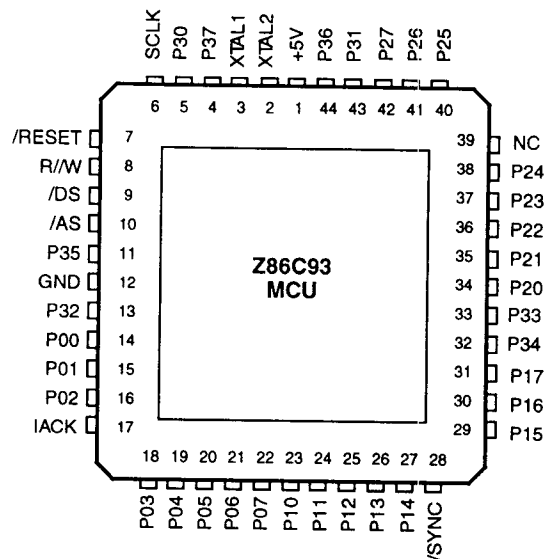


Figure 3. 40-Pin DIP

Table 1. 40-Pin DIP Pin Identification

| Pin # | Symbol          | Function                   | Direction |
|-------|-----------------|----------------------------|-----------|
| 1     | V <sub>CC</sub> | Power Supply               | Input     |
| 2     | XTAL1           | Crystal, Oscillator Clock  | Input     |
| 3     | XTAL2           | Crystal, Oscillator Clock  | Output    |
| 4     | P37             | Port 3 pin 7               | Output    |
| 5     | P30             | Port 3 pin 0               | Input     |
| 6     | /RESET          | Reset                      | Input     |
| 7     | R/W             | Read/Write                 | Output    |
| 8     | /DS             | Data Strobe                | Output    |
| 9     | /AS             | Address Strobe             | Output    |
| 10    | P35             | Port 3 pin 5               | Output    |
| 11    | GND             | Ground, GND                | Input     |
| 12    | P32             | Port 3 pin 2               | Input     |
| 13-20 | P00-P07         | Port 0 pin 0,1,2,3,4,5,6,7 | In/Output |
| 21-28 | P10-P17         | Port 1 pin 0,1,2,3,4,5,6,7 | In/Output |
| 29    | P34             | Port 3 pin 4               | Output    |
| 30    | P33             | Port 3 pin 3               | Input     |
| 31-38 | P20-P27         | Port 2 pin 0,1,2,3,4,5,6,7 | In/Output |
| 39    | P31             | Port 3 pin 1               | Input     |
| 40    | P36             | Port 3 pin 6               | Output    |



### Figure 4. 44-Pin PLCC

### Table 2. 44-Pin PLCC Pin Identification

| No | Symbol          | Function            | Direction |
|----|-----------------|---------------------|-----------|
| 1  | V <sub>CC</sub> | Power Supply        | Input     |
| 2  | XTAL2           | Crystal, Osc. Clock | Output    |
| 3  | XTAL1           | Crystal, Osc. Clock | Input     |
| 4  | P37             | Port 3 pin 7        | Output    |
| 5  | P30             | Port 3 pin 0        | Input     |
| 6  | SCLK            | System Clock        | Output    |
| 7  | /RESET          | Reset               | Input     |
| 8  | R/W             | Read/Write          | Output    |
| 9  | /DS             | Data Strobe         | Output    |
| 10 | /AS             | Address Strobe      | Output    |
| 11 | P35             | Port 3 pin 5        | Output    |
| 12 | GND             | Ground GND          | Input     |
| 13 | P32             | Port 3 pin 2        | Input     |

| No    | Symbol  | Function               | Direction |
|-------|---------|------------------------|-----------|
| 14-16 | P00-P02 | Port 0 pin 0,1,2       | In/Output |
| 17    | IACK    | Int. Acknowledge       | Output    |
| 18-22 | P03-P07 | Port 0 pin 3,4,5,6,7   | In/Output |
| 23-27 | P10-P14 | Port 1 pin 0,1,2,3,4   | In/Output |
| 28    | /SYNC   | Synchronize Pin        | Output    |
| 29-31 | P15-P17 | Port 1 pin 5,6,7       | In/Output |
| 32    | P34     | Port 3 pin 4           | Output    |
| 33    | P33     | Port 3 pin 3           | Input     |
| 34-38 | P20-P24 | Port 2 pin 0,1,2,3,4   | In/Output |
| 39    | N/C     | Not Connected (20 MHz) | Input     |
|       | /WAIT   | WAIT (25 or 33 MHz)    | Input     |
| 40-42 | P25-P27 | Port 2 pin 5,6,7       | In/Output |
| 43    | P31     | Port 3 pin 1           | Input     |
| 44    | P36     | Port 3 pin 6           | Output    |

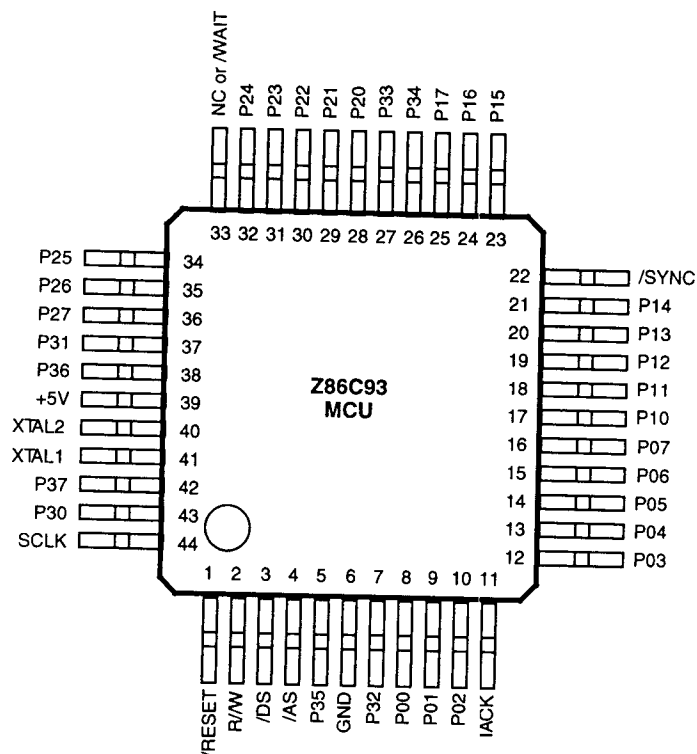
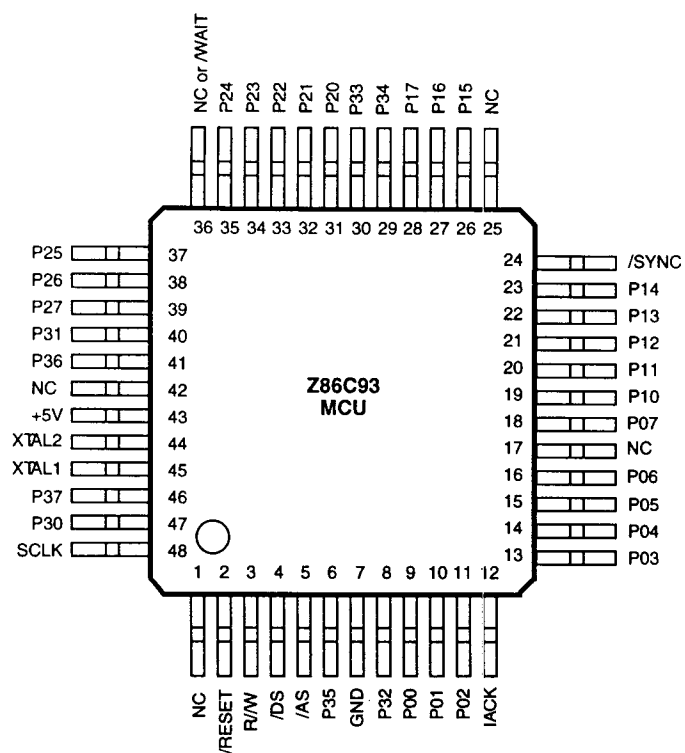


Figure 5. 44-Pin QFP

Table 3. 44-Pin QFP Pin Identification

| No    | Symbol  | Function             | Direction | No    | Symbol          | Function               | Direction |
|-------|---------|----------------------|-----------|-------|-----------------|------------------------|-----------|
| 1     | /RESET  | Reset                | Input     | 26    | P34             | Port 3 pin 4           | Output    |
| 2     | R/W     | Read/Write           | Output    | 27    | P33             | Port 3 pin 3           | Input     |
| 3     | /DS     | Data Strobe          | Output    | 28-32 | P20-P24         | Port 2 pin 0,1,2,3,4   | In/Output |
| 4     | /AS     | Address Strobe       | Output    | 33    | N/C             | Not Connected (20 MHz) | Input     |
| 5     | P35     | Port 3 pin 5         | Input     |       | /WAIT           | WAIT (25 or 33 MHz)    | Input     |
| 6     | GND     | Ground GND           | Input     | 34-36 | P25-P27         | Port 2 pin 5,6,7       | In/Output |
| 7     | P32     | Port 3 pin 2         | Input     | 37    | P31             | Port 3 pin 1           | Input     |
| 8-10  | P00-P02 | Port 0 pin 0,1,2     | In/Output | 38    | P36             | Port 3 pin 6           | Output    |
| 11    | IACK    | Int. Acknowledge     | Output    | 39    | V <sub>cc</sub> | Power Supply           | Input     |
| 12-16 | P03-P07 | Port 0 pin 3,4,5,6,7 | In/Output | 40    | XTAL2           | Crystal, Osc. Clock    | Output    |
| 17-21 | P10-P14 | Port 1 pin 0,1,2,3,4 | In/Output | 41    | XTAL1           | Crystal, Osc. Clock    | Input     |
| 22    | /SYNC   | Synchronize Pin      | Output    | 42    | P37             | Port 3 pin 7           | Output    |
| 23-25 | P15-P17 | Port 1 pin 5,6,7     | In/Output | 43    | P30             | Port 3 pin 0           | Input     |
|       |         |                      |           | 44    | SCLK            | System Clock           | Output    |



**Figure 6. 48-Pin VQFP Package**

**Table 4. 48-Pin VQFP Pin Identification**

| No    | Symbol  | Function             | Direction | No    | Symbol          | Function               | Direction |
|-------|---------|----------------------|-----------|-------|-----------------|------------------------|-----------|
| 1     | N/C     | Not Connected        | Input     | 25    | N/C             | Not Connected          | Input     |
| 2     | /RESET  | Reset                | Input     | 26-28 | P15-P17         | Port 1 pin 5,6,7       | In/Output |
| 3     | R/W     | Read/Write           | Output    | 29    | F34             | Port 3 pin 4           | Output    |
| 4     | /DS     | Data Strobe          | Output    | 30    | F33             | Port 3 pin 33          | Input     |
| 5     | /AS     | Address Strobe       | Output    | 31-35 | P20-P24         | Port 2 pin 0,1,2,3,4   | In/Output |
| 6     | P35     | Port 3 pin 5         | Input     | 36    | N/C             | Not Connected (20 MHz) | Input     |
| 7     | GND     | Ground GND           | Input     |       | /WAIT           | WAIT (25 or 33 MHz)    | Input     |
| 8     | P32     | Port 3 pin 2         | Input     | 37-39 | P25-P27         | Port 2 pin 5,6,7       | In/Output |
| 9-11  | P00-P02 | Port 0 pin 3,4,5,6   | In/Output | 40    | F31             | Port 3 pin 1           | Input     |
| 12    | IACK    | Int. Acknowledge     | Output    | 41    | P36             | Port 3 pin 6           | Output    |
| 13-16 | P03-P06 | Port 0 pin 3,4,5,6   | In/Output | 42    | N/C             | Not Connected          | Input     |
| 17    | N/C     | Not Connected        | Input     | 43    | V <sub>cc</sub> | Power Supply           | Input     |
| 18    | P07     | Port 0 pin 7         | In/Output | 44    | XTAL2           | Crystal, Osc. Clock    | Output    |
| 19-23 | P10-P14 | Port 1 pin 0,1,2,3,4 | In/Output | 45    | XTAL1           | Crystal, Osc. Clock    | Input     |
| 24    | /SYNC   | Synchronize Pin      | Output    | 46    | P37             | Port 3 pin 7           | Output    |
|       |         |                      |           | 47    | P30             | Port 3 pin 0           | Input     |
|       |         |                      |           | 48    | SCLK            | System Clock           | Output    |

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## PIN FUNCTIONS

**/DS.** (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

**/AS.** (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is via Port 1 for all external programs. When /RESET is asserted, /AS toggles. Memory address transfers are valid at the trailing edge of /AS.

**XTAL1, XTAL2.** *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

**R/W.** (output, read High/write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory. It is High when the MCU is reading from the external program or data memory.

**/RESET.** (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C93 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the 5<sup>th</sup> clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of 2TpC. When /RESET is deactivated, program execution begins at location 000CH. Reset time must be held Low for 50 ms or until V<sub>cc</sub> is stable, whichever is longer.

**SCLK.** *System Clock* (output). The internal system clock is available at this pin. Available in the PLCC, QFP and VQFP packages only.

**IACK.** *Interrupt Acknowledge* (output, active High). This output, when High, indicates that the Z86C93 is in an interrupt cycle. Available in the PLCC, QFP and VQFP packages only.

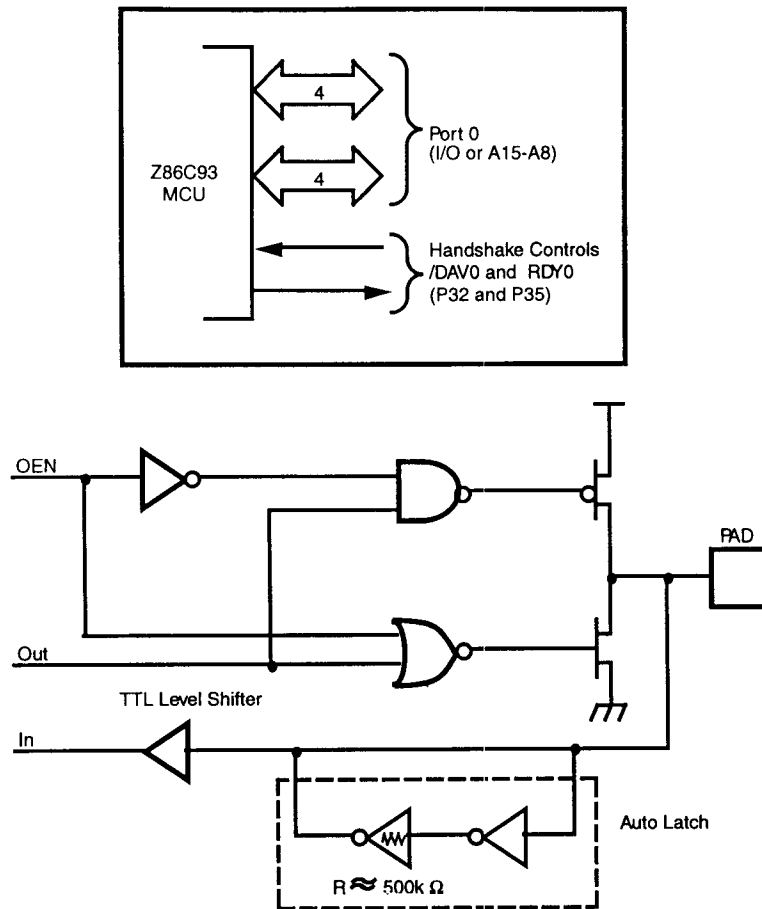
**/SYNC.** (output, active Low). This signal indicates the last clock cycle of the currently executing instruction. Available in the PLCC, QFP and VQFP packages only.

**/WAIT.** (input, active Low). Introduces asynchronous wait states into the external memory fetch cycle. When this input goes Low during an external memory access, the Z86C93 freezes the fetch cycle until this pin goes High. This pin is sampled after /DS goes Low; should be pulled up if not used. Available in the 25 MHz and 33 MHz devices only.

**Port 0 P00-P07.** Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble to be under handshake control. Port 0 comes up as A15-A8 Address lines after /RESET.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register. After a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 7). The /OEN (Output Enable) signal in Figure 7 is an internal signal.

The Auto Latch on Port 0 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.



**Figure 7. Port 0 Configuration**

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## PIN FUNCTIONS (Continued)

Port 1. (P10-P17). Port 1 is an 8-bit, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports for interfacing external memory (Figure 8).

If more than 256 external locations are required, Port 0 must output the additional lines.

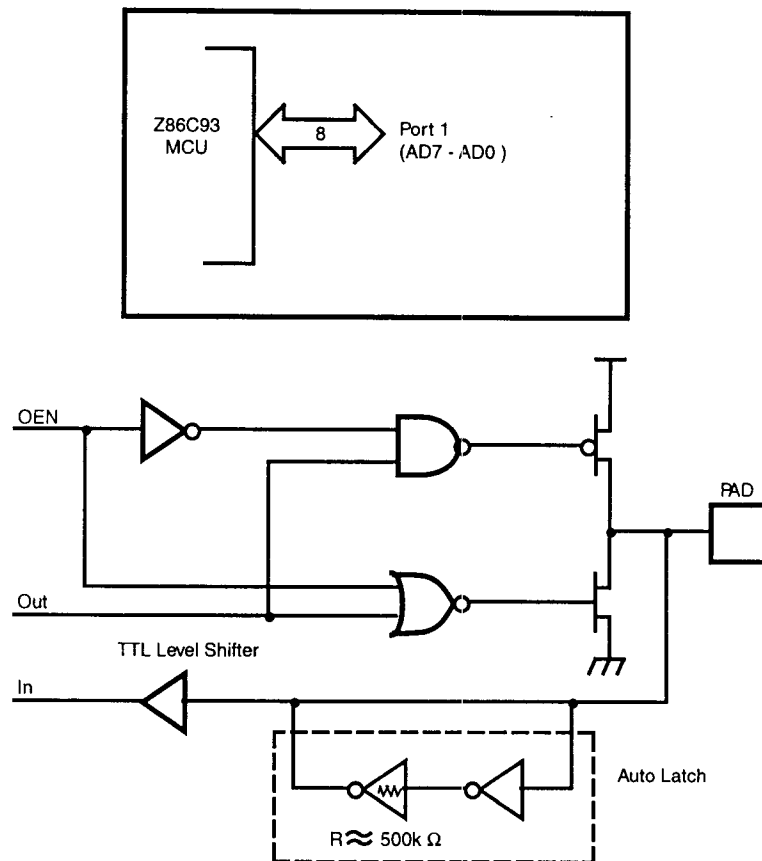


Figure 8. Port 1 Configuration

Port 2. (P20-P27). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal

assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 9).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

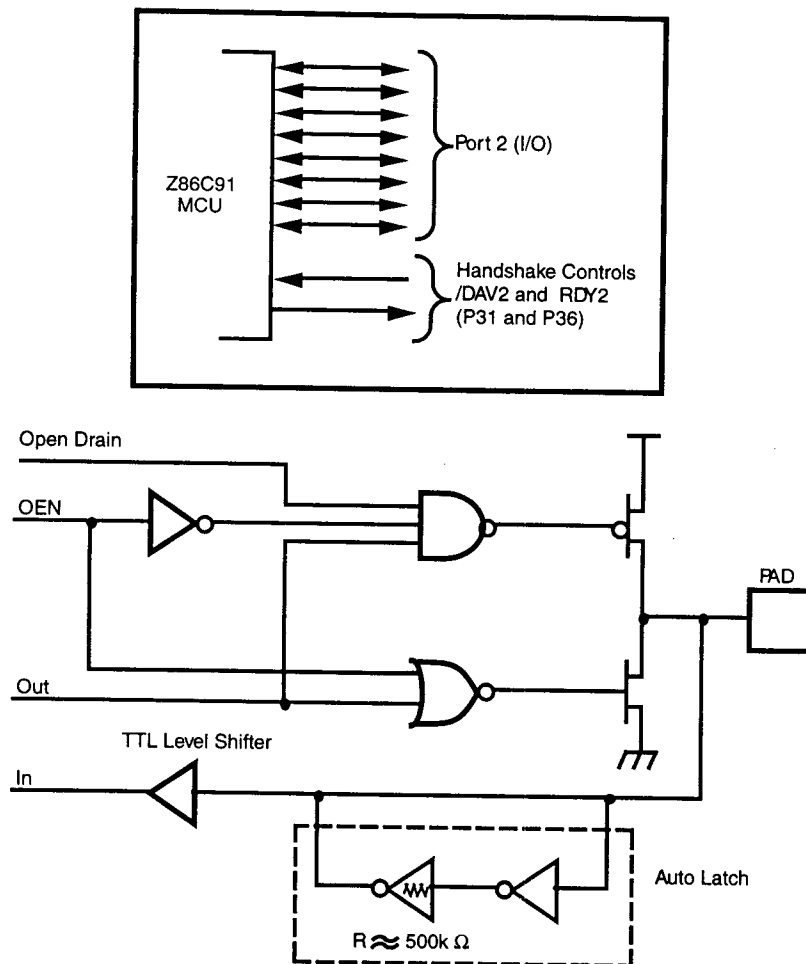


Figure 9. Port 2 Configuration

Port 3 P30-P37. Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output ports. These eight I/O lines have four fixed (P30-P33) input and four fixed (P34-P37) output

ports. Port 3 pins P30 and P37 when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10 and Table 5).

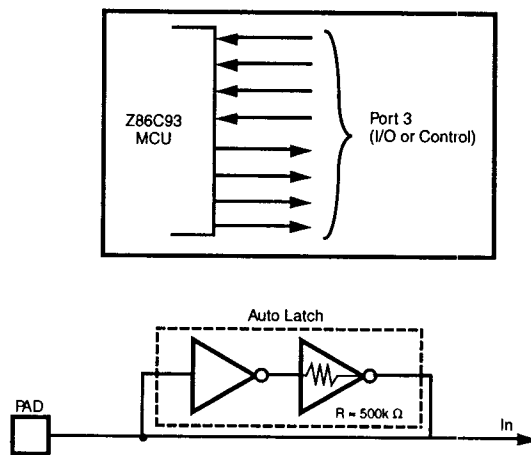


Figure 10. Port 3 Configuration

Table 5. Port 3 Pin Assignments

| Pin # | I/O | CTC1      | Int. | P0HS | P2HS | UART       | Ext. |
|-------|-----|-----------|------|------|------|------------|------|
| P30   | In  | $T_{IN}$  | IRQ3 | D/R  | D/R  | Serial In  |      |
| P31   | In  |           | IRQ2 |      |      |            |      |
| P32   | In  |           | IRQ0 |      |      |            |      |
| P33   | In  |           | IRQ1 |      |      |            |      |
| P34   | Out | $T_{OUT}$ |      | R/D  | R/D  | Serial Out | DM   |
| P35   | Out |           |      |      |      |            |      |
| P36   | Out |           |      |      |      |            |      |
| P37   | Out |           |      |      |      |            |      |

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals ( $T_{IN}$  and  $T_{OUT}$ ), and Data Memory Select (/DM).

Port 3 lines P30 and P37 can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer 0.

The Z86C93 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted,

regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

The Auto Latch on Port 3 puts a valid CMOS level on all CMOS inputs that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level rather than a floating node reduces excessive supply current flow in the input buffer.

## PIN FUNCTIONS (Continued)

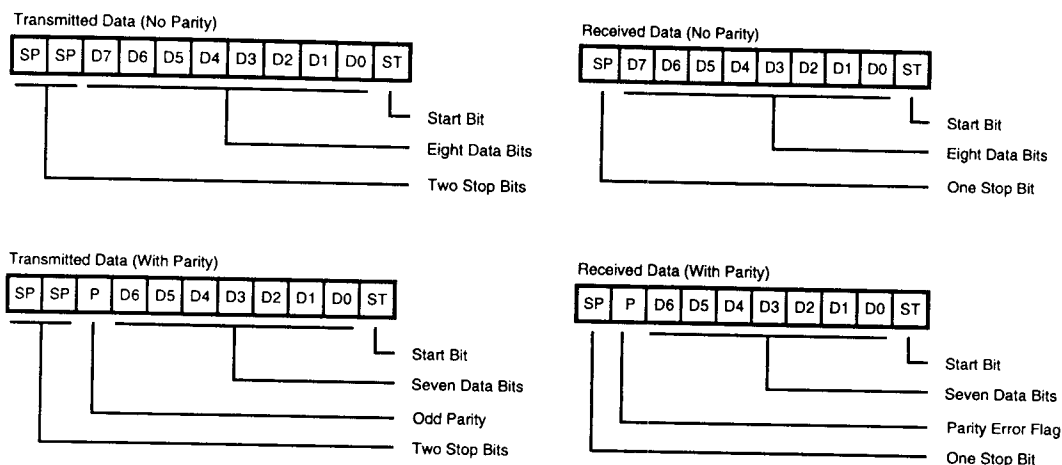


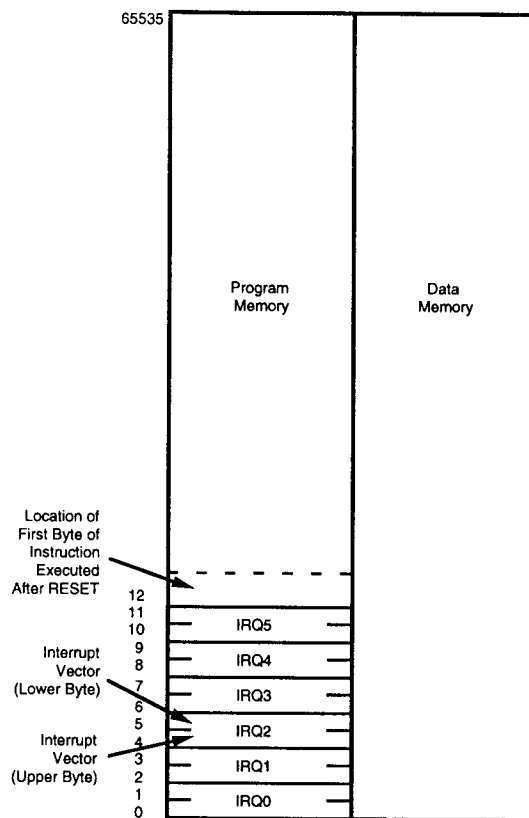
Figure 11. Serial Data Formats

## ADDRESS SPACE

**Program Memory.** The Z86C93 can address up to 64 Kbytes of external program memory. Program execution begins at external location 000CH after a reset.

**Data Memory.** The Z96C93 can address up to 64 Kbytes of external data memory. External data memory is included with, or separated from, the external program memory

space. /DM, an optional I/O function that can be programmed to appear on pin P34 is used to distinguish between data and program memory space (Figure 12). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.



**Figure 12. Program and Data Memory Configuration**

**Expanded Register File.** The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area (Figure 13). The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 14). The registers that are used in the multiply/divide unit reside in the Expanded Register File at Bank E and those for the additional timer control words reside in Bank D. The rest of the Expanded Register is not physically implemented and is open for future expansion.

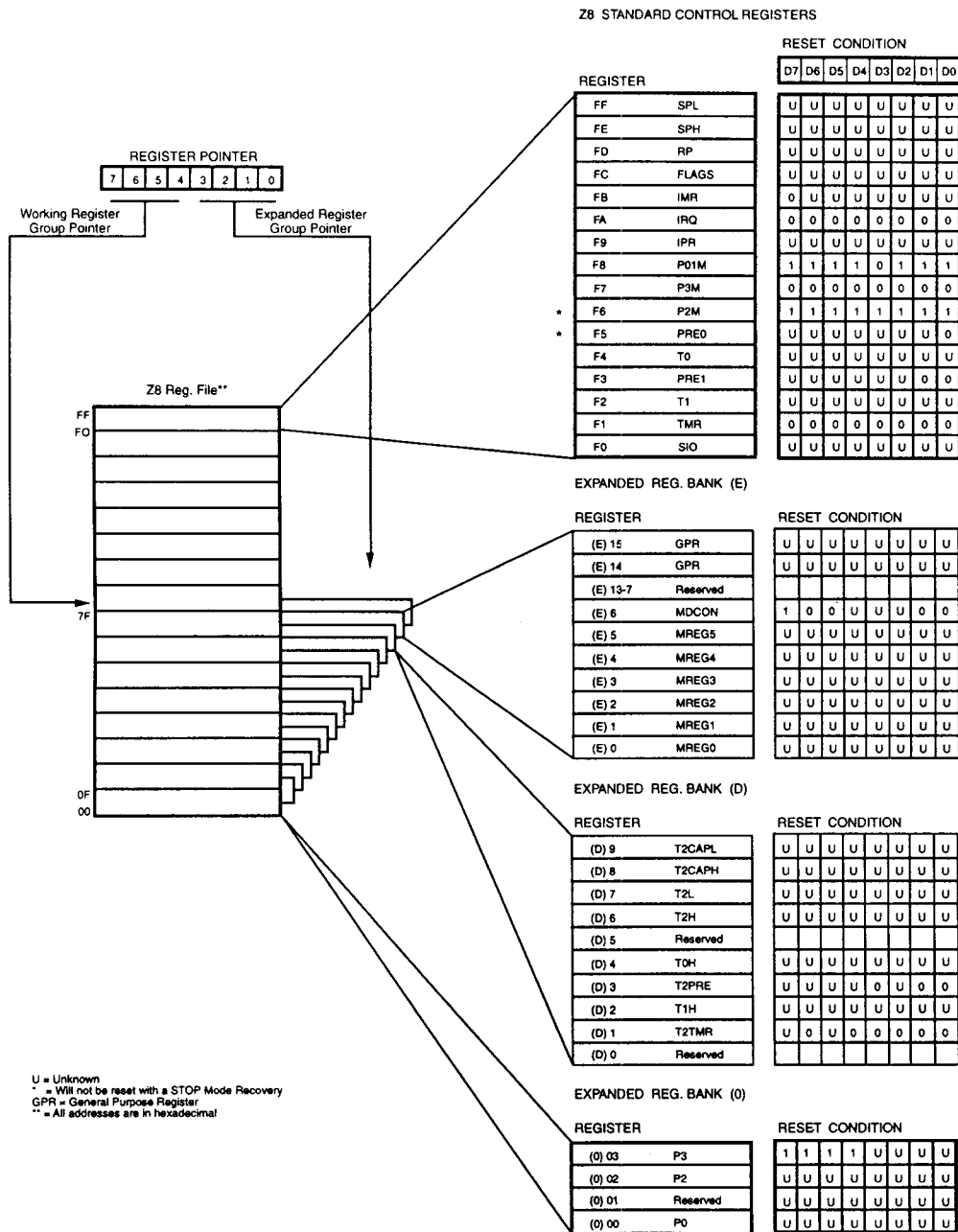
**Register File.** The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control

and status registers. The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C93 also allows short 4-bit register addressing using the Register Pointer (Figure 15). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

**Note:** Register Group E0-EF can only be accessed through working registers and indirect addressing modes.

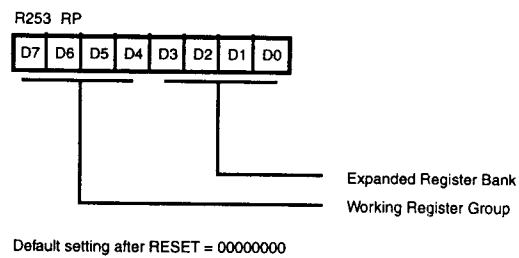
**Stack.** The Z86C93 has a 16-bit Stack Pointer (R254-R255), used for external stack, that resides anywhere in the data memory. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH, Bits 8-15) can be used as a general-purpose register when using internal stack only.

## ADDRESS SPACE (Continued)

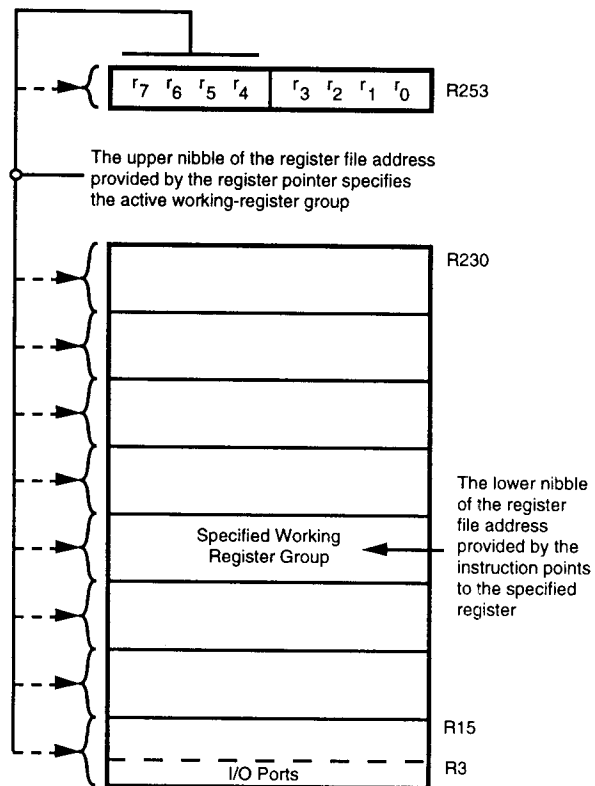


U = Unknown  
 \* = Will not be reset with a STOP Mode Recovery  
 GPR = General Purpose Register  
 \*\* = All addresses are in hexadecimal

Figure 13. Register File



**Figure 14. Register Pointer Register**



**Figure 15. Register Pointer**

## FUNCTIONAL DESCRIPTION

This section breaks down the Z86C93 into its main functional parts.

### Multiply/Divide Unit

The Multiply/Divide unit describes the basic features, implementation details of the interface between the Z8 and the multiply/divide unit.

Basic features:

- 16-bit by 16-bit multiply with 32-bit product
- 32-bit by 16-bit divide with 16-bit quotient and 16-bit remainder
- Unsigned integer data format
- Simple interface to Z8

**Interface to Z8.** The following is a brief description of the register mapping in the multiply/divide unit and its interface to the Z8 (Figure 16).

The multiply/divide unit is interfaced like a peripheral. The only addressing mode available with the peripheral interface is register addressing. In other words, all of the operands are in the respective registers before a multiplication/division can start.

**Register mapping.** The registers used in the multiply/divide unit are mapped onto the expanded register file in Bank E. The exact register locations used are shown below.

| REGISTER | ADDRESS |
|----------|---------|
| MREG0    | (E) 00  |
| MREG1    | (E) 01  |
| MREG2    | (E) 02  |
| MREG3    | (E) 03  |
| MREG4    | (E) 04  |
| MREG5    | (E) 05  |
| MDCON    | (E) 06  |
| GPR      | (E) 14  |
| GPR      | (E) 15  |

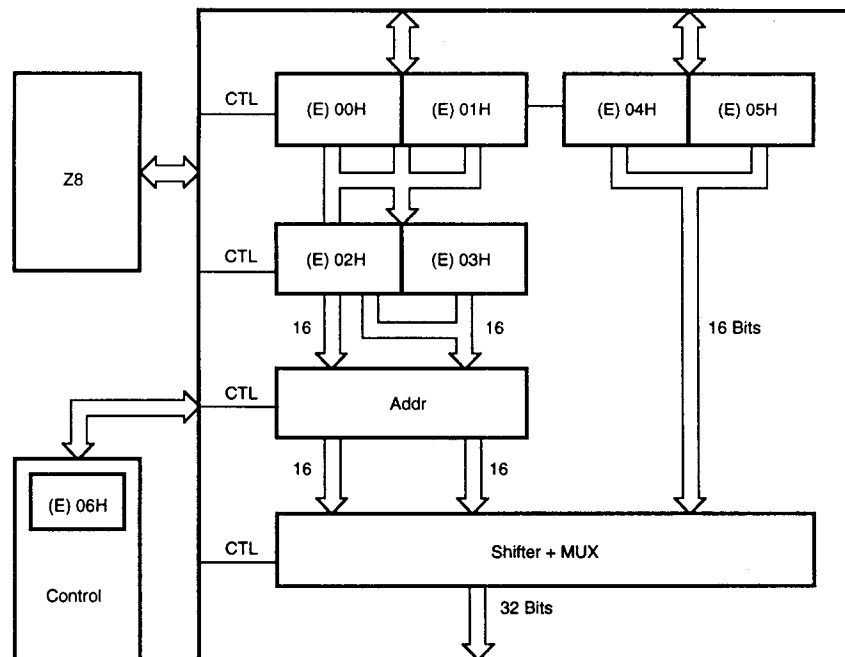


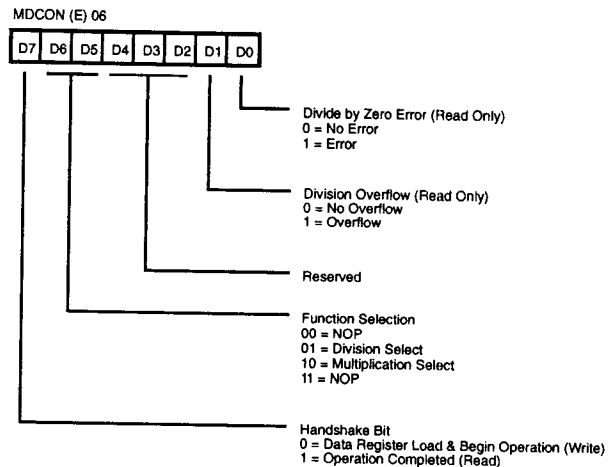
Figure 16. Multiply/Divide Unit Block Diagram

**Register allocation.** The following is the register allocation during multiplication.

|                                  |       |
|----------------------------------|-------|
| Multiplier high byte             | MREG2 |
| Multiplier low byte              | MREG3 |
| Multiplicand high byte           | MREG4 |
| Multiplicand low byte            | MREG5 |
| Result high byte of high word    | MREG0 |
| Result low byte of high word     | MREG1 |
| Result high byte of low word     | MREG2 |
| Result low byte of low word      | MREG3 |
| Multiply/Divide Control register | MDCON |

The following is the register allocation during division.

|                                    |       |
|------------------------------------|-------|
| High byte of high word of dividend | MREG0 |
| Low byte of high word of dividend  | MREG1 |
| High byte of low word of dividend  | MREG2 |
| Low byte of low word of dividend   | MREG3 |
| High byte of divisor               | MREG4 |
| Low byte of divisor                | MREG5 |
| High byte of remainder             | MREG0 |
| Low byte of remainder              | MREG1 |
| High byte of quotient              | MREG2 |
| Low byte of quotient               | MREG3 |
| Multiply/Divide Control register   | MDCON |



**Figure 17. Multiply/Divide Control Register (MDCON)**

**Control register.** The MDCON (Multiply/Divide Control Register) is used to interface with the multiply/divide unit (Figure 16). Specific functions of various bits in the control register are given below.

**DONE bit (D7).** This bit is a handshake bit between the math unit and the external world. On power up, this bit is set to 1 to indicate that the math unit has completed the previous operation and is ready to perform the next operation.

Before starting a new multiply/divide operation, this bit should be reset to 0 by the processor/programmer. This indicates that all the data registers have been loaded and the math unit can now begin a multiply/divide operation. During the process of multiplication or division, this bit is write-protected. Once the math unit completes its operation it sets this bit to indicate the completion of operation. The processor/programmer can then read the result.

**MULSL. Multiply Select (D6).** If this bit is set to 1, it indicates a multiply operation directive. Like the DONE bit, this bit is also write-protected during math unit operation and is reset to 0 by the math unit upon starting of the multiply/divide operation.

**DIVSL. Division Select (D5).** Similar to D6, D5 starts a division operation.

**D4-D2. Reserved.**

**DIVOVF. Division Overflow (D1).** This bit indicates an overflow during the division process. Division overflow occurs when the high word of the dividend is greater than or equal to the divisor. This bit is read only. When set to 1, it indicates overflow error.

---

## FUNCTIONAL DESCRIPTION (Continued)

**DIVZR. Division by Zero (D0).** When set to 1, this indicates an error of division by 0. This bit is read only.

Example:

Upon reset, the status of the MDCON register is 100uuu00b (D7 to D0).

u = Undefined  
x = Irrelevant  
b = Binary

If multiplication operation is desired, the MDCON register is set to 010xxxxb.

If the MDCON register is READ during multiplication, it would have a value of 000uuu00b.

Upon completion of multiplication, the result of the MDCON register is 100uuu00b.

If division operation is desired, the MDCON register is set to 001xxxxb.

During division operation, the register would contain 000uu??b (? - value depends on the DIVIDEND, DIVISOR).

Upon completion of division operation, the MDCON register contains 100uuu??b.

Note that once the multiplication/division operation starts, all data registers (MREG5 through MREG0) are write-protected and so are the writable bits of the MDCON register. The write protection is released once the math unit operation is complete. However, the registers may be read at any time.

A multiplication sequence would look like:

1. Load multiplier and multiplicand.
2. Load MDCON register to start multiply operation.
3. Wait for the DONE bit of the MDCON register to be set to 1 and then read results.

Note that while the multiply/divide operation is in progress, the programmer can use the Z8 to do other things. Also, since the multiplication/division takes a fixed number of cycles, he can start reading the results before the DONE bit is set.

During a division operation, the error flag bits are set at the beginning of the division operation which means the flag bits can be checked by the Z8 while the division operation is being done.

The two general purpose registers can be used as scratch pad registers or as external data memory address pointers during an LDE instruction. MREG0 through MREG5, if not used for multiplication or division, can be used as general purpose registers.

**Performance of multiplication.** The actual multiplication takes 17 internal clock cycles. It is expected that the chip would run at a 10 MHz internal clock frequency (external clock divided by two). This results in an actual multiplication time (16-bit x 16-bit) of 1.7  $\mu$ s. If the time to load operands and read results is included:

Number of internal clock cycles to load 5 registers: 30  
Number of internal clock cycles to read 4 registers: 24

The total internal clock cycles to perform a multiplication is 71. This results in a net multiplication time of 7.1  $\mu$ s. Note that this would be the worst case. This assumes that all of the operands are loaded from the external world as opposed to some of the operands being already in place as a result of a previous operation whose destination register is one of the math unit registers.

**Performance of division.** The actual division needs 20 internal clock cycles. This translates to 2.0  $\mu$ s for the actual division at 10 MHz (internal clock speed). If the time to load operands and read results is included:

Number of internal clock cycles to load operands: 42  
Number of internal clock cycles to read results: 24

The total internal clock cycles to perform a division is 86. This translates to 8.6  $\mu$ s at 10 MHz.

### Counter/Timers

This section describes the enhanced features of the counter/timers (CTC) on the Z86C93. It contains the register mapping of CTC registers and the bit functions of the newly added Timer2 control register.

In a standard Z8, there are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only.

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers are cascaded by connecting the T0 output to the input of T1. Either T0 or T1 can be outputted via P36.

The following are the enhancements made to the counter/timer block on the Z86C93 (Figure 18):

- T0 counter length is extended to 16 bits. For example, T0 now has a 6-bit prescaler and 16-bit down counter.
- T1 counter length is extended to 16 bits. For example, T1 now has a 6-bit prescaler and 16-bit down counter.
- A new counter/timer T2 is added. T2 has a 4-bit prescaler and a 16-bit down counter with capture register.

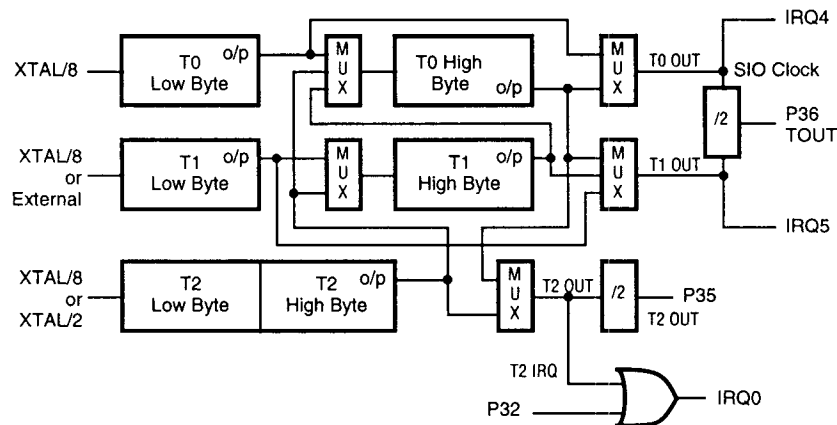
These three counters are cascadable as shown in Table 6. The result is that T2 may be extendable to 32 bits and T1 extendable to 24 bits. Bits 1 and 0 (CAS1 AND CAS0) of the T2 Prescaler Register (PRE2) determine the counter length.

**Table 6. Counter Length Configurations**

| CAS 1 | CAS0 | T0 | T1 | T2 |
|-------|------|----|----|----|
| 0     | 0    | 8  | 8  | 32 |
| 0     | 1    | 16 | 16 | 16 |
| 1     | 0    | 8  | 24 | 16 |
| 1     | 1    | 8  | 16 | 24 |

The controlling clock input to T2 is programmed to XTAL/2 or XTAL/8 (only when T2 counter length is 16 bits), which results in a resolution of 100 ns at an external XTAL clock speed of 20 MHz.

**Capture Register.** T2 has a 16-bit capture register associated with T2 HIGH BYTE and T2 LOW BYTE registers. The negative going transition on pin P33 enables the latching of the current T2 value (16 bits) into the capture register. The register mapping of the capture register is in Bank D (Figure 13). Note that the negative transition on P33 is capable of generating an interrupt. Also, the negative transition on P33 always latches the current T2 value into the capture register. There is no need for a control bit to enable/disable the latching; the capture register is read only.



**Figure 18. Counter/Timer Block Diagram**

## FUNCTIONAL DESCRIPTION (Continued)

### Operation

Except for the programmable down counter length and clock input, T2 is identical to T0.

T0 and T1 retain all their features except that now they are extendable interims of the down-counter length.

The output of T2, under program control, goes to an output pin (P35). Also, the interrupt generated by T2 is ORed with the interrupt request generated by P32. Note that the service routine then has to poll the T2 flag bit and also clear it (Bit 7 of T2 Timer Mode Register).

On power up, T0 and T1 are configured in the 8-bit down counter length mode (to be compatible with Z86C91) and T2 is in the 32-bit mode with its output disabled (no interrupt is generated and T2 output DOES NOT go to port pin P35).

The UART uses T0 for generating the bit clock. This means, while using UART, T0 should be in 8-bit mode. So, while using the UART there are only two independent timer/counters.

The counters are configured in the following manner:

| Timer | Mode   | Byte                                                             |
|-------|--------|------------------------------------------------------------------|
| T0    | 8-bit  | Low Byte (T0)                                                    |
| T0    | 16-bit | High Byte (T0) + Low Byte (T0)                                   |
| T1    | 8-bit  | Low Byte (T1)                                                    |
| T1    | 16-bit | High Byte (T1) + Low Byte (T1)                                   |
| T1    | 24-bit | High Byte (T0) + High Byte (T1) + Low Byte (T1)                  |
| T2    | 16-bit | High Byte (T2) + Low Byte (T2)                                   |
| T2    | 24-bit | High Byte (T0) + High Byte (T2) + Low Byte (T2)                  |
| T2    | 32-bit | High Byte (T0) + High Byte (T1) + High Byte (T2) + Low Byte (T2) |

Note that the T2 interrupt is logically ORed with P32 to generate IRQ0.

The T2 Timer Mode register is shown in Figure 19. Upon reaching end of count, bit 7 of this register is set to one. This bit IS NOT reset in hardware and it has to be cleared by the interrupt service routine.

T2 interrogates the state of the Count Mode Bit (D2) once it has counted down to its zero value. T2 then makes the decision to continue counting (Module N Mode) or stop (Single Pass Mode). Observe this functionality if attempting to modify the count mode prior to the end of count bit (D7) being set.

The register map of the new CTC registers is shown in Figure 13. T0 high byte and T1 high byte are at the same relative locations as their respective low bytes, but in a different register bank.

The T2 prescaler register is shown in Figure 19. Bits 1 and 0 of this register control the various cascade modes of the counters.

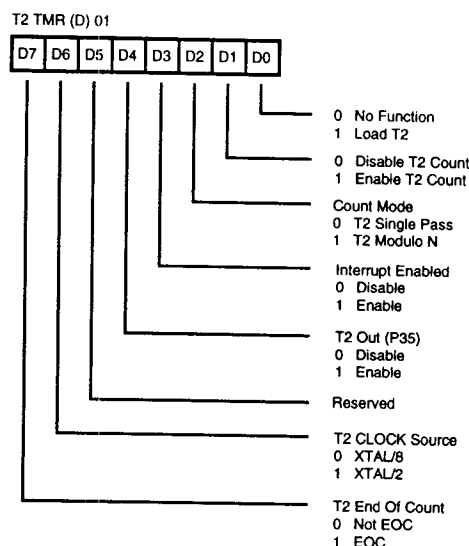


Figure 19. T2 Timer Mode Register (T2)

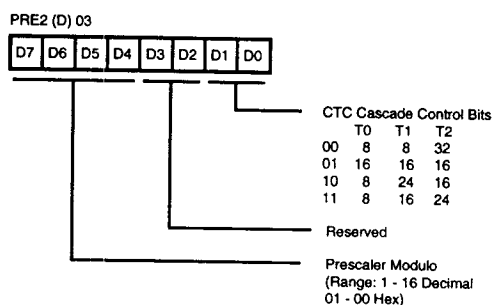


Figure 20. T2 Prescaler Register (PRE2)

## Interrupts

The Z86C93 has six different interrupts from nine different sources. The interrupts are maskable and prioritized. The nine sources are divided as follow: four sources are claimed by Port 3 lines P30-P33, one in Serial Out, one in Serial In, and three in the counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C93 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58<sup>th</sup> TpC cycle following the internal sample point, which corresponds to the 63<sup>rd</sup> TpC cycle following the external interrupt sample point.

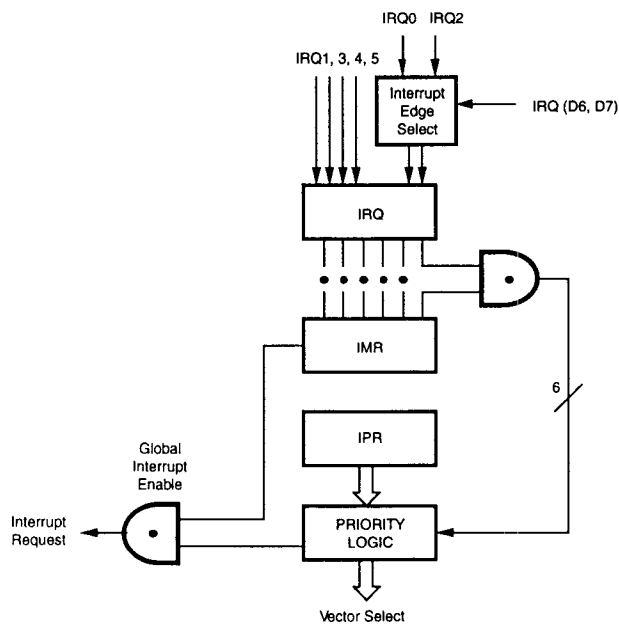


Figure 21. Interrupt Block Diagram

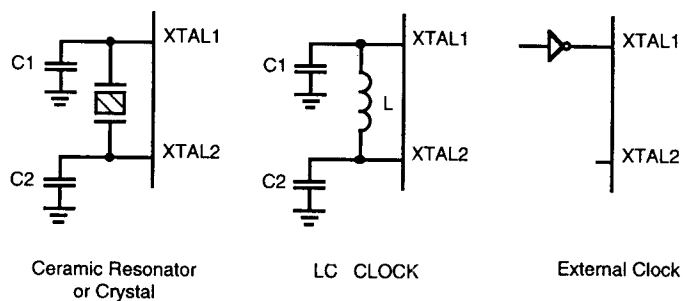
**Table 7. Interrupt Types, Sources, and Vectors**

| Name   | Source                       | Vector Location | Comments                                                 |
|--------|------------------------------|-----------------|----------------------------------------------------------|
| IRQ 0  | /DAV 0, P32, T2              | 0, 1            | External (P32), Programmable Rise or Fall Edge Triggered |
| IRQ 1, | P33                          | 2, 3            | External (P33), Fall Edge Triggered                      |
| IRQ 2  | /DAV 2, P31, T <sub>IN</sub> | 4, 5            | External (P31), Programmable Rise or Fall Edge Triggered |
| IRQ 3  | P30, Serial In               | 6, 7            | External (P30), Fall Edge Triggered                      |
| IRQ 4  | T0, Serial Out               | 8, 9            | Internal                                                 |
| IRQ 5  | T1                           | 10, 11          | Internal                                                 |

## Clock

The Z86C93 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1=Input, XTAL2=Output). The external clock levels

are not TTL. The crystal should be AT cut, 1 MHz to 25 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground (Figure 20).



**Figure 22. Oscillator Configuration**

## Power Down Modes

**HALT.** Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. During HALT mode, /DS, /AS and R/W are HIGH. The outputs retain their preview value, and the inputs are floating.

**STOP.** This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10  $\mu$ A or less. The STOP mode is terminated by a /RESET, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=OFFH) immediately before the appropriate sleep instruction, i.e.:

```
FF NOP ; clear the pipeline
6F STOP ; enter STOP mode
or
FF NOP ; clear the pipeline
7F HALT ; enter HALT mode
```

## ABSOLUTE MAXIMUM RATINGS

| Symbol    | Description       | Min  | Max  | Units |
|-----------|-------------------|------|------|-------|
| $V_{CC}$  | Supply Voltage*   | -0.3 | +7.0 | V     |
| $T_{STG}$ | Storage Temp      | -65  | +150 | C     |
| $T_A$     | Oper Ambient Temp | †    | †    | C     |

\* Voltages on all pins with respect to GND.

† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin Test Load Diagram (Figure 23).

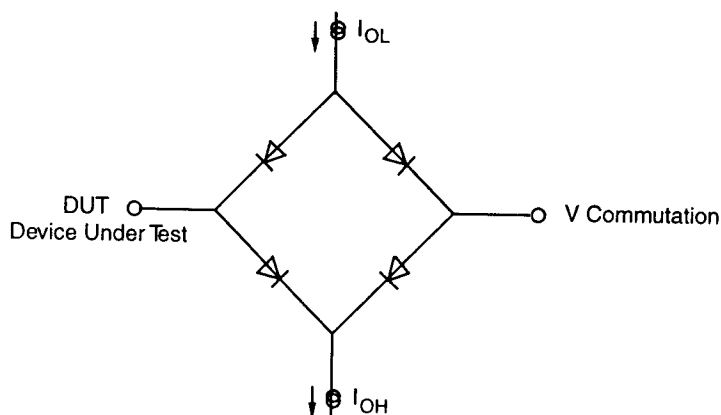


Figure 23. Test Load Diagram

## DC ELECTRICAL CHARACTERISTICS

$$V_{CC} = 3.3V \pm 10\%$$

| Sym       | Parameter                    | $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ |                     | Typical<br>at $25^\circ\text{C}$ | Units         | Conditions                                             |
|-----------|------------------------------|-----------------------------------------------|---------------------|----------------------------------|---------------|--------------------------------------------------------|
|           |                              | Min                                           | Max                 |                                  |               |                                                        |
|           | Max Input Voltage            |                                               | 7                   |                                  | V             | $I_{IN} = 250 \mu\text{A}$                             |
| $V_{CH}$  | Clock Input High Voltage     | $0.8 V_{CC}$                                  | $V_{CC}$            |                                  | V             | Driven by External Clock Generator                     |
| $V_{CL}$  | Clock Input Low Voltage      | -0.03                                         | $0.1 \times V_{CC}$ |                                  | V             | Driven by External Clock Generator                     |
| $V_{IH}$  | Input High Voltage           | $0.7 \times V_{CC}$                           | $V_{CC}$            |                                  | V             |                                                        |
| $V_{IL}$  | Input Low Voltage            | -0.3                                          | $0.1 \times V_{CC}$ |                                  | V             |                                                        |
| $V_{OH}$  | Output High Voltage          | 1.8                                           |                     |                                  | V             | $I_{OH} = -1.0 \text{ mA}$                             |
| $V_{OHI}$ | Output High Voltage          | $V_{CC} - 100\text{mV}$                       |                     |                                  | V             | $I_{OH} = -100 \mu\text{A}$                            |
| $V_{OL}$  | Output Low Voltage           |                                               | 0.4                 |                                  | V             | $I_{OL} = +1.0 \text{ mA}$                             |
| $V_{RH}$  | Reset Input High Voltage     | $0.8 \times V_{CC}$                           | $V_{CC}$            |                                  | V             |                                                        |
| $V_{RL}$  | Reset Input Low Voltage      | -0.03                                         | $0.1 \times V_{CC}$ |                                  | V             |                                                        |
| $I_{IL}$  | Input Leakage                | -2                                            | 2                   |                                  | $\mu\text{A}$ | Test at 0V, $V_{CC}$                                   |
| $I_{OL}$  | Output Leakage               | -2                                            | 2                   |                                  | $\mu\text{A}$ | Test at 0V, $V_{CC}$                                   |
| $I_{IR}$  | Reset Input Current          |                                               | -80                 |                                  | $\mu\text{A}$ | $V_{RL} = 0\text{V}$                                   |
| $I_{CC}$  | Supply Current               |                                               | 30                  | 20                               | mA            | @ 25 MHz [1]                                           |
| $I_{CC1}$ | Stand By Current (HALT Mode) |                                               | 12                  | 8                                | mA            | HALT Mode $V_{IN} = 0\text{V}$ , $V_{CC}$ @ 25 MHz [1] |
| $I_{CC2}$ | Stand By Current (HALT Mode) |                                               | 8                   | 1                                | $\mu\text{A}$ | STOP Mode $V_{IN} = 0\text{V}$ , $V_{CC}$ [1]          |
| $I_{AL}$  | Auto Latch Low Current       | -10                                           | 10                  | 5                                | $\mu\text{A}$ |                                                        |

### Note:

[1] All inputs driven to 0V,  $V_{CC}$  and outputs floating.

## DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$

| Sym       | Parameter                   | $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ |          | Typical<br>at $25^\circ\text{C}$ | Units         | Conditions                                      |
|-----------|-----------------------------|-----------------------------------------------|----------|----------------------------------|---------------|-------------------------------------------------|
|           |                             | Min                                           | Max      |                                  |               |                                                 |
|           | Max Input Voltage           |                                               | 7        |                                  | V             | $I_{IN} = 250 \mu\text{A}$                      |
| $V_{CH}$  | Clock Input High Voltage    | 3.8                                           | $V_{CC}$ |                                  | V             | Driven by External Clock Generator              |
| $V_{CL}$  | Clock Input Low Voltage     | -0.03                                         | 0.8      |                                  | V             | Driven by External Clock Generator              |
| $V_{IH}$  | Input High Voltage          | 2.0                                           | $V_{CC}$ |                                  | V             |                                                 |
| $V_{IL}$  | Input Low Voltage           | -0.3                                          | 0.8      |                                  | V             |                                                 |
| $V_{OH}$  | Output High Voltage         | 2.4                                           |          |                                  | V             | $I_{OH} = -2.0 \text{ mA}$                      |
| $V_{OH}$  | Output High Voltage         | $V_{CC} - 100\text{mV}$                       |          |                                  | V             | $I_{OH} = -100 \mu\text{A}$                     |
| $V_{OL}$  | Output Low Voltage          |                                               | 0.4      |                                  | V             | $I_{OL} = +5 \text{ mA}$                        |
| $V_{RH}$  | Reset Input High Voltage    | 3.8                                           | $V_{CC}$ |                                  | V             |                                                 |
| $V_{RL}$  | Reset Input Low Voltage     | -0.03                                         | 0.8      |                                  | V             |                                                 |
| $I_{IL}$  | Input Leakage               | -2                                            | 2        |                                  | $\mu\text{A}$ | Test at 0V, $V_{CC}$                            |
| $I_{OL}$  | Output Leakage              | -2                                            | 2        |                                  | $\mu\text{A}$ | Test at 0V, $V_{CC}$                            |
| $I_{IR}$  | Reset Input Current         |                                               | -80      |                                  | $\mu\text{A}$ | $V_{RL} = 0V$                                   |
| $I_{CC}$  | Supply Current              |                                               | 55       | 35                               | mA            | @ 33 MHz [1]                                    |
|           |                             |                                               | 40       | 25                               | mA            | @ 25 MHz [1]                                    |
|           |                             |                                               | 30       | 20                               | mA            | @ 20 MHz [1]                                    |
| $I_{CC1}$ | Standby Current (HALT Mode) |                                               | 15       | 9                                | mA            | HALT Mode $V_{IN} = 0V$ , $V_{CC}$ @ 25 MHz [1] |
|           |                             |                                               | 20       | 15                               |               | HALT Mode $V_{IN} = 0V$ , $V_{CC}$ @ 33 MHz [1] |
|           |                             |                                               | 12       | 7                                | mA            | HALT Mode $V_{IN} = 0V$ , $V_{CC}$ @ 20 MHz [1] |
| $I_{CC2}$ | Standby Current (STOP Mode) |                                               | 10       | 1                                | $\mu\text{A}$ | STOP Mode $V_{IN} = 0V$ , $V_{CC}$ [1]          |
| $I_{AL}$  | Auto Latch Current          | -16                                           | 16       | 5                                | $\mu\text{A}$ |                                                 |

### Note:

[1] All inputs driven to 0V, or  $V_{CC}$  and outputs floating.

## AC CHARACTERISTICS

### External I/O or Memory Read/Write Timing Diagram

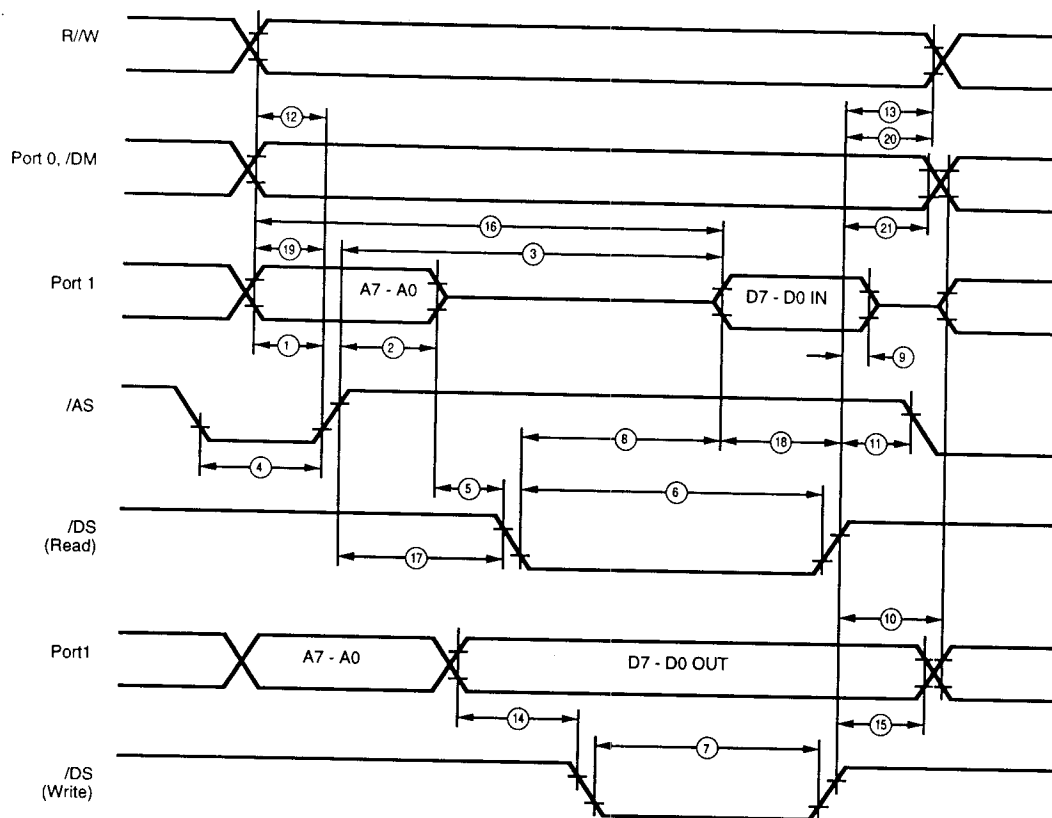


Figure 24. External I/O or Memory Read/Write Timing

## AC CHARACTERISTICS

External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

|    |            |                                         | T <sub>A</sub> = 0°C to +70°C |     |        |     |        |     |                                         |       |
|----|------------|-----------------------------------------|-------------------------------|-----|--------|-----|--------|-----|-----------------------------------------|-------|
| No | Sym        | Parameter                               | 33 MHz                        |     | 25 MHz |     | 20 MHz |     | Typical<br>V <sub>cc</sub> =5.0V @ 25°C | Units |
|    |            |                                         | Min                           | Max | Min    | Max | Min    | Max |                                         |       |
| 1  | TdA(AS)    | Address Valid To /AS Rise Delay         | 13                            |     | 22     |     | 26     |     |                                         | ns    |
| 2  | TdAS(A)    | /AS Rise To Address Hold Time           | 20                            |     | 25     |     | 28     |     |                                         | ns    |
| 3  | TdAS(DI)   | /AS Rise Data In Req'd Valid Delay      |                               | 90  |        | 130 |        | 160 |                                         | ns    |
| 4  | TwAS       | /AS Low Width                           | 20                            |     | 28     |     | 36     |     |                                         | ns    |
| 5  | TdAZ(DSR)  | Address Float To /DS (Read)             | 0                             |     | 0      |     | 0      |     |                                         | ns    |
| 6  | TwDSR      | /DS (Read) Low Width                    | 65                            |     | 100    |     | 130    |     |                                         | ns    |
| 7  | TwDSW      | /DS (Write) Low Width                   | 40                            |     | 65     |     | 75     |     |                                         | ns    |
| 8  | TdDSR(DI)  | /DS (Read) To Data in Req'd Valid Delay |                               | 30  |        | 78  |        | 100 |                                         | ns    |
| 9  | ThDSR(DI)  | /DS Rise (Read) to Data In Hold Time    | 0                             |     | 0      |     | 0      |     |                                         | ns    |
| 10 | TdDS(A)    | /DS Rise To Address Active Delay        | 25                            |     | 34     |     | 40     |     |                                         | ns    |
| 11 | TdDS(AS)   | /DS Rise To /AS Delay                   | 16                            |     | 30     |     | 36     |     |                                         | ns    |
| 12 | TdR/W(AS)  | R/W To /AS Rise Delay                   | 12                            |     | 26     |     | 32     |     |                                         | ns    |
| 13 | TdDS(R/W)  | /DS Rise To R/W Valid Delay             | 12                            |     | 30     |     | 36     |     |                                         | ns    |
| 14 | TdDO(DSW)  | Data Out To /DS (Write) Delay           | 12                            |     | 34     |     | 40     |     |                                         | ns    |
| 15 | ThDSW(DO)  | /DS Rise (Write) To Data Out Hold Time  | 12                            |     | 34     |     | 40     |     |                                         | ns    |
| 16 | TdA(DI)    | Address To Data In Req'd Valid Delay    |                               | 110 |        | 160 |        | 200 |                                         | ns    |
| 17 | TdAS(DSR)  | /AS Rise To /DS (Read) Delay            | 20                            |     | 40     |     | 48     |     |                                         | ns    |
| 18 | TaDI(DSR)  | Data In Set-up Time To /DS Rise Read    | 16                            |     | 30     |     | 36     |     |                                         | ns    |
| 19 | TdDM(AS)   | /DM To /AS Rise Delay                   | 10                            |     | 22     |     | 26     |     |                                         | ns    |
| 20 | TdDS(DM)   | /DS Rise To /DM Valid Delay             |                               |     |        |     |        |     | 34*                                     | ns    |
| 21 | ThDS(A)    | /DS Rise To Address Valid Hold Time     |                               |     |        |     |        |     | 34*                                     | ns    |
| 22 | TdXT(SCR)  | XTAL Falling to SCLK Rising             |                               |     |        |     |        |     | 20*                                     | ns    |
| 23 | TdXT(SCF)  | XTAL Falling to SCLK Falling            |                               |     |        |     |        |     | 23*                                     | ns    |
| 24 | TdXT(DSRF) | XTAL Falling to/DS Read Falling         |                               |     |        |     |        |     | 29*                                     | ns    |
| 25 | TdXT(DSRR) | XTAL Falling to /DS Read Rising         |                               |     |        |     |        |     | 29*                                     | ns    |
| 26 | TdXT(DSWF) | XTAL Falling to /DS Write Falling       |                               |     |        |     |        |     | 29*                                     | ns    |
| 27 | TdXT(DSWF) | XTAL Falling to /DS Write Rising        |                               |     |        |     |        |     | 29*                                     | ns    |
| 28 | TsW(XT)    | Wait Set-up Time                        |                               |     |        |     |        |     | 10*                                     | ns    |
| 29 | ThW(XT)    | Wait Hold Time                          |                               |     |        |     |        |     | 15*                                     | ns    |
| 30 | TwW        | Wait Width (One Wait Time)              |                               |     |        |     |        |     | 25*                                     | ns    |

### Notes:

When using extended memory timing add 2 TpC.

Timing numbers given are for minimum TpC.

\* Preliminary value to be characterized.

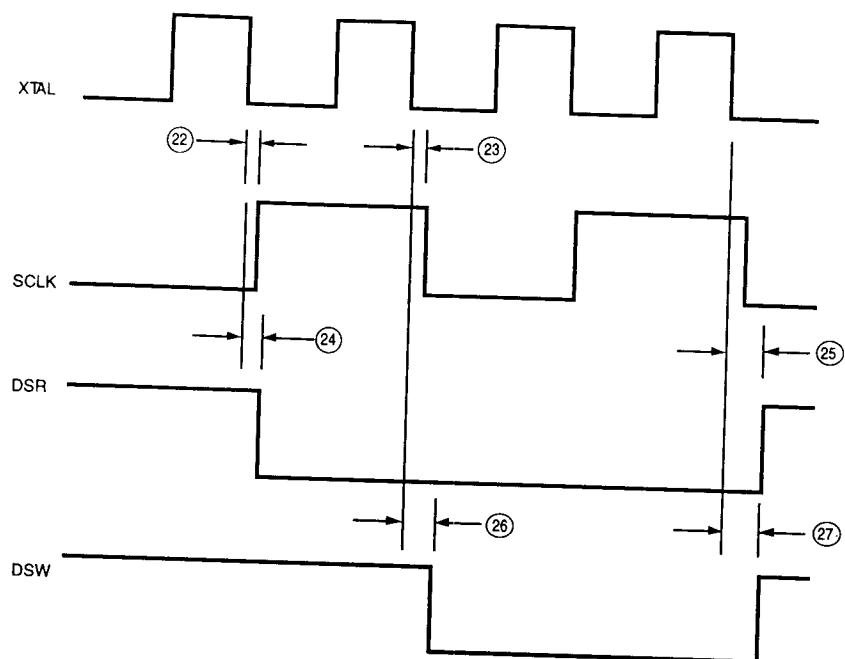


Figure 25. XTAL/SCLK To DSR and DSW Timing

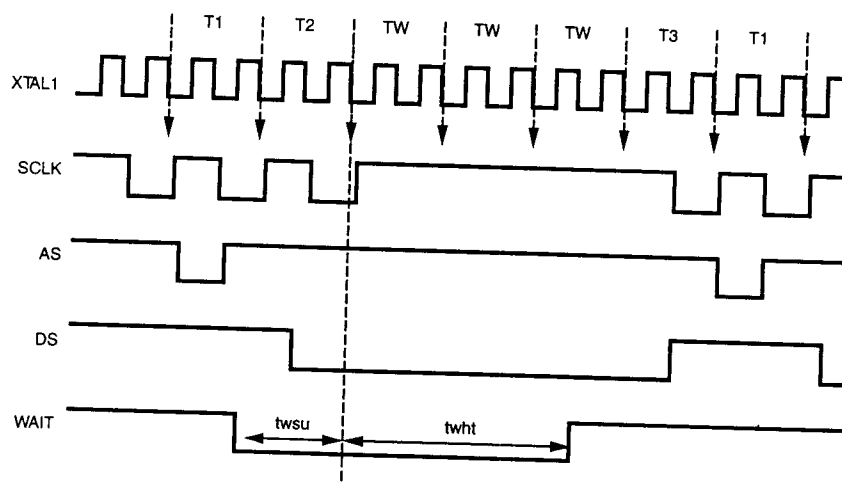


Figure 26. XTAL/SCLK To WAIT Timing  
(25 MHz Device Only)

## AC CHARACTERISTICS

### Additional Timing Diagram

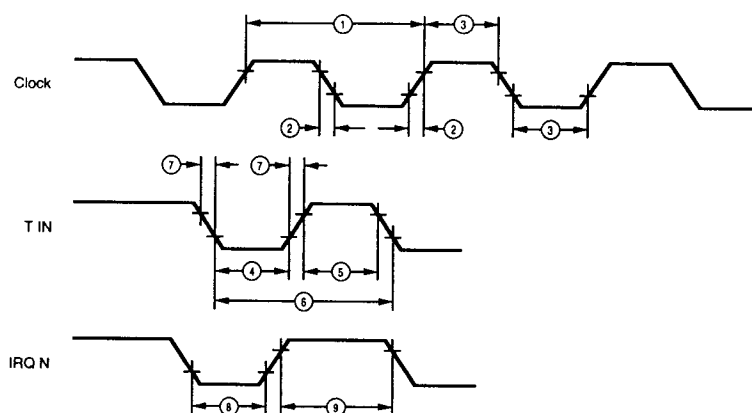


Figure 27. Additional Timing

## AC CHARACTERISTICS

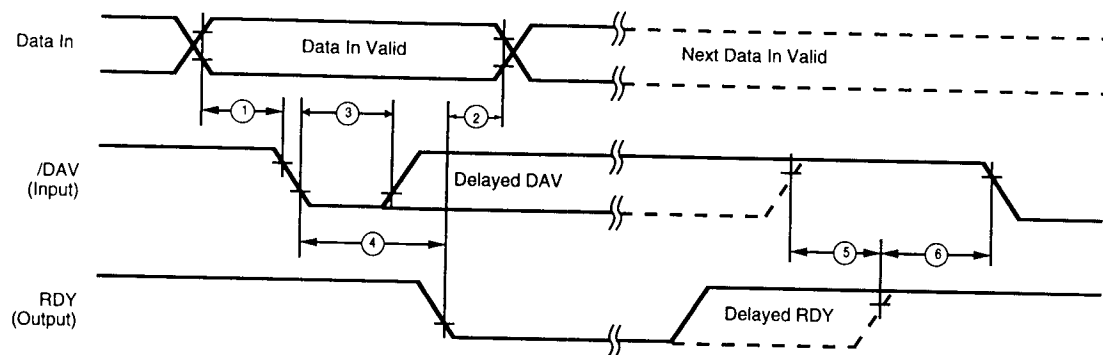
### Additional Timing Table

| No | Symbol      | Parameter                          | T <sub>A</sub> = 0°C to +70° C |      |        |      |        |      | Units | Notes |
|----|-------------|------------------------------------|--------------------------------|------|--------|------|--------|------|-------|-------|
|    |             |                                    | 33 MHz                         |      | 24 MHz |      | 20 MHz |      |       |       |
|    |             |                                    | Min                            | Max  | Min    | Max  | Min    | Max  |       |       |
| 1  | TpC         | Input Clock Period                 | 30                             | 1000 | 42     | 1000 | 50     | 1000 | ns    | [1]   |
| 2  | TrC,TfC     | Clock Input Rise & Fall Times      |                                | 5    |        | 10   |        | 10   | ns    | [1]   |
| 3  | TwC         | Input Clock Width                  | 10                             |      | 11     |      | 15     |      | ns    | [1]   |
| 4  | TwTinL      | Timer Input Low Width              | 75                             |      | 75     |      | 75     |      | ns    | [2]   |
| 5  | TwTinH      | Timer Input High Width             | 3TpC                           |      | 3TpC   |      | 3TpC   |      |       | [2]   |
| 6  | TpTin       | Timer Input Period                 | 8TpC                           |      | 8TpC   |      | 8TpC   |      |       | [2]   |
| 7  | TrTin,TfTin | Timer Input Rise & Fall Times      | 100                            |      | 100    |      | 100    |      | ns    | [2]   |
| 8A | TwIL        | Interrupt Request Input Low Times  | 70                             |      | 70     |      | 70     |      | ns    | [2,4] |
| 8B | TwIL        | Interrupt Request Input Low Times  | 5TpC                           |      | 5TpC   |      | 5TpC   |      |       | [2,5] |
| 9  | TwIH        | Interrupt Request Input High Times | 3TpC                           |      | 3TpC   |      | 3TpC   |      |       | [2,3] |

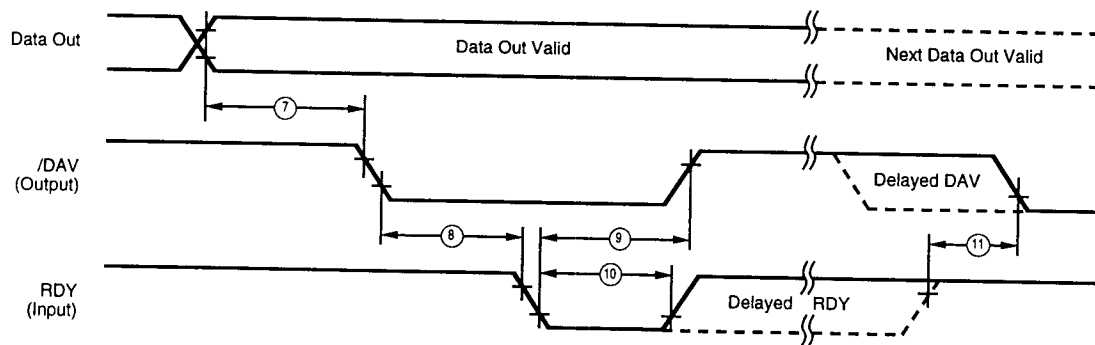
#### Notes:

- [1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- [2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- [3] Interrupt references request via Port 3.
- [4] Interrupt request via Port 3 (P31-P33).
- [5] Interrupt request via Port 30.

# **AC CHARACTERISTICS** Handshake Timing Diagrams



**Figure 28. Input Handshake Timing**



**Figure 29. Output Handshake Timing**

# AC CHARACTERISTICS Handshake Timing Table

| No | Symbol         | Parameter                  | T <sub>A</sub> = 0°C to +70°C |     | Units | Data Direction |
|----|----------------|----------------------------|-------------------------------|-----|-------|----------------|
|    |                |                            | Min                           | Max |       |                |
| 1  | TsDI(DAV)      | Data In Setup Time to /DAV | 0                             |     | ns    | In             |
| 2  | ThDI(DAV)      | RDY to Data In Hold Time   | 0                             |     | ns    | In             |
| 3  | TwDAV          | /DAV Width                 | 40                            |     | ns    | In             |
| 4  | TdDAVI(RDYf)   | /DAV to RDY Delay          |                               | 70  | ns    | In             |
| 5  | TdDAVI(RDYr)   | DAV Rise to RDY Wait Time  |                               | 40  | ns    | In             |
| 6  | TdRDYOr(DAVf)  | RDY Rise to DAV Delay      | 0                             |     | ns    | In             |
| 7  | TdDO(DAV)      | Data Out to DAV Delay      |                               | TpC | ns    | Out            |
| 8  | TdDAVO(RDYf)   | /DAV to RDY Delay          | 0                             |     | ns    | Out            |
| 9  | TdRDYIf(DAVOr) | RDY to /DAV Rise Delay     |                               | 70  | ns    | Out            |
| 10 | TwRDY          | RDY Width                  | 40                            |     | ns    | Out            |
| 11 | TdRDYIr(DAVOr) | RDY Rise to DAV Wait Time  |                               | 40  | ns    | Out            |

## EXPANDED REGISTER FILE CONTROL REGISTERS

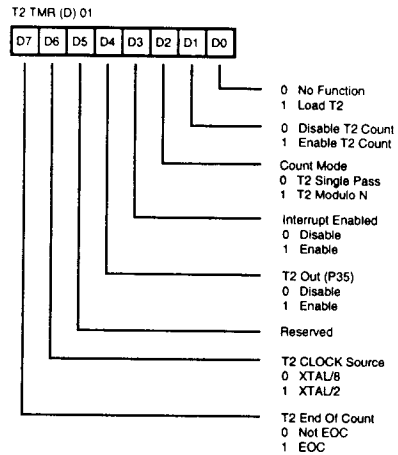


Figure 30. Timer 2 Mode Register (01H: Read/Write)

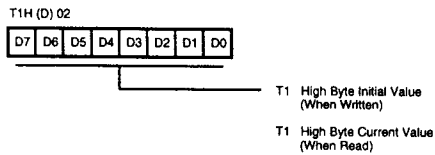


Figure 31. Counter Timer 1 Register High Byte (02H: Read/Write)

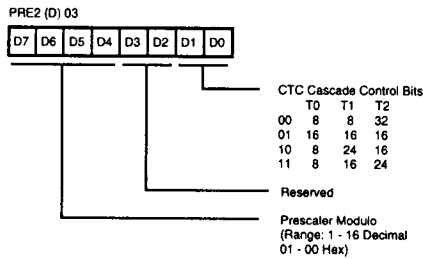


Figure 32. Prescaler 2 Register High Byte (03H: Write Only)

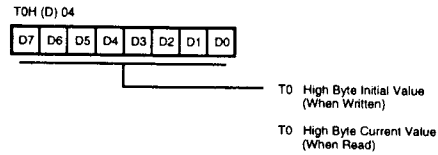


Figure 33. Counter Timer 0 Register High Byte (04H: Read/Write)

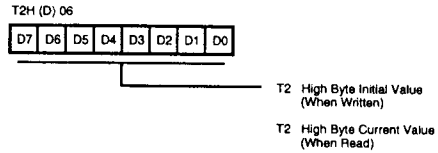


Figure 34. Counter Timer 2 Register High Byte (06H: Read/Write)

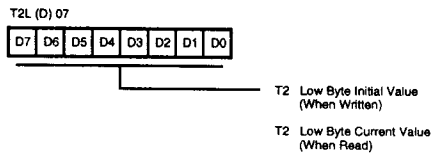


Figure 35. Counter Timer 2 Register Low Byte (07H: Read/Write)

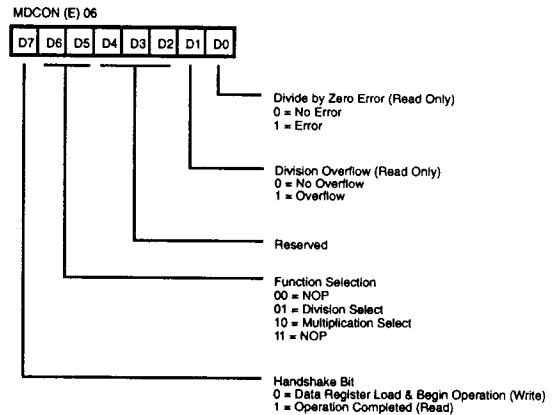
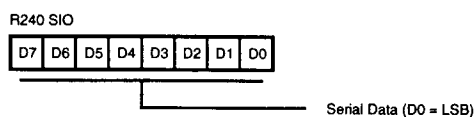
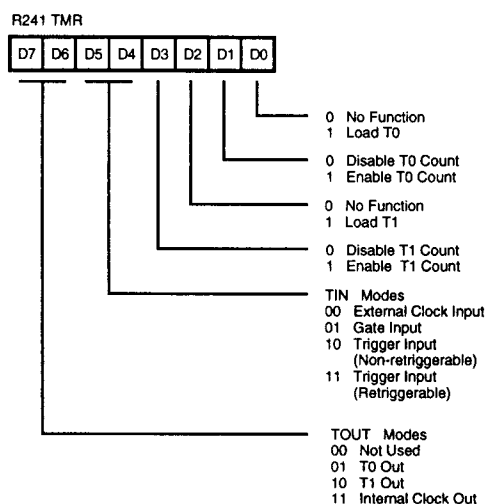


Figure 36. Multiply/Divide Control Register (MDCON)

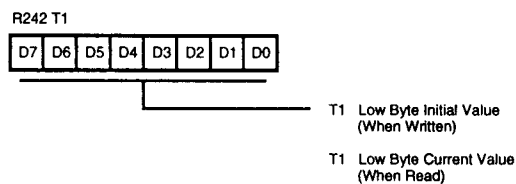
## Z8 CONTROL REGISTERS



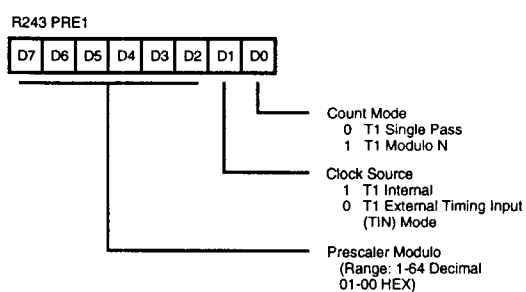
**Figure 37. Serial I/O Register**  
(F0H: Read/Write)



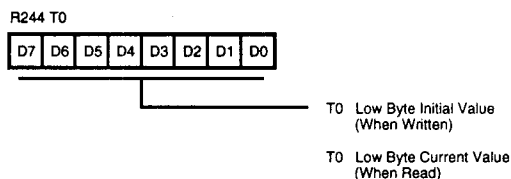
**Figure 38. Timer Mode Register**  
(F1H: Read/Write)



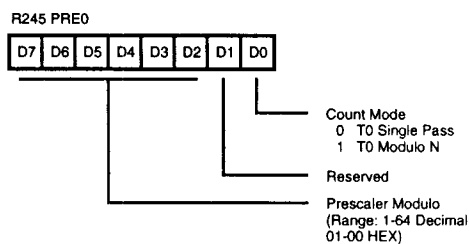
**Figure 39. Counter/Timer 1 Register**  
(F2H: Read/Write)



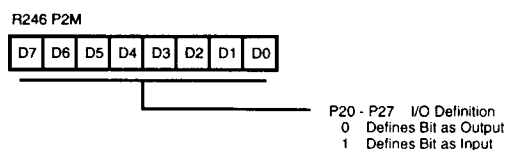
**Figure 40. Prescaler 1 Register**  
(F3H: Write Only)



**Figure 41. Counter/Timer 0 Register**  
(F4H: Read/Write)



**Figure 42. Prescaler 0 Register**  
(F5H: Write Only)



**Figure 43. Port 2 Mode Register**  
(F6H: Write Only)

## Z8 CONTROL REGISTERS (Continued)

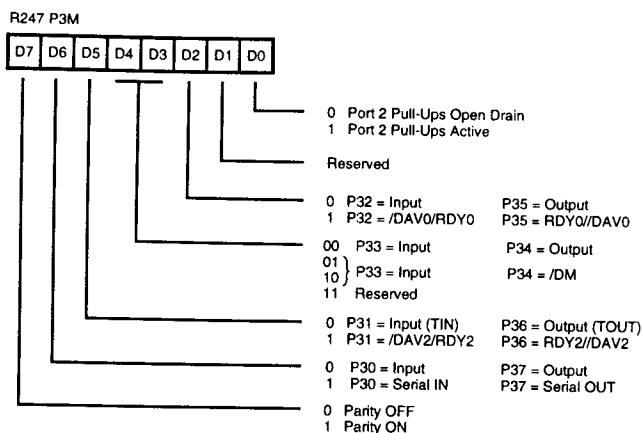


Figure 44. Port 3 Mode Register  
(F7H: Write Only)

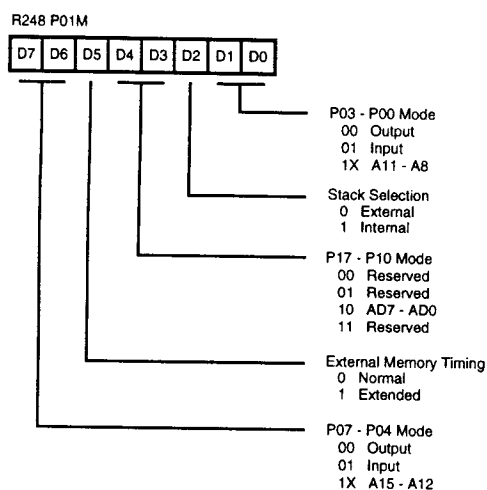


Figure 45. Ports 0 and 1 Mode Registers  
(F8H: Write Only)

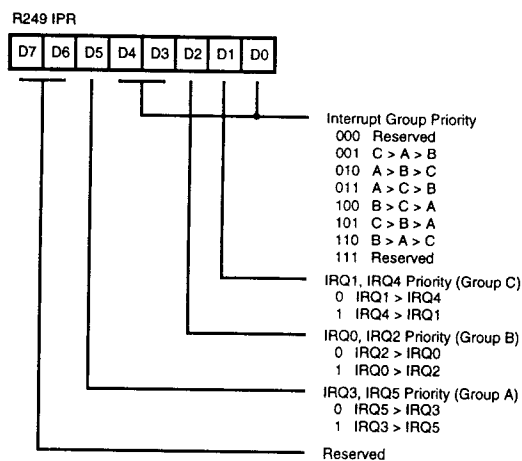
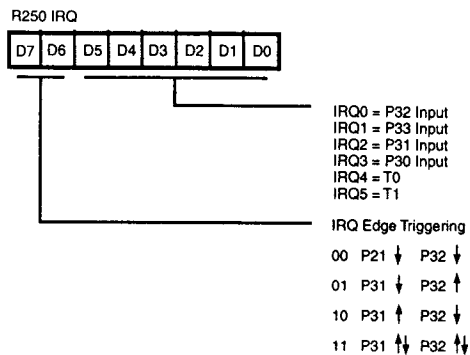
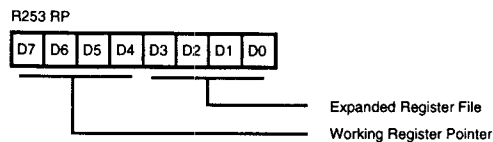


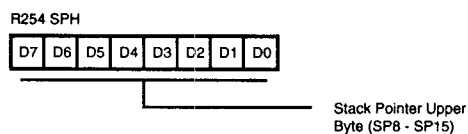
Figure 46. Interrupt Priority Register  
(F9H: Write Only)



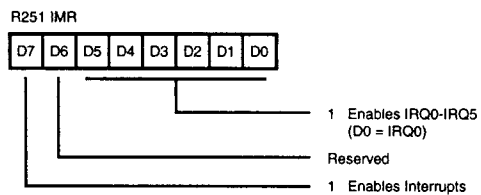
**Figure 47. Interrupt Request Register (FAH: Read/Write)**



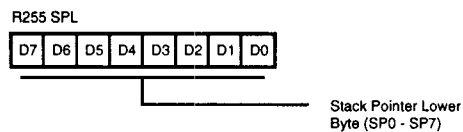
**Figure 50. Register Pointer (FDH: Read/Write)**



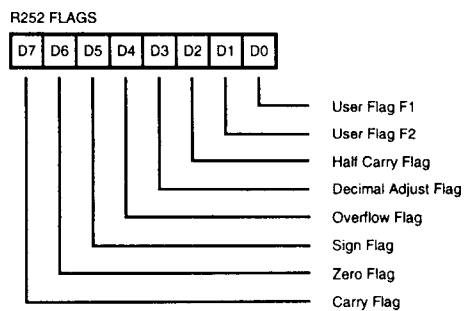
**Figure 51. Stack Pointer High (FEH: Read/Write)**



**Figure 48. Interrupt Mask Register (FBH: Read/Write)**



**Figure 52. Stack Pointer Low (FFH: Read/Write)**



**Figure 49. Flag Register (FCH: Read/Write)**

## INSTRUCTION SET NOTATION

**Addressing Modes.** The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

| Symbol | Meaning                                                          |
|--------|------------------------------------------------------------------|
| IRR    | Indirect register pair or indirect working-register pair address |
| Irr    | Indirect working-register pair only                              |
| X      | Indexed address                                                  |
| DA     | Direct address                                                   |
| RA     | Relative address                                                 |
| IM     | Immediate                                                        |
| R      | Register or working-register address                             |
| r      | Working-register address only                                    |
| IR     | Indirect-register or indirect working-register address           |
| Ir     | Indirect working-register address only                           |
| RR     | Register pair or working register pair address                   |

**Symbols.** The following symbols are used in describing the instruction set.

| Symbol | Meaning                              |
|--------|--------------------------------------|
| dst    | Destination location or contents     |
| src    | Source location or contents          |
| cc     | Condition code                       |
| @      | Indirect address prefix              |
| SP     | Stack Pointer                        |
| PC     | Program Counter                      |
| FLAGS  | Flag register (Control Register 252) |
| RP     | Register Pointer (R253)              |
| IMR    | Interrupt mask register (R251)       |

**Flags.** Control register (R252) contains the following six flags:

| Symbol | Meaning             |
|--------|---------------------|
| C      | Carry flag          |
| Z      | Zero flag           |
| S      | Sign flag           |
| V      | Overflow flag       |
| D      | Decimal-adjust flag |
| H      | Half-carry flag     |

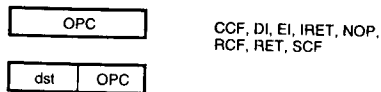
Affected flags are indicated by:

|   |                                     |
|---|-------------------------------------|
| 0 | Clear to zero                       |
| 1 | Set to one                          |
| * | Set to clear according to operation |
| - | Unaffected                          |
| x | Undefined                           |

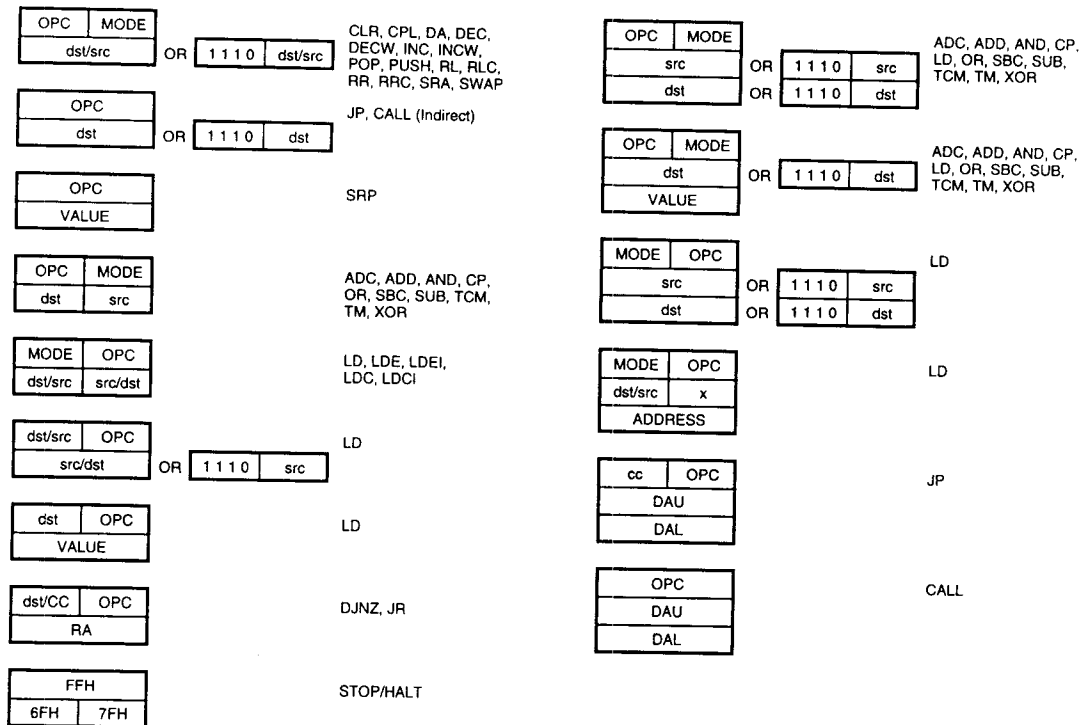
## CONDITION CODES

| Value | Mnemonic | Meaning                        | Flags Set             |
|-------|----------|--------------------------------|-----------------------|
| 1000  |          | Always True                    |                       |
| 0111  | C        | Carry                          | C = 1                 |
| 1111  | NC       | No Carry                       | C = 0                 |
| 0110  | Z        | Zero                           | Z = 1                 |
| 1110  | NZ       | Not Zero                       | Z = 0                 |
| 1101  | PL       | Plus                           | S = 0                 |
| 0101  | MI       | Minus                          | S = 1                 |
| 0100  | OV       | Overflow                       | V = 1                 |
| 1100  | NOV      | No Overflow                    | V = 0                 |
| 0110  | EQ       | Equal                          | Z = 1                 |
| 1110  | NE       | Not Equal                      | Z = 0                 |
| 1001  | GE       | Greater Than or Equal          | (S XOR V) = 0         |
| 0001  | LT       | Less than                      | (S XOR V) = 1         |
| 1010  | GT       | Greater Than                   | [Z OR (S XOR V)] = 0  |
| 0010  | LE       | Less Than or Equal             | [Z OR (S XOR V)] = 1  |
| 1111  | UGE      | Unsigned Greater Than or Equal | C = 0                 |
| 0111  | ULT      | Unsigned Less Than             | C = 1                 |
| 1011  | UGT      | Unsigned Greater Than          | (C = 0 AND Z = 0) = 1 |
| 0011  | ULE      | Unsigned Less Than or Equal    | (C OR Z) = 1          |
| 0000  |          | Never True                     |                       |

## INSTRUCTION FORMATS



### One-Byte Instructions



### Two-Byte Instructions

### Three-Byte Instructions

## INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " $\leftarrow$ ". For example:

$$\text{dst} \leftarrow \text{dst} + \text{src}$$

indicates that the source data is added to the destination data and the result is stored in the destination location. The

notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

$$\text{dst} (7)$$

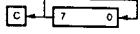
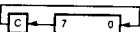
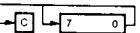
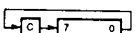
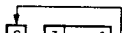
refers to bit 7 of the destination operand.

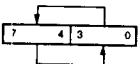
## INSTRUCTION SUMMARY (Continued)

| Instruction<br>and Operation                                                     | Address<br>Mode<br>dst src | Opcode<br>Byte (Hex) | Flags<br>Affected |   |   |   |   |   |  |
|----------------------------------------------------------------------------------|----------------------------|----------------------|-------------------|---|---|---|---|---|--|
|                                                                                  |                            |                      | C                 | Z | S | V | D | H |  |
| <b>ADC</b> dst, src<br>dst←dst + src + C                                         | †                          | 1[ ]                 | *                 | * | * | * | 0 | * |  |
| <b>ADD</b> dst, src<br>dst←dst + src                                             | †                          | 0[ ]                 | *                 | * | * | * | 0 | * |  |
| <b>AND</b> dst, src<br>dst←dst AND src                                           | †                          | 5[ ]                 | -                 | * | * | 0 | - | - |  |
| <b>CALL</b> dst<br>SP←SP - 2<br>@SP←PC,<br>PC←dst                                | DA<br>IRR                  | D6<br>D4             | -                 | - | - | - | - | - |  |
| <b>CCF</b><br>C←NOT C                                                            |                            | EF                   | *                 | - | - | - | - | - |  |
| <b>CLR</b> dst<br>dst←0                                                          | R<br>IR                    | B0<br>B1             | -                 | - | - | - | - | - |  |
| <b>COM</b> dst<br>dst←NOT dst                                                    | R<br>IR                    | 60<br>61             | -                 | * | * | 0 | - | - |  |
| <b>CP</b> dst, src<br>dst - src                                                  | †                          | A[ ]                 | *                 | * | * | * | - | - |  |
| <b>DA</b> dst<br>dst←DA dst                                                      | R<br>IR                    | 40<br>41             | *                 | * | * | X | - | - |  |
| <b>DEC</b> dst<br>dst←dst - 1                                                    | R<br>IR                    | 00<br>01             | -                 | * | * | * | - | - |  |
| <b>DECW</b> dst<br>dst←dst - 1                                                   | RR<br>IR                   | 80<br>81             | -                 | * | * | * | - | - |  |
| <b>DI</b><br>IMR(7)←0                                                            |                            | 8F                   | -                 | - | - | - | - | - |  |
| <b>DJNZ</b> r, dst<br>r←r - 1<br>if r ≠ 0<br>PC←PC + dst<br>Range: +127,<br>-128 | RA                         | rA<br>r = 0 - F      | -                 | - | - | - | - | - |  |
| <b>EI</b><br>IMR(7)←1                                                            |                            | 9F                   | -                 | - | - | - | - | - |  |
| <b>HALT</b>                                                                      |                            | 7F                   | -                 | - | - | - | - | - |  |

| Instruction<br>and Operation                                                | Address<br>Mode<br>dst src                                                | Opcode<br>Byte (Hex)                                                                    | Flags<br>Affected |   |   |   |   |   |  |
|-----------------------------------------------------------------------------|---------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|-------------------|---|---|---|---|---|--|
|                                                                             |                                                                           |                                                                                         | C                 | Z | S | V | D | H |  |
| <b>INC</b> dst<br>dst←dst + 1                                               | r<br>R<br>IR                                                              | rE<br>r = 0 - F<br>20<br>21                                                             | -                 | * | * | * | - | - |  |
| <b>INCW</b> dst<br>dst←dst + 1                                              | RR<br>IR                                                                  | A0<br>A1                                                                                | -                 | * | * | * | - | - |  |
| <b>IRET</b><br>FLAGS←@SP;<br>SP←SP + 1<br>PC←@SP;<br>SP←SP + 2;<br>IMR(7)←1 |                                                                           | BF                                                                                      | *                 | * | * | * | * | * |  |
| <b>JP</b> cc, dst<br>if cc is true<br>PC←dst                                | DA<br>IRR                                                                 | cD<br>c = 0 - F<br>30                                                                   | -                 | - | - | - | - | - |  |
| <b>JR</b> cc, dst<br>if cc is true,<br>PC←PC + dst<br>Range: +127,<br>-128  | RA                                                                        | cB<br>c = 0 - F                                                                         | -                 | - | - | - | - | - |  |
| <b>LD</b> dst, src<br>dst←src                                               | r<br>r<br>R<br>r<br>r<br>X<br>r<br>r<br>R<br>R<br>R<br>R<br>IR<br>IR<br>R | lm<br>rC<br>r8<br>r9<br>r = 0 - F<br>C7<br>D7<br>E3<br>F3<br>E4<br>E5<br>E6<br>E7<br>F5 | -                 | - | - | - | - | - |  |
| <b>LDC</b> dst, src                                                         | r<br>lrr                                                                  | C2                                                                                      | -                 | - | - | - | - | - |  |
| <b>LDCI</b> dst, src<br>dst←src<br>r←r + 1;<br>rr←rr + 1                    | lr<br>lrr                                                                 | C3                                                                                      | -                 | - | - | - | - | - |  |

# INSTRUCTION SUMMARY (Continued)

| Instruction<br>and Operation                                                                          | Address<br>Mode |     | Opcode<br>Byte (Hex) | Flags<br>Affected |   |   |   |   |   |   |
|-------------------------------------------------------------------------------------------------------|-----------------|-----|----------------------|-------------------|---|---|---|---|---|---|
|                                                                                                       | dst             | src |                      | C                 | Z | S | V | D | H |   |
| <b>NOP</b>                                                                                            |                 |     | FF                   | -                 | - | - | - | - | - | - |
| <b>OR</b> dst, src<br>dst ← dst OR src                                                                | †               |     | 4[ ]                 | -                 | * | * | 0 | - | - | - |
| <b>POP</b> dst<br>dst ← @SP;<br>SP ← SP + 1                                                           | R               |     | 50                   | -                 | - | - | - | - | - | - |
|                                                                                                       | IR              |     | 51                   | -                 | - | - | - | - | - | - |
| <b>PUSH</b> src<br>SP ← SP - 1;<br>@SP ← src                                                          | R               |     | 70                   | -                 | - | - | - | - | - | - |
|                                                                                                       | IR              |     | 71                   | -                 | - | - | - | - | - | - |
| <b>RCF</b><br>C ← 0                                                                                   |                 |     | CF                   | 0                 | - | - | - | - | - | - |
| <b>RET</b><br>PC ← @SP;<br>SP ← SP + 2                                                                |                 |     | AF                   | -                 | - | - | - | - | - | - |
| <b>RL</b> dst<br>    | R               |     | 90                   | *                 | * | * | * | - | - | - |
|                                                                                                       | IR              |     | 91                   | *                 | * | * | * | - | - | - |
| <b>RLC</b> dst<br>   | R               |     | 10                   | *                 | * | * | * | - | - | - |
|                                                                                                       | IR              |     | 11                   | *                 | * | * | * | - | - | - |
| <b>RRC</b> dst<br> | R               |     | E0                   | *                 | * | * | * | - | - | - |
|                                                                                                       | IR              |     | E1                   | *                 | * | * | * | - | - | - |
| <b>RRC</b> dst<br> | R               |     | C0                   | *                 | * | * | * | - | - | - |
|                                                                                                       | IR              |     | C1                   | *                 | * | * | * | - | - | - |
| <b>SBC</b> dst, src<br>dst ← dst ← src ← C                                                            | †               |     | 3[ ]                 | *                 | * | * | * | 1 | * | * |
| <b>SCF</b><br>C ← 1                                                                                   |                 |     | DF                   | 1                 | - | - | - | - | - | - |
| <b>SRA</b> dst<br> | R               |     | D0                   | *                 | * | * | 0 | - | - | - |
|                                                                                                       | IR              |     | D1                   | *                 | * | * | 0 | - | - | - |
| <b>SRP</b> src<br>RP ← src                                                                            |                 | Im  | 31                   | -                 | - | - | - | - | - | - |

| Instruction<br>and Operation                                                                          | Address<br>Mode |     | Opcode<br>Byte (Hex) | Flags<br>Affected |   |   |   |   |   |   |
|-------------------------------------------------------------------------------------------------------|-----------------|-----|----------------------|-------------------|---|---|---|---|---|---|
|                                                                                                       | dst             | src |                      | C                 | Z | S | V | D | H |   |
| <b>STOP</b>                                                                                           |                 |     | 6F                   | -                 | - | - | - | - | - | - |
| <b>SUB</b> dst, src<br>dst ← dst ← src                                                                | †               |     | 2[ ]                 | *                 | * | * | * | 1 | * | * |
| <b>SWAP</b> dst<br> | R               |     | F0                   | X                 | * | * | X | - | - | - |
|                                                                                                       | IR              |     | F1                   | X                 | * | * | X | - | - | - |
| <b>TCM</b> dst, src<br>(NOT dst)<br>AND src                                                           | †               |     | 6[ ]                 | -                 | * | * | 0 | - | - | - |
| <b>TM</b> dst, src<br>dst AND src                                                                     | †               |     | 7[ ]                 | -                 | * | * | 0 | - | - | - |
| <b>XOR</b> dst, src<br>dst ← dst<br>XOR src                                                           | †               |     | B[ ]                 | -                 | * | * | 0 | - | - | - |

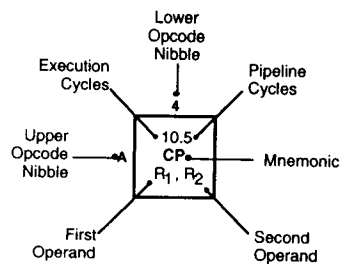
† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

| Address Mode |     | Lower<br>Opcode Nibble |
|--------------|-----|------------------------|
| dst          | src |                        |
| r            | r   | [2]                    |
| r            | Ir  | [3]                    |
| R            | R   | [4]                    |
| R            | IR  | [5]                    |
| R            | IM  | [6]                    |
| IR           | IM  | [7]                    |

# OPCODE MAP

|                    |   | Lower Nibble (Hex)    |                        |                        |                          |                       |                        |                       |                         |                     |                     |                           |                         |                     |                         |                  |              |
|--------------------|---|-----------------------|------------------------|------------------------|--------------------------|-----------------------|------------------------|-----------------------|-------------------------|---------------------|---------------------|---------------------------|-------------------------|---------------------|-------------------------|------------------|--------------|
|                    |   | 0                     | 1                      | 2                      | 3                        | 4                     | 5                      | 6                     | 7                       | 8                   | 9                   | A                         | B                       | C                   | D                       | E                | F            |
| Upper Nibble (Hex) | 0 | 6.5<br>DEC<br>R1      | 6.5<br>DEC<br>IR1      | 6.5<br>ADD<br>r1, r2   | 6.5<br>ADD<br>r1, Ir2    | 10.5<br>ADD<br>R2, R1 | 10.5<br>ADD<br>IR2, R1 | 10.5<br>ADD<br>R1, IM | 10.5<br>ADD<br>IR1, IM  | 6.5<br>LD<br>r1, R2 | 6.5<br>LD<br>r2, R1 | 12/10.5<br>DJNZ<br>r1, RA | 12/10.0<br>JR<br>cc, RA | 6.5<br>LD<br>r1, IM | 12.10.0<br>JP<br>cc, DA | 6.5<br>INC<br>r1 |              |
|                    | 1 | 6.5<br>RLC<br>R1      | 6.5<br>RLC<br>IR1      | 6.5<br>ADC<br>r1, r2   | 6.5<br>ADC<br>r1, Ir2    | 10.5<br>ADC<br>R2, R1 | 10.5<br>ADC<br>IR2, R1 | 10.5<br>ADC<br>R1, IM | 10.5<br>ADC<br>IR1, IM  |                     |                     |                           |                         |                     |                         |                  |              |
|                    | 2 | 6.5<br>INC<br>R1      | 6.5<br>INC<br>IR1      | 6.5<br>SUB<br>r1, r2   | 6.5<br>SUB<br>r1, Ir2    | 10.5<br>SUB<br>R2, R1 | 10.5<br>SUB<br>IR2, R1 | 10.5<br>SUB<br>R1, IM | 10.5<br>SUB<br>IR1, IM  |                     |                     |                           |                         |                     |                         |                  |              |
|                    | 3 | 8.0<br>JP<br>IRR1     | 6.1<br>SRP<br>IM       | 6.5<br>SBC<br>r1, r2   | 6.5<br>SBC<br>r1, Ir2    | 10.5<br>SBC<br>R2, R1 | 10.5<br>SBC<br>IR2, R1 | 10.5<br>SBC<br>R1, IM | 10.5<br>SBC<br>IR1, IM  |                     |                     |                           |                         |                     |                         |                  |              |
|                    | 4 | 8.5<br>DA<br>R1       | 8.5<br>DA<br>IR1       | 6.5<br>OR<br>r1, r2    | 6.5<br>OR<br>r1, Ir2     | 10.5<br>OR<br>R2, R1  | 10.5<br>OR<br>IR2, R1  | 10.5<br>OR<br>R1, IM  | 10.5<br>OR<br>IR1, IM   |                     |                     |                           |                         |                     |                         |                  |              |
|                    | 5 | 10.5<br>POP<br>R1     | 10.5<br>POP<br>IR1     | 6.5<br>AND<br>r1, r2   | 6.5<br>AND<br>r1, Ir2    | 10.5<br>AND<br>R2, R1 | 10.5<br>AND<br>IR2, R1 | 10.5<br>AND<br>R1, IM | 10.5<br>AND<br>IR1, IM  |                     |                     |                           |                         |                     |                         |                  |              |
|                    | 6 | 6.5<br>COM<br>R1      | 6.5<br>COM<br>IR1      | 6.5<br>TCM<br>r1, r2   | 6.5<br>TCM<br>r1, Ir2    | 10.5<br>TCM<br>R2, R1 | 10.5<br>TCM<br>IR2, R1 | 10.5<br>TCM<br>R1, IM | 10.5<br>TCM<br>IR1, IM  |                     |                     |                           |                         |                     |                         |                  | 6.0<br>STOP  |
|                    | 7 | 10/12.1<br>PUSH<br>R2 | 12/14.1<br>PUSH<br>IR2 | 6.5<br>TM<br>r1, r2    | 6.5<br>TM<br>r1, Ir2     | 10.5<br>TM<br>R2, R1  | 10.5<br>TM<br>IR2, R1  | 10.5<br>TM<br>R1, IM  | 10.5<br>TM<br>IR1, IM   |                     |                     |                           |                         |                     |                         |                  | 7.0<br>HALT  |
|                    | 8 | 10.5<br>DECW<br>RR1   | 10.5<br>DECW<br>IR1    | 12.0<br>LDE<br>r1, Ir2 | 18.0<br>LDEI<br>Ir1, Ir2 |                       |                        |                       |                         |                     |                     |                           |                         |                     |                         |                  | 6.1<br>DI    |
|                    | 9 | 6.5<br>RL<br>R1       | 6.5<br>RL<br>IR1       | 12.0<br>LDE<br>r2, Ir1 | 18.0<br>LDEI<br>Ir2, Ir1 |                       |                        |                       |                         |                     |                     |                           |                         |                     |                         |                  | 6.1<br>EI    |
|                    | A | 10.5<br>INCW<br>RR1   | 10.5<br>INCW<br>IR1    | 6.5<br>CP<br>r1, r2    | 6.5<br>CP<br>r1, Ir2     | 10.5<br>CP<br>R2, R1  | 10.5<br>CP<br>IR2, R1  | 10.5<br>CP<br>R1, IM  | 10.5<br>CP<br>IR1, IM   |                     |                     |                           |                         |                     |                         |                  | 14.0<br>RET  |
|                    | B | 6.5<br>CLR<br>R1      | 6.5<br>CLR<br>IR1      | 6.5<br>XOR<br>r1, r2   | 6.5<br>XOR<br>r1, Ir2    | 10.5<br>XOR<br>R2, R1 | 10.5<br>XOR<br>IR2, R1 | 10.5<br>XOR<br>R1, IM | 10.5<br>XOR<br>IR1, IM  |                     |                     |                           |                         |                     |                         |                  | 16.0<br>IRET |
|                    | C | 6.5<br>RRC<br>R1      | 6.5<br>RRC<br>IR1      | 12.0<br>LDC<br>r1, Ir2 | 18.0<br>LDCI<br>Ir1, Ir2 |                       |                        |                       | 10.5<br>LD<br>r1, x, R2 |                     |                     |                           |                         |                     |                         |                  | 6.5<br>RCF   |
|                    | D | 6.5<br>SRA<br>R1      | 6.5<br>SRA<br>IR1      | 12.0<br>LDC<br>r2, Ir1 | 18.0<br>LDCI<br>Ir2, Ir1 | 20.0<br>CALL*<br>IRR1 |                        | 20.0<br>CALL<br>DA    | 10.5<br>LD<br>r2, x, R1 |                     |                     |                           |                         |                     |                         |                  | 6.5<br>SCF   |
|                    | E | 6.5<br>RR<br>R1       | 6.5<br>RR<br>IR1       |                        | 6.5<br>LD<br>r1, Ir2     | 10.5<br>LD<br>R2, R1  | 10.5<br>LD<br>IR2, R1  | 10.5<br>LD<br>R1, IM  | 10.5<br>LD<br>IR1, IM   |                     |                     |                           |                         |                     |                         |                  | 6.5<br>CCF   |
|                    | F | 8.5<br>SWAP<br>R1     | 8.5<br>SWAP<br>IR1     |                        | 6.5<br>LD<br>Ir1, r2     |                       | 10.5<br>LD<br>R2, IR1  |                       |                         |                     |                     |                           |                         |                     |                         |                  | 6.0<br>NOP   |



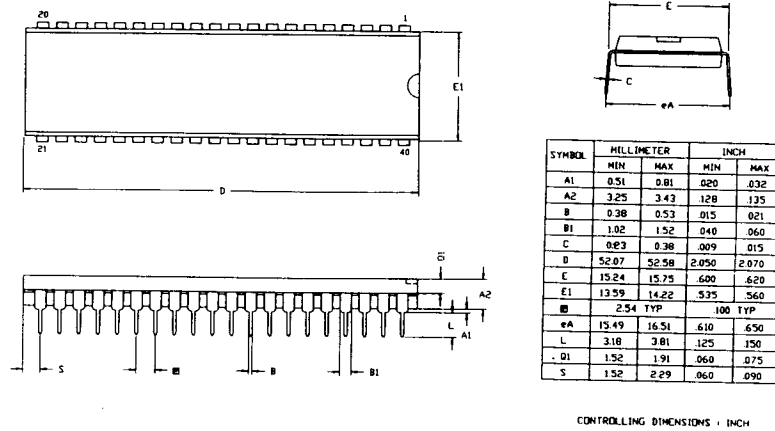
**Legend:**  
R = 8-bit address  
r = 4-bit address  
R<sub>1</sub> or r<sub>2</sub> = Dst address  
R<sub>1</sub> or r<sub>2</sub> = Src address

**Sequence:**  
Opcode, First Operand,  
Second Operand

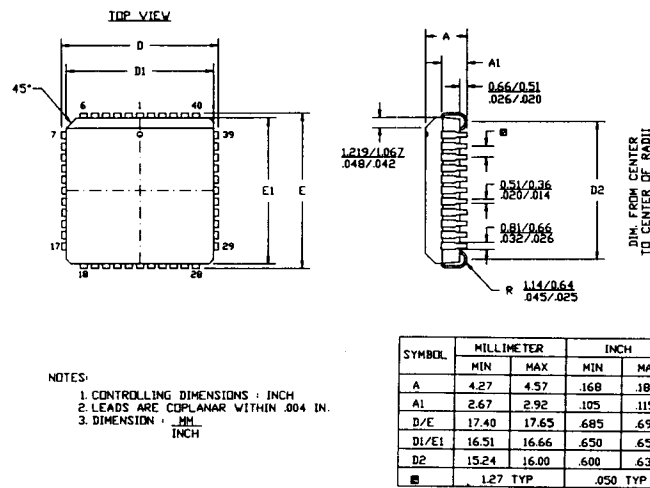
**Note:** The blank areas are not defined.

\* 2-byte instruction appears  
as a 3-byte instruction

## PACKAGE INFORMATION



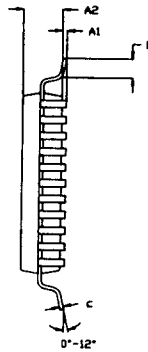
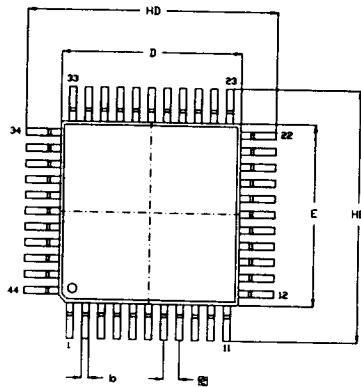
40-Pin DIP Package Diagram



44-Pin PLCC Package Diagram

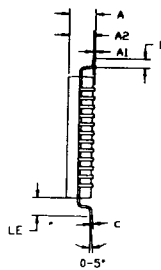
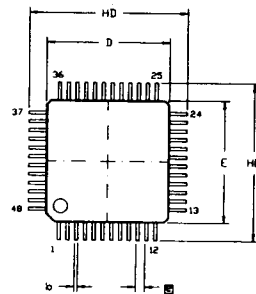
## PACKAGE INFORMATION (Continued)

NOTES:  
1. CONTROLLING DIMENSIONS : MILLIMETER  
2. LEAD COPLANARITY : MAX .10mm  
.004"



| SYMBOL | MILLIMETER |       | INCH     |      |
|--------|------------|-------|----------|------|
|        | MIN        | MAX   | MIN      | MAX  |
| A1     | 0.05       | 0.25  | .002     | .010 |
| A2     | 2.05       | 2.25  | .081     | .089 |
| b      | 0.25       | 0.45  | .010     | .018 |
| c      | 0.13       | 0.20  | .005     | .008 |
| HD     | 13.70      | 14.30 | .539     | .563 |
| D      | 9.90       | 10.10 | .390     | .398 |
| HE     | 13.70      | 14.30 | .539     | .563 |
| E      | 9.90       | 10.10 | .390     | .398 |
| □      | 0.80 TYP   |       | .031 TYP |      |
| L      | 0.60       | 1.20  | .024     | .047 |

44-Pin QFP Package Diagram



| SYMBOL | MILLIMETER |      | INCH     |      |
|--------|------------|------|----------|------|
|        | MIN        | MAX  | MIN      | MAX  |
| A      | 1.35       | 1.60 | .053     | .063 |
| A1     | 0.05       | 0.20 | .002     | .008 |
| A2     | 1.30       | 1.50 | .051     | .059 |
| b      | 0.15       | 0.26 | .006     | .010 |
| c      | 0.10       | 0.18 | .004     | .007 |
| HD     | 8.60       | 9.40 | .339     | .370 |
| D      | 6.90       | 7.10 | .272     | .280 |
| HE     | 8.60       | 9.40 | .339     | .370 |
| E      | 6.90       | 7.10 | .272     | .280 |
| □      | 0.50 TYP   |      | .020 TYP |      |
| L      | 0.30       | 0.70 | .012     | .028 |
| LE     | 0.90       | 1.10 | .035     | .043 |

1. CONTROLLING DIMENSIONS : MM  
2. MAX COPLANARITY : .10mm  
.004"

48-Pin VQFP Package Diagram

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## ORDERING INFORMATION

### Z86C93

20 MHz

44-pin PLCC  
Z86C9320VSC

44-pin QFP  
Z86C9320FSC

40-pin DIP  
Z86C9320PSC

48-pin VQFP  
Z80C9320ASC

25 MHz

44-pin PLCC  
Z86C9325VSC

44-pin QFP  
Z86C9325FSC

40-pin DIP  
Z86C9325PSC

48-pin VQFP  
Z80C9325ASC

33 MHz

44-pin PLCC  
Z86C9333VSC

44-pin QFP  
Z86C9333FSC

40-pin DIP  
Z86C9333PSC

48-pin VQFP  
Z80C9333ASC

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#### Package

V = Plastic Leaded Chip Carrier

P = Plastic Dual In Line Package

#### Longer Lead Time

F = Plastic Quad Flat Pack

A = Very Small Quad Flat Pack

#### Temperature

S = 0°C to +70°C

#### Speed

20 = 20 MHz

25 = 25 MHz

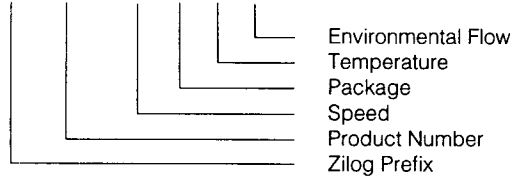
33 = 33 MHz

#### Environmental

C = Standard Flow

#### Example:

Z 86C93 33 V S C is an 86C93 33 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow



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Notes:

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