

Embedded 56-pin Industrial Temperature Range CK505 Compatible Clock

ICS9ERS3125

Recommended Application:

Industrial temperature CK505-compatible clock

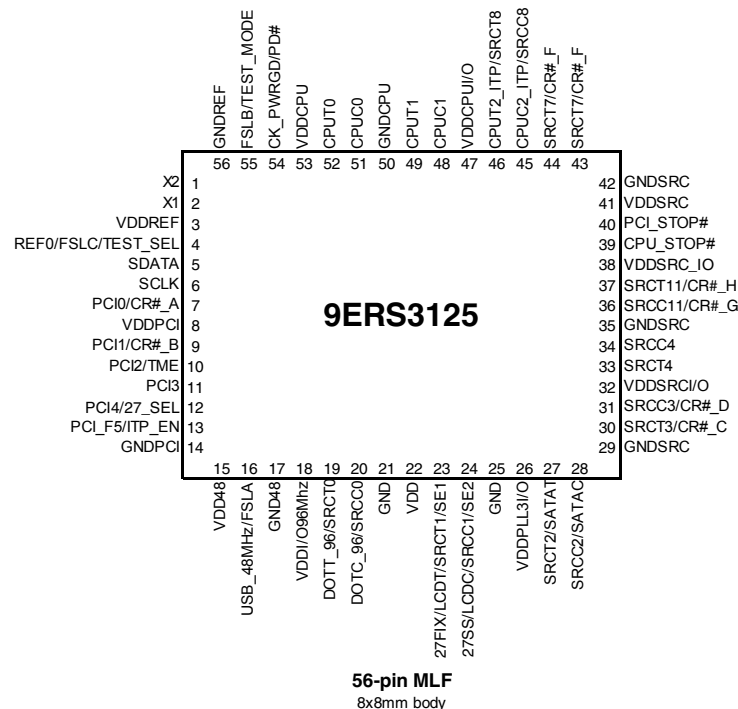
Output Features:

- 2 - CPU differential push-pull pairs
- 4 - SRC differential push-pull pairs
- 1 - CPU/SRC selectable differential push-pull pair
- 1 - DOT96/SRC selectable differential push-pull pair
- 1 - 27M/SRC/SE selectable pair
- 1 - SRC/SATA selectable differential push-pull pair
- 5 - PCI, 33MHz
- 1 - PCI_F 33MHz free running
- 1 - USB, 48MHz
- 1 - REF, 14.31818MHz

Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC output cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 100ppm frequency accuracy on all outputs

Pin Configuration



Features/Benefits:

- Fully integrated Vreg
- Differential outputs have integrated series resistors to give Zo = 50 Ohms
- Supports spread spectrum modulation, 0 to -0.5% down spread
- Supports CPU clks up to 400MHz
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning

Table 1: CPU Frequency Select Table

| FS _L C ² B0b7 | FS _L B ¹ B0b6 | FS _L A ¹ B0b5 | CPU MHz | SRC MHz | PCI MHz | REF MHz | USB MHz | DOT MHz |
|--|--|--|------------|------------|------------|------------|------------|------------|
| 0 | 0 | 0 | 266.66 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 |
| 0 | 0 | 1 | 133.33 | | | | | |
| 0 | 1 | 0 | 200.00 | | | | | |
| 0 | 1 | 1 | 166.66 | | | | | |
| 1 | 0 | 0 | 333.33 | | | | | |
| 1 | 0 | 1 | 100.00 | | | | | |
| 1 | 1 | 0 | 400.00 | | | | | |
| 1 | 1 | 1 | Reserved | | | | | |

1. FS_LA and FS_LB are low-threshold inputs. Please see V_{IL,FS} and V_{IH,FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2. FS_LC is a three-level input. Please see the V_{IL,FS} and V_{IH,FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

| 27_SEL | pin19 | pin20 |
|------------|--------|--------|
| 0 (B1b7=1) | DOT96T | DOT96C |
| 1 (B1b7=0) | SRCT0 | SRCC0 |

| 27_SEL | pin23 | pin24 |
|--------|---------|---------|
| 0 | LCDT_SS | LCDC_SS |
| 1 | 27FIX | 27SS |

NOTE: Pin 23/24 defaults to a different spread domain than SRC without BIOS intervention.

| CR # Control Table | PCIEX pair control | CR # SEL | |
|--------------------|--------------------|----------|------|
| | | 0 | 1 |
| CR #A | SRC0 or SRC2 | SRC0 | SRC2 |
| CR #B | SRC1 or SRC4 | SRC1 | SRC4 |
| CR #C | SRC0 or SRC2 | SRC0 | SRC2 |
| CR #D | SRC1 or SRC4 | SRC1 | SRC4 |
| CR #E | SRC6 | - | - |
| CR #F | SRC8 | - | - |
| CR #G | N/A | - | - |
| CR #H | N/A | - | - |

Pin Description

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------------|------|--|
| 1 | X2 | OUT | Crystal output, nominally 14.318MHz. |
| 2 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 3 | VDDREF | PWR | Power pin for the REF outputs, 3.3V nominal. |
| 4 | REF0/FSLC/TEST_SEL | I/O | 3.3V 14.318MHz reference clock/3.3V tolerant low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values/ TEST_SEL: 3-level latched input to enable test mode. Refer to Test Clarification Table. |
| 5 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 6 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 7 | PCI0/CR#_A | I/O | 3.3V PCI clock output or Clock Request control A for either SRC0 or SRC2 pair The power-up default is PCI0 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 0 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_A_EN bit located in byte 5 of SMBUS address space. Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair |
| 8 | VDDPCI | PWR | Power supply pin for the PCI outputs, 3.3V nominal |
| 9 | PCI1/CR#_B | I/O | 3.3V PCI clock output/Clock Request control B for either SRC1 or SRC4 pair The power-up default is PCI1 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 1 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_B_EN bit located in byte 5 of SMBUS address space. Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 4 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair |
| 10 | PCI2/TME | I/O | 3.3V PCI clock output / Trusted Mode Enable (TME) Latched Input. This pin is sampled on power-up as follows 0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed After being sampled on power-up, this pin becomes a 3.3V PCI Output |
| 11 | PCI3 | OUT | 3.3V PCI clock output. |
| 12 | PCI4/27_SEL | I/O | 3.3V PCI clock output / 27MHz mode select for pin23, 24 strap. On powerup, the logic value on this pin determines the power-up default of DOT_96/SRC0 and 27MHz/LCD/SRC1 output and the function table for the pin23 and pin24. |
| 13 | PCI_F5/ITP_EN | I/O | Free running PCI clock output and ITP/SRC8 enable strap. This output is not affected by the state of the PCI_STOP# pin. On powerup, the state of this pin determines whether pins 45 and 46 are an ITP or SRC pair. 0 =SRC8/SRC8# 1 = ITP/ITP# |
| 14 | GNDPCI | PWR | Ground for PCI clocks. |
| 15 | VDD48 | PWR | Power supply for USB clock, nominal 3.3V. |
| 16 | USB_48MHz/FSLA | I/O | Fixed 48MHz USB clock output. 3.3V./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. |
| 17 | GND48 | PWR | Ground pin for the 48MHz outputs. |
| 18 | VDD96_IO | PWR | Power supply for DOT96 output. 1.05 to 3.3V +/-5%. |
| 19 | DOTT_96/SRCT0 | OUT | True clock of SRC or DOT96. The power-up default function is SRC0. After powerup, this pin function may be changed to DOT96 via SMBus Byte 1, bit 7 as follows: 0= SRC0 1=DOT96 |
| 20 | DOTC_96/SRCC0 | OUT | Complement clock of SRC or DOT96. The power-up default function is SRC0#. After powerup, this pin function may be changed to DOT96# via SMBus Byte 1, bit 7 as follows 0= SRC0# 1=DOT96# |

Pin Description (continued)

| | | | |
|----|-------------------------|-----|---|
| 21 | GND | PWR | Ground pin for the DOT96 clocks. |
| 22 | VDD | PWR | Power supply for SRC / SE1 and SE2 clocks, 3.3V nominal. |
| 23 | 27FIX/LCDT/SRCT_LR1/SE1 | OUT | Single-ended 3.3V 27MHz fix clock output / True clock of differential SRC1 or LCD clock pair / Single ended 3.3V peripheral clock output. The default output selection is determined by the SEL_27 default latch value. See below: 27_SEL=0: LCD100 with -0.5% down spread is selected as default. LCD100 spread percentage can be adjusted OR output can be changed to SRC or 3.3V single-ended peripheral clock output via SMBUs B1b[4:1]. 27_SEL=1: Single-ended 27FIX output is selected. |
| 24 | 27SS/LCDC/SRCC_LR1/SE2 | OUT | Single-ended 3.3V 27MHz fix clock output / Complementary clock of differential SRC1 or LCD clock pair / Single ended 3.3V peripheral clock output. The default output selection is determined by the SEL_27 default latch value. See below: 27_SEL=0: LCD100 with -0.5% down spread is selected as default. LCD100 spread percentage can be adjusted OR output can be changed to SRC or 3.3V single-ended peripheral clock output via SMBUs B1b[4:1]. 27_SEL=1: Single-ended 27SS output is selected with -0.5% down spread as default. Spread percentage can be adjusted via SMBus B1b[4:1]. |
| 25 | GND | PWR | Ground pin for SRC / SE1 and SE2 clocks, PLL3. |
| 26 | VDDPLL3_IO | PWR | Power supply for PLL3 output. 1.05 to 3.3V +/-5%. |
| 27 | SRCT2/SATAT | OUT | True clock of differential SRC/SATA clock pair. |
| 28 | SRCC2/SATAC | OUT | Complement clock of differential SRC/SATA clock pair. |
| 29 | GNDSRC | PWR | Ground pin for SRC clocks. |
| 30 | SRCT3/CR#_C | I/O | True clock of differential SRC clock pair/ Clock Request control C for either SRC0 or SRC2 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space. After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_C_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair |
| 31 | SRCC3/CR#_D | I/O | Complementary clock of differential SRC clock pair/ Clock Request control D for either SRC1 or SRC4 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space. After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_D_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default), 1 = CR#_D controls SRC4 pair |
| 32 | VDDSRC_IO | PWR | Power supply for SRC clocks. 1.05 to 3.3V +/-5%. |
| 33 | SRCT4 | I/O | True clock of differential SRC clock pair 4 |
| 34 | SRCC4 | I/O | Complement clock of differential SRC clock pair 4 |
| 35 | GNDSRC | PWR | Ground for SRC clocks |
| 36 | SRCC11/CR#_G | I/O | SRCC11 complement /Clock Request control for SRC10 pair The power-up default is SRC11#, but this pin may also be used as a Clock Request control of SRC10 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC10 pair using byte 6, bit 5 of SMBus configuration space Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC10 NOTE: SRC10 NOT AVAILABLE ON 9LRS3125 |

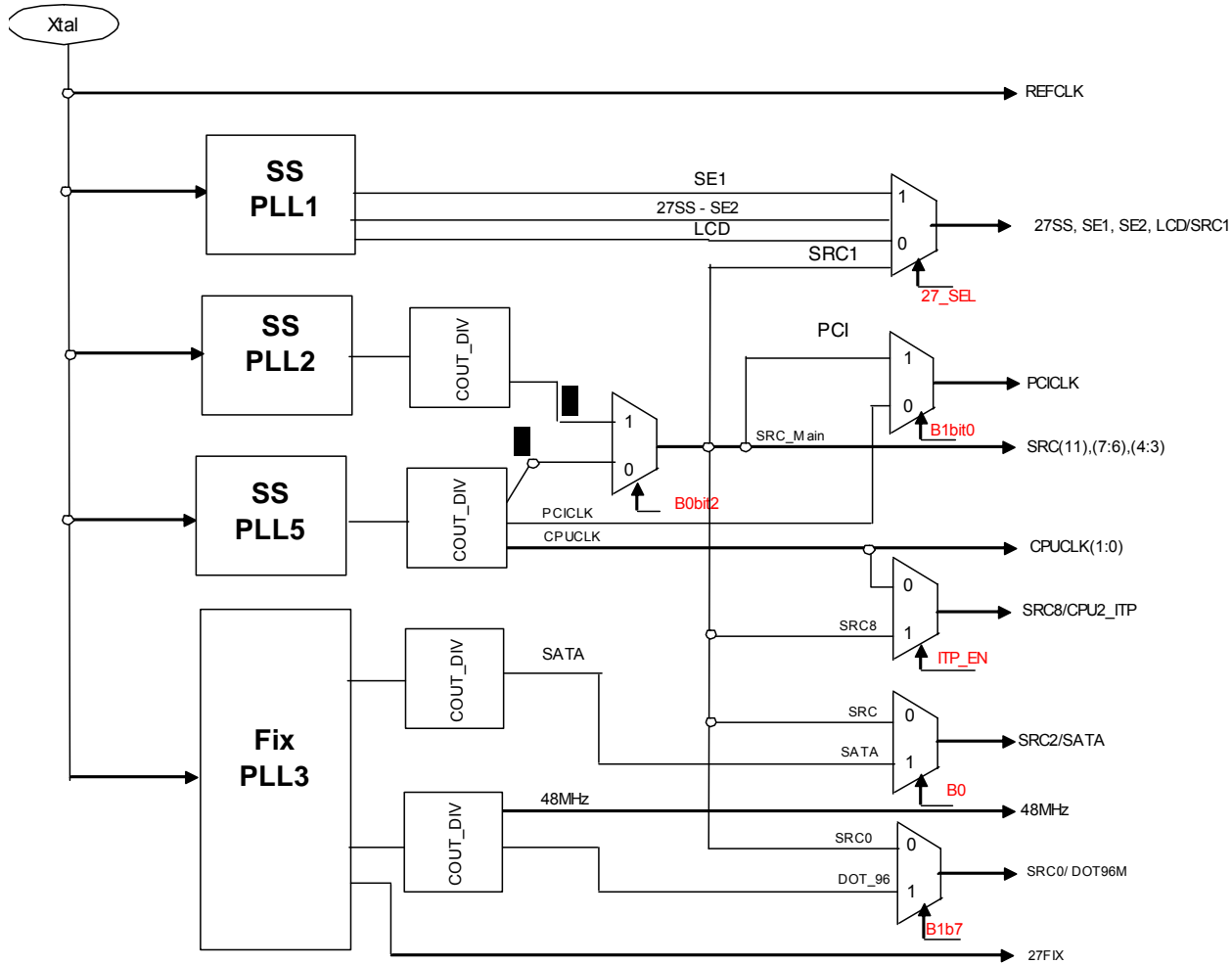
Pin Description (continued)

| | | | |
|----|-----------------|-----|---|
| 37 | SRCT11/CR#_H | I/O | SRC11 true or Clock Request control H for SRC11 pair The power-up default is SRC11, but this pin may also be used as a Clock Request control of SRC3 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC3 pair using byte 6, bit 4 of SMBus configuration space Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC3. NOTE: SRC10 NOT AVAILABLE ON 9LRS3125 |
| 38 | VDDSRC_IO | PWR | Power supply for SRC outputs. 1.05 to 3.3V +/-5%. |
| 39 | CPU_STOP# | IN | Stops all CPU Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values |
| 40 | PCI_STOP# | IN | Stops all PCI/SRC Clocks, except those set to be free running clocks. In AMT mode, this pin is a clock input which times the FSC, FSB, FSA bits shifted in on CPU_STOP#. |
| 41 | VDDSRC | PWR | 3.3V Power supply for SRC PLL and Logic |
| 42 | GNDSRC | PWR | Ground for SRC clocks |
| 43 | SRCC7CR#_E | I/O | SRC7 complement or Clock Request control E for SRC6 pair The power-up default is SRC7#, but this pin may also be used as a Clock Request control of SRC6 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space . After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC6 pair using byte 6, bit 7 of SMBus configuration space Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_E controls SRC6. |
| 44 | SRCT7/CR#_F | I/O | SRC7 true or Clock Request control 8 for SRC8 pair The power-up default is SRC7, but this pin may also be used as a Clock Request control of SRC8 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC8 pair using byte 6, bit 6 of SMBus configuration space Byte 6, bit 6 0 = SRC7# enabled (default) 1 = CR#_F controls SRC8. |
| 45 | CPUC2_ITP/SRCC8 | OUT | Complement clock of low power differential CPU2/Complement clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 14, PCIF5/ITP_EN on powerup. The function is as follows: Pin 14 latched input Value 0 = SRC8# 1 = ITP# |
| 46 | CPUT2_ITP/SRCT8 | OUT | True clock of low power differential CPU2/True clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 14, PCIF5/ITP_EN on powerup. The function is as follows: Pin 14 latched input Value 0 = SRC8 1 = ITP |
| 47 | VDDCPU/O | PWR | Power supply for CPU outputs. 1.05 to 3.3V +/-5%. |
| 48 | CPUC1_F | OUT | Complement clock of low power differential CPU clock pair. This clock will be free-running during iAMT. |
| 49 | CPUT1_F | OUT | True clock of low power differential CPU clock pair. This clock will be free-running during iAMT. |
| 50 | GNDCPU | PWR | Ground Pin for CPU Outputs |
| 51 | CPUC0 | OUT | Complement clock of low power differential CPU clock pair. |
| 52 | CPUT0 | OUT | True clock of low power differential CPU clock pair. |
| 53 | VDDCPU | PWR | 3.3V Power Supply for CPU. |
| 54 | CK_PWRGD/PD# | IN | Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode |
| 55 | FSLB/TEST_MODE | IN | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for V_{iL_FS} and V_{iH_FS} values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 56 | GNDREF | PWR | Ground pin for crystal oscillator circuit |

General Description

ICS9ERS3125 is electrically compliant to the Intel CK505 Yellow Cover specification. This clock synthesizer provides a single chip solution for Intel chipsets. ICS9ERS3125 is driven with a 14.318MHz crystal.

Block Diagram



Power Groups

| Pin Number | | Description | |
|------------|------------|-----------------------|-------------------|
| VDD | GND | | |
| 47 | 50 | CPUCLK | Low power outputs |
| 53 | 50 | Master Clock, Analog | |
| 26, 32, 38 | 29, 35, 42 | SRCCLK | Low power outputs |
| 41 | 42 | | PLL2 |
| 26 | 25 | PLL1/SE | Low power outputs |
| 22 | 25 | | PLL1 |
| 18 | 21 | DOT 96Mhz | Low power outputs |
| 15 | 17 | USB 48 output and PLL | |
| 3 | 56 | Xtal, REF | |
| 8 | 14 | PCICLK | |

Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|------------------------|-------------------|-------------------------------------|-----------|-----|-------|-------|
| Maximum Supply Voltage | VDDxxx | Supply Voltage | | 4.6 | V | 1,7 |
| Maximum Supply Voltage | VDDxxx_IO | Low-Voltage Differential I/O Supply | | 3.8 | V | 1,7 |
| Maximum Input Voltage | V _{IH} | 3.3V LVCMOS Inputs | | 4.6 | V | 1,7,8 |
| Minimum Input Voltage | V _{IL} | Any Input | GND - 0.5 | | V | 1,7 |
| Storage Temperature | T _s | - | -65 | 150 | °C | 1,7 |
| Case Temperature | T _{case} | | | 115 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | V | 1,7 |

Electrical Characteristics - Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYPICAL | MAX | UNITS | Notes |
|--|-------------------------|--|-----------------------|---------|-----------------------|-------|-------|
| Ambient Operating Temp | T _{ambient} | - | -40 | | 85 | °C | 1 |
| Supply Voltage | VDDxxx | Supply Voltage | 3.135 | | 3.465 | V | 1 |
| Supply Voltage | VDDxxx_IO | Low-Voltage Differential I/O Supply | 1 | | 3.465 | V | 1 |
| Input High Voltage | V _{IHSE} | Single-ended inputs | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{ILSE} | Single-ended inputs | V _{SS} - 0.3 | | 0.8 | V | 1 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | µA | 1 |
| Input Leakage Current | I _{INRES} | Inputs with pull or pull down resistors V _{IN} = V _{DD} , V _{IN} = GND | -200 | | 200 | µA | 1 |
| Output High Voltage | V _{OHSE} | Single-ended outputs, I _{OH} = -1mA | 2.4 | | | V | 1 |
| Output Low Voltage | V _{OLSE} | Single-ended outputs, I _{OL} = 1 mA | | | 0.4 | V | 1 |
| Output High Voltage | V _{OHDF} | Differential Outputs | 0.7 | | 0.9 | V | 1 |
| Output Low Voltage | V _{OLDIF} | Differential Outputs | | | 0.4 | V | 1 |
| Low Threshold Input-High Voltage (Test Mode) | V _{IH_FS_TEST} | 3.3 V +/-5% | 2 | | V _{DD} + 0.3 | V | 1 |
| Low Threshold Input-High Voltage | V _{IH_FS} | 3.3 V +/-5% | 0.7 | | 1.5 | V | 1 |
| Low Threshold Input-Low Voltage | V _{IL_FS} | 3.3 V +/-5% | V _{SS} - 0.3 | | 0.35 | V | 1 |
| Operating Supply Current | I _{DD_DEFAULT} | 3.3V supply, PLL1,2 off | | 95 | 125 | mA | 1 |
| | I _{DD_PLL3DIF} | 3.3V supply, PLL1,2 Differential Out | | 106 | 125 | mA | 1 |
| | I _{DD_PLL3SE} | 3.3V supply, PLL1,2 Single-ended Out | | 101 | 125 | mA | 1 |
| | I _{DD_IO} | 0.8V supply, Differential IO current, all outputs enabled | 25 | 32 | 50 | mA | 1 |
| Power Down Current | I _{DD_PD3.3} | 3.3V supply, Power Down Mode | | 26 | 30 | mA | 1 |
| | I _{DD_PDIO} | 0.8V IO supply, Power Down Mode | | 0.23 | 0.5 | mA | 1 |
| iAMT Mode Current | I _{DD_iAMT3.3} | 3.3V supply, iAMT Mode | | 47 | 60 | mA | 1 |
| | I _{DD_iAMT0.8} | 0.8V IO supply, iAMT Mode | | 5 | 10 | mA | 1 |
| Input Frequency | F _i | V _{DD} = 3.3 V | | | 14.318 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Input Capacitance | C _{IN} | Logic Inputs | 1.5 | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| | C _{INX} | X1 & X2 pins | | | 5 | pF | 1 |
| Spread Spectrum Modulation Frequency | f _{SSMOD} | Triangular Modulation | 30 | | 33 | kHz | 1 |

Electrical Characteristics - SMBus Interface

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|--------------|---|-----|------|-------|-------|
| SMBus Voltage | V_{DD} | | 2.7 | 5.5 | V | 1 |
| Low-level Output Voltage | V_{OLSMB} | @ I_{PULLUP} | | 0.4 | V | 1 |
| Current sinking at $V_{OLSMB} = 0.4$ V | I_{PULLUP} | SMB Data Pin | 4 | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | T_{R12C} | (Max VIL - 0.15) to (Min VIH + 0.15) | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | T_{F12C} | (Min VIH + 0.15) to (Max VIL - 0.15) | | 300 | ns | 1 |
| Maximum SMBus Operating Frequency | F_{SMBUS} | Block Mode | | 100 | kHz | 1 |

AC Electrical Characteristics - Input/Common Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|-------------------|-------------|--|-----|-----|-------|-------|
| Clk Stabilization | T_{STAB} | From VDD Power-Up or de-assertion of PD# to 1st clock | | 1.8 | ms | 1 |
| Tdrive_SRC | T_{DRSRC} | SRC output enable after PCI_STOP# de-assertion | | 15 | ns | 1 |
| Tdrive_PD# | T_{DRPD} | Differential output enable after PD# de-assertion | | 300 | us | 1 |
| Tdrive_CPU | T_{DRSRC} | CPU output enable after CPU_STOP# de-assertion | | 10 | ns | 1 |
| Tfall_PD# | T_{FALL} | Fall/rise time of PD#, PCI_STOP# and CPU_STOP# inputs | | 5 | ns | 1 |
| Trise_PD# | T_{RISE} | | | 5 | ns | 1 |

AC Electrical Characteristics - Low Power Differential Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|------------------------------|----------------|--------------------------|-----------|------|-------|-------|
| Rising Edge Slew Rate | t_{SLR} | Differential Measurement | 2.5 | 8 | V/ns | 1,2 |
| Falling Edge Slew Rate | t_{FLR} | Differential Measurement | 2.5 | 8 | V/ns | 1,2 |
| Slew Rate Variation | t_{SLVAR} | Single-ended Measurement | | 20 | % | 1 |
| Maximum Output Voltage | V_{HIGH} | Includes overshoot | | 1150 | mV | 1 |
| Minimum Output Voltage | V_{LOW} | Includes undershoot | -300 | | mV | 1 |
| Differential Voltage Swing | V_{SWING} | Differential Measurement | 300 | | mV | 1 |
| Crossing Point Voltage | V_{XABS} | Single-ended Measurement | 300 | 550 | mV | 1,3,4 |
| Crossing Point Variation | $V_{XABSVAR}$ | Single-ended Measurement | | 140 | mV | 1,3,5 |
| Duty Cycle | D_{CYC} | Differential Measurement | 45 | 55 | % | 1 |
| CPU Jitter - Cycle to Cycle | $CPUJ_{C2C}$ | Differential Measurement | | 85 | ps | 1 |
| SRC Jitter - Cycle to Cycle | $SRCJ_{C2C}$ | Differential Measurement | | 125 | ps | 1 |
| SATA Jitter - Cycle to Cycle | $SATAJ_{C2C}$ | Differential Measurement | | 125 | ps | 1 |
| DOT Jitter - Cycle to Cycle | $DOTJ_{C2C}$ | Differential Measurement | | 250 | ps | 1 |
| CPU[1:0] Skew | CPU_{SKEW10} | Differential Measurement | | 100 | ps | 1 |
| CPU[2_ITP:0] Skew | CPU_{SKEW20} | Differential Measurement | | 150 | ps | 1 |
| SRC[11,7,4,2,0] Skew | SRC_{SKEW} | Differential Measurement | 0 nominal | | ps | 1 |
| SRC[11:0] Skew | SRC_{SKEW} | Differential Measurement | | 3 | ns | 1 |

*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs= 0Ω, CL = 2pF

Electrical Characteristics - PCICLK/PCICLK_F

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---------------------------|----------------------|---------------------------------|-------------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 1,6 |
| Clock period | T _{period} | 33.33MHz output nominal | 29.99718 | 30.50300 | ns | 6 |
| | | 33.33MHz output spread | | 30.15320 | ns | 6 |
| Absolute min/max period | T _{abs} | 33.33MHz output nominal/spread | 29.49718 | 30.65320 | ns | 6 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -33 | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 30 | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | 38 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | d _{tt} | V _T = 1.5 V | 45 | 55 | % | 1 |
| Skew | t _{skew} | V _T = 1.5 V | | 250 | ps | 1 |
| Intentional PCI-PCI delay | t _{delay} | V _T = 1.5 V | 200 nominal | | ps | 1,9 |
| Jitter, Cycle to cycle | t _{jcy-cyc} | V _T = 1.5 V | | 500 | ps | 1 |

*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs = 39Ω, CL = 5pF

Electrical Characteristics - USB48MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|-------------------------|----------------------|---------------------------------|----------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 1,6 |
| Clock period | T _{period} | 48.00MHz output nominal | 20.83125 | 20.83542 | ns | 6 |
| Absolute min/max period | T _{abs} | 48.00MHz output nominal | 20.13125 | 21.53542 | ns | 6 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -29 | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | -23 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 29 | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | 27 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 2 | V/ns | 1 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 2 | V/ns | 1 |
| Duty Cycle | d _{tt} | V _T = 1.5 V | 45 | 55 | % | 1 |
| Jitter, Cycle to cycle | t _{jcy-cyc} | V _T = 1.5 V | | 350 | ps | 1 |

*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs = 39Ω, CL = 5pF

Electrical Characteristics - REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|-------------------------|----------------------|---|---------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 1,6 |
| Clock period | T _{period} | 14.318MHz output nominal | 69.8343 | 69.8483 | ns | 6 |
| Absolute min/max period | T _{abs} | 14.318MHz output nominal | 68.8343 | 70.84825 | ns | 6 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V, V _{OH} @ MAX = 3.135 V | -33 | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V, V _{OL} @ MAX = 0.4 V | 30 | 38 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | d _{tt} | V _T = 1.5 V | 45 | 55 | % | 1 |
| Jitter | t _{jcy-cyc} | V _T = 1.5 V | | 1000 | ps | 1 |

*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs = 39Ω, CL = 5pF

Electrical Characteristics - 27MHz_Spread / 27MHz_NonSpread

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---------------------|---------------|--|---------|---------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -50 | 50 | ppm | 1,6 |
| Clock period | T_{period} | 27.000MHz output nominal | 37.0352 | 37.0389 | ns | 6 |
| Output High Voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1 \text{ mA}$ | | 0.55 | V | 1 |
| Output High Current | I_{OH} | $V_{OH} @ \text{MIN} = 1.0 \text{ V}$ | -29 | | mA | 1 |
| | | $V_{OH} @ \text{MAX} = 3.135 \text{ V}$ | | -23 | mA | 1 |
| Output Low Current | I_{OL} | $V_{OL} @ \text{MIN} = 1.95 \text{ V}$ | 29 | | mA | 1 |
| | | $V_{OL} @ \text{MAX} = 0.4 \text{ V}$ | | 27 | mA | 1 |
| Edge Rate | $t_{slew/f}$ | Rising/Falling edge rate | 1 | 4 | V/ns | 1 |
| Rise Time | t_{r1} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | 0.5 | 2 | ns | 1 |
| Fall Time | t_{f1} | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.5 | 2 | ns | 1 |
| Duty Cycle | d_{t1} | $V_T = 1.5 \text{ V}$ | 45 | 55 | % | 1 |
| Jitter | t_{tj} | Long Term (10us), $V_T = 1.5 \text{ V}$ | | 800 | ps | 1 |
| | t_{pk-pk} | $V_T = 1.5 \text{ V}$ | -200 | 200 | ps | 1 |
| | $t_{jvc-cyc}$ | $V_T = 1.5 \text{ V}$ | | 200 | ps | 1 |

*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs = 39Ω, CL = 5pF

Electrical Characteristics - Differential Jitter Parameters

| PARAMETER | Symbol | Conditions | Min | TYP | Max | Units | Notes |
|---------------|-----------------|--|-----|-----|-----|-------------|-------|
| Jitter, Phase | $t_{phasePLL}$ | PCIe Gen 1 | | | 86 | ps (p-p) | 1,11 |
| | $t_{phaseLo}$ | PCIe Gen 2 10kHz < f < 1.5MHz | | | 3 | ps (RMS) | 1,11 |
| | $t_{phaseHigh}$ | PCIe Gen 2 1.5MHz < f < Nyquist (50MHz) | | | 3.1 | ps (RMS) | 1,11 |

*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs = 0Ω, CL = 2pF

Notes on Electrical Characteristics:

- Guaranteed by design and characterization, not 100% tested in production.
- Slew rate measured through Vswing centered around differential zero
- Vxabs is defined as the voltage where CLK = CLK#
- Only applies to the differential rising edge (CLK rising and CLK# falling)
- Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#. The average cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
- All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz
- Operation under these conditions is neither implied, nor guaranteed.
- Maximum input voltage is not to exceed maximum VDD
- See PCI Clock-to-Clock Delay Figure
- At nominal voltage and temperature
- See <http://www.pcisig.com> for complete specs

Figure 11. PCI Clock to Clock Delay

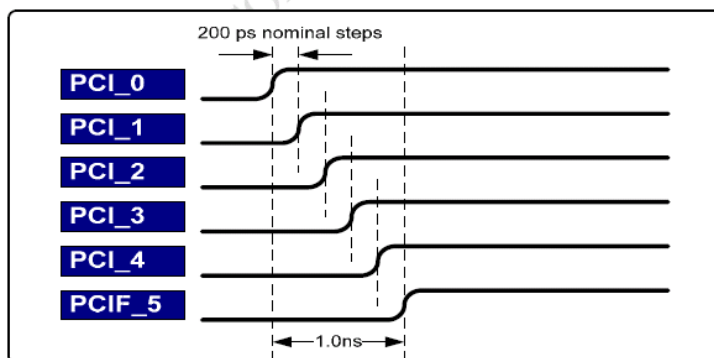


Table 1: CPU Frequency Select Table

| FS _L C ² B0b7 | FS _L B ¹ B0b6 | FS _L A ¹ B0b5 | CPU MHz | SRC MHz | PCI MHz | REF MHz | USB MHz | DOT MHz |
|--|--|--|------------|------------|------------|------------|------------|------------|
| 0 | 0 | 0 | 266.66 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 |
| 0 | 0 | 1 | 133.33 | | | | | |
| 0 | 1 | 0 | 200.00 | | | | | |
| 0 | 1 | 1 | 166.66 | | | | | |
| 1 | 0 | 0 | 333.33 | | | | | |
| 1 | 0 | 1 | 100.00 | | | | | |
| 1 | 1 | 0 | 400.00 | | | | | |
| 1 | 1 | 1 | Reserved | | | | | |

- FS_LA and FS_LB are low-threshold inputs. Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
- FS_LC is a three-level input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Table 2: 27FIX/LCDT/SRCT_LR1/SE1, 27SS/LCDC/SRCC_LR1/SE2 Configuration

| 27_SEL | B1b4 | B1b3 | B1b2 | B1b1 | 27FIX/LCDT/SRCT_LR1/SE1 | 27SS/LCDC/SRCC_LR1/SE2 | Spread % | Comment |
|--------|------|------|------|------|-------------------------|------------------------|-------------|------------------------------------|
| | | | | | MHz | MHz | | |
| 0 | 0 | 0 | 0 | 0 | PLL1 & PLL2 disabled | | | |
| 0 | 0 | 0 | 0 | 1 | 100.00 | 100.00 | | SRCCLK1 from SRC_MAIN |
| 0 | 0 | 0 | 1 | 0 | 100.00 | 100.00 | -0.50% | LCDCLK from PLL1 |
| 0 | 0 | 0 | 1 | 1 | 100.00 | 100.00 | -1% | LCDCLK from PLL1 |
| 0 | 0 | 1 | 0 | 0 | 100.00 | 100.00 | -1.50% | LCDCLK from PLL1 |
| 0 | 0 | 1 | 0 | 1 | 100.00 | 100.00 | +/-0.25% | LCDCLK from PLL1 |
| 0 | 0 | 1 | 1 | 0 | 100.00 | 100.00 | +/-0.5% | LCDCLK from PLL1 |
| 0 | 0 | 1 | 1 | 1 | N/A | N/A | N/A | N/A |
| 0 | 1 | 0 | 0 | 0 | 24.576 | 24.576 | None | 24.576Mhz on SE1 and SE2 |
| 0 | 1 | 0 | 0 | 1 | 24.576 | 98.304 | None | 24.576Mhz on SE1, 98.304Mhz on SE2 |
| 0 | 1 | 0 | 1 | 0 | 98.304 | 98.304 | None | 98.304Mhz on SE1 and SE2 |
| 0 | 1 | 0 | 1 | 1 | 27.000 | 27.000 | None | 27Mhz on SE1 and SE2 |
| 0 | 1 | 1 | 0 | 0 | 25.000 | 25.000 | None | 25Mhz on SE1 and SE2 |
| 0 | 1 | 1 | 0 | 1 | | | | N/A |
| 0 | 1 | 1 | 1 | 0 | N/A | N/A | N/A | N/A |
| 0 | 1 | 1 | 1 | 1 | N/A | N/A | N/A | N/A |
| 1 | 0 | 0 | 0 | 0 | N/A | N/A | N/A | N/A |
| 1 | 0 | 0 | 0 | 1 | N/A | N/A | N/A | N/A |
| 1 | 0 | 0 | 1 | 0 | 27MHz_nonSS | 27MHz_SS | -0.5% | |
| 1 | 0 | 0 | 1 | 1 | 27MHz_nonSS | 27MHz_SS | -1% | |
| 1 | 0 | 1 | 0 | 0 | 27MHz_nonSS | 27MHz_SS | -1.5% | |
| 1 | 0 | 1 | 0 | 1 | 27MHz_nonSS | 27MHz_SS | -2% | |
| 1 | 0 | 1 | 1 | 0 | 27MHz_nonSS | 27MHz_SS | -0.75% | |
| 1 | 0 | 1 | 1 | 1 | 27MHz_nonSS | 27MHz_SS | -1.25% | |
| 1 | 1 | 0 | 0 | 0 | 27MHz_nonSS | 27MHz_SS | -1.75% | |
| 1 | 1 | 0 | 0 | 1 | 27MHz_nonSS | 27MHz_SS | +0.5% | |
| 1 | 1 | 0 | 1 | 0 | 27MHz_nonSS | 27MHz_SS | +0.75% | |
| 1 | 1 | 0 | 1 | 1 | N/A | N/A | | |
| 1 | 1 | 1 | 0 | 0 | N/A | N/A | | |
| 1 | 1 | 1 | 0 | 1 | N/A | N/A | | |
| 1 | 1 | 1 | 1 | 0 | N/A | N/A | | |
| 1 | 1 | 1 | 1 | 1 | N/A | N/A | | |

Note: Mode 00000 ~ 00110 on Table 2 only applies when SRC_MAIN source is from PLL5.

Table 3: IO_Vout select table

| B9b2 | B9b1 | B9b0 | IO_Vout |
|------|------|------|---------|
| 0 | 0 | 0 | 0.3V |
| 0 | 0 | 1 | 0.4V |
| 0 | 1 | 0 | 0.5V |
| 0 | 1 | 1 | 0.6V |
| 1 | 0 | 0 | 0.7V |
| 1 | 0 | 1 | 0.8V |
| 1 | 1 | 0 | 0.9V |
| 1 | 1 | 1 | 1.0V |

Table 4: Device ID table

| B8b7 | B8b6 | B8b5 | B8b4 | Comment |
|------|------|------|------|-------------|
| 0 | 0 | 0 | 0 | 9LRS3125BIK |
| 0 | 0 | 0 | 1 | Reserved |
| 0 | 0 | 1 | 0 | Reserved |
| 0 | 0 | 1 | 1 | Reserved |
| 0 | 1 | 0 | 0 | Reserved |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | Reserved |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

CPU Power Management Table

| PD# | CPU_STOP# | PCI_STOP# | PEREQ# | SMBus Register OE | CPU0 | CPU0# | CPU1 | CPU1# | CPU2 | CPU2# |
|-----|-----------|-----------|--------|-------------------|---------|---------|---------|---------|---------|---------|
| 1 | 1 | 1 | X | Enable | Running | Running | Running | Running | Running | Running |
| 0 | X | X | X | Enable | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| 1 | 0 | X | X | Enable | High | Low | High | Low | High | Low |
| 1 | X | X | X | Disable | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| M1 | | | | | Low/20K | Low | Running | Running | Low/20K | Low |

PCIEX, LCD Power Management Table

| PD# | CPU_STOP# | PCI_STOP# | PEREQ# | SMBus Register OE | PCIeT | PCIeC | PCIeT | PCIeC | LCD | LCD # | LCD | LCD # | SATA | SATA# | SATA | SATA# |
|-----|-----------|-----------|--------|-------------------|----------|---------|-----------|---------|----------|---------|-----------|---------|----------|---------|-----------|---------|
| | | | | | Free-Run | | Stoppable | | Free-Run | | Stoppable | | Free-Run | | Stoppable | |
| 1 | X | 1 | 0 | Enable | Running | Running | Running | Running | Running | Running | Running | Running | Running | Running | Running | Running |
| 0 | X | X | X | Enable | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| 1 | X | 0 | 0 | Enable | Running | Running | High | Low | Running | Running | High | Low | Running | Running | High | Low |
| 1 | X | X | 1 | Enable | Running | Running | Low/20K | Low | Running | Running | Running | Running | Running | Running | Running | Running |
| 1 | X | X | X | Disable | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| M1 | | | | | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low |

DOT Power Management Table

| PD# | CPU_STOP# | PCI_STOP# | PEREQ# | SMBus Register OE | DOT | DOT# |
|-----|-----------|-----------|--------|-------------------|---------|---------|
| 1 | X | 1 | X | Enable | Running | Running |
| 0 | X | X | X | Enable | Low/20K | Low |
| 1 | X | 0 | X | Enable | Running | Running |
| 1 | X | X | X | Enable | Running | Running |
| 1 | X | X | X | Disable | Low/20K | Low |
| M1 | | | | | Low/20K | Low |

Singled-Ended Power Management Table

| PD# | CPU_STOP# | PCI_STOP# | PEREQ# | SMBus Register OE | PCIF/PCI Free-Run | PCIF/PCI Stoppable | USB48 | REF | 27M | SE |
|-----|-----------|-----------|--------|-------------------|-------------------|--------------------|---------|---------|---------|---------|
| 1 | X | 1 | X | Enable | Running | Running | Running | Running | Running | Running |
| 0 | X | X | X | Enable | Low | Low | Low | Low | Low | Low |
| 1 | X | 0 | X | Enable | Running | Low | Running | Running | Running | Running |
| 1 | X | X | X | Disable | Low | Low | Low | Low | Low | Low |
| M1 | | | | | Low | Low | Low | Low | Low | Low |

Differential Clock Tolerances

| | CPU | SRC | DOT96 | | |
|-----------------------|--------|--------|-------|--|-----|
| PPM tolerance | 100 | 100 | 100 | | ppm |
| Cycle to Cycle Jitter | 50 | 125 | 250 | | ps |
| Spread | -0.50% | -0.50% | 0 | | % |

Clock Periods - Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|-------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter | | |
| CPU | 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2 |
| | 133.33 | 7.44925 | | 7.49925 | 7.50000 | 7.50075 | | 7.55075 | ns | 1,2 |
| | 166.67 | 5.94940 | | 5.99940 | 6.00000 | 6.00060 | | 6.05060 | ns | 1,2 |
| | 200.00 | 4.94950 | | 4.99950 | 5.00000 | 5.00050 | | 5.05050 | ns | 1,2 |
| | 266.67 | 3.69962 | | 3.74962 | 3.75000 | 3.75037 | | 3.80037 | ns | 1,2 |
| | 333.33 | 2.94970 | | 2.99970 | 3.00000 | 3.00030 | | 3.05030 | ns | 1,2 |
| | 400.00 | 2.44975 | | 2.49975 | 2.50000 | 2.50025 | | 2.55025 | ns | 1,2 |
| SRC | 100.00 | 9.87400 | 9.99900 | 10.00000 | 10.00100 | 10.12600 | ns | 1,2 | | |
| DOT96 | 96.00 | 10.16563 | 10.41563 | 10.41667 | 10.41771 | 10.66771 | ns | 1,2 | | |

Clock Periods - Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|-------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter | | |
| CPU | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2 |
| | 133.00 | 7.44930 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.58830 | ns | 1,2 |
| | 166.25 | 5.94944 | 5.99944 | 6.01444 | 6.01504 | 6.01564 | 6.03064 | 6.08064 | ns | 1,2 |
| | 199.50 | 4.94953 | 4.99953 | 5.01203 | 5.01253 | 5.01303 | 5.02553 | 5.07553 | ns | 1,2 |
| | 266.00 | 3.69965 | 3.74965 | 3.75902 | 3.75940 | 3.75977 | 3.76915 | 3.81915 | ns | 1,2 |
| | 332.50 | 2.94972 | 2.99972 | 3.00722 | 3.00752 | 3.00782 | 3.01532 | 3.06532 | ns | 1,2 |
| | 399.00 | 2.44977 | 2.49977 | 2.50602 | 2.50627 | 2.50652 | 2.51277 | 2.56277 | ns | 1,2 |
| SRC | 99.75 | 9.87406 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.17607 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy specifications are guaranteed with the assumption that the crystal input is tuned to exactly 14.31818MHz.

General SMBus serial interface information for the ICS9ERS3125

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address $D2_{(H)}$ | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | X Byte |
| ○ | | |
| ○ | | |
| ○ | | |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address $D2_{(H)}$ | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address $D3_{(H)}$ | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count = X |
| ACK | | X Byte |
| ACK | | |
| ○ | | |
| ○ | | |
| ○ | | |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

Byte 0 FS Readback & PLL Selection Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|--------------|--|------|--|---------------------|----------------------|
| 7 | FSLC | CPU Freq. Sel. Bit (Most Significant) | R | See Table 1 : CPU Frequency Select Table | | Latch |
| 6 | FSLB | CPU Freq. Sel. Bit | R | | | Latch |
| 5 | FSLA | CPU Freq. Sel. Bit (Least Significant) | R | | | Latch |
| 4 | iAMT_EN | Set via SMBus or dynamically by CK505 if detects dynamic M1 | R | Legacy Mode | iAMT Enabled | iAMT power on status |
| 3 | Reserved | | | | | 1 |
| 2 | SRC_Main_SEL | Select source for SRC Main | RW | SRC Main = PLL5 | SRC Main = PLL2 | 0 |
| 1 | SATA_SEL | Select source for SATA clock | RW | SATA = SRC_Main | SATA = PLL3 | 0 |
| 0 | PD_Restore | 1 = on Power Down de-assert return to last known state 0 = clear all SMBus configurations as if cold power-on and go to latches open state This bit is ignored and treated at '1' if device is in iAMT mode. | RW | Configuration Not Saved | Configuration Saved | 1 |

Byte 1 DOT96 Select & PLL3 Quick Config Register,**Note 1 : When 27_Select pin = 0, B1b7 Default = 1; When 27_Select pin = 1, Default = 0**

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|--------------|--------------------------------|------|---|-------------------|---------|
| 7 | SRC0_SEL | Select SRC0 or DOT96 | RW | SRC0 | DOT96 | Note 1 |
| 6 | PLL5_SSC_SEL | Select 0.5% down or center SSC | RW | Down spread | Center spread | 0 |
| 5 | PLL2_SSC_SEL | Select 0.5% center or down SSC | RW | Down | Center | 0 |
| 4 | PLL1_CF3 | PLL1 Quick Config Bit 3 | RW | See Table 2: pin 27FIX/LCDT/SRCT_LR1/SE1, 27SS/LCDC/SRCC_LR1/SE2 Configuration Only applies if Byte 0, bit 2 = 0. | | 0 |
| 3 | PLL1_CF2 | PLL1 Quick Config Bit 2 | RW | | | 0 |
| 2 | PLL1_CF1 | PLL1 Quick Config Bit 1 | RW | | | 1 |
| 1 | PLL1_CF0 | PLL1 Quick Config Bit 0 | RW | | | 0 |
| 0 | PCI_SEL | PCI_SEL | RW | PCI from PLL5 | PCI from SRC_MAIN | 1 |

Byte 2 Single Ended Output Enable Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|----------|------------------------|------|-----------------|----------------|---------|
| 7 | REF_OE | Output enable for USB | RW | Output Disabled | Output Enabled | 1 |
| 6 | USB_OE | Output enable for USB | RW | Output Disabled | Output Enabled | 1 |
| 5 | PCIF5_OE | Output enable for PCI5 | RW | Output Disabled | Output Enabled | 1 |
| 4 | PCI4_OE | Output enable for PCI4 | RW | Output Disabled | Output Enabled | 1 |
| 3 | PCI3_OE | Output enable for PCI3 | RW | Output Disabled | Output Enabled | 1 |
| 2 | PCI2_OE | Output enable for PCI2 | RW | Output Disabled | Output Enabled | 1 |
| 1 | PCI1_OE | Output enable for PCI1 | RW | Output Disabled | Output Enabled | 1 |
| 0 | PCI0_OE | Output enable for PCI0 | RW | Output Disabled | Output Enabled | 1 |

Byte 3 SRC Output Enable Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|-------------|-------------------------------|------|-----------------|----------------|---------|
| 7 | SRC11_OE | Output enable for SRC11 | RW | Output Disabled | Output Enabled | 1 |
| 6 | Reserved | | | | | 1 |
| 5 | Reserved | | | | | 1 |
| 4 | SRC8/ITP_OE | Output enable for SRC8 or ITP | RW | Output Disabled | Output Enabled | 1 |
| 3 | SRC7_OE | Output enable for SRC7 | RW | Output Disabled | Output Enabled | 1 |
| 2 | SRC6_OE | Output enable for SRC6 | RW | Output Disabled | Output Enabled | 1 |
| 1 | Reserved | | | | | 1 |
| 0 | SRC4_OE | Output enable for SRC4 | RW | Output Disabled | Output Enabled | 1 |

Byte 4 SRC/CPU/DOT Output Enable & Spread Spectrum Disable Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|---------------|---------------------------------|------|-----------------|----------------|---------|
| 7 | SRC3_OE | Output enable for SRC3 | RW | Output Disabled | Output Enabled | 1 |
| 6 | SATA/SRC2_OE | Output enable for SATA/SRC2 | RW | Output Disabled | Output Enabled | 1 |
| 5 | SRC1_OE | Output enable for SRC1 | RW | Output Disabled | Output Enabled | 1 |
| 4 | SRC0/DOT96_OE | Output enable for SRC0/DOT96 | RW | Output Disabled | Output Enabled | 1 |
| 3 | CPU1_OE | Output enable for CPU1 | RW | Output Disabled | Output Enabled | 1 |
| 2 | CPU0_OE | Output enable for CPU0 | RW | Output Disabled | Output Enabled | 1 |
| 1 | PLL5_SSC_ON | Enable PLL5's spread modulation | RW | Spread Disabled | Spread Enabled | 1 |
| 0 | PLL2_SSC_ON | Enable PLL2's spread modulation | RW | Spread Disabled | Spread Enabled | 1 |

Byte 5 Clock Request Enable/Configuration Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|-----------|---|------|---------------|---------------|---------|
| 7 | CR#_A_EN | Enable CR#_A (clk req) for SRC0 or SRC2 | RW | Disable CR#_A | Enable CR#_A | 0 |
| 6 | CR#_A_SEL | Sets CR#_A to control either SRC0 or SRC2 | RW | CR#_A -> SRC0 | CR#_A -> SRC2 | 0 |
| 5 | CR#_B_EN | Enable CR#_B (clk req) for SRC1 or SRC4 | RW | Disable CR#_B | Enable CR#_B | 0 |
| 4 | CR#_B_SEL | Sets CR#_B to control either SRC1 or SRC4 | RW | CR#_B -> SRC1 | CR#_B -> SRC4 | 0 |
| 3 | CR#_C_EN | Enable CR#_C (clk req) for SRC0 or SRC2 | RW | Disable CR#_C | Enable CR#_C | 0 |
| 2 | CR#_C_SEL | Sets CR#_C to control either SRC0 or SRC2 | RW | CR#_C -> SRC0 | CR#_C -> SRC2 | 0 |
| 1 | CR#_D_EN | Enable CR#_D (clk req) for SRC1 or SRC4 | RW | Disable CR#_D | Enable CR#_D | 0 |
| 0 | CR#_D_SEL | Sets CR#_D to control either SRC1 or SRC4 | RW | CR#_D -> SRC1 | CR#_D -> SRC4 | 0 |

Byte 6 Clock Request Enable/Configuration Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|--------------------|--|------|---------------|--------------------------------|---------|
| 7 | CR#_E_EN | Enable CR#_E (clk req) for SRC6 | RW | Disable CR#_E | Enable CR#_E | 0 |
| 6 | CR#_F_EN | Enable CR#_F (clk req) for SRC8 | RW | Disable CR#_F | Enable CR#_F | 0 |
| 5 | | Reserved | | | | 0 |
| 4 | | Reserved | | | | 0 |
| 3 | | Reserved | | | | 0 |
| 2 | | Reserved | | | | 0 |
| 1 | LCD/SRC1_STP_CRTL* | If set, LCD_SS/SRC1 stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 0 | SRC0_STP_CRTL | If set, SRC0 stop with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |

Byte 7 Vendor ID/ Revision ID Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|-----------------|----------------------------------|------|-----------------|---|---------|
| 7 | Rev Code Bit 3 | Revision ID | R | Vendor specific | | 0 |
| 6 | Rev Code Bit 2 | | R | | | 0 |
| 5 | Rev Code Bit 1 | | R | | | 0 |
| 4 | Rev Code Bit 0 | | R | | | 1 |
| 3 | Vendor ID bit 3 | Vendor ID ICS is 0001, binary | R | | | 0 |
| 2 | Vendor ID bit 2 | | R | | | 0 |
| 1 | Vendor ID bit 1 | | R | | | 0 |
| 0 | Vendor ID bit 0 | | R | 1 | | |

Byte 8 Device ID & Output Enable Register

| Bit | Name | Description | Type | 0 | 1 | Default (MLF) |
|-----|--------------------|--|------|-----------------------|---------|---------------|
| 7 | Device_ID3 | Table of Device identifier codes, used for differentiating between CK505 package options, etc. | R | See Device ID Table 4 | | 0 |
| 6 | Device_ID2 | | R | | | 0 |
| 5 | Device_ID1 | | R | | | 0 |
| 4 | Device_ID0 | | R | | | 0 |
| 3 | | Reserved | | | | 0 |
| 2 | | Reserved | | | | 0 |
| 1 | 27MHz_nonSS/SE1_OE | Output enable for SE1 | RW | Disabled | Enabled | 1 |
| 0 | 27MHz_SS/SE2_OE | Output enable for SE2 | RW | Disabled | Enabled | 1 |

Byte 9 Test and Output Control Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|------------------|--|------|--|--------------------------------|-----------|
| 7 | PCIF5_STOP_EN | Allows control of PCIF5 with assertion of PCI_STOP# | RW | Free running | Stops with PCI_STOP# assertion | 0 |
| 6 | TME_Readback | Trusted Mode Enable (TME) strap status | R | normal operation | no overclocking | TME latch |
| 5 | | Reserved | | | | 1 |
| 4 | Test Mode Select | Allows test select, ignores REF/FSC/TestSel | RW | Outputs HI-Z | Outputs = REF/N | 0 |
| 3 | Test Mode Entry | Allows entry into test mode, ignores FSB/TestMode | RW | Normal operation | Test mode | 0 |
| 2 | CPU IO_VOUT2 | CPU IO Output Voltage Select (Most Significant Bit) | RW | See Table 3: V_IO Selection (Default is 0.8V) | | 1 |
| 1 | CPU IO_VOUT1 | CPU IO Output Voltage Select | RW | | | 0 |
| 0 | CPU IO_VOUT0 | CPU IO Output Voltage Select (Least Significant Bit) | RW | | | 1 |

Byte 10 Output Control Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|-----------------------|--|------|-------------------|--------------------------------|--------------|
| 7 | 27_SEL Latch Readback | Readback of 27_Select latch | R | Dot96/ LCD_SS /SE | SRC0/ 27MHz | 27_SEL latch |
| 6 | PCI4 STOP EN | Allows control of PCI4 with assertion of PCI_STOP# | RW | Free running | Stops with PCI_STOP# assertion | 1 |
| 5 | PCI3 STOP EN | Allows control of PCI3 with assertion of PCI_STOP# | RW | Free running | Stops with PCI_STOP# assertion | 1 |
| 4 | PCI2 STOP EN | Allows control of PCI2 with assertion of PCI_STOP# | RW | Free running | Stops with PCI_STOP# assertion | 1 |
| 3 | PCI1 STOP EN | Allows control of PCI1 with assertion of PCI_STOP# | RW | Free running | Stops with PCI_STOP# assertion | 1 |
| 2 | PCI0 STOP EN | Allows control of PCI0 with assertion of PCI_STOP# | RW | Free running | Stops with PCI_STOP# assertion | 1 |
| 1 | CPU1 Stop Enable | Enables control of CPU1 with CPU_STOP# | RW | Free Running | Stoppable | 1 |
| 0 | CPU0 Stop Enable | Enables control of CPU0 with CPU_STOP# | RW | Free Running | Stoppable | 1 |

Byte 11 iAMT/CPU2 Control Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|------------------|--|------|--------------|-----------|---------|
| 7 | | Reserved | | | | 0 |
| 6 | | Reserved | | | | 0 |
| 5 | | Reserved | | | | 0 |
| 4 | | Reserved | | | | 0 |
| 3 | CPU2_AMT_EN | M1 mode clk enable, only if ITP_EN=1 | RW | Disable | Enable | 0 |
| 2 | CPU1_AMT_EN | M1 mode clk enable | RW | Disable | Enable | 1 |
| 1 | Reserved | Reserved | RW | - | - | 0 |
| 0 | CPU2 Stop Enable | Enables control of CPU2 with CPU_STOP# | RW | Free Running | Stoppable | 1 |

Byte 12 Byte Count Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|------|--|------|---|---|---------|
| 7 | | Reserved | | | | 0 |
| 6 | | Reserved | | | | 0 |
| 5 | BC5 | Read Back byte count register, max bytes = 32 | RW | - | - | 0 |
| 4 | BC4 | | RW | - | - | 0 |
| 3 | BC3 | | RW | - | - | 1 |
| 2 | BC2 | | RW | - | - | 1 |
| 1 | BC1 | | RW | - | - | 0 |
| 0 | BC0 | | RW | - | - | 1 |

Byte 13 Single Ended Output Slew Rate Control Register

| Bit | Name | Description | RW | 0 | 1 | Default |
|-----|---------|-------------------|----|---------------|---------------|---------|
| 7 | REF | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 6 | REF | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |
| 5 | 27M_FIX | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 4 | 27M_FIX | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |
| 3 | 27M_SS | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 2 | 27M_SS | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |
| 1 | | Reserved | | | | 0 |
| 0 | | Reserved | | | | 0 |

Byte 14 Reserved

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|------|-------------|------|---|---|---------|
| 7 | | Reserved | | | | X |
| 6 | | Reserved | | | | X |
| 5 | | Reserved | | | | X |
| 4 | | Reserved | | | | X |
| 3 | | Reserved | | | | X |
| 2 | | Reserved | | | | X |
| 1 | | Reserved | | | | X |
| 0 | | Reserved | | | | X |

Byte 15 Reserved

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|------|-------------|------|---|---|---------|
| 7 | | Reserved | | | | X |
| 6 | | Reserved | | | | X |
| 5 | | Reserved | | | | X |
| 4 | | Reserved | | | | X |
| 3 | | Reserved | | | | X |
| 2 | | Reserved | | | | X |
| 1 | | Reserved | | | | X |
| 0 | | Reserved | | | | X |

Byte 16 Reserved

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|------|-------------|------|---|---|---------|
| 7 | | Reserved | | | | X |
| 6 | | Reserved | | | | X |
| 5 | | Reserved | | | | X |
| 4 | | Reserved | | | | X |
| 3 | | Reserved | | | | X |
| 2 | | Reserved | | | | X |
| 1 | | Reserved | | | | X |
| 0 | | Reserved | | | | X |

Byte 17 SRC Output Control Register

| Bit | Name | Description | RW | 0 | 1 | Default |
|-----|--------------------|--|----|--------------|--------------------------------|---------|
| 7 | SATA/SRC2_STP_CTRL | If set, SATA/SRC2 stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 6 | SRC3_STP_CTRL | If set, SRC3 stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 5 | SRC4_STP_CTRL | If set, SRC4 stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 4 | SRC6_STP_CTRL | If set, SRC6 stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 3 | SRC7_STP_CTRL | If set, SRC7 stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 2 | | Reserved | | | | 0 |
| 1 | SRC8_STP_CTRL | If set, SRC8 stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 0 | | Reserved | | | | 0 |

Byte 18 Differential Output Control Register

| Bit | Name | Description | RW | 0 | 1 | Default |
|-----|--------------------------|--|----|--|--------------------------------|---------|
| 7 | | Reserved | | | | 0 |
| 6 | SRC11_STP_CTRL | If set, SRC11 stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 5 | SRC/CPUITP_SRC8 IO_VOUT2 | SRC & CPUITP_SRC8 IO Output Voltage Select (Most Significant Bit) | RW | See Table 3: V_IO Selection (Default is 0.8V) | | 1 |
| 4 | SRC/CPUITP_SRC8 IO_VOUT1 | SRC IO & CPUITP_SRC8 Output Voltage Select | RW | | | 0 |
| 3 | SRC/CPUITP_SRC8 IO_VOUT0 | SRC & CPUITP_SRC8 IO Output Voltage Select (Least Significant Bit) | RW | | | 1 |
| 2 | SATA/SRC2 IO_VOUT2 | SATA_SRC2 IO Output Voltage Select (Most Significant Bit) | RW | See Table 3: V_IO Selection (Default is 0.8V) | | 1 |
| 1 | SATA/SRC2 IO_VOUT1 | SATA_SRC2 IO Output Voltage Select | RW | | | 0 |
| 0 | SATA/SRC2 IO_VOUT0 | SATA_SRC2 IO Output Voltage Select (Least Significant Bit) | RW | | | 1 |

Byte 19 Differential Output Control Register

| Bit | Name | Description | RW | 0 | 1 | Default |
|-----|------------------------|---|----|--|---|---------|
| 7 | LCD_SS (SRC1) IO_VOUT2 | LCD_SS IO Output Voltage Select (Most Significant Bit) | RW | See Table 3: V_IO Selection (Default is 0.8V) | | 1 |
| 6 | LCD_SS (SRC1) IO_VOUT1 | LCD_SS IO Output Voltage Select | RW | | | 0 |
| 5 | LCD_SS (SRC1) IO_VOUT0 | LCD_SS IO Output Voltage Select (Least Significant Bit) | RW | | | 1 |
| 4 | SRC0/DOT96 IO_VOUT2 | SRC0_DOT96 IO Output Voltage Select (Most Significant Bit) | RW | See Table 3: V_IO Selection (Default is 0.8V) | | 1 |
| 3 | SRC0/DOT96 IO_VOUT1 | SRC0_DOT96 IO Output Voltage Select | RW | | | 0 |
| 2 | SRC0/DOT96 IO_VOUT0 | SRC0_DOT96 IO Output Voltage Select (Least Significant Bit) | RW | | | 1 |
| 1 | | Reserved | | | | 0 |
| 0 | | Reserved | | | | 0 |

Byte 20 Single Ended Slew Rate Control Register

| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|-------|-------------------|------|---------------|---------------|---------|
| 7 | 48MHz | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 6 | 48MHz | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |
| 5 | PCIF5 | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 4 | PCIF5 | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |
| 3 | PCI4 | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 2 | PCI4 | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |
| 1 | PCI3 | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 0 | PCI3 | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |

Byte 21 Single Ended Slew Rate & M/N Enable Control Register

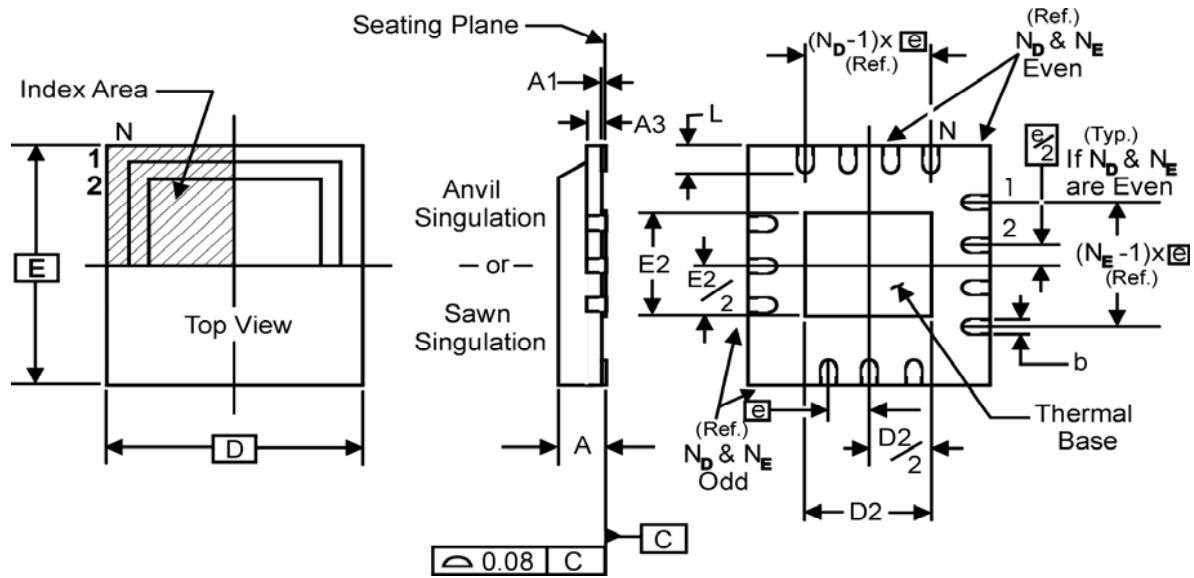
| Bit | Name | Description | Type | 0 | 1 | Default |
|-----|------|-------------------|------|---------------|---------------|---------|
| 7 | PCI2 | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 6 | PCI2 | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |
| 5 | PCI1 | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 4 | PCI1 | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |
| 3 | PCI0 | Slew Rate Control | RW | 00 = Hi-Z | 01 = 1.4 V/ns | 0 |
| 2 | PCI0 | | RW | 10 = 2.0 V/ns | 11 = 2.4 V/ns | 1 |
| 1 | | Reserved | | | | 0 |
| 0 | | Reserved | | | | 0 |

Test Clarification Table

| Comments | HW | | SW | | OUTPUT |
|--|-----------------------------|------------------------------|---------------------------|--------------------------|--------|
| | FSLC/ TEST_SEL HW PIN | FSLB/ TEST_MODE HW PIN | TEST ENTRY BIT B9b3 | REF/N or HI-Z B9b4 | |
| | <2.0V | X | 0 | 0 | NORMAL |
| CK_PWRG=1 w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode FSLC./TEST_SEL -->3-level latched input If CK_PWRG=1 w/ V>2.0V then use TEST_SEL If CK_PWRG=1 w/ V<2.0V then use FSLC FSLB/TEST_MODE -->low Vth input TEST_MODE is a real time input | >2.0V | 0 | X | 0 | HI-Z |
| | >2.0V | 0 | X | 1 | REF/N |
| | >2.0V | 1 | X | 0 | REF/N |
| | >2.0V | 1 | X | 1 | REF/N |
| If TEST_SEL HW pin is 0 after CK_PWRG=1, test mode can be invoked through B9b3. If test mode is invoked by B9b3, only B9b4 is used to select HI-Z or REF/N FSLB/TEST_Mode pin is not used. Cycle power to disable test mode, one shot control | <2.0V | X | 1 | 0 | HI-Z |
| | <2.0V | X | 1 | 1 | REF/N |

B9b3: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B9b4: 1= REF/N, Default = 0 (HI-Z)



**THERMALLY ENHANCED, VERY THIN, FINE PITCH
 QUAD FLAT / NO LEAD PLASTIC PACKAGE**

DIMENSIONS

| | |
|--------|-----|
| SYMBOL | 56L |
| N | 56 |
| ND | 14 |
| NE | 14 |

DIMENSIONS (mm)

| SYMBOL | MIN. | MAX. |
|----------------|----------------|------|
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |
| D x E BASIC | 8.00 x 8.00 | |
| D2 MIN. / MAX. | 4.35 | 4.65 |
| E2 MIN. / MAX. | 5.05 | 5.35 |
| L MIN. / MAX. | 0.3 | 0.5 |

Ordering Information

| Part/Order Number | Shipping Packaging | Package | Temperature |
|-------------------|--------------------|------------|---------------|
| 9ERS3125BKILF | Tubes | 56-pin MLF | -40 to +85° C |
| 9ERS3125BKILFT | Tape and Reel | 56-pin MLF | -40 to +85° C |

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant. Due to package size constraints, actual top-side marking may differ from the full orderable part number.

Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|-------------------|--------|
| 0.1 | 07/31/09 | Initial Release | - |
| A | 08/19/09 | Released to final | |
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