KAI-50140

10440 (H) x 4800 (V) Interline CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAI−50140 image sensor is a 50 megapixel Interline Transfer CCD in a 2.18 to 1 aspect ratio, making it well suited to inspect displays commonly found on modern smartphones. Leveraging a 4.5 μm pixel design that provides a 70% resolution increase compared to the KAI−29050 and KAI−29052 devices, the KAI−50140 provides excellent image uniformity and broad dynamic range. A flexible output architecture supports 1, 2, or 4 outputs for full resolution readout of up to 4 frames per second, and a true electronic shutter enables image capture without motion artifacts across a broad range of exposure times.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD, Progressive Scan
Total Number of Pixels	10560 (H) × 4920 (V)
Number of Effective Pixels	10480 (H) × 4840 (V)
Number of Active Pixels	10440 (H) × 4800 (V)
Pixel Size	4.5 μm (H) × 4.5 μm (V)
Active Image Size	46.98 mm (H) × 21.60 mm (V) 51.71 mm (Diag.) 645 1.3× Optical Format
Aspect Ratio	2.175:1
Number of Outputs	1, 2 or 4
Charge Capacity	13,000 electrons
Output Sensitivity	42 μV/e⁻
Quantum Efficiency Pan (−AXA, −QXA) R, G, B (−FXA, −QXA)	 45% 27%, 34%, 37%
Read Noise (f = 40 MHz)	13 electrons rms
Dark Current Photodiode VCCD	 7 electrons/s 50 electrons/s
Dynamic Range	60 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 300 X
Smear	−98 dB
Image Lag	< 10 electrons
Maximum Pixel Clock Speed	60 MHz
Maximum Frame Rates Quad Output Dual Output Single Output	 3.9 fps 2.0 fps 1.1 fps
Package	72 pin PGA
Cover Glass	AR coated, 2 Sides, Sealed Clear Glass, Taped

NOTE: All parameters are specified at T = 40°C unless otherwise noted.

Figure 1. KAI−50140 CCD Image Sensor

Features

- True Electronic Shutter with Broad Exposure Latitude
- Low Noise Architecture
- Excellent Smear Performance
- Monochrome and Bayer Color CFA Configurations

Applications

- Industrial Imaging and Inspection
- Security and Surveillance

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION

Part Number	Description	Marking Code
KAI−50140−AXA−JD−B1	Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1	KAI−50140−AXA Serial Number
KAI−50140−AXA−JD−B2	Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2	
KAI−50140−AXA−JD−AE	Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
KAI−50140−AXA−JP−B1	Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass (no coatings), Grade 1	KAI−50140−AXA Serial Number
KAI−50140−AXA−JP−B2	Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass (no coatings), Grade 2	
KAI−50140−AXA−JP−AE	Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass (no coatings), Engineering Grade	
KAI−50140−FXA−JD−B1	Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1	KAI−50140−FXA Serial Number
KAI−50140−FXA−JD−B2	Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2	
KAI−50140−FXA−JD−AE	Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

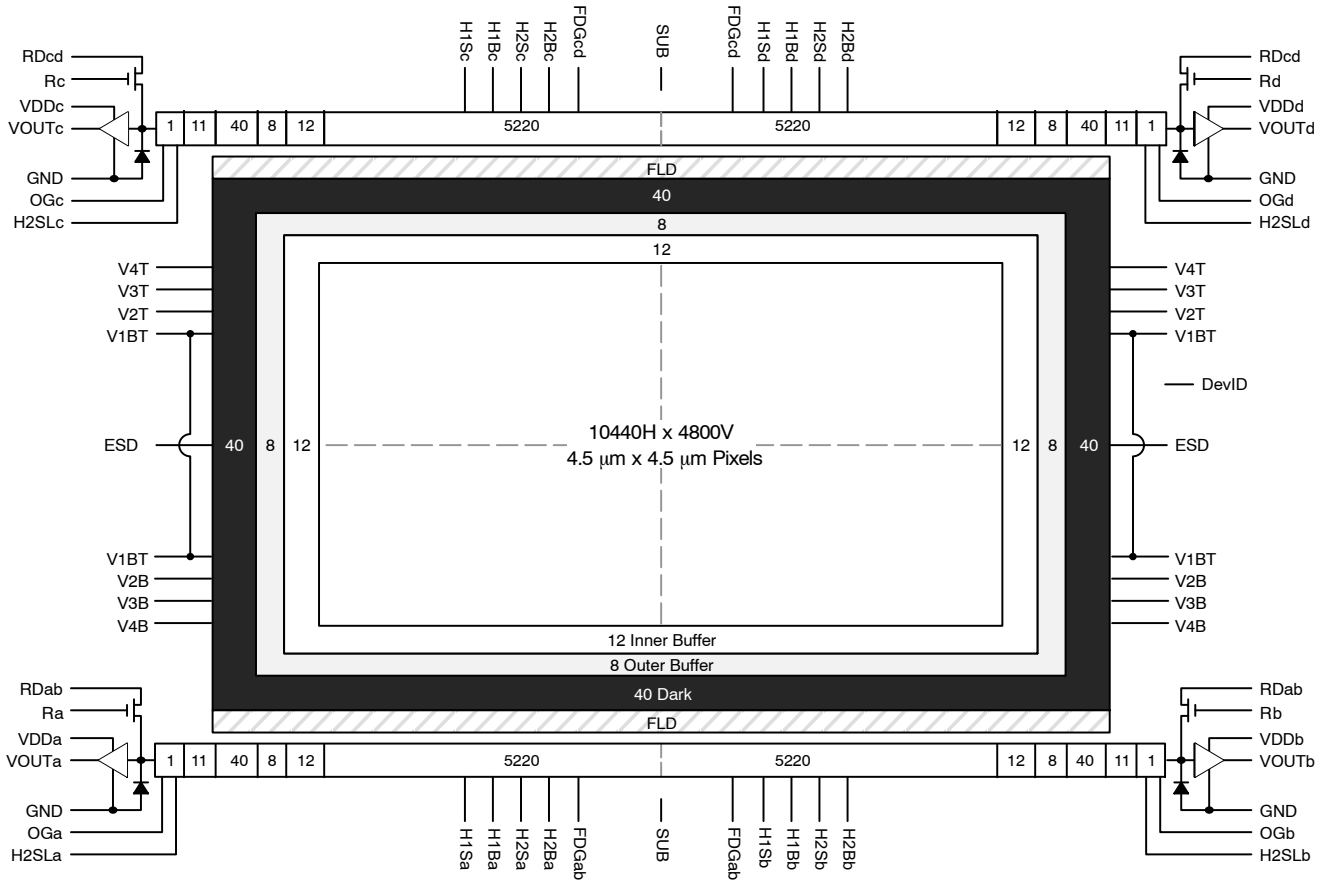


Figure 2. Block Diagram

Dark Reference Pixels

There are 40 dark reference rows at the top and 40 dark rows at the bottom of the image sensor. The dark rows are not entirely dark and so should not be used for a dark reference level. Use the 40 dark columns on the left or right side of the image sensor as a dark reference. Under normal circumstances use only the center 38 columns of the 40 column dark reference due to potential light leakage.

Dummy Pixels

Within each horizontal shift register there are 12 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level. In addition, there is one dummy row of pixels at the top and bottom of the image.

Active Buffer Pixels

20 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non−uniformities. The 8 outer buffer pixels are less sensitive than the inner buffer pixels. The inner buffer pixels have the same sensitivity as the 10440 by 4800 active pixels.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron−hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photo−site. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non−linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

ESD Protection

Adherence to the power−up and power−down sequence is critical. Failure to follow the proper power−up and power−down sequences may cause damage to the sensor. See Power−Up and Power−Down Sequence section.

Bayer Color Filter

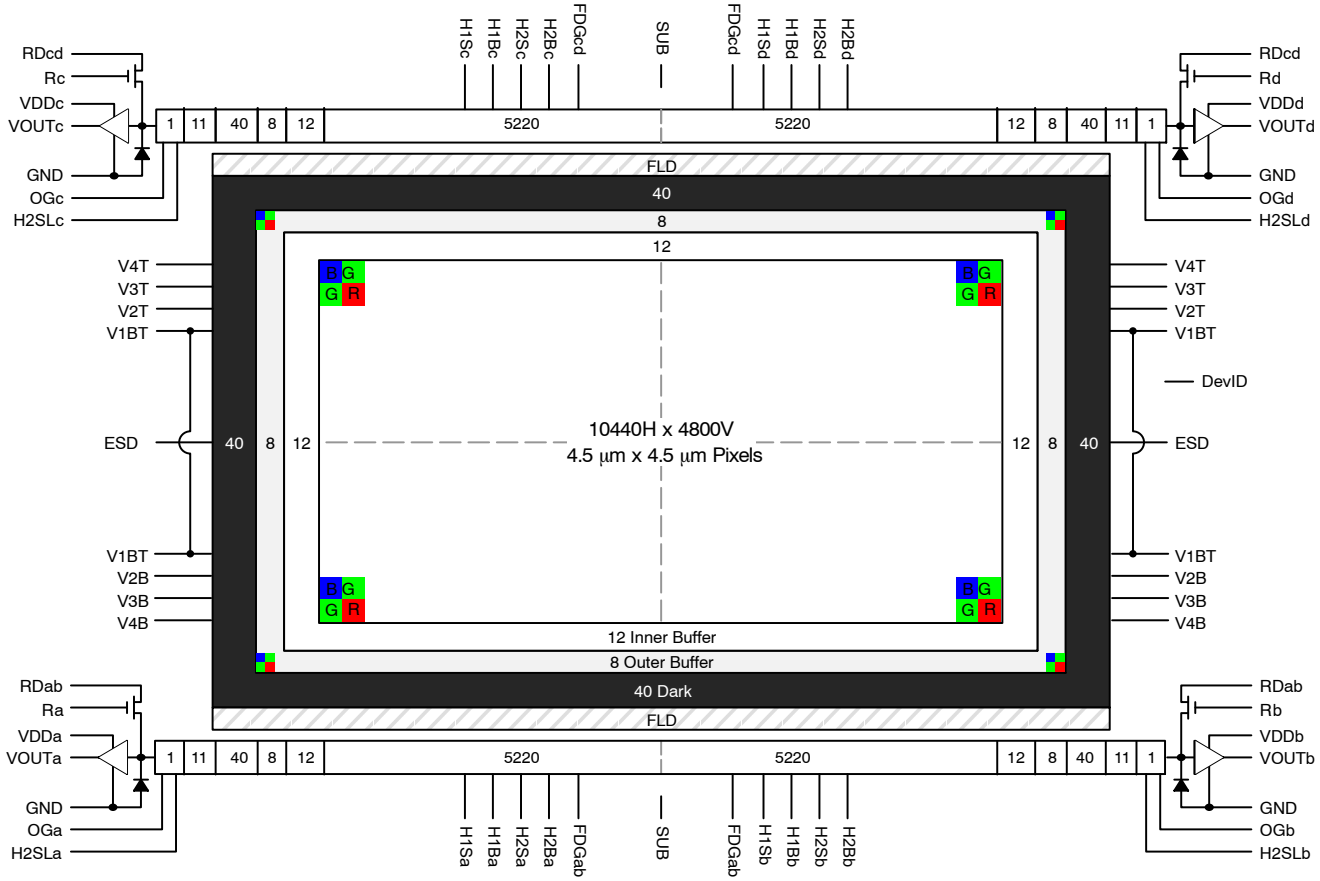


Figure 3. Bayer Color Filter Pattern

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

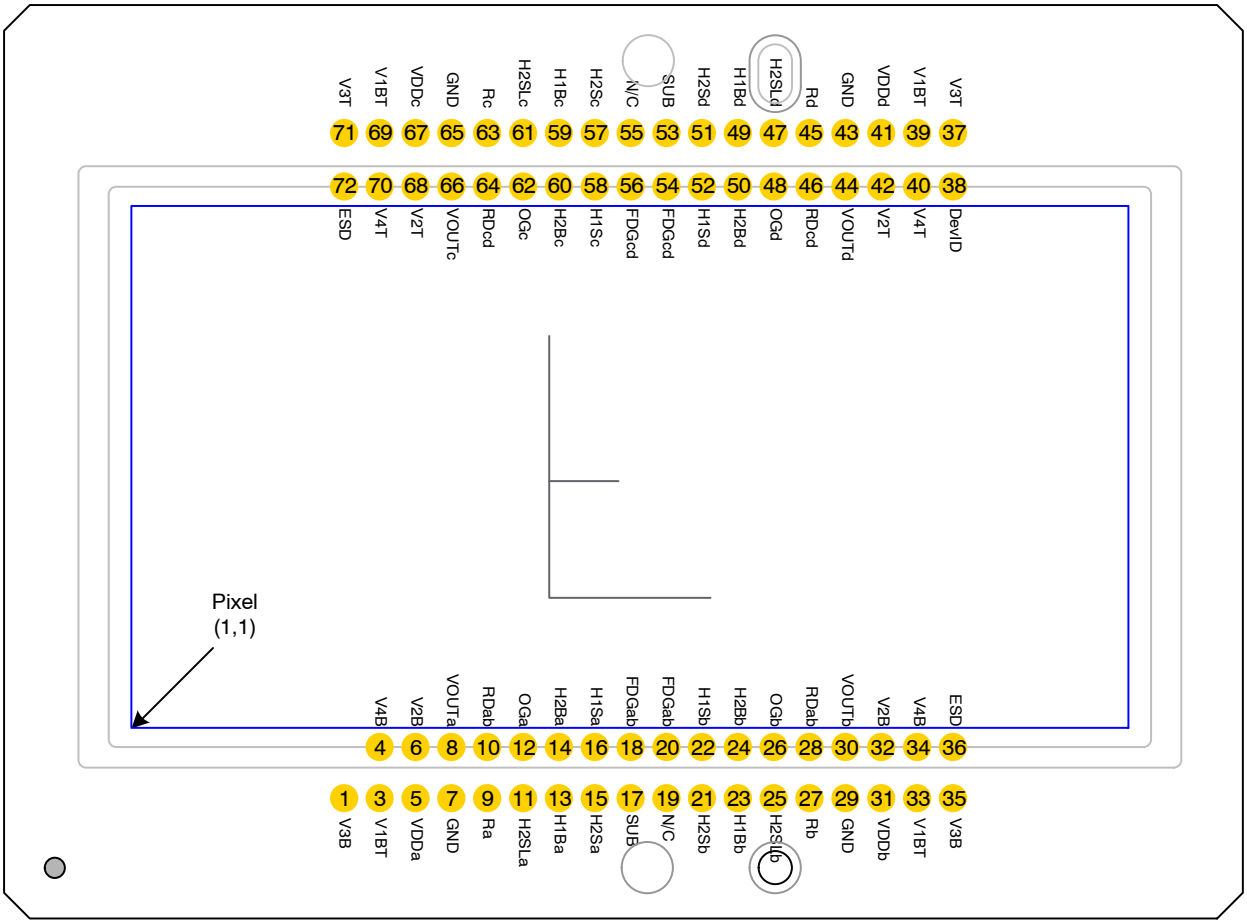


Figure 4. Package Pin Description − Top View

Table 3. PIN DESCRIPTION

Pin	Name	Description	Pin	Name	Description
1	V3B	Vertical CCD Clock, Phase 3, Bottom	72	ESD	ESD Protection Disable
			71	V3T	Vertical CCD Clock, Phase 3, Top
3	V1BT	Vertical CCD Clock, Phase 1, Bottom and Top	70	V4T	Vertical CCD Clock, Phase 4, Top
4	V4B	Vertical CCD Clock, Phase 4, Bottom	69	V1BT	Vertical CCD Clock, Phase 1, Bottom and Top
5	VDDa	Output Amplifier Supply, Quadrant a	68	V2T	Vertical CCD Clock, Phase 2, Top
6	V2B	Vertical CCD Clock, Phase 2, Bottom	67	VDDc	Output Amplifier Supply, Quadrant c
7	GND	Ground	66	VOUTc	Video Output, Quadrant c
8	VOUTa	Video Output, Quadrant a	65	GND	Ground
9	Ra	Reset Gate, Quadrant a	64	RDcd	Reset Drain, Quadrants c and d
10	RDab	Reset Drain, Quadrants a and b	63	Rc	Reset Gate, Quadrant c
11	H2SLa	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a	62	OGc	Output Gate, Quadrant c
12	OGa	Output Gate, Quadrant a	61	H2SLc	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c
13	H1Ba	Horizontal CCD Clock, Phase 1, Barrier, Quadrant a	60	H2Bc	Horizontal CCD Clock, Phase 2, Barrier, Quadrant c
14	H2Ba	Horizontal CCD Clock, Phase 2, Barrier, Quadrant a	59	H1Bc	Horizontal CCD Clock, Phase 1, Barrier, Quadrant c
15	H2Sa	Horizontal CCD Clock, Phase 2, Storage, Quadrant a	58	H1Sc	Horizontal CCD Clock, Phase 1, Storage, Quadrant c
16	H1Sa	Horizontal CCD Clock, Phase 1, Storage, Quadrant a	57	H2Sc	Horizontal CCD Clock, Phase 2, Storage, Quadrant c
17	SUB	Substrate	56	FDGcd	Fast Line Dump Gate, Top
18	FDGab	Fast Line Dump Gate, Bottom	55	N/C	No Connect
19	N/C	No Connect	54	FDGcd	Fast Line Dump Gate, Top
20	FDGab	Fast Line Dump Gate, Bottom	53	SUB	Substrate
21	H2Sb	Horizontal CCD Clock, Phase 2, Storage, Quadrant b	52	H1Sd	Horizontal CCD Clock, Phase 1, Storage, Quadrant d
22	H1Sb	Horizontal CCD Clock, Phase 1, Storage, Quadrant b	51	H2Sd	Horizontal CCD Clock, Phase 2, Storage, Quadrant d
23	H1Bb	Horizontal CCD Clock, Phase 1, Barrier, Quadrant b	50	H2Bd	Horizontal CCD Clock, Phase 2, Barrier, Quadrant d
24	H2Bb	Horizontal CCD Clock, Phase 2, Barrier, Quadrant b	49	H1Bd	Horizontal CCD Clock, Phase 1, Barrier, Quadrant d
25	H2SLb	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b	48	OGd	Output Gate, Quadrant b
26	OGb	Output Gate, Quadrant b	47	H2SLd	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d
27	Rb	Reset Gate, Quadrant b	46	RDcd	Reset Drain, Quadrants c and d
28	RDab	Reset Drain, Quadrants a and b	45	Rd	Reset Gate, Quadrant d
29	GND	Ground	44	VOUTd	Video Output, Quadrant d
30	VOUTb	Video Output, Quadrant b	43	GND	Ground
31	VDDb	Output Amplifier Supply, Quadrant b	42	V2T	Vertical CCD Clock, Phase 2, Top
32	V2B	Vertical CCD Clock, Phase 2, Bottom	41	VDDd	Output Amplifier Supply, Quadrant d
33	V1BT	Vertical CCD Clock, Phase 1, Bottom and Top	40	V4T	Vertical CCD Clock, Phase 4, Top
34	V4B	Vertical CCD Clock, Phase 4, Bottom	39	V1BT	Vertical CCD Clock, Phase 1, Bottom and Top
35	V3B	Vertical CCD Clock, Phase 3, Bottom	38	DevID	Device Identification
36	ESD	ESD Protection Disable	37	V3T	Vertical CCD Clock, Phase 3, Top

1. Like named pins are internally connected and should have a common drive signal.
2. N/C pins (19, 55) should be left floating.

IMAGING PERFORMANCE

Table 4. TYPICAL OPERATION CONDITIONS

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

Description	Condition	Notes
Light Source	Continuous Red, Green and Blue LED Illumination	For monochrome sensor, only green LED used
Operation	Nominal operating voltages and timing	

Table 5. PERFORMANCE PARAMETERS

Performance parameters are by design

Description		Symbol	Nom.	Units	Notes
Maximum Photo−response Nonlinearity		NL	2	%	2
Horizontal CCD Charge Capacity		HNe	40	ke^-	
Vertical CCD Charge Capacity		VNe	16	ke^-	
Photodiode Charge Capacity		PNe	13	ke^-	3
Image Lag		Lag	< 10	e^-	
Anti−blooming Factor		Xab	> 300X		
Vertical Smear		Smr	−98	dB	7
Read Noise		n_{e-T}	13	e^-rms	4
Dynamic Range		DR	60	dB	4, 5
Output Amplifier DC Offset		Vodc	8	V	
Output Amplifier Bandwidth		f_{-3db}	398	MHz	6
Output Amplifier Impedance		Rout	80	Ω	
Output Amplifier Sensitivity		ΔV/ΔN	42	$\mu V/e^-$	
Peak Quantum Efficiency (KAI − 50140 − AXA and KAI − 50140 − QXA Configurations)		QEmax	45	%	
Peak Quantum Efficiency (KAI − 50140 − AXA and KAI − 50140 − QXA Configurations)	Blue Green Red	QEmax	37 34 27	%	

Table 6. PERFORMANCE SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Temperature Tested At (°C)	Notes
Dark Field Global Non−Uniformity	DSNU	−	−	5	mVpp	40	
Bright Field Global Non−Uniformity	BSNU	−	−	5	%rms	20, 40	1
Bright Field Global Peak to Peak Non−Uniformity	PRNU	−	−	30	%pp	20, 40	1
Maximum Gain Difference Between Outputs	ΔG	−	−	10	%	20, 40	2
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	−		20, 40	
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	−		20, 40	
Photodiode Dark Current	Ipd	−	7	50	e/p/s	20, 40	
Vertical CCD Dark Current	Ivd	−	50	200	e/p/s	20, 40	

1. Per color.
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is 546 mV.
4. At 60 MHz.
5. Uses 20 × LOG (PNe/ n_{e-T}).
6. $f_{-3dB} = 1 / (2\pi \cdot R_{OUT} \cdot C_{LOAD})$ where C_{LOAD} = 5 pF.
7. Green LED illumination.

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome with Microlens

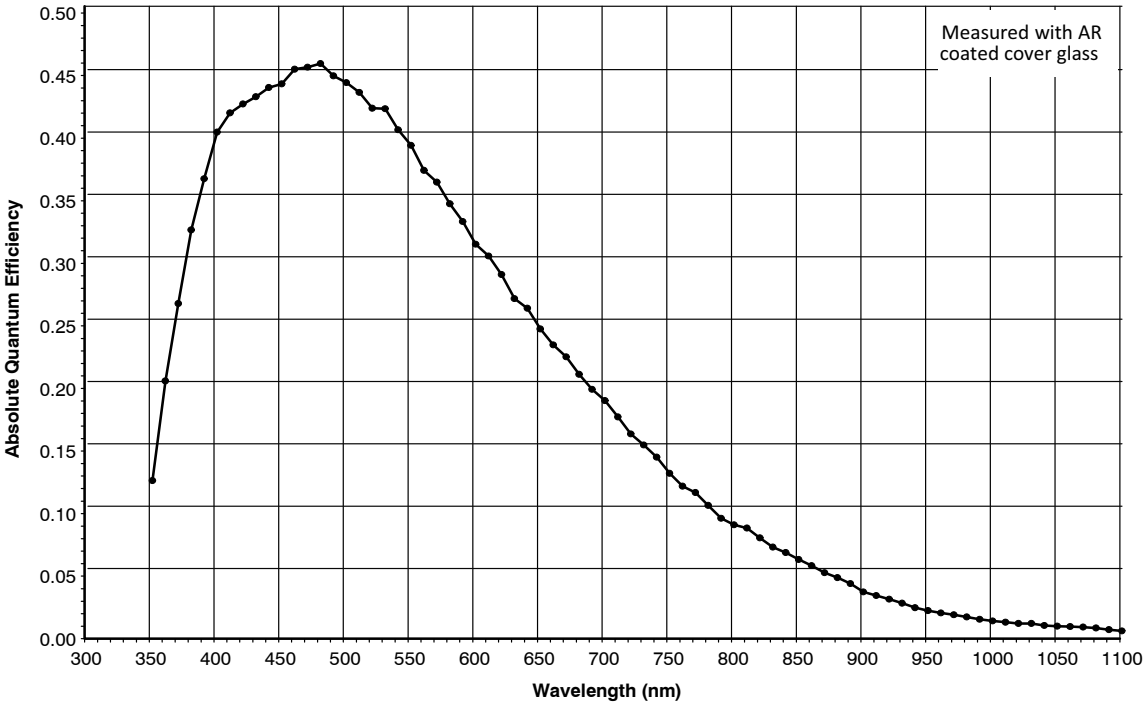


Figure 5. Monochrome with Microlens Quantum Efficiency

Gen2 Color (Bayer RGB) with Microlens

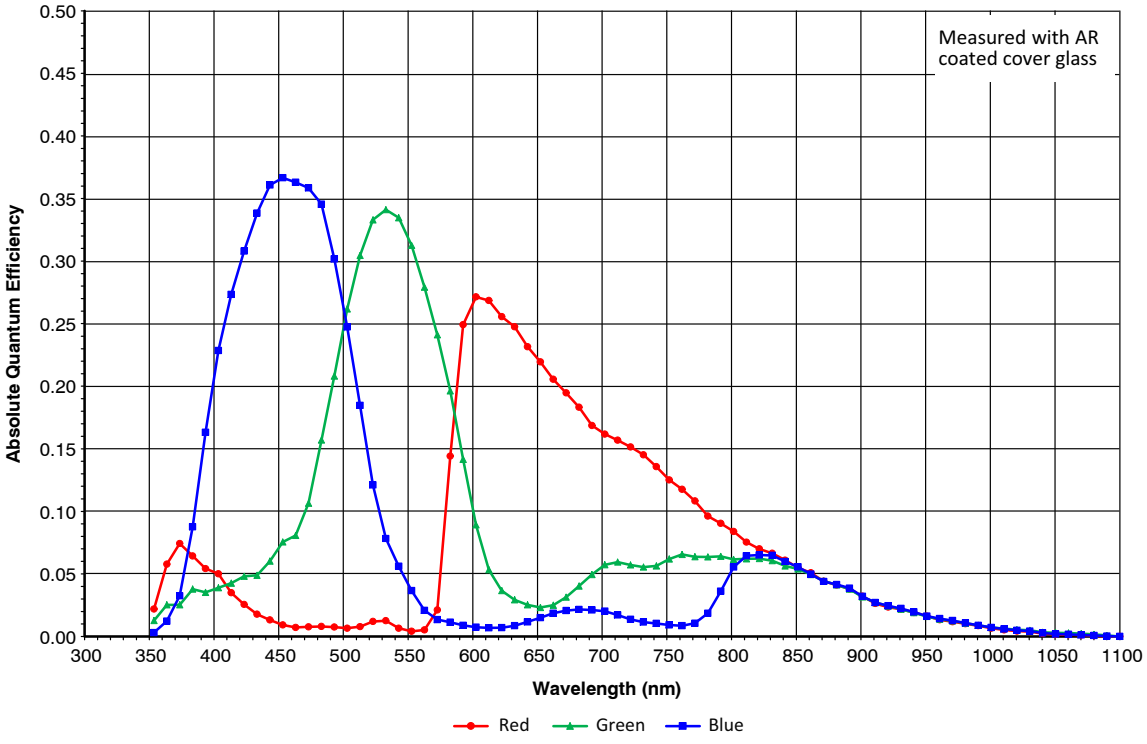


Figure 6. Gen2 Color (Bayer RGB) with Microlens Quantum Efficiency

Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.
For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

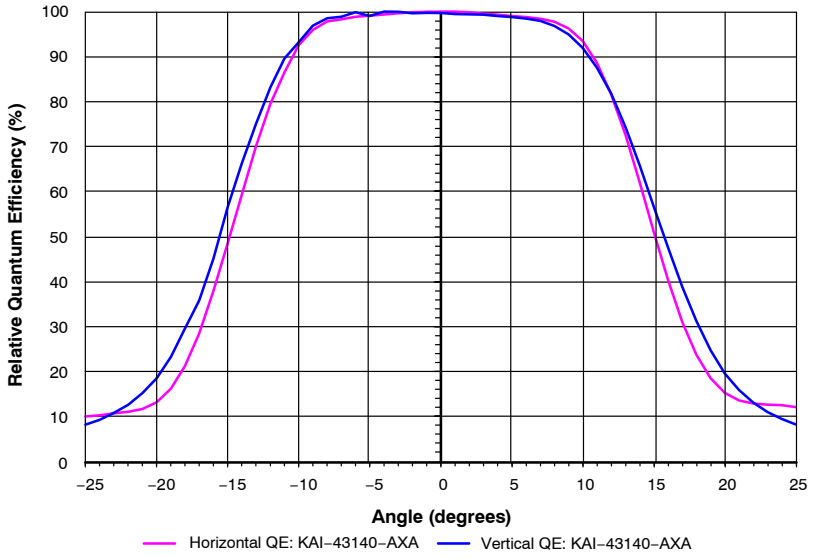


Figure 7. Monochrome with Microlens Angular Quantum Efficiency

Dark Current versus Temperature

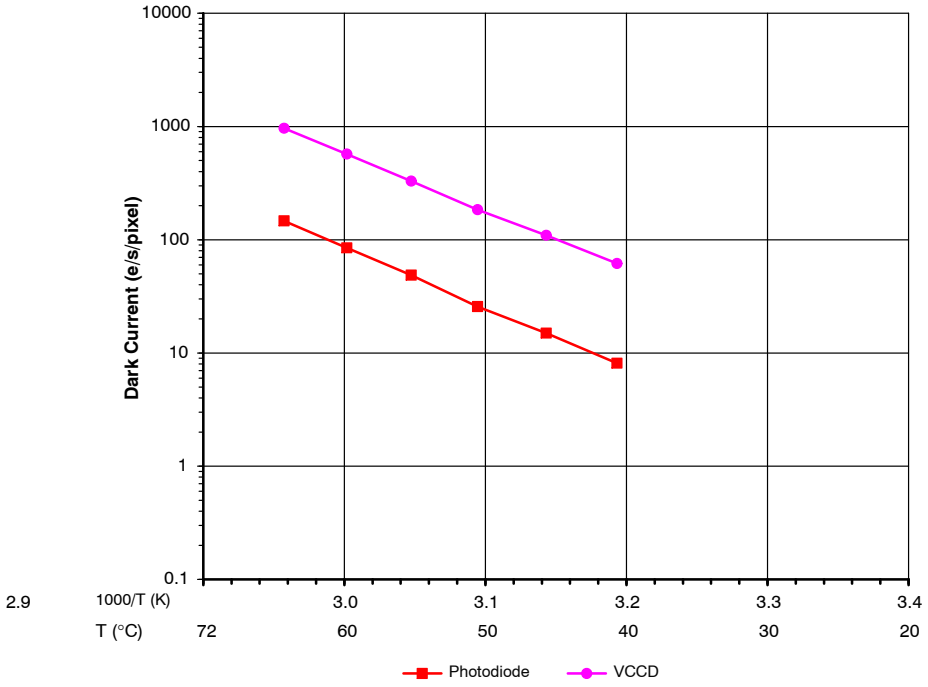


Figure 8. Dark Current vs. Temperature

Power-Estimated

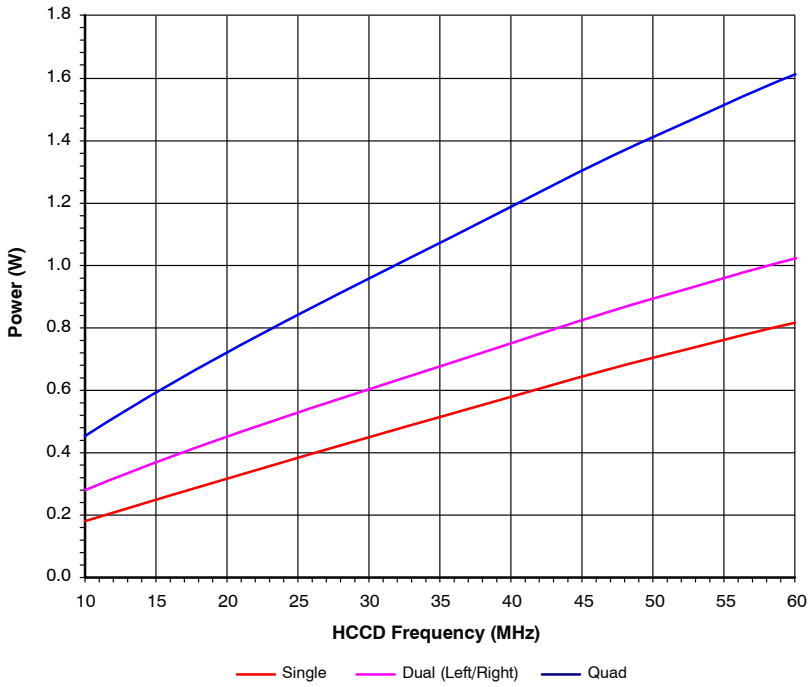


Figure 9. Power

Frame Rates

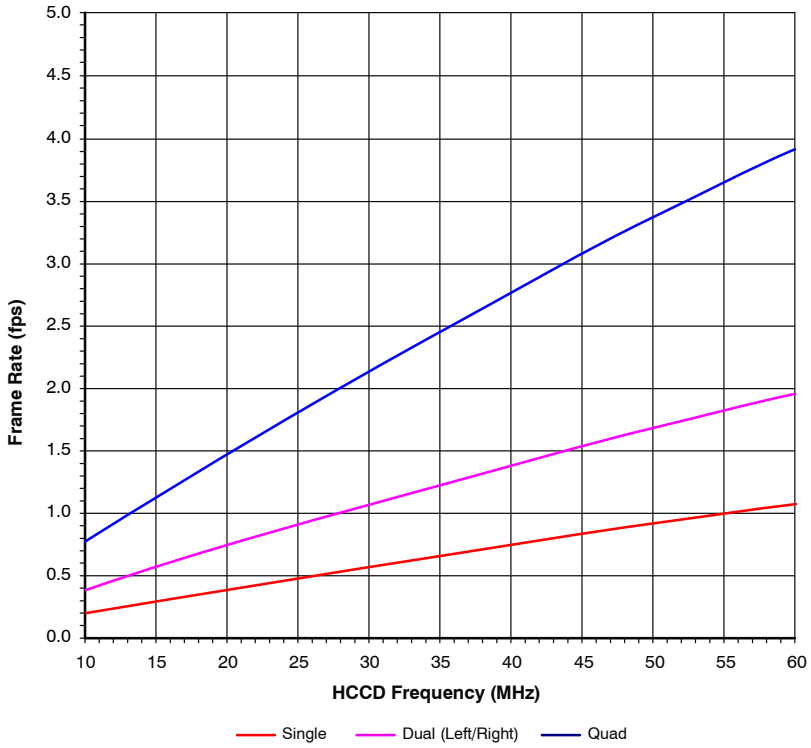


Figure 10. Frame Rates

DEFECT DEFINITIONS

Table 7. OPERATING CONDITIONS

Description	Condition	Notes
Light Source	Continuous Red, Green, Blue, and/or Blue LED Illumination	For the monochrome sensor, only the green LED is used
Operation	Nominal Operating Voltages and Timing	

Table 8. OPERATING PARAMETERS

Description	1 Output	4 Outputs
HCCD Clock Frequency	20 MHz	20 MHz
Pixels Per Line	10560	5280
Lines Per Frame	4920	2460
Line Time	549.6 μs	285.6 μs
Frame Time	2704.1 ms	702.7 ms

Table 9. TIMING MODES

Timing Modes	Conditions
Mode A	1 Output, no electronic shutter used. Photodiode integration time is equal to the Frame Time
Mode B	4 Outputs, no electronic shutter used. Photodiode integration time is equal to the Frame time

Table 10. DEFECT DEFINITIONS

Description	Definition	Grade 1	Grade 2 (mono)	Grade 2 (color)
Column Defect	A group of more than 10 contiguous pixels along a single column that deviate from the neighboring columns by: • more than 97 mV in the dark field using Timing Mode A at 40°C • more than 97 mV in the dark field using Timing Mode A at 20°C • more than −12% or +16% in the bright field using Timing Mode A at 20°C or 40°C	0	7	2
Cluster Defect	A group of 2 to N contiguous defective pixels, but no more than W adjacent defects horizontally, that deviate from the neighboring pixels by: • more than 570 mV in the dark field using Timing Mode A at 40°C • more than 268 mV in the dark field using Timing Mode A at 20°C • more than −12% or +16% in the bright field using Timing Mode A at 20°C or 40°C	30 W = 4 N−19	70 W = 5 N−38	70 W = 5 N−38
Major Point Defect	A single defective pixel that deviates from the neighboring pixels by: • more than 570 mV in the dark field using Timing Mode A at 40°C • more than 268 mV in the dark field using Timing Mode A at 20°C • more than −12% or +16% in the bright field using Timing Mode A at 20°C or 40°C	400	800	800
Minor Point Defect	A single defective pixel that deviates from the neighboring pixels by: • more than 285 mV in the dark field using Timing Mode A at 40°C	4000	8000	8000

1. Bright field is define as where the average signal level of the sensor is 382 mV, with the substrate voltage set to the recommend VAB setting such that the capacity of the photodiodes is 546 mV (13,000 electrons).
2. For the color devices (KAI−50140−FXA or KAI−50140−QXA), a bright field defective pixel is with respect to pixels of the same color.
3. Column and cluster defects are separated by no less than two (2) non−defective pixels in any direction (excluding single pixel defects).

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps.

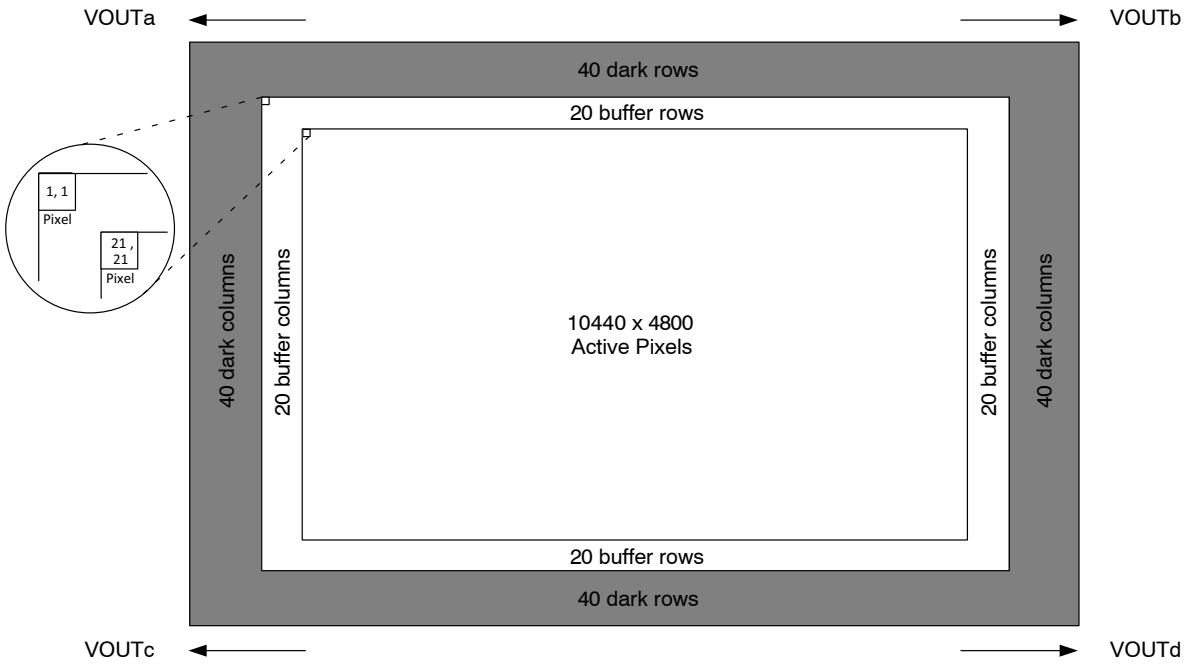


Figure 11. Pixel 1, 1 Location

OPERATION

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

The KAI−50140 image sensors have configurations with epoxy sealed cover glass. The seal formed is non−hermetic, and may allow moisture ingress over time, depending on the storage environment. As a result, care must be taken to avoid cooling the device below the dew point inside the package cavity, since this may result in condensation on the sensor. For all KAI−50140 configurations, no warranty, expressed or implied, covers condensation.

Table 11. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	Top	−50	+60	°C	1
Parameter Specification Temperature Range	TPSR	+20	+40	°C	2
Output Bias Current, Total for Each Output	Iout	–	−15	mA	3

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Device degradation is not evaluated outside of these temperature ranges.
2. The device will operate effectively within a specified temperature range. Performance may not be guaranteed per the PERFORMANCE SPECIFICATION table for temperatures that are different than those specified within. Noise performance may degrade beyond the specification at die temperatures higher than specified here. Additionally, charge transfer may degrade beyond the specification at temperatures lower than specified here.
3. Avoid shorting output pins to ground or any low impedance source during operation. Irreparable damage will occur and is not covered by warranty. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

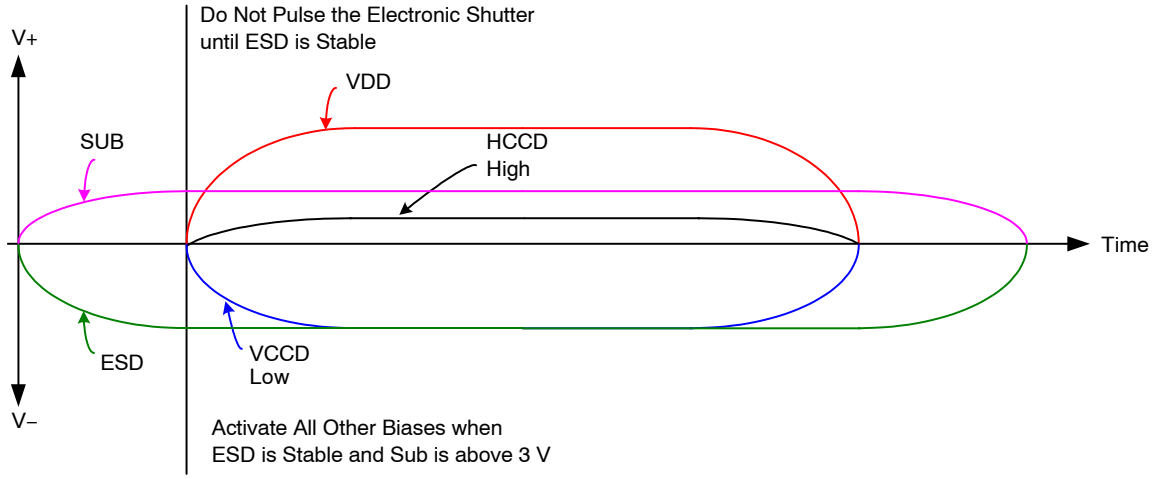
Table 12. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

Description	Minimum	Maximum	Units	Notes
VDDα, VOUTα	−0.4	+17.5	V	1
RDα	−0.4	+15.5	V	1
V1TB	ESD − 0.4	ESD + 24.0	V	
V2B, V2T, V3B, V3T, V3B, V3T	ESD − 0.4	ESD + 14.0	V	
FDGab, FDGcd	ESD − 0.4	ESD + 15.0	V	
H1α, H2α, H2Lα	ESD − 0.4	ESD + 14.0	V	1
Rα	ESD − 0.4	ESD + 20.0	V	1
ESD	−10.0	0.0	V	
SUB	−0.4	40.0	V	2

1. α refers to a, b, c, or d.
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

Power-Up and Power-Down Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.



NOTES:

1. Activate all other biases when ESD is stable and SUB is above 3 V.
2. Do not pulse the electronic shutter until ESD is stable.
3. VDD cannot be +15 V when SUB is 0 V.
4. The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage. See Figure 13.
5. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See Figure 14.

Figure 12. Power-Up and Power-Down Sequence

The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.

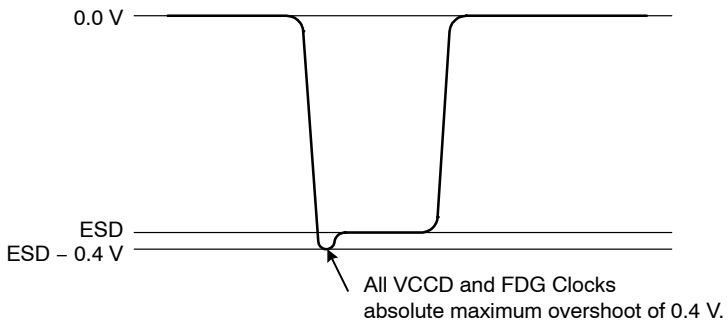


Figure 13. VCCD Clock Overshoots

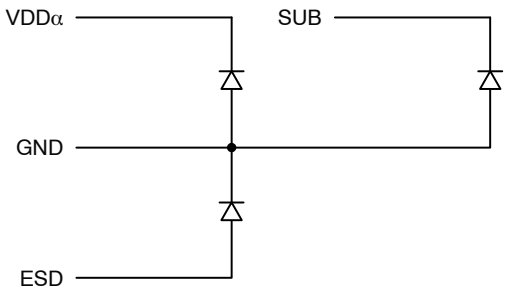


Figure 14. External Diode Protection

Table 13. DC BIAS OPERATING CONDITIONS

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Max. DC Current	Notes
Reset Drain	RDα	RD	+12.3	+12.5	+12.7	V	10 μA	1
Output Gate	OGα	OG	+2.0	+2.2	+2.4	V	10 μA	1
Output Amplifier Supply	VDDα	VDD	+14.5	+15.0	+15.5	V	11 mA	1, 2
Ground	GND	GND	+0.0	+0.0	+0.0	V	−1.0 mA	
Substrate	SUB	VSUB	+5.0	VAB	VDD	V	50 μA	3, 8
ESD Protection Disable	ESD	ESD	−9.2	−9.0	−8.8	V	50 μA	6, 7
Output Bias Current	VOUTα	Iout	−3.0	−5.0	−10.0	mA		1, 4, 5

1. α denotes a, b, c, or d.
2. The maximum DC current is for one output. Idd = Iout + Iss. See Figure 15.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is the nominal PNe (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 60 MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power−Up and Power−Down Sequence section.
7. ESD maximum value must be less than or equal to V1_L − 0.4 V and V2_L − 0.4 V.
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

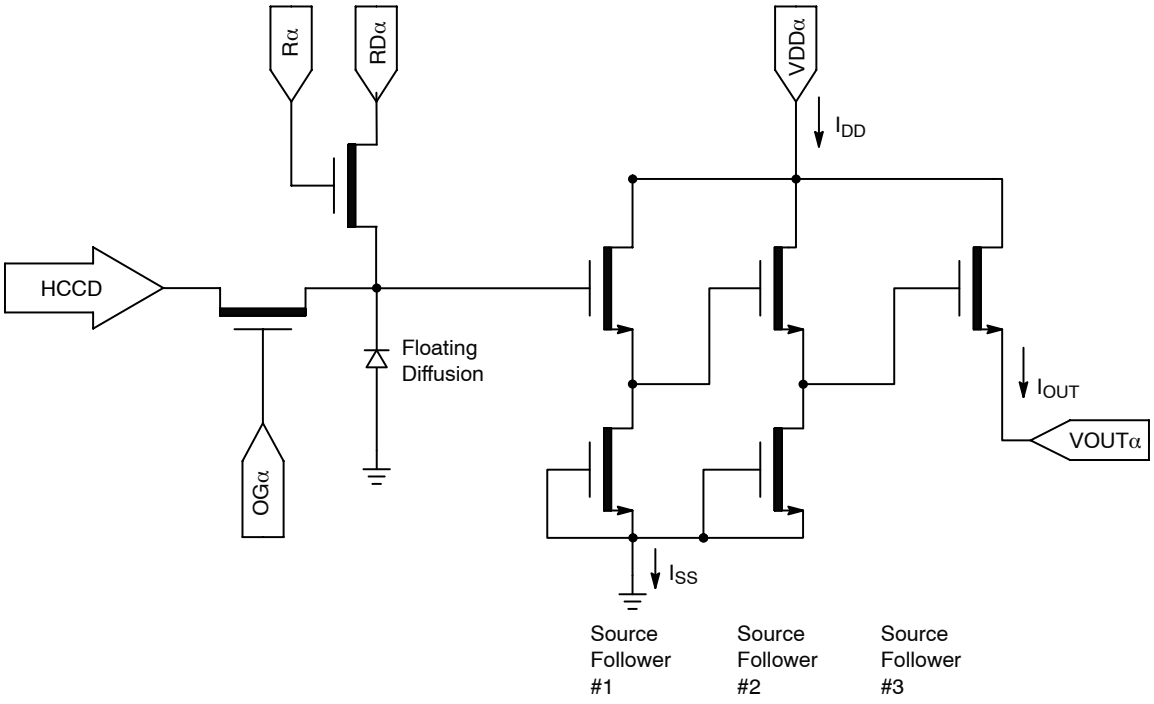


Figure 15. Output Amplifier

AC Operating Conditions

Table 14. CLOCK LEVELS

Description	Pins (Note 1)	Symbol	Level	Minimum	Nominal	Maximum	Units	Capacitance (Note 2)
Vertical CCD Clock, Phase 1	V1B, V1T	V1_L	Low	−8.2	−8.0	−7.8	V	490 nF
		V1_M	Mid	−0.2	0.0	0.2		
		V1_H	High	+10.3	+10.5	+10.7		
Vertical CCD Clock, Phase 2	V2B, V2T	V2_L	Low	−8.2	−8.0	−7.8	V	280 nF
		V2_H	High	−0.2	0.0	+0.2		
Vertical CCD Clock, Phase 3	V3B, V3T	V3_L	Low	−8.2	−8.0	−7.8	V	300 nF
		V3_H	High	−0.2	0.0	+0.2		
Vertical CCD Clock, Phase 4	V4B, V4T	V4_L	Low	−8.2	−8.0	−7.8	V	280 nF
		V4_H	High	−0.2	0.0	+0.2		
Horizontal CCD Clock, Phase 1 Storage	H1Sα	H1S_L	Low	−0.2	0.0	+0.2	V	840 pF
		H1S_H	High	+4.8	+5.0	+5.2		
Horizontal CCD Clock, Phase 1 Barrier	H1Bα	H1B_L	Low	−0.2	0.0	+0.2	V	880 pF
		H1B_H	High	+4.8	+5.0	+5.2		
Horizontal CCD Clock, Phase 2 Storage	H2Sα	H2S_L	Low	−0.2	0.0	+0.2	V	720 pF
		H2S_H	High	+4.8	+5.0	+5.2		
Horizontal CCD Clock, Phase 2 Barrier	H2Bα	H2B_L	Low	−0.2	0.0	+0.2	V	600 pF
		H2B_H	High	+4.8	+5.0	+5.2		
Horizontal CCD Clock, Last Phase (Note 3)	H2SLα	H2SL_L	Low	−0.2	0.0	+0.2	V	20 pF
		H2LS_A	High	4.8	+5.0	+5.2		
Reset Gate	Rα	R_L (Note 4)	Low	+2.0	+.3.0	+3.2	V	20 pF
		R_H	High	+6.8	+7.0	+7.2		
Electronic Shutter (Note 5, 8)	SUB	VES	High	–	–	+40	V	14 nF
		VES_ Offset	Offset	VAB+24	VAB+25	–	V	
Fast Line Dump Gate	FDGab, FDGcd	FDG_L	Low	−8.2	−8.0	−7.8	V	260 pF
		FDG_H	High	+4.5	+5.0	+5.5		

1. α denotes a, b, c, or d.
2. Capacitance is total for all like named pins.
3. Use separate clock driver for improved speed performance.
4. Reset low should be set to +2.0 volts for signal levels greater than 26,000 electrons.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*
6. Capacitance values are estimated.
7. If the minimum horizontal clock low level is used (−0.2 V), then the maximum horizontal clock amplitude should be used (5 V amplitude) to create a −2.0 V to 4.8 V clock.
8. Figure 16 shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground. The VES_Offset is referenced to VSUB.

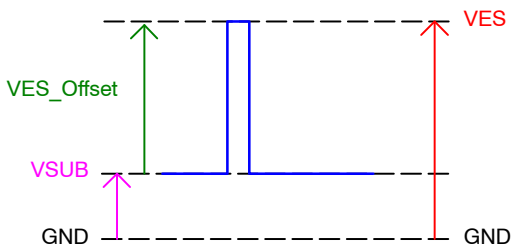


Figure 16. VSUB and VES Reference

Device Identification

The device identification pin (DevID) may be used to determine which ON Semiconductor 4.5 micron pixel interline CCD sensor is being used.

Table 15. DEVICE IDENTIFICATION

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Max. DC Current	Notes
Device Identification	DevID	DevID	4,000	5,000	6,000	Ω	50 μA	1, 2, 3

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

Recommended Circuit

Note that V1 must be a different value than V2.

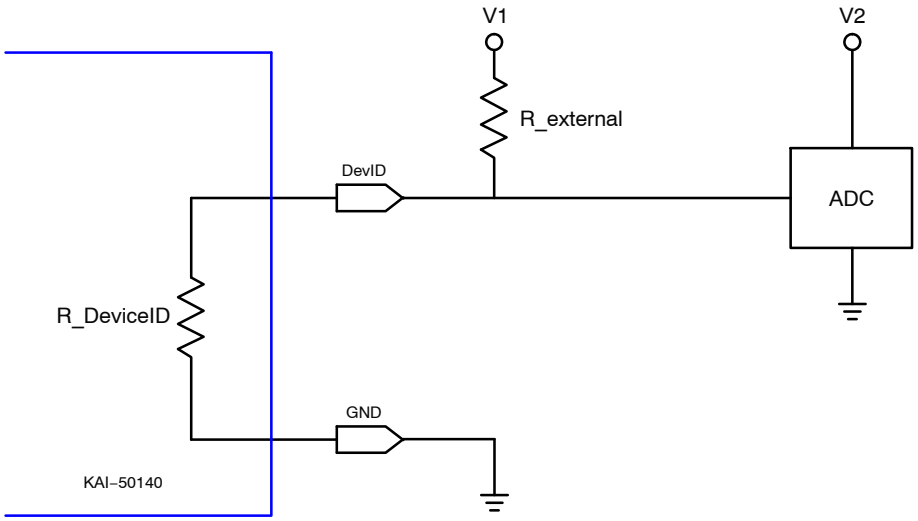


Figure 17. Device Identification Recommended Circuit

TIMING

Table 16. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Photodiode Transfer	T_{PD}	6	−	−	μs	
VCCD Leading Pedestal	T_{3P}	16	−	−	μs	
VCCD Trailing Pedestal	T_{3D}	16	−	−	μs	
VCCD Transfer Delay	T_D	4	−	−	μs	
VCCD Transfer	T_V	10	−	−	μs	
VCCD Clock Cross-Over	V_{VCR}	75	−	100	%	1
VCCD Rise, Fall Time	T_{VR}, T_{VF}	5	−	10	%	1, 2
FDG Delay	T_{FDG}	5	−	−	μs	
HCCD Delay	T_{HS}	1	−	−	μs	
HCCD Transfer	T_E	16.66	−	−	ns	
Shutter Transfer	T_{SUB}	1	−	−	μs	
Shutter Delay	T_{HD}	1	−	−	μs	
Reset Pulse	T_R	2.5	−	−	ns	
Reset − Video Delay	T_{RV}	−	2.2	−	ns	
H2SL − Video Delay	T_{HV}	−	3.1	−	ns	
Line Time	T_{LINE}	104.2	−	−	μs	Dual/Quad HCCD Readout
		192.2	−	−		Single HCCD Readout
Frame Time	T_{FRAME}	256.4	−	−	ms	Quad HCCD Readout
		512.7	−	−		Dual HCCD Readout
		945.7	−	−		Single HCCD Readout

1. Refer to Figure 22: VCCD Clock Rise Time, Fall Time and Edge Alignment.
2. Relative to the pulse width.

Timing Flow Charts

The timing sequence for the clocked device pins may be represented as one of seven patterns (P1 − P7) as shown in the table below. The patterns are defined in Figure 18 and Figure 19. Contact ON Semiconductor Application Engineering for other readout modes.

Table 17. TIMING SEQUENCES

Device Pin	Quad Readout	Dual Readout VOUTa, VOUTb	Dual Readout VOUTa, VOUTc	Single Readout VOUTa
V1BT	P1BT	P1BT	P1BT	P1BT
V2T	P2T	P4B	P2T	P4B
V3T	P3T	P3B	P3T	P3B
V4T	P4T	P2B	P4T	P2B
V1BT	P1BT			
V2B	P2B			
V3B	P3B			
V4B	P4B			
H1Sa	P5			
H1Ba				
H2Sa (Note 2)	P6			
H2Ba				
Ra	P7			
H1Sb	P5		P5	
H1Bb			P6	
H2Sb (Note 2)	P6		P6	
H2Bb			P5	
Rb	P7		P7 (Note 1) or Off (Note 3)	P7 (Note 1) or Off (Note 3)
H1Sc	P5	P5 (Note 1) or Off (Note 3)	P5	P5 (Note 1) or Off (Note 3)
H1Bc				
H2Sc (Note 2)	P6	P6 (Note 1) or Off (Note 3)	P6	P6 (Note 1) or Off (Note 3)
H2Bc				
Rc	P7	P7 (Note 1) or Off (Note 3)	P7	P7 (Note 1) or Off (Note 3)
H1Sd	P5	P5 (Note 1) or Off (Note 3)	P5	P5 (Note 1) or Off (Note 3)
H1Bd			P6	
H2Sd (Note 2)	P6	P6 (Note 1) or Off (Note 3)	P6	P6 (Note 1) or Off (Note 3)
H2Bd			P5	
Rd	P7	P7 (Note 1) or Off (Note 3)	P7 (Note 1) or Off (Note 3)	P7 (Note 1) or Off (Note 3)

# Lines/Frame (Minimum)	2460	4920	2460	4920
# Pixels/Line (Minimum)	5292		10572	

1. For optimal performance of the sensor. May be clocked at a lower frequency. If clocked at a lower frequency, the frequency selected should be a multiple of the frequency used on the a and b register.
2. H2SLx follows the same pattern as H2Sx For optimal speed performance, use a separate clock driver.
3. Off = R_H for the Reset Gate and H_H for the Horizontal CCD gates. Note that there may be operating conditions (high temperature and/or very bright light sources) that will cause blooming from the unused c/d register into the image area.

Photodiode Transfer Timing

A row of charge is transferred to the HCCD on the falling edge of V1 as indicated in the P1 pattern below. Using this timing sequence, the leading dummy row or line is combined with the first dark row in the HCCD. The “Last Line” is dependent on readout mode – either 5292 or 10572 minimum counts required. It is important to note that, in general, the rising edge of a vertical clock (patterns P1 − P4) should be coincident or slightly leading a falling edge at the same time interval. This is particularly true at the point where P1 returns from the high (3rd level) state to the mid − state when P4 transitions from the low state to the high state.

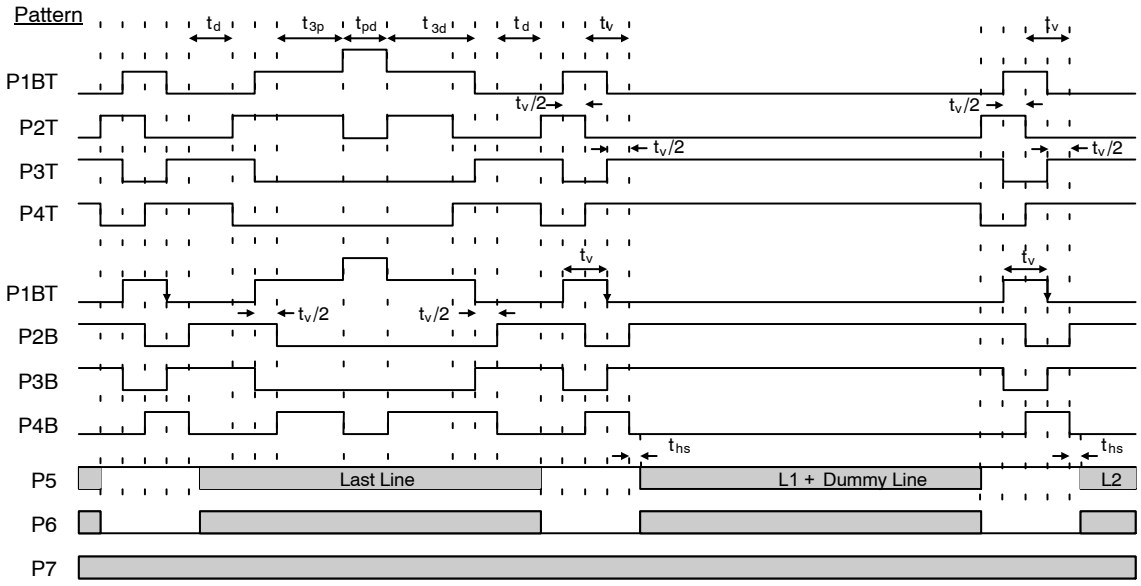


Figure 18. Photodiode Transfer Timing

Line and Pixel Timing

Each row of charge is transferred to the output, as illustrated below, on the falling edge of H2SL (indicated as P6 pattern). The number of pixels in a row is dependent on readout mode – either 5292 or 10572 minimum counts required.

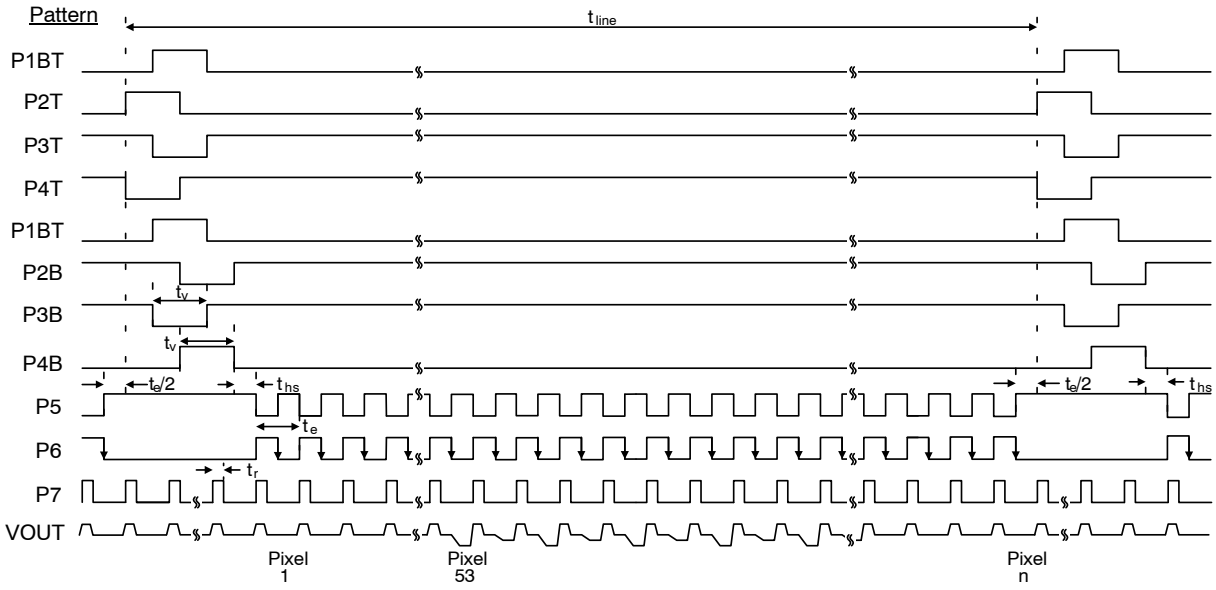


Figure 19. Line and Pixel Timing

Pixel Timing Detail

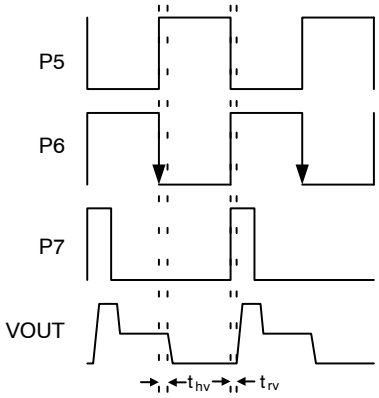


Figure 20. Pixel Timing Detail

Frame/Electronic Shutter Timing

The SUB pin may be optionally clocked to provide electronic shuttering capability as shown below. The resulting photodiode integration time is defined from the falling edge of SUB to the falling edge of V1 (P1 pattern).

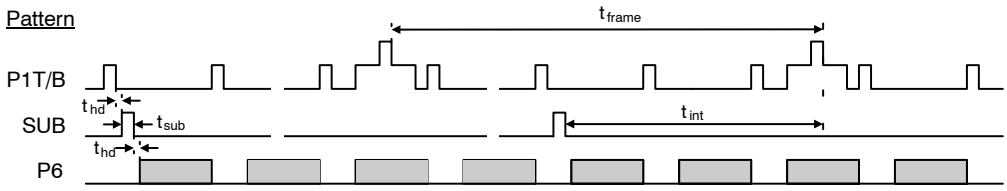


Figure 21. Electronic Shutter Timing

VCCD Clock Edge Alignment

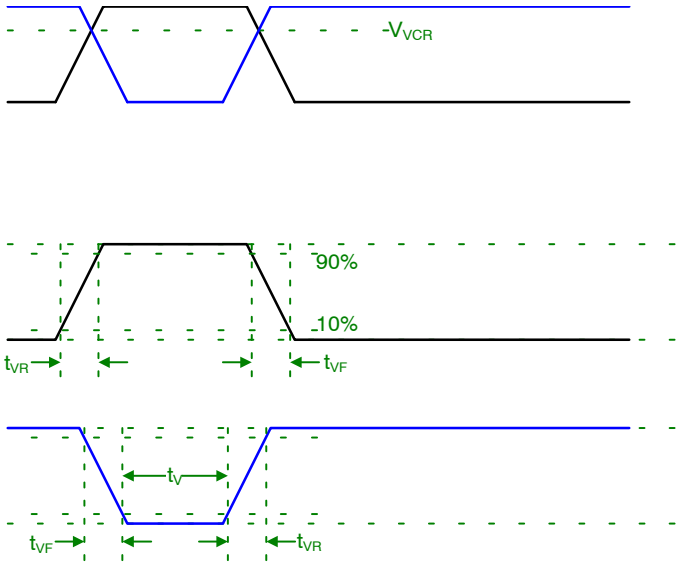


Figure 22. VCCD Clock Rise Time, Fall Time and Edge Alignment

Line and Pixel Timing − Vertical Binning by 2

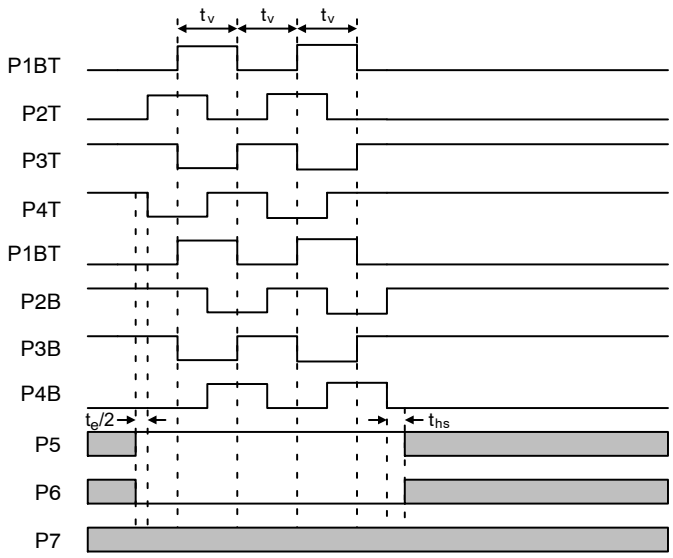


Figure 23. Line and Pixel Timing − Vertical Binning by 2

Fast Line Dump Timing

The FDG pins may be optionally clocked to efficiently remove unwanted lines in the image resulting for increased frame rates at the expense of resolution. Below is an example of a 2 line dump sequence followed by a normal readout line.

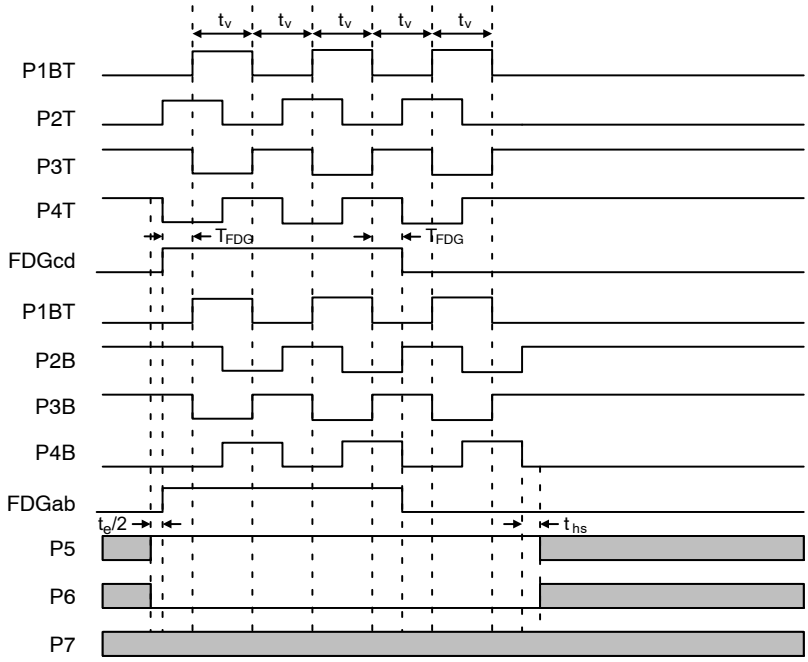


Figure 24. Fast Line Dump Timing

STORAGE AND HANDLING DETAILS

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com. Please note that CCD products are not shipped or stored in Moisture Barrier Bags (MBB) and Moisture Sensitivity Level (MSL) ratings are not specified.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For information on charge binning, please download the KAE−08151 Charge Binning Application Note (AND9569/D) from www.onsemi.com.

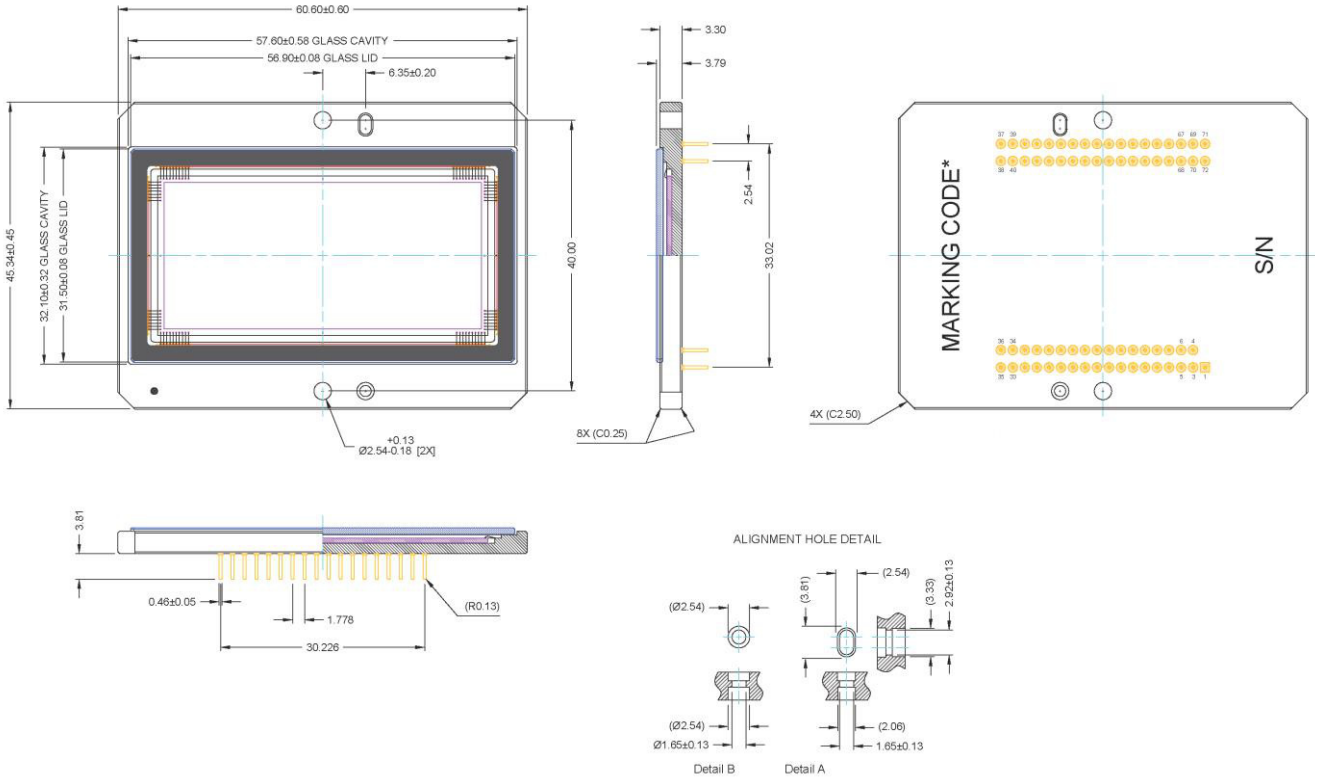
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

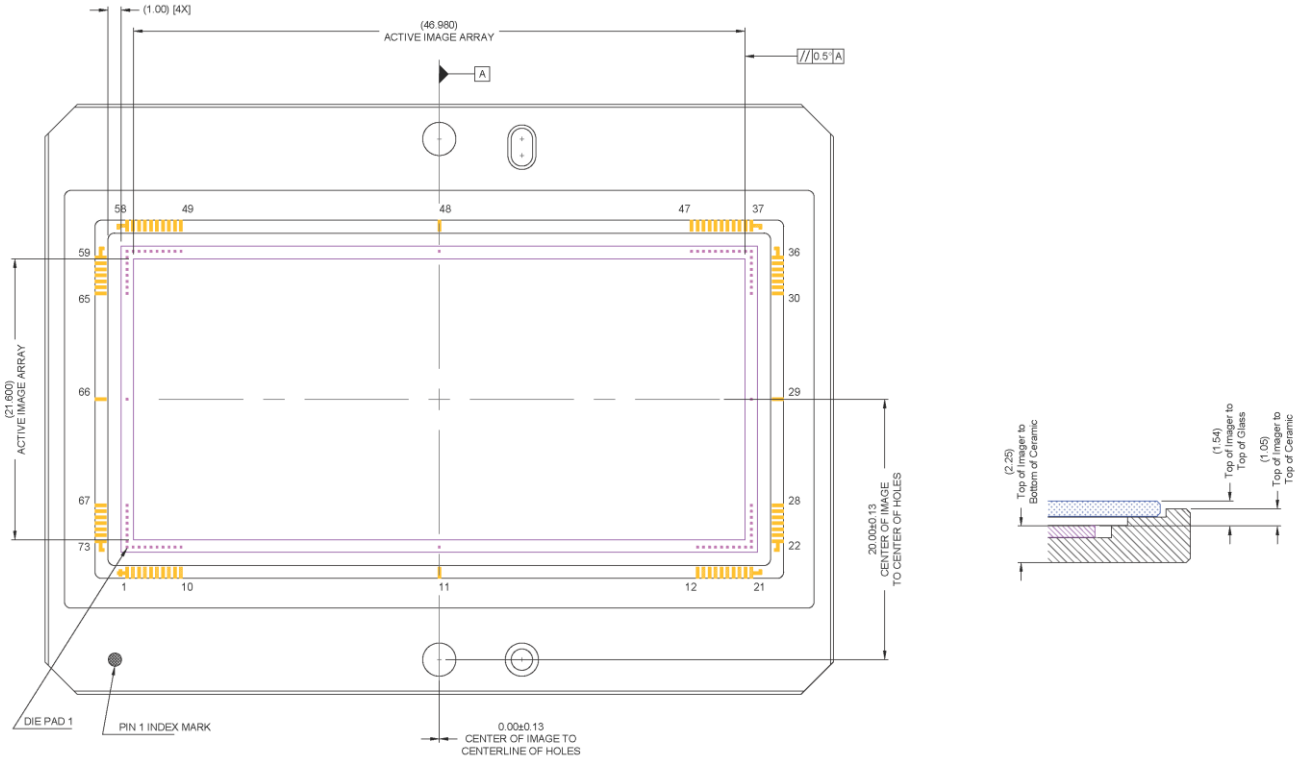
Completed Assembly



Notes:

1. See Ordering Information for marking code.
2. Glass epoxy not to extend over image array.
3. No materials to interfere with clearance through package holes.
4. Units: mm

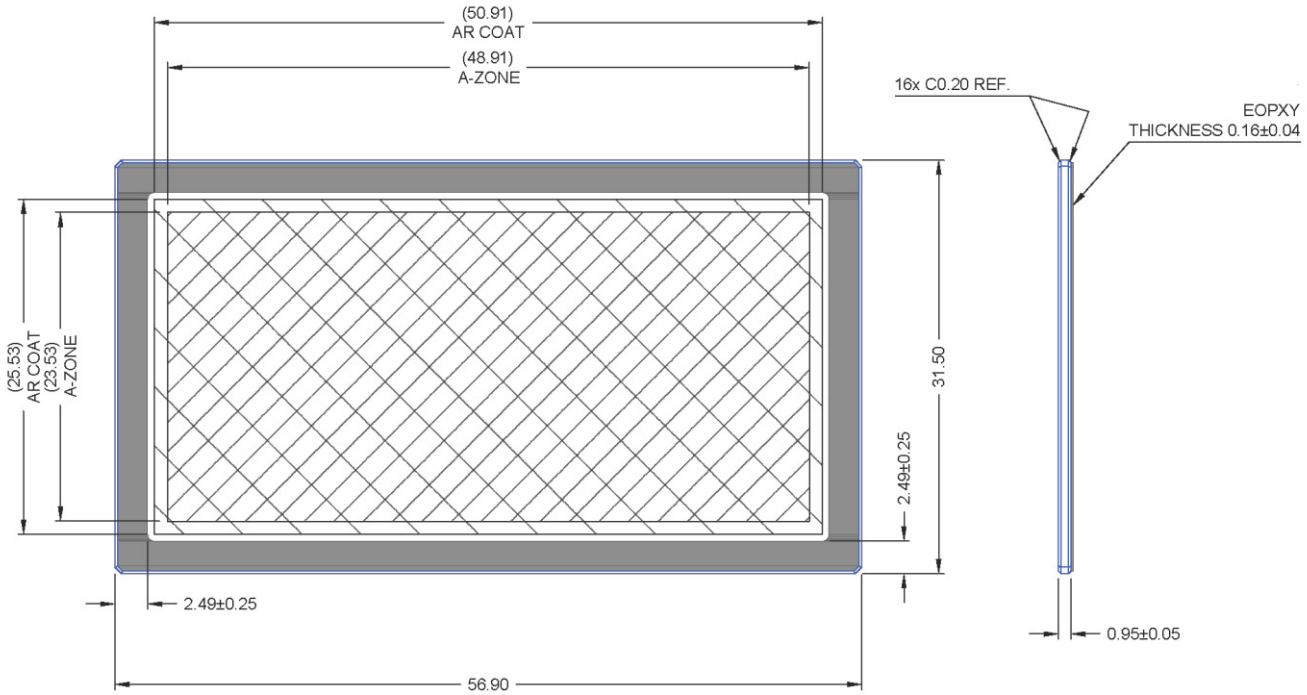
Figure 25. Completed Assembly (1 of 2)



Notes:
1. Units: mm

Figure 26. Completed Assembly (2 of 2)

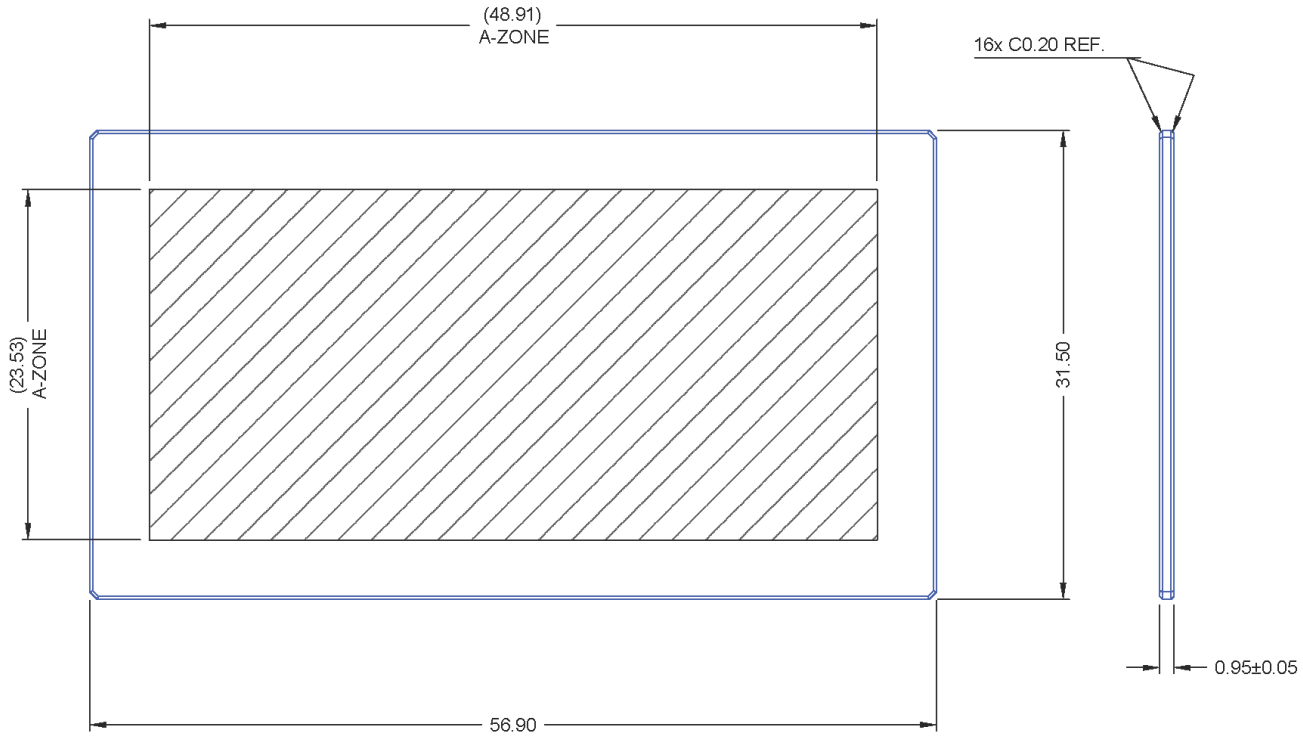
Cover Glass



Notes:

1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification:
   a. 20 μm Max size in Zone A
3. MAR coated both sides
4. Spectral Transmission
   a. 350 − 365 nm: T ≥ 88%
   b. 365 − 405 nm: T ≥ 94%
   c. 405 − 450 nm: T ≥ 98%
   c. 450 − 650 nm: T ≥ 99%
   e. 650 − 690 nm: T ≥ 98%
   f. 690 − 770 nm: T ≥ 94%
   g. 770 − 870 nm: T ≥ 88%
5. Units: mm

Figure 27. Cover Glass with AR Coatings



1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification:
   a. 20 microns maximum size in Zone A
3. Units: mm
4. Cover glass does not have epoxy

Figure 28. Cover Glass without AR Coatings

Cover Glass Transmission

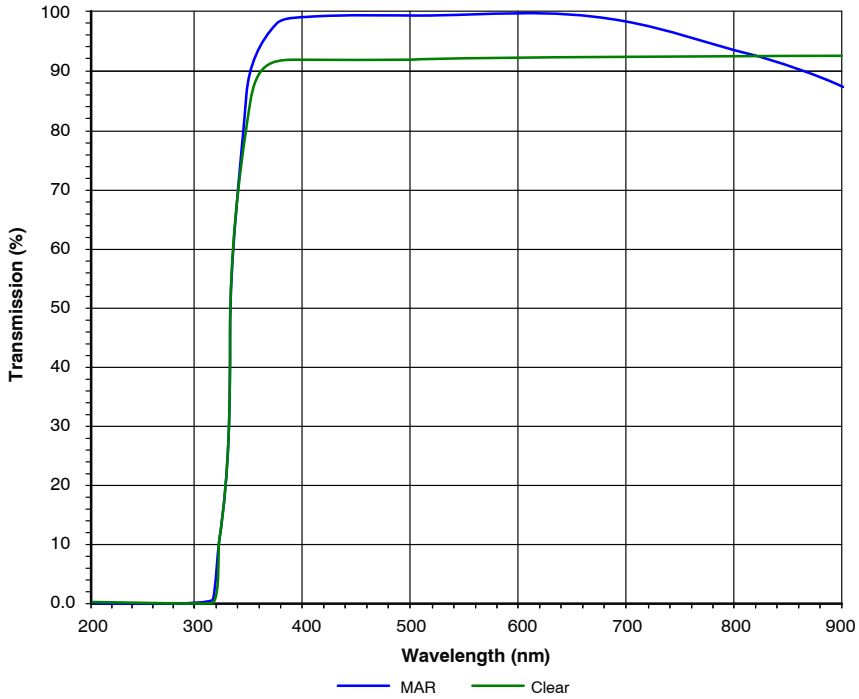


Figure 29. Cover Glass Transmission

PUBLICATION ORDERING INFORMATION

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9