GLS55LC200
NAND Controller (CompactFlash Interface)

Fact Sheet 01.000
February 2012

Features

- **Supports CompactFlash Revision 3.0 Standard Interface**
  - Host Interface: 16-bit access
  - Supports up to PIO Mode-6
  - Supports up to Multi-word DMA Mode-4
  - Supports up to Ultra DMA Mode-4
- **Interface for Standard NAND Flash Media**
  - Flash Media Interface: Single or Dual 8-bit access
    - Supports up to 4 flash media devices per channel
    - Supports up to 8 flash media devices directly
  - Supports Single-Level Cell (SLC) or Multi-Level Cell (MLC) flash media
    -2 KByte and 4 KByte program page size
- **3.3V Power Supply and NAND Flash Interface**
- **5.0V or 3.3V Host Interface Through V_{DDQ} Pins**
- **Low Current Operation**
  - Active mode:
    25 mA/35 mA (3.3V/5.0V) (typical)
  - Sleep mode:
    80 µA/100 µA (3.3V/5.0V) (typical)
- **Power Management Unit**
  - Immediate disabling of unused circuitry without host intervention
  - Zero wake-up latency
- **20-Byte Unique ID for Enhanced Security**
  - Factory pre-programmed 10-Byte unique ID
  - User-programmable 10-Byte ID
- **Programmable, Multitasking NAND Interface**
- **Firmware Storage in Embedded SuperFlash®**
- **Pre-programmed Embedded Firmware**
  - Performs self-initialization on first system Power-on
  - Executes industry-standard CompactFlash commands
  - Implements advanced wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
- **Built-in Hardware ECC**
  - Corrects up to 8 random single-bit errors per 512-byte sector
- **Built-in Internal System Clock**
- **Multi-tasking Technology Enables Fast Sustained Write Performance (Host to Flash)**
  - Supports up to 30 MByte/sec
- **Fast Sustained Read Performance (Flash to Host)**
  - Up to 30 MByte/sec
- **Automatic Recognition and Initialization of Flash Media Devices**
  - Seamless integration into a standard SMT manufacturing process
  - 5 sec. (typical) for flash drive recognition and setup
- **Commercial and Industrial Temperature Ranges**
  - 0°C to 70°C for commercial operation
  - -40°C to +85°C for industrial operation
- **Packages Available**
  - 100-lead TQFP – 14mm x 14mm
- **All Devices are RoHS Compliant**

Product Description

The GLS55LC200 NAND Controller is the core of a high-performance, flash media-based, data storage system. The controller recognizes the control, address and data signals on the CF bus and translates them into memory accesses for standard NAND-type flash media. Using both Single Level Cell (SLC) and Multi-Level Cell (MLC) flash media, this technology supports solid state mass storage applications by offering new, expanded functionality while enabling smaller, lighter designs with lower power consumption.

The NAND Controller supports standard CF protocols with up to PIO Mode-6, Multi-word DMA Mode-4, and Ultra DMA Mode-4 interface. The CF interface is widely used in products such as portable and desktop computers, digital cameras, music players, handheld data collection scanners, PDAs, handy terminals, personal communicators, audio recorders, monitoring devices and set-top boxes.

The NAND Controller uses SuperFlash® memory technology, and is factory pre-programmed with an embedded flash file system. Upon initial power-on, the GLS55LC200 recognizes the flash media devices, sets up a bad block table, executes all the necessary handshaking routines for flash media support, and, finally, performs the low-level format. This process typically takes about 3 second plus 0.5 seconds per GByte of drive capacity, allowing a 4 GByte flash drive to be fully initialized in about 5 seconds. For added manufacturing flexibility, system debug, re-initialization and user customization can be accomplished through the CF interface.

The GLS55LC200 high-performance NAND Controller offers sustained read and write performance up to 30MByte/sec. The GLS55LC200 directly supports up to eight flash media devices with appropriate output loading and frequency.

The NAND Controller comes pre-programmed with a 10-byte unique serial ID. For even greater system security, the user has the option of programming an additional 10 Bytes of ID space to create a unique, 20-byte ID.

The NAND controller comes packaged in an industry-standard 100-lead TQFP package for easy integration into an SMT manufacturing process.

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GENERAL DESCRIPTION

The NAND Controller contains a microcontroller and embedded flash file system integrated in a TQFP package. Refer to Figure 1 for the NAND Controller block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

Performance-optimized NAND Controller

The NAND Controller translates standard CF signals into flash media data and control signals. The following components contribute to the controller's operation.

Microcontroller Unit (MCU)

The MCU coordinates all related components to complete requested operations.

Internal Direct Memory Access (DMA)

The NAND Controller uses internal DMA which allows instant data transfer from buffer to flash media. This increases the data transfer rate by eliminating the microcontroller overhead associated with the traditional, firmware-based approach.

Power Management Unit (PMU)

The power management unit controls the power consumption of the NAND Controller. It reduces the power consumption of the NAND Controller by putting circuitry not in operation into sleep mode. The PMU has zero wake-up latency.

SRAM Buffer

The NAND Controller performs as an SRAM buffer to optimize the host's data transfer to and from the flash media.

Embedded Flash File System

The embedded flash file system is an integral part of the NAND Controller. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads
2. Provides flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media
3. Keeps track of data file structures

Error Correction Code (ECC)

The NAND Controller uses BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to eight random single-bit errors for each 512-byte block of data.

High performance is achieved through hardware-based error detection and correction.

Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed to provide trace information during debugging process. To aid in validation, always provide the SCI access to PCB design.

Programmable, Multi-tasking NAND Interface

The multi-tasking interface enables fast, sustained write and read performance by allowing multiple Read, Program and Erase operations to multiple flash media devices. The programmable NAND interface enables timely support of fast changing NAND technology.

FUNCTIONAL BLOCKS

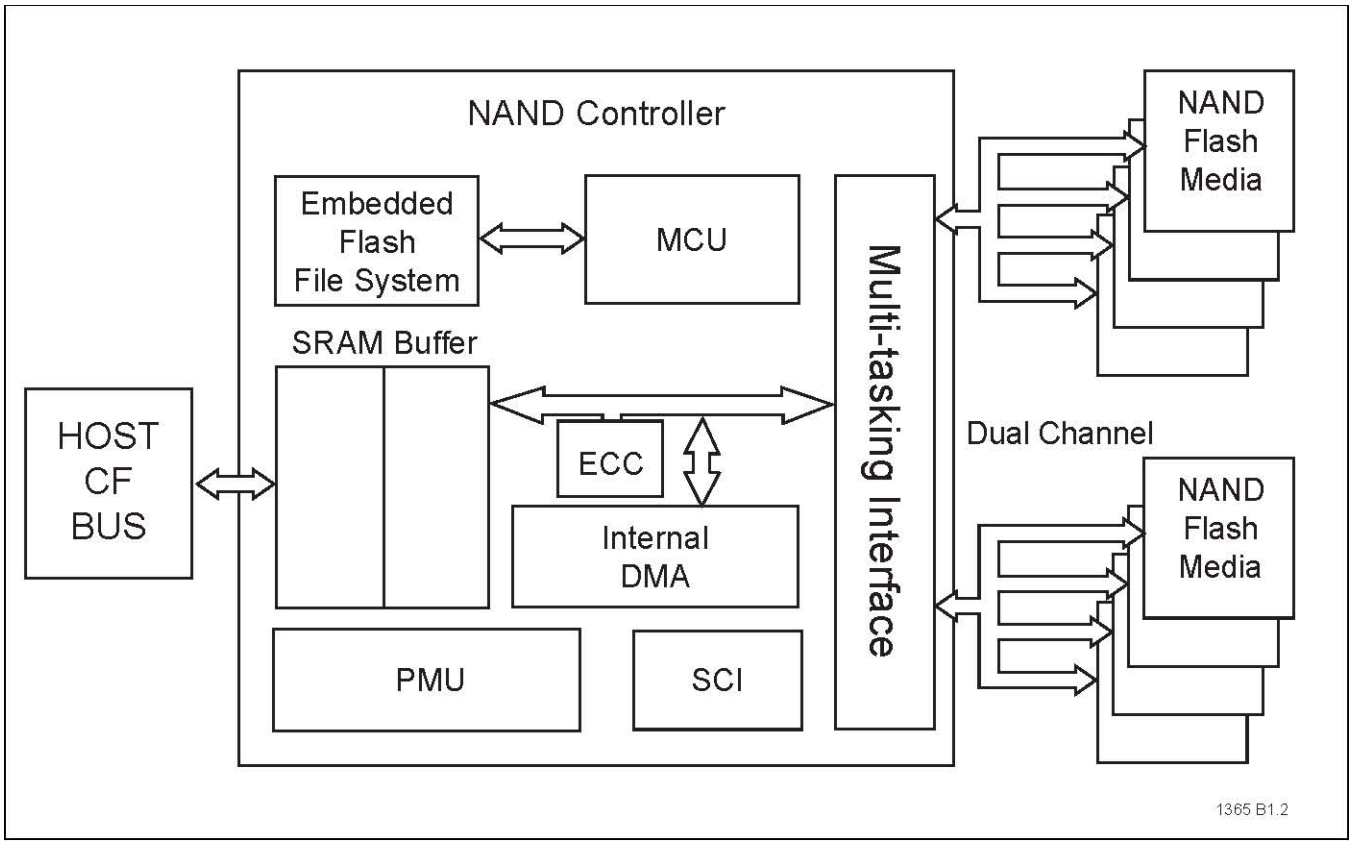

Figure 1: NAND Controller Block Diagram

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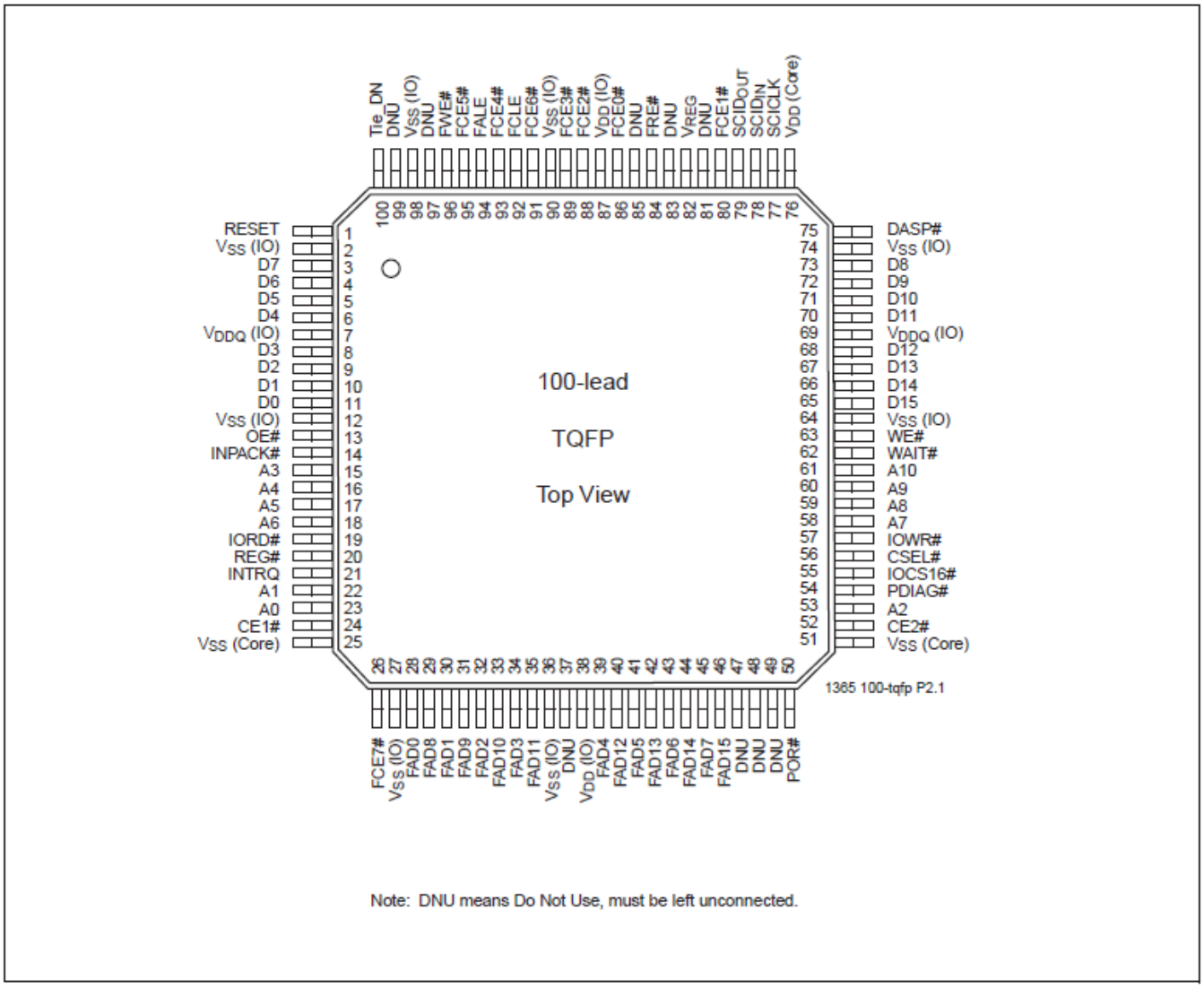
PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 1. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the Host are designated as inputs while signals that the NAND controller sources are outputs.



Note: DNU means Do Not Use, must be left unconnected.

Figure 2: Pin Assignments for 100-Lead TQFP

Table 1: Pin Assignments (1 of 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
Host Interface				
A_{10}-A_0 (Memory Card mode)	61 60 59 58	I	I1Z	These address lines, along with the REG# signal, are used to select the following: The I/O port address registers within the NAND, the memory mapped port address registers within the NAND, a byte in the card's information structure and its configuration control and status registers.
A_{10}-A_0 (PC Card I/O mode)	18 17 16 15 53 22 23			This signal is the same as the PC Card Memory mode signal.
A_2-A_0 (True IDE mode)	53 22 23			In True IDE mode only A[2:0] are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host.
A_{10}-A_3	61 60 59 58 18 17 16 15			
BVD1 (Memory Card mode)	54	I/O	I1U, O1	This signal is asserted high as BVD1 is not supported.
STSCHG# (PC Card I/O mode)				This signal is asserted low to alert the host to changes in the Ready and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status register.
PDIAG# (True IDE mode)				In the True IDE mode, this input/output is the Pass Diagnostic signal in the master/slave handshake protocol.
BVD2 (Memory Card mode)	75	I/O	I1U, O6	This signal is asserted high as BVD2 is not supported.
SPKR# (PC Card I/O mode)				This output line is always driven to a high state in I/O mode since the NAND controller does not support the audio function.
DASP# (True IDE mode)				In the True IDE mode, this input/output is the Disk Active/Slave Present signal in the master/slave handshake protocol.
CE1#, CE2# (Memory Card mode)	24 52	I	I2U	**Card Enable:** These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the Odd Byte of the word. CE1# accesses the Even Byte or the Odd Byte of the word depending on A_0 and CE2#. A multiplexing scheme based on A_0, CE1#, CE2# allows 8-bit hosts to access all data on D_0-D_7.
CE1#, CE2# (PC Card I/O mode)				**Card Enable:** This signal is the same as the PC Card Memory mode signal.
CS0#, CS1# (True IDE mode)				In the True IDE mode CS0# is the chip select for the task file registers while CS1# is used to select the Alternate Status register and the Device Control register.

Table 1: Pin Assignments (2 of 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
CSEL# (Memory Card mode)	56	I	I1U	This signal is not used for this mode.
CSEL# (PC Card I/O mode)				This signal is not used for this mode.
CSEL# (True IDE mode)				This internally pulled up signal is used to configure this device as a master or a slave when configured in the True IDE mode. When this pin is grounded, this device is configured as a master. When the pin is open, this device is configured as a slave.
D_{15}-D_0 (Memory Card mode)	65 66 67 68 70 71 72 73 3 4 5 6 8 9 10 11	I/O	I1Z, O2	These lines carry the Data, Commands and Status information between the host and the controller. D_0 is the LSB of the Even Byte of the Word. D_8 is the LSB of the Odd Byte of the Word.
D_{15}-D_0 (PC Card I/O mode)				This signal is the same as the PC Card Memory mode signal.
D_{15}-D_0 (True IDE mode)				In True IDE mode, all Task File operations occur in Byte-Mode on the low order bus D_7-D_0 while all data transfers are 16 bit using D_{15}-D_0.
INPACK# (Memory Card mode)	14	O	O1	This signal is not used in this mode.
INPACK# (PC Card I/O mode)				The Input Acknowledge signal is asserted by the NAND when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the NAND and the CPU.
DMARQ (True IDE mode)				In True IDE mode DMA request to host.
IORD# (Memory Card mode)	19	I	I2U	This signal is not used in this mode.
IORD# (PC Card I/O mode)				This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the NAND when the card is configured to use the I/O interface.
IORD# (True IDE mode)				In True IDE mode, this signal has the same function as in PC card I/O mode.
HDMARDY# (True IDE mode)				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY# to pause an Ultra DMA transfer.
HSTROBE (True IDE mode)				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.

Table 1: Pin Assignments (3 of 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
IOWR# (Memory Card mode)	57	I	I2U	This signal is not used in this mode.
IOWR# (PC Card I/O mode)				The I/O Write strobe pulse is used to clock I/O data on the card data bus into the NAND controller registers when the NAND is configured to use the I/O interface.
IOWR# (True IDE mode)				In True IDE mode, this signal has the same function as in PC Card I/O mode.
STOP (True IDE mode)				When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst
OE# (Memory Card mode)	13	I	I2U	This is an Output Enable strobe generated by the host interface. It is used to read data from the NAND in Memory mode and to read the CIS and configuration registers.
OE# (PC Card I/O mode)				In PC Card I/O mode, this signal is used to read the CIS and configuration registers.
ATASEL# (True IDE mode)				To enable True IDE mode this input should be grounded by the host.
Ready (Memory Card mode)	21	O	O1	In Memory mode this signal is set high when the NAND is ready to accept a new data transfer operation and held low when the card is busy. At power up and at Reset, the Ready signal is held low (busy) until the NAND has completed its power up or reset function. No access of any type should be made to the NAND during this time.
IREQ# (PC Card I/O mode)				I/O Operation - After the NAND has been configured for I/O operation, this signal is used as Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE mode)				In True IDE mode signal is the active high Interrupt Request to the host.
REG# (Memory Card mode)	20	I	I2U	This signal is used during Memory cycles to distinguish between Common Memory and Register (Attribute) Memory Attribute Memory Select accesses. High for Common Memory, Low for Attribute Memory.
REG# (PC Card I/O mode)				The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
DMACK (True IDE mode)				In True IDE mode DMA Acknowledge - input from host.
RESET (Memory Card mode)	1	I	I2U	When the pin is high, this signal Resets the NAND. The NAND is Reset only at power up if this pin is left high or open from power-up. The NAND is also Reset when the Soft-Reset bit in the Card Configuration Option register is set.
RESET (PC Card I/O mode)				This signal is the same as the PC Card Memory mode signal.
RESET# (True IDE mode)				In the True IDE mode this input pin is the active low hardware reset from the host.

Table 1: Pin Assignments (4 of 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
WAIT# (Memory Card mode)	62	O	O1	The WAIT# signal is driven low by the NAND to signal the host to delay completion of a memory or I/O cycle that is in progress.
WAIT# (PC Card I/O mode)				This signal is the same as the PC Card Memory mode signal.
IORDY# (True IDE mode)				In true IDE mode, except in Ultra DMA modes, this signal may be used as IORDY.
DDMARDY# (True IDE mode)				When Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer.
DSTROBE (True IDE mode)				When Ultra DMA mode DMA Write is active, this signal is the data-out strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
WE# (Memory Card mode)	63	I	I2U	This is a signal driven by the host and used for strobing memory write data to the registers of the NAND when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
WE# (PC Card I/O mode)				In PC Card I/O mode, this signal is used for writing the configuration registers.
WE# (True IDE mode)				In True IDE mode this input signal is not used and should be connected to V_{DD} by the host.
WP (Memory Card mode)	55	O	O2	The NAND does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
IOIS16# (PC Card I/O mode)				When the NAND is configured for I/O Operation Pin 55 is used for the I/O# Selected is 16-bit Port (IOIS16#) function. A Low signal indicates that a 16 bit or Odd Byte only operation can be performed at the addressed port.
IOCS16# (True IDE mode)				In True IDE mode this output signal is asserted low when this device is expecting a word data transfer cycle.

Table 1: Pin Assignments (5 of 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
Flash Media Interface				
FRE#	84	O	O5	Active Low Flash Media Chip Read
FWE#	96	O	O5	Active Low Flash Media Chip Write
FCLE	92	O	O5	Active High Flash Media Chip Command Latch Enable
FALE	94	O	O5	Active High Flash Media Chip Address Latch Enable
FAD15	46	I/O	I3U/O5	Flash Media Chip High Byte Address/Data Bus pins
FAD14	44			
FAD13	42			
FAD12	40			
FAD11	35			
FAD10	33			
FAD9	31			
FAD8	29			
FAD7	45	I/O	I3U/O5	Flash Media Chip Low Byte Address/Data Bus pins
FAD6	43			
FAD5	41			
FAD4	39			
FAD3	34			
FAD2	32			
FAD1	30			
FAD0	28			
FCE7#	26	O	O4	Active Low Flash Media Chip Enable pin
FCE6#	91			
FCE5#	95			
FCE4#	93			
FCE3#	89			
FCE2#	88			
FCE1#	80			
FCE0#	86			
Serial Communication Interface (SCI)				
SCICLK	77	I	I3U	SCI interface clock
$SCID_{IN}$	78	I	I3U	SCI interface data input
$SCID_{OUT}$	79	O	O4	SCI interface data output
Miscellaneous				
V_{DD} (core)	76	PWR		V_{DD} (3.3V)
V_{DD} (IO)	38 87	PWR		V_{DD} (3.3V)
V_{DDQ} (IO)	7 69	PWR		V_{DDQ} (5V/3.3V) for Host interface
V_{REG}	82	O		External capacitor pin. Connect this pin with a 4.7uF capacitor to ground.

Table 1: Pin Assignments (6 of 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
V_{SS} (core)	25 51	PWR		Ground for core
V_{SS} (IO)	2 12 27 36 64 74 90 98	PWR		Ground for I/O
POR#	50	I	Analog Input[2]	**Power-on Reset (POR):** Active Low
Tie_DN	100			Pin must be connected to V_{SS}
DNU[3]	37 47 48 49 81 83 85 97 99			Do Not Use, must be left unconnected.

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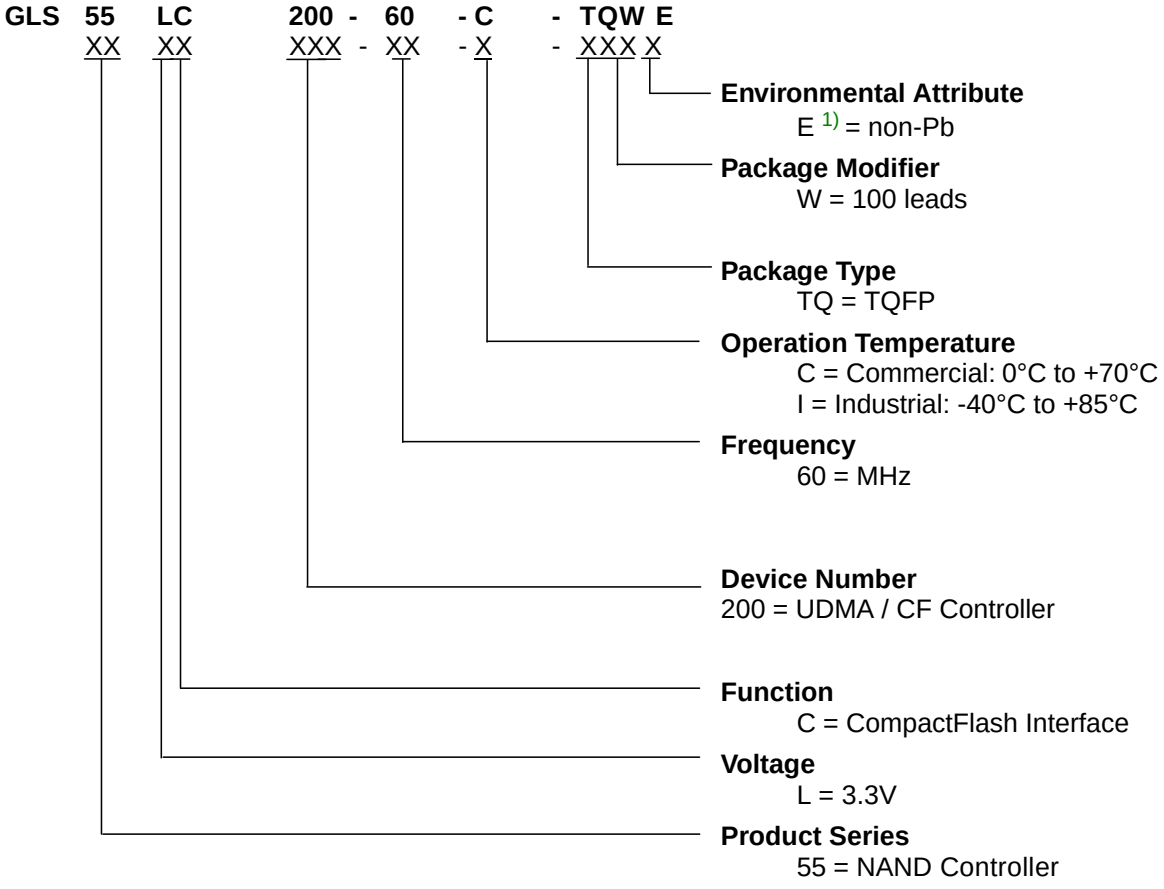
1. IxU = Input with on-chip pull-up.
   IxZ = Input without on-chip pull-up.
2. Analog input for supply voltage detection
3. All DNU pins should not be connected.

PRODUCT ORDERING INFORMATION



1) Environmental suffix "E" denotes non-Pb solder. Greenliant non-Pb solder devices are "RoHS Compliant."

Valid Combinations 2)

GLS55LC200-60-C-TQWE

GLS55LC200-60-I-TQWE

2) Valid product combinations are those that are in the mass production or will be in the mass production. Consult your Greenliant sales representative to confirm availability of the valid product combinations and to determine availability of new product combinations.

PACKAGING DIAGRAM

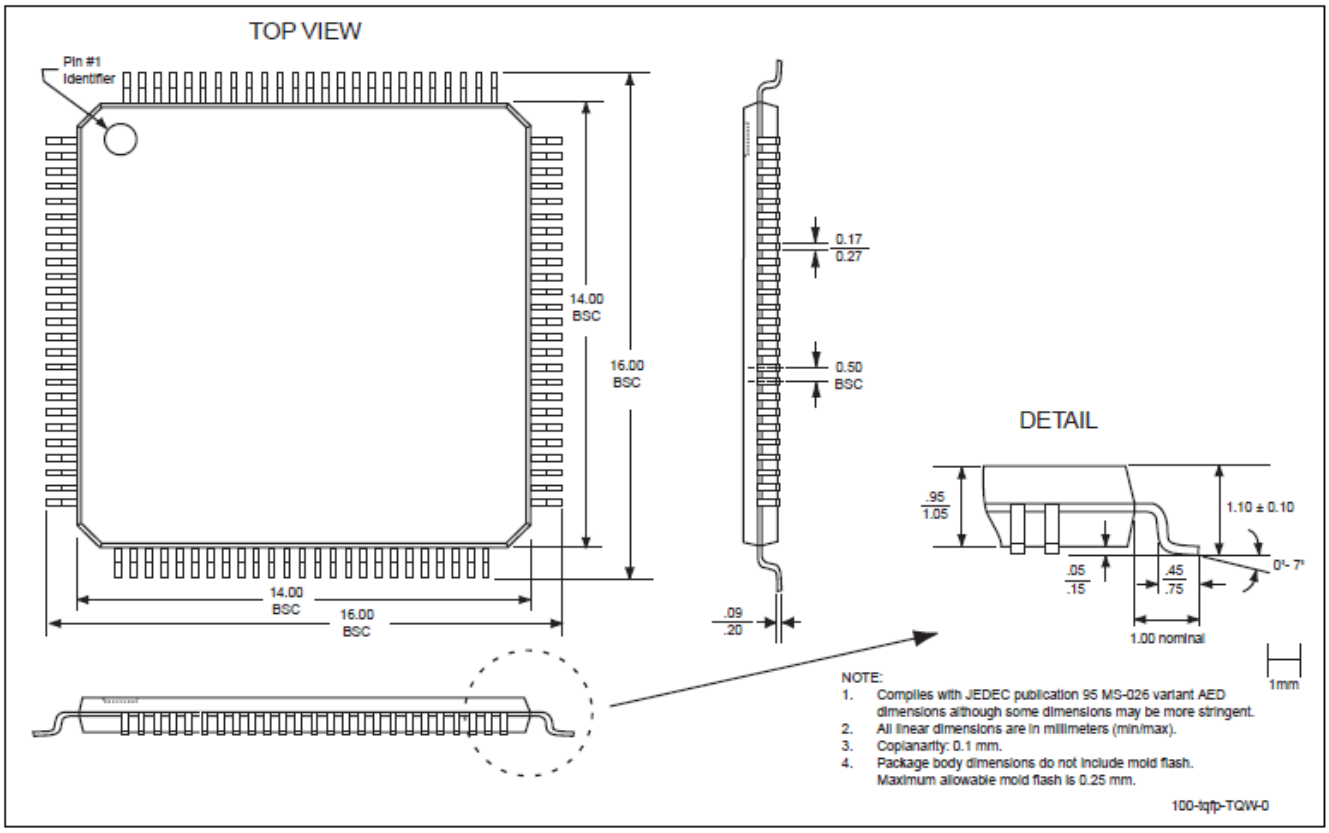


Figure 3: 100-lead Thin Quad Flat Pack (TQFP)
Greenliant Package Code: TQW

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REVISION HISTORY

Revision	Description	Date
01.000	Initial release of Fact Sheet	February 1, 2012

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