AAT4712

Power Path with Input Current Limit and Capacitor Charger

General Description

The AAT4712 is a programmed, current limited P-channel MOSFET power switch designed for high-side load-switching applications for SSD memory buffer saving solutions. With the programmed current limit, the AAT4712 ensures that the power ratings of the host are not exceeded and balances the system load and supercap charging current automatically to provide enough system load current in top-priority. The integrated discharge path control assures that the system load can still be supported in the short term when the input power has not fully charged the supercap. The current limit is programmed by an external resistor allowing ±10% accuracy at room temperature.

The AAT4712 integrates discharge path for SYS (to system load) from VCC input or OUT input (connect to supercap). The low $R_{DS(ON)}$ from OUT to SYS prolongs the supercap backup time when VCC drops below a threshold voltage which is programmed by an external resistor from ADJ to ground.

The AAT4712 incorporates a POK function which can indicate system input power good. An ADJ pin is provided with the addition of an external resistor for setting the input power good detect threshold. The AAT4712 also incorporates a supercap charge ready (RDY) indicate function. The quiescent supply current is typically a low 70µA from the discharge path of VCC to SYS.

The AAT4712 is available in a 16-pin TDFN34 package and is specified over a -40 to 85°C temperature range.

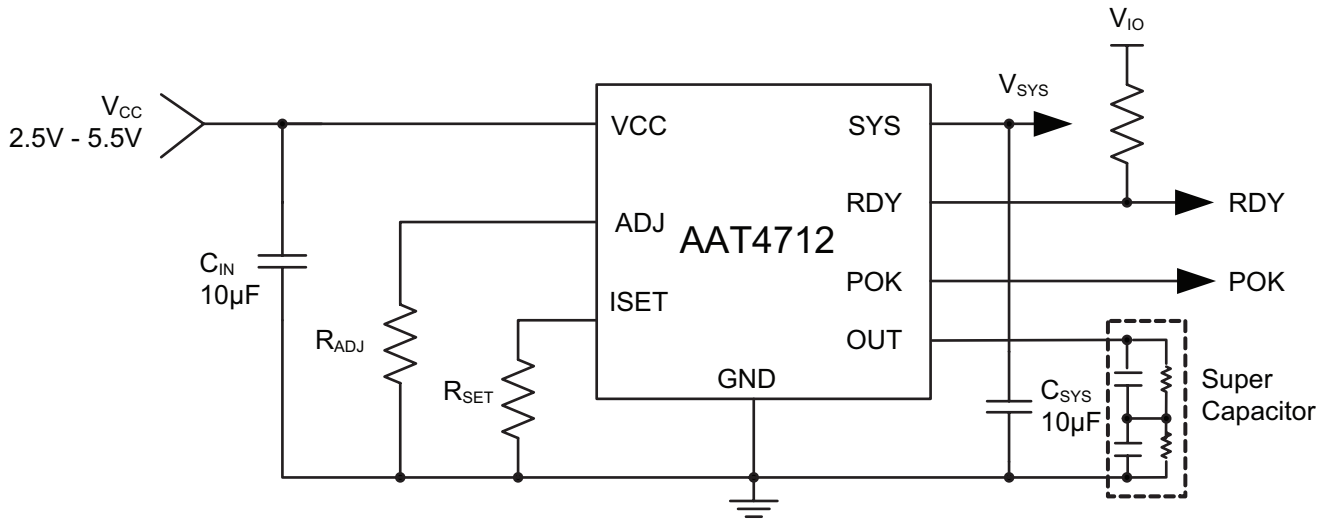
Features

- V_{CC} Range: 2.5V – 5.5V
- Input Current Limits:
  - 150mA - 2400mA
  - ±10% Current Accuracy at 2A Input Current Limit Setting
- Low Quiescent Current:
  - 70µA Typical (VCC Input)
  - 12µA Typical (OUT Input)
- Under-Voltage Lockout
- Integrated Discharge Path for SYS (to System Load) from VCC Input or OUT Input (Connect to Supercap)
- Maximum 100mΩ $R_{DS(ON)}$ from OUT to SYS at 5V V_{CC}
- Reverse Blocking Protection
- Power Loop Current Reduction
- Over-Temperature Protection
- SYS Short Circuit Protection
- Input Power Good Detect Threshold Setting (ADJ)
- Input Power Good Indicate (POK)
- Supercap Charge Ready (RDY) Output
- Temperature Range: -40 to 85°C
- 16-Pin TDFN34 Package

Applications

- SSD

Typical Application

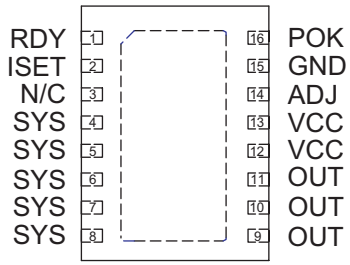


Pin Descriptions

Pin #	Symbol	Function
1	RDY	Supercap charge ready output, initiated when the capacitor is 98% charged. Open drain, active high.
2	ISET	Input current-limit set input. A resistor from ISET to ground is necessary and sets the maximum current limit for the switch. The current limit can be programmed from 150mA to 2000mA.
3	N/C	No connect.
4, 5, 6, 7, 8	SYS	System power output supplied from the VCC input or OUT input.
9, 10, 11	OUT	Connect to super capacitor from OUT to GND.
12, 13	VCC	Input pins to the P-channel MOSFET source. Connect a 10µF capacitor from VCC to GND.
14	ADJ	Input power good detect threshold. An internal 50kΩ resistor is integrated between ADJ and VCC.
15	GND	Device ground connection.
16	POK	Input power good indicator. Push pull, active high.

Pin Configuration

TDFN34-16
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_P	VCC, OUT to GND	-0.3 to 6	V
V_{RDY}, V_{POK} , V_{ADJ}	RDY, POK, ADJ to GND	-0.3 to V_P + 0.3	V
V_{ISET}, V_{SYS}	ISET, SYS to GND	-0.3 to V_P + 0.3	V
I_{MAX}	Maximum Continuous Switch Current	2.5	A
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at Leads)	300	°C

Thermal Characteristics[2]

Symbol	Description	Value	Units
Θ_{JA}	Maximum Thermal Resistance[3]	50	°C/W
P_D	Maximum Power Dissipation[3]	2	W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a FR4 board.
3. Derate 50mW/°C above 25°C.

Electrical Characteristics[1]

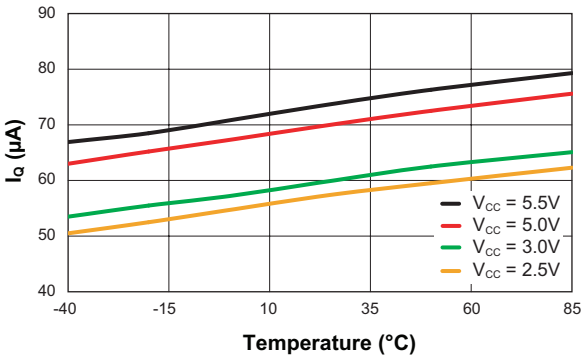
V_{CC} = 2.5V to 5.5V, T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CC}	Normal Operation Voltage		2.5		5.5	V
I_Q	V_{CC} Quiescent Current	I_{OUT} = 0, No Load at SYS Pin		70	120	µA
I_{OUT_OP}	OUT Operating Current	V_{OUT} = 5V, V_{CC} = GND, No Load at SYS Pin		12	30	µA
V_{UVLO_VCC}	V_{CC} Under-Voltage Lockout	Falling Edge		2.1	2.4	V
		Hysteresis		150		mV
V_{UVLO_OUT}	OUT Under-Voltage Lockout	Falling Edge		1.8	2	V
		Hysteresis		250		mV
$R_{DS(ON)\_SWA}$	V_{CC} to SYS On-Resistance	V_{CC} = 5V, R_{SET} = 1.24MΩ, I_{LOAD} = 600mA		50	100	mΩ
		V_{CC} = 3.3V, R_{SET} = 1.24MΩ, I_{LOAD} = 600mA		65	120	
$R_{DS(ON)\_SWB}$	V_{CC} to OUT On-Resistance	V_{CC} = 5V, R_{SET} = 1.24MΩ, I_{LOAD} = 600mA		140	300	mΩ
		V_{CC} = 3.3V, R_{SET} = 1.24MΩ, I_{LOAD} = 600mA		160	320	
$R_{DS(ON)\_SWC}$	OUT to SYS On-Resistance	V_{OUT} = 3V ~ 5V			100	mΩ
$I_{LIMHACC}$	Input High Current Limit Accuracy	R_{SET} = 1.24MΩ, T_A = 25°C	1800	2000	2200	mA
$I_{LIM(MIN)}$	Minimum Input Current Limit			150		mA
T_{RESP}	Current Limit Response Time	V_{CC} = 5V, R_{SET} = 1.24MΩ		2		µs
$T_{DEL(OFF)}$	Turn-Off Delay Time	V_{CC} = 5V		0.4	10	µs
T_{SW}	OUT to SYS Switch Turn On Response Time	VCC Voltage Step-Down Signal from 5V to 4.5V		6		µs
V_{ADJ}	ADJ Pin Voltage with Trigger Comparator			1.2		V
T_{DETECT}	ADJ Pin Detect Delay Time	ADJ Voltage Step Down Signal from 1.3V to 1.1V		2		µs
$V_{POK(L)}$	Output Low Voltage	ADJ ≤ 1.2V			0.4	V
$V_{POK(H)}$	Output High Voltage	ADJ > 1.2V	0.8 V_{CC}			V
V_{RDY}	Supercap Charge Ready Trip Threshold	V_{OUT} Rising, T_A = 25°C		98		% of V_{CC}
V_{RDYSYS}	Supercap Charge Ready Hysteresis			200		mV
$V_{RDY(L)}$	RDY Output Low Voltage	RDY Pin Sinks 1mA			0.4	V
OTMP	Shutdown Temperature			150		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C

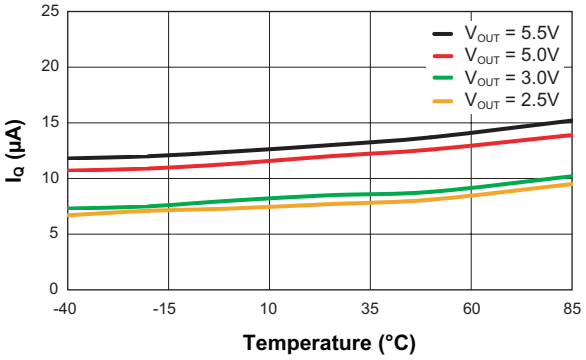
1. The AAT4712 is guaranteed to meet performance specifications over the -40°C to 85°C operating temperature range and is assured by design, characterization and correlation with statistical process controls.

Typical Characteristics

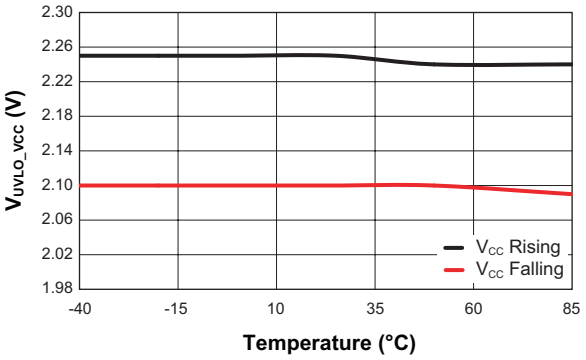
V_{CC} Quiescent Current vs. Temperature



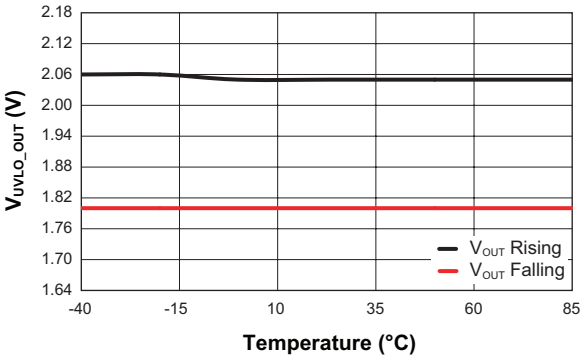
V_{OUT} Quiescent Current vs. Temperature



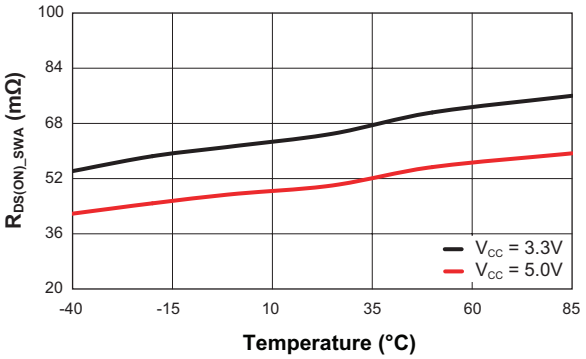
V_{UVLO_VCC} vs. Temperature



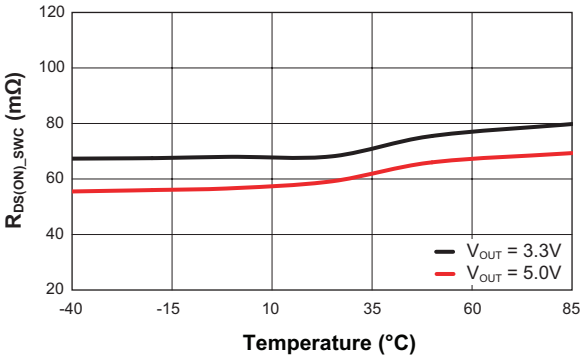
V_{UVLO_OUT} vs. Temperature



$R_{DS(ON)\_SWA}$ vs. Temperature
(Load Current = 600mA, R_{SET} = 1.24MΩ)

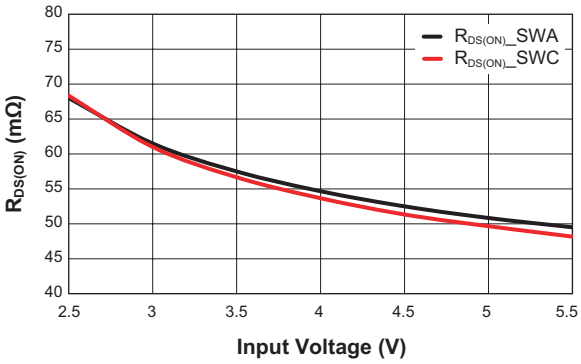


$R_{DS(ON)\_SWC}$ vs. Temperature
(Load Current = 600mA, R_{SET} = 1.24MΩ)

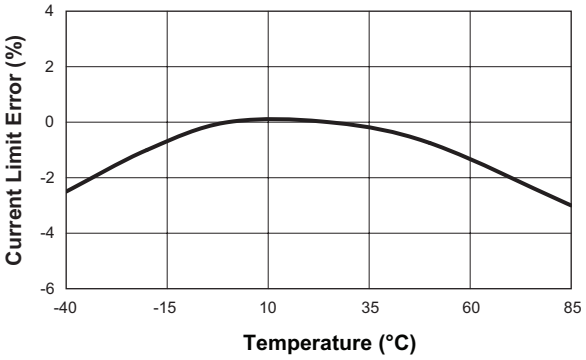


Typical Characteristics

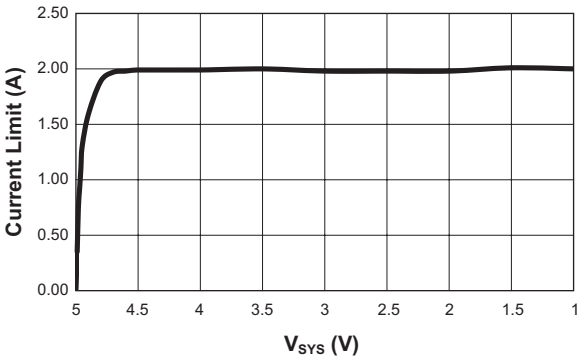
$R_{DS(ON)}$ vs. Input Voltage
(Load Current = 600mA, R_{SET} = 1.24MΩ)



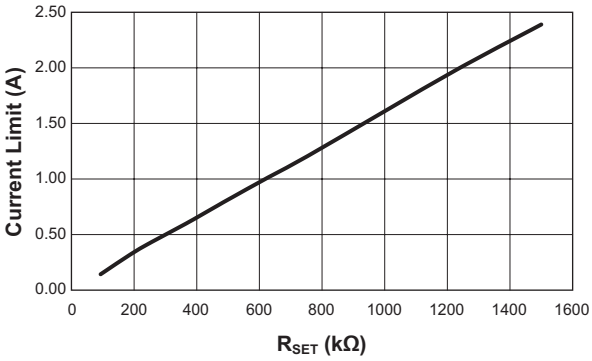
Current Limit Error vs. Temperature
(V_{CC} = 5.0V, R_{SET} = 1.24MΩ)



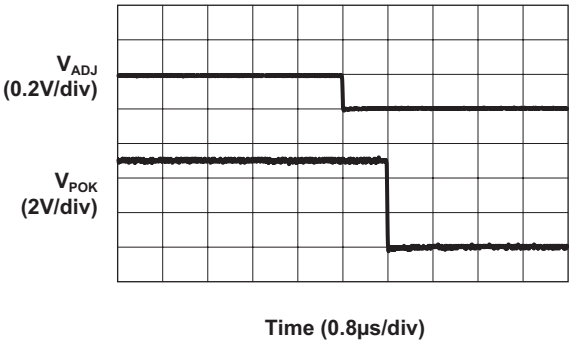
Current Limit vs. SYS Voltage
(R_{ADJ} = 18.2kΩ, R_{SET} = 1.24MΩ, C_{IN} = C_{SYS} = 10µF)



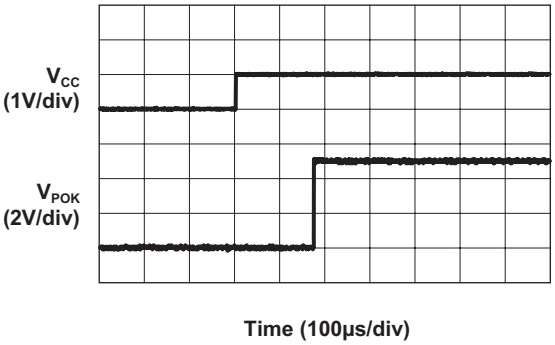
Current Limit vs. R_{SET}
(V_{CC} = 5.0V)



ADJ Detect Delay Time
(V_{CC} = 5.0V, R_{SET} = 1.24MΩ)

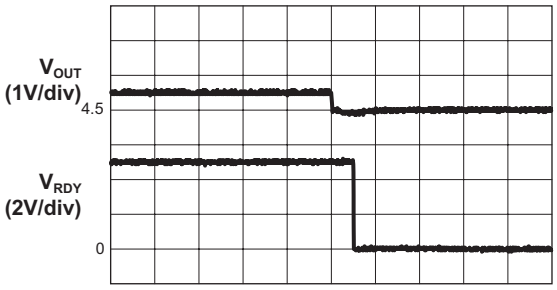


POK Delay Time
(R_{ADJ} = 18.2kΩ)



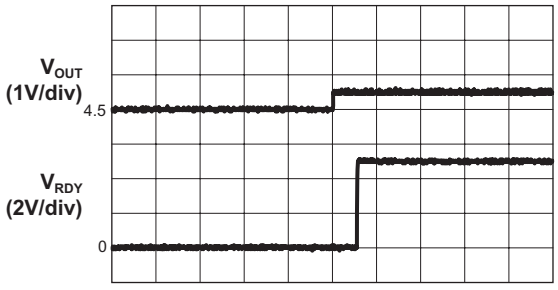
Typical Characteristics

RDY Delay Time From High to Low
(V_{CC} = 5.0V, R_{SET} = 1.24MΩ)



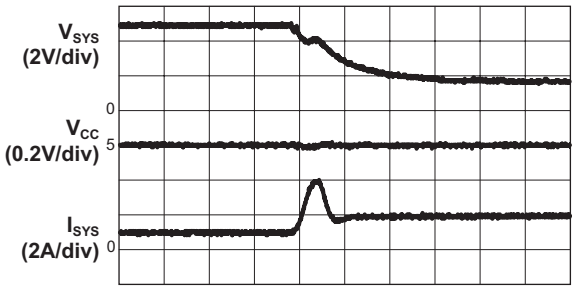
Time (2µs/div)

RDY Delay Time From Low to High
(V_{CC} = 5.0V, R_{SET} = 1.24MΩ)



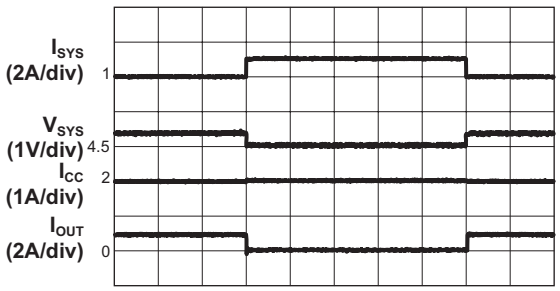
Time (100µs/div)

Current Limit Response
(V_{CC} = 5.0V, R_{SET} = 1.24MΩ, R_{LOAD} = 5Ω to 1Ω)



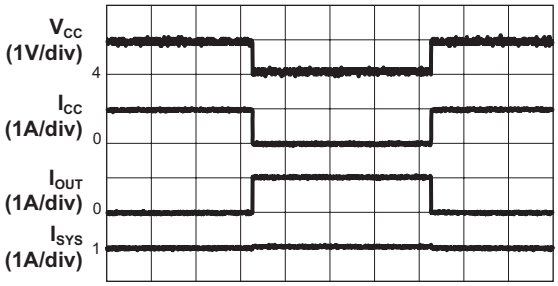
Time (20µs/div)

Load Transient
(V_{CC} = 5.0V, V_{OUT} = 2.0V,
R_{SET} = 1.24MΩ, I_{SYS} = 1A to 2A)



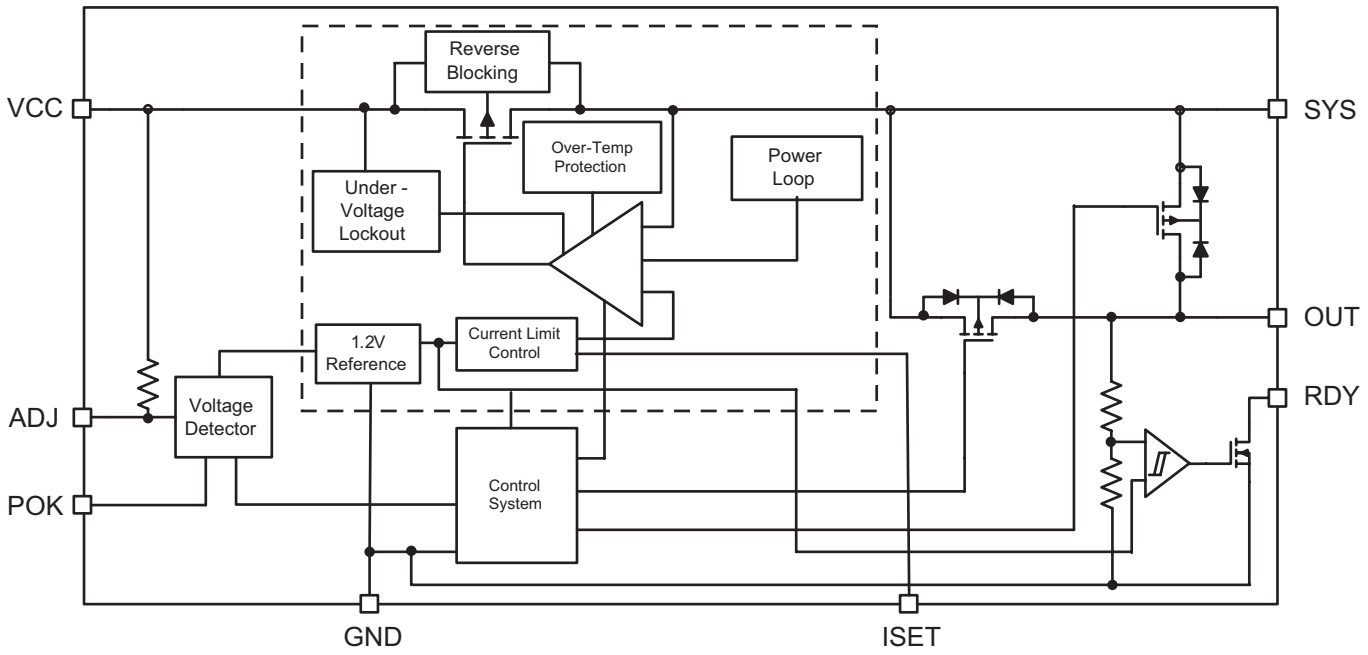
Time (10ms/div)

Discharge Path Switching
(V_{OUT} = 5.0V, R_{SET} = 1.24MΩ, R_{ADJ} = 18.2kΩ,
V_{CC} = 5V to 4V, 1A Load)



Time (100ms/div)

Functional Block Diagram



Functional Description

The AAT4712 is an integrated P-channel MOSFET load switch with adjustable current limits, integrated discharge path, over temperature protection, a power loop and a super capacitor charger. The input current limit control is combined with an over-temperature thermal limit and power loop circuit to provide a comprehensive system to protect the load switch and its supply from load conditions exceeding the supply specifications. The AAT4712 integrates the discharge path for SYS (to system load) from the VCC input or OUT input (connected to supercap) determined by whether VCC is higher than the programmed threshold setting by ADJ through an external resistor.

The input current is limited and is programmed by an external resistor for both system load and supercapacitor charging; system load always has higher priority. The device decreases supercapacitor charging current to provide more current to system load when the system load increases and keeps the host power rating from exceeding the input current limit.

The integrated over-temperature circuits act independently of the input current limit. The device input current limit is activated when the output load current exceeds an internal threshold level. The input current limit threshold in each case is determined by external resistors connected between the ISET pin and ground. The minimum input current limit threshold is specified by $I_{LIM(MIN)}$. If the load condition maintains the device in current limit and the chip temperature reaches a critical point, then an internal power loop will reduce the current to a safe level.

VCC pin under-voltage lockout circuitry ensures that the V_{CC} supply is high enough for correct operation of the IC. OUT pin under-voltage lockout circuitry ensures that the V_{OUT} supply is high enough for correct operation of the IC when no VCC input power or V_{CC} below UVLO voltage. An integrated POK function is adopted to indicate the system input power good.

Setting the Input Current Limit

The AAT4712 current limit is set via the ISET resistor. The ISET node operates within a window of 0.6V to 1.2V for resistor values ranging from 93.75kΩ to 1.5MΩ. Resistor values outside this range are not recommended. The ISET source current varies with the resistor value as shown in Table 1.

$$V_{ISET} = R_{SET} \cdot I_{ISET} = 0.6V \text{ to } 1.2V$$

If the set pin is open circuit or allowed to exceed 2V, all power devices are disabled and the input is disconnected from the output.

SYS Load and Capacitor Charge

The input current limit is equal to the SYS current plus the OUT charging current. If the SYS current increases/decreases, the OUT charging current will automatically decrease/increase accordingly by the device control loop. For example, if the input current limit is programmed to 1A and the SYS load current is 0.5A, then the OUT charging current is 0.5A; if the SYS load current increases to 0.8A, the OUT current decreases to 0.2A accordingly; if the SYS load current decreases to 0.2A, the OUT current increases to 0.8A dynamically.

Discharge Path Control

When the input voltage drops below the power good detect threshold programmed by the external resistor from ADJ pin to GND and the OUT pin voltage is greater than the V_{UVLO_OUT} and SYS pin voltage, the AAT4712 turns on the OUT to SYS switch discharge path after 6µs (T_{SW}) response time, then turns off the path of VCC to the SYS P-channel load switch. The OUT to SYS switch remains continuously on until the OUT pin voltage falls below V_{UVLO_OUT}.

Power Loop

The AAT4712's power loop limits the load current if device power dissipation becomes excessive. The power loop decreases the load current gradually to 1/32 of the current limit set point when the die temperature exceeds 130°C. The load current then increases in increments of 1/32 of the current limit set point until the set current limit point is reached or the die temperature exceeds 130°C. Figures 1 and 2 show the the power loop function as the device temperature increases and decreases at a 1A current limit setting.

R_{SET} Range (Ω)	I_{ISET} (µA)	I_{LIM}/V_{ISET} (A/V)	Current Limit Range (A)	Current Limit
1.5M - 750k	0.8	2	2.4-1.2	R_{SET}*0.8*2
750k - 375k	1.6	1	1.2-0.6	R_{SET}*1.6*1
375k - 187.5k	3.2	0.5	0.6-0.3	R_{SET}*3.2*0.5
187.5k - 93.75k	6.4	0.25	0.3-0.15	R_{SET}*6.4*0.25

Table 1: R_{SET} Values for Setting the Input Current.

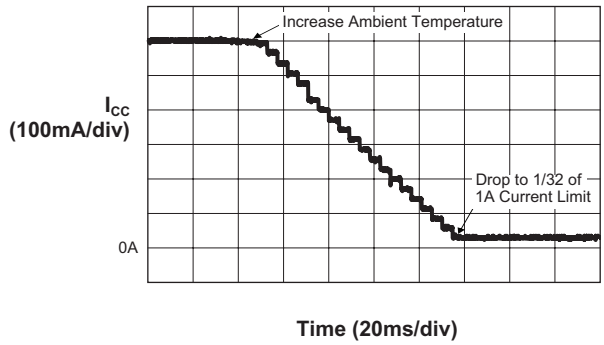


Figure 1: AAT4712 Power Loop Function at 1A Current Limit with Ambient Temperature Increasing.

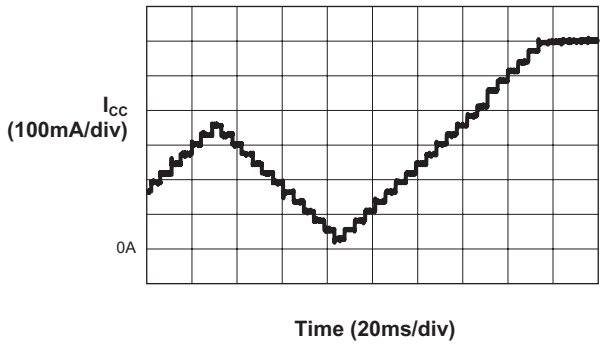


Figure 2: AAT4712 Power Loop Function at 1A Current Limit with Ambient Temperature Decreasing.

The delay time between die temperature measurements varies depending on the load current limit set point. The delay ranges from 0.5ms for a 150mA current limit set point to 4ms for a 2.4A current limit set point.

Over-Temperature Protection

If the die temperature rises quickly enough to exceed the power loop regulated temperature, over-temperature shutdown disables the device. The over-temperature threshold is 150°C. After over-temperature shutdown, soft start is initiated once the die temperature drops to 135°C.

Power OK Indicator (POK)

On initial power-up, if VCC is higher than the power good detect threshold programmed by the external resistor from the ADJ pin to GND, the POK signal switches from low to high after 2µs delay time (T_{DETECT}) to indicate input power good.

If VCC drops below the power good detect point, the POK signal switches from high to low after 2µs delay time (T_{DETECT}).

Capacitor Charge Ready Indicator (RDY)

The internal comparator senses the OUT voltage and delivers a high level as ready signal to the external microcontroller when the OUT voltage reaches 98% of the VCC voltage with fixed 200mV hysteresis.

The capacitor charge ready pin (RDY) is an open drain output. A external pull up resistor with a typical value of 100kΩ is required.

Application Information

Input Current Limit Setting

The input current limit is programmed by R_{SET} from ISET to ground in the range from 150mA to 2.4A. The current limit limits the maximum current of both VCC to SYS and VCC to OUT. The R_{SET} can be calculated by:

$$R_{SET} = \frac{I_{LIM}}{1.6} \text{ (Current in A, resistance in kΩ)}$$

Table 2 lists some 1% standard metal film resistor values for current limit settings from 150mA to 2.4A.

R_{SET} (kΩ)	Current Limit (A)
1500	2.4
1240	2
1000	1.6
750	1.2
620	1
499	0.8
374	0.6
249	0.4
187	0.3
93.1	0.15

Table 2: Recommended Current Limit R_{SET} Values.

Power Good Detect Threshold Setting

The power good detect threshold (V_{POK_TH}) determines the point at which the discharge path changes from VCC – SYS to OUT – SYS if the OUT pin voltage is above V_{UVLO_OUT} and the SYS pin voltage. The power good detect threshold is programmed by the external resistor R_{ADJ} connected from the ADJ pin to GND. The R_{ADJ} value can be calculated by:

$$R_{ADJ} = \frac{60}{V_{POK\_TH} - 1.2} \text{ (Voltage in V, resistance in kΩ)}$$

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Table 3 summarizes some 1% standard metal film resistor values for various V_{POK_TH} settings.

R_{ADJ} (kΩ)	V_{POK_TH} (V)
15.8	5.0
18.2	4.5
20.5	4.0
26.1	3.5
33.2	3.0
47	2.5

Table 3: Recommended Resistor Values for V_{POK_TH} Settings.

Discharge Path Control

As the AAT4712 powers the system load, the device automatically selects VCC or OUT as the power source. OUT is designed to connect a supercapacitor as a backup source. Figure 3 shows the discharge path control operation at 1A current limit setting. When VCC is powered on from zero to 5V, the SYS voltage also rises to 5V and 500mA current is passed through from VCC to SYS as system load. With the 1A current limit, the additional 500mA is used to charge the supercapacitor via IOUT as shown. After 3.5 seconds, the 550mF supercapacitor is fully charged; the charging current decreases to zero, and ICC current decreases to 500mA. When VCC drops from 5V to zero, the backup power source VOUT provides the 500mA load current to SYS until the supercapacitor voltage is discharged to below the UVLO voltage threshold (typ. 1.8V).

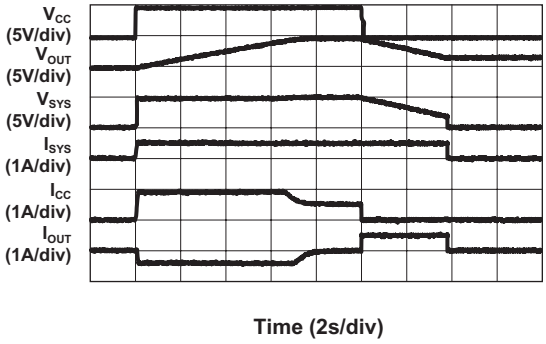


Figure 3: Discharge Path Control with 550mF Supercapacitor at 1A Current Limit Setting and 500mA System Load.

Reverse Blocking

The internal reverse blocking comparator disconnects the VCC to SYS path by turning off the power PMOSFETs when SYS is higher than VCC minus 18mV, preventing any reverse current from the system load to the input. With 22mV hysteresis, the VCC to SYS path will be reconnected by turning on the power PMOSFETs when the SYS voltage drops to VIN minus 40mV. The reverse blocking comparator has a typical 5µs delay time, which may lead to output voltage ripple on the SYS output at light load. Increasing the SYS output capacitor value can improve the output voltage ripple when the application has special SYS voltage ripple requirements.

Input Capacitor

A 10µF capacitor is typically recommended for C_{IN}. C_{IN} should be located as close to the device VCC pin as practically possible. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor equivalent series resistance (ESR) requirement for C_{IN}. However, for higher current operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources.

System Output Capacitor

A small output capacitance of approximately 10µF is required at the system output. The output capacitor helps to filter the SYS voltage when the device works between reverse blocking and normal operation. For higher output voltage ripple requirements at light load (below 1/3 current limit), a greater output capacitor value is required.

OUT Supercapacitor

The AAT4712's OUT pin is designed to connect a supercapacitor to ground to give the system a backup when VCC experiences short power interrupts. A supercapacitor offers high capacitance in a small package; it adopts special electrodes and some electrolyte. Three types of electrode materials are suitable for the supercapacitor: high surface area activated carbons, metal oxide, and conducting polymers. The first option is the lowest cost to manufacture; the electrolyte usually is aqueous or organic. An aqueous electrolyte offers low internal resis-

tance but limits the voltage to 1V; the organic allows 2.5V of charge but has higher internal resistance. For higher voltage applications, supercapacitors are connected in series. To prevent any cell from charging overvoltage, a balance resistor is required on a string of more than three cells.

Three parameters should be considered when selecting a supercapacitor. These parameters are capacitance, rated voltage, and ESR. Table 4 shows some recommended supercapacitors. Other parameters such as temperature range, RMS current, leakage current, etc. should also be considered during the system design.

SYS Short Circuit Protection

The series pass power MOSFET from VCC to SYS limits the current to a low level after the SYS output shorts to ground to protect the device and downstream components. During the fault condition, the power loop is still active to monitor the die temperature and reduce the current when the die temperature exceeds 130°C. Once the short-circuit fault is removed, the SYS voltage recovers to the normal value automatically.

The AAT4712 also includes short-circuit protection circuitry for the discharge path from OUT to SYS to avoid large current discharging through the device over a long term and avoid damage to the device.

PCB Layout Recommendations

For proper thermal management and to take advantage of the low $R_{DS(ON)}$ of the AAT4712, certain circuit board layout rules should be followed:

1. V_{CC}, V_{OUT}, and V_{SYS} should be routed using wide traces.
2. GND should be connected to a ground plane. The ground plane area connected to the ground pins should be made as large as possible.
3. For best performance, C_{IN} and C_{SYS} should be placed close to the VCC and SYS pins.
4. For maximum power dissipation of the AAT4712 TDFN package, the exposed pad should be soldered to the board ground plane to further increase local heat dissipation. A ground pad below the exposed pad is strongly recommended.

Manufacturer	Part Number	Capacitance (mF)	Rated Voltage (V)	ESR (mΩ)	Size LxWxH (mm)
Cap-xx	HS 203F	250	5.5	70	39x17x2.15
	HS 211F	370	5.5	55	39x17x2.9
	HS 206F	600	5.5	70	39x17x2.4
	HW 207F	450	5.5	100	28.5x17x2.9
TDK	EDLC152344-551-2F-30	550	5.5	30	44x23x1.5
	EDLC262020-501-2F-50	500	5.5	50	20x20x2.6

Table 4: Recommended Supercapacitors

Evaluation Board Schematic

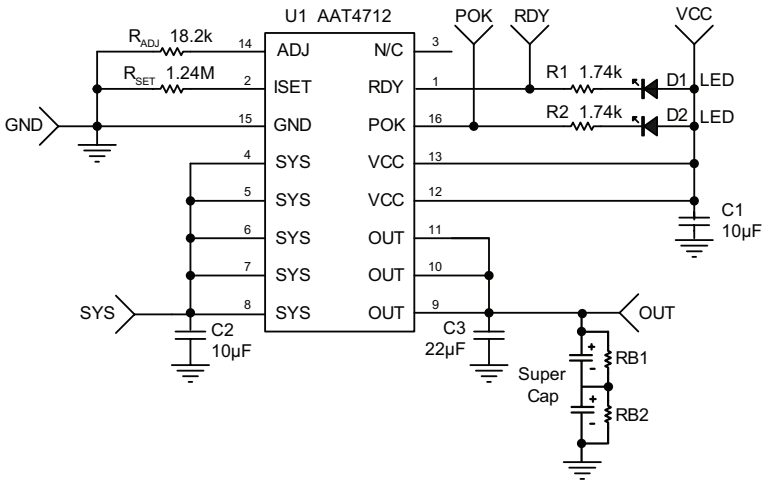
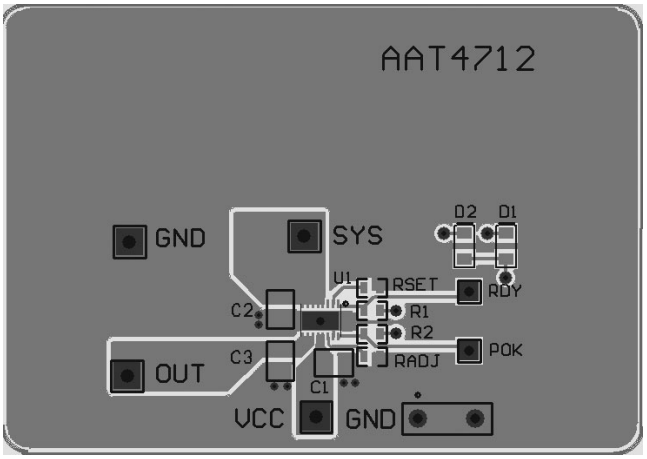
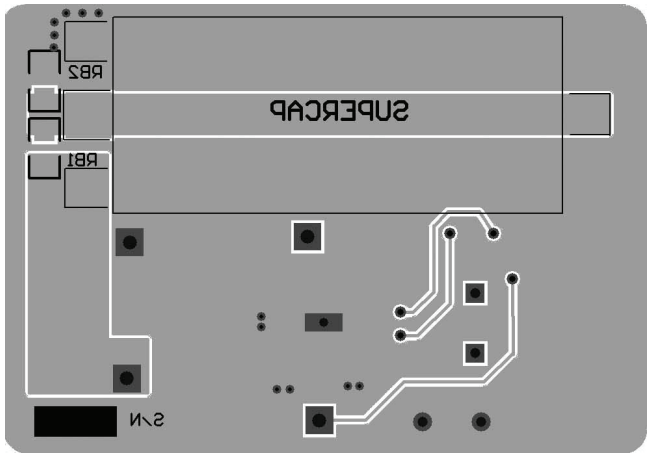


Figure 4: AAT4712 Evaluation Board Schematic.

Evaluation Board Layout



a: Top Side



b: Bottom Side

Figure 5: AAT4712 Evaluation Board Layout.

Component	Part Number	Description	Manufacturer
U1	AAT4712	Current Limited Switch with Capacitor Charger	Skyworks
R1,R2	RC0603FR-071K74L	Res 1.74KΩ 1/10W 1% 0603 SMD	Yageo
R_{SET}	RC0603FR-071M24L	Res 1.24MΩ 1/10W 1% 0603 SMD	
R_{ADJ}	RC0603FR-0718K2L	Res 18.2KΩ 1/10W 1% 0603 SMD	
C1, C2	GRM21BR61C106K	Cap Ceramic 10µF 0805 X5R 16V 10%	Murata
C3	GRM21BR60J226M	Cap Ceramic 22µF 0805 X5R 6.3V 20%	
D1, D2	0805KRCT	Red LED 0805	HB
SUPERCAP, RB1, RB2	Not populated		

Table 5: AAT4712 Evaluation Board Bill of Materials.

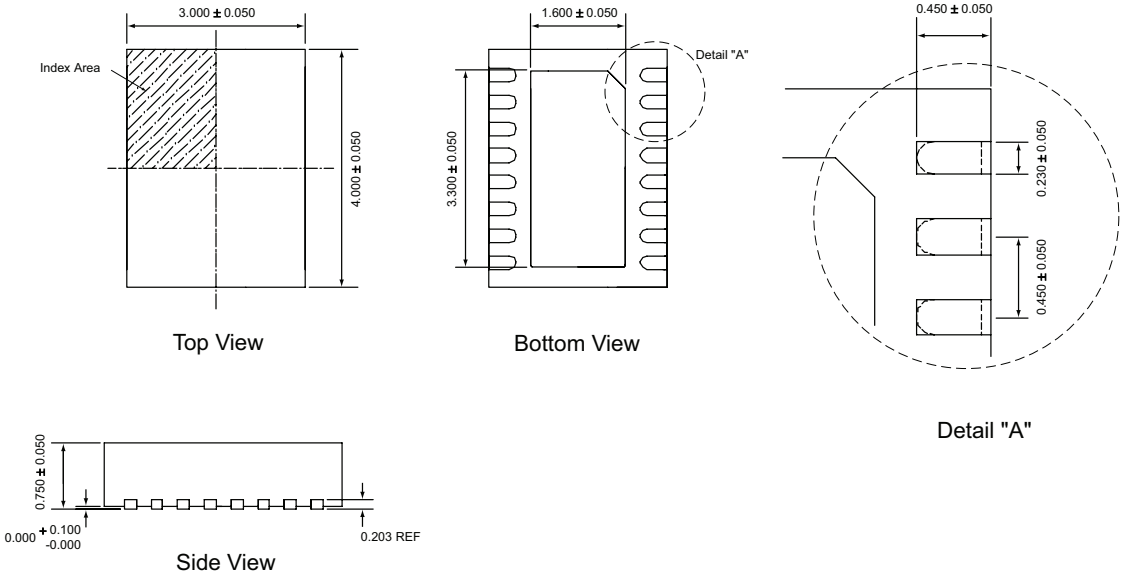
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TDFN34-16	G9XYY	**AAT4712IRN-T1**

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Package Information[3]

TDFN34-16



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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