



## CeraLink

Capacitor for fast-switching semiconductors

<b>Series/Type:</b>	<b>Flex Assembly (FA) series</b>
<b>Ordering code:</b>	<b>B58035U*</b>
Date:	2019-09-25
Version:	6.2

## Applications

- Power converters and inverters
- DC link/snubber capacitor for power converters and inverters

## Features

- High ripple current capability
- High temperature robustness
- Low equivalent serial inductance (ESL)
- Low equivalent serial resistance (ESR)
- Low power loss
- Low dielectric absorption
- Optimized for high frequencies up to several MHz
- Increasing capacitance with DC bias up to operating voltage
- High capacitance density
- Minimized dielectric loss at high temperatures
- Qualification based on AEC-Q200 rev. D
- Suitable for reflow soldering only



## Construction

- RoHS-compatible PLZT ceramic (lead lanthanum zirconium titanate)
- Copper inner electrodes
- Silver outer electrodes
- Silver coated copper-invar lead frame
- Epoxy resin adhesive

## General technical data

Dissipation factor	$\tan \delta$	< 0.02	
Insulation resistance	$R_{ins, typ}^{1)}$	> 0.1	GΩ
Operating device temperature	$T_{device}$	-40 ... +150	°C

<sup>1)</sup> Typical insulation resistance, measured at operating voltage  $V_{op}$  and measurement time > 240s, +25 °C

## Overview of available types

		<b>V<sub>R</sub> (V<sub>dc</sub>)</b>		
		500	700	900
<b>C<sub>nom, typ</sub> (μF)</b>	0.5			FA2
	0.75			FA3
	1		FA2	
	1.5		FA3	
	2	FA2		
	2.5			FA10
	3	FA3		
	5		FA10	
	10	FA10		

## Electrical specifications and ordering codes

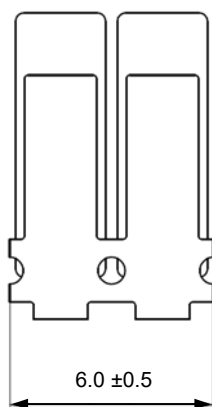
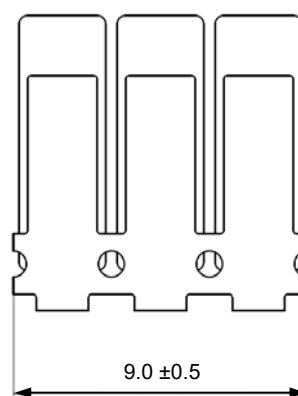
<b>Type</b>	<b>V<sub>pk, max</sub> V</b>	<b>V<sub>R</sub> V</b>	<b>V<sub>op</sub> V</b>	<b>C<sub>nom, typ</sub> μF</b>	<b>C<sub>eff</sub> μF</b>	<b>C<sub>0</sub> μF</b>	<b>Ordering code</b>
<b>FA2</b>	650	500	400	2	1.20 ±20%	0.70 ±20%	B58035U5205M062 B58035U5205M052 *)
<b>FA3</b>	650	500	400	3	1.80 ±20%	1.05 ±20%	B58035U5305M062 B58035U5305M052 *)
<b>FA10</b>	650	500	400	10	6.00 ±20%	3.50 ±20%	B58035U5106M001
<b>FA2</b>	1000	700	600	1	0.50 ±20%	0.28 ±20%	B58035U7105M062 B58035U7105M052 *)
<b>FA3</b>	1000	700	600	1.5	0.75 ±20%	0.42 ±20%	B58035U7155M062 B58035U7155M052 *)
<b>FA10</b>	1000	700	600	5	2.50 ±20%	1.40 ±20%	B58035U7505M001
<b>FA2</b>	1300	900	800	0.5	0.26 ±20%	0.14 ±20%	B58035U9504M062 B58035U9504M052 *)
<b>FA3</b>	1300	900	800	0.75	0.39 ±20%	0.21 ±20%	B58035U9754M062 B58035U9754M052 *)
<b>FA10</b>	1300	900	800	2.5	1.30 ±20%	0.70 ±20%	B58035U9255M001

\*) smaller packaging unit (180-mm reel), see section "Packaging" for details

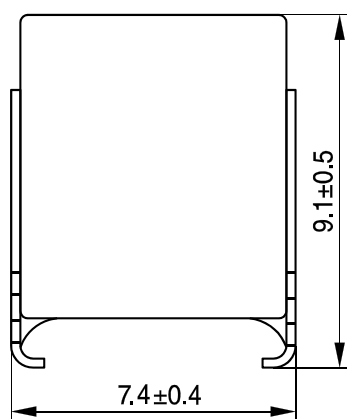
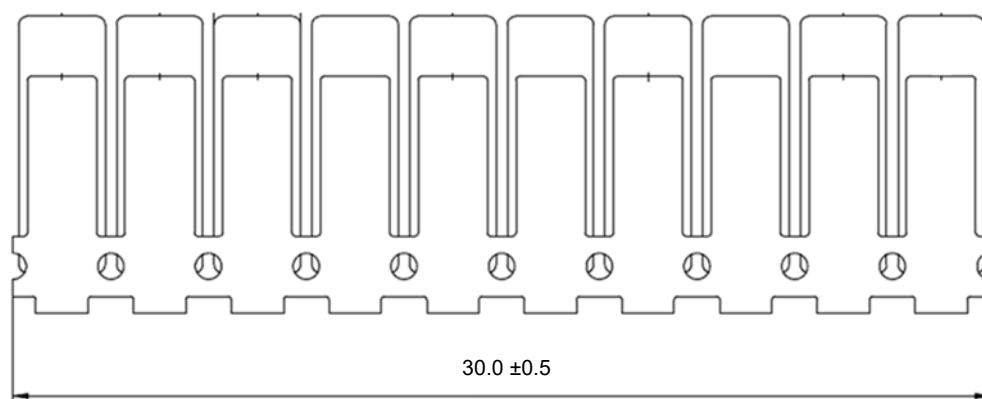
**Typical values as a design reference for CeraLink® applications**

Type	V <sub>R</sub>	Weight	ESR 0 V <sub>DC</sub> , 0.5 V <sub>RMS</sub> , 25°C, 1kHz Ω	ESR 0 V <sub>DC</sub> , 0.5 V <sub>RMS</sub> , 25°C, 1MHz mΩ	ESL nH	I <sub>op</sub> <sup>1)</sup> 100 kHz, T <sub>A</sub> = 85°C A <sub>RMS</sub>	I <sub>op</sub> <sup>1)</sup> 100 kHz, T <sub>A</sub> = 105°C A <sub>RMS</sub>
	V	G					
<b>FA2</b>	500	2.3	3	5	3	17	14
<b>FA3</b>	500	3.5	2	4	3	20	17
<b>FA10</b>	500	11.5	1	3	2	47	38
<b>FA2</b>	700	2.3	6	17	3	12	11
<b>FA3</b>	700	3.5	4	12	3	16	13
<b>FA10</b>	700	11.5	1	5	2	39	30
<b>FA2</b>	900	2.3	11	29	3	8	7
<b>FA3</b>	900	3.5	7	20	3	11	9
<b>FA10</b>	900	11.5	2	7	2	32	23

<sup>1)</sup> Normal operating current without forced cooling at T<sub>device</sub> = +150 °C. Higher values permissible at reduced lifetime.

**Dimensional drawings**
**FA 2**

**FA 3**


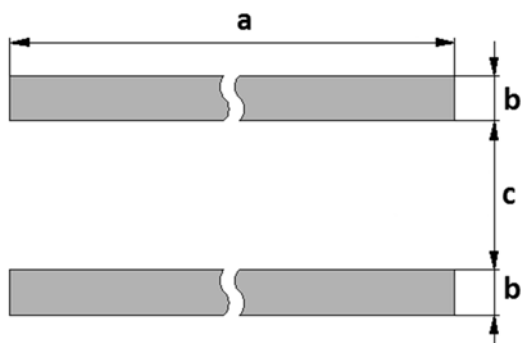
## FA 10



CLC0023-J

Dimensions in mm

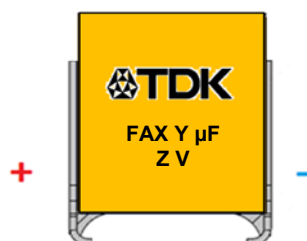
## Recommended solder pads



Type	a	b	c
FA2	7	2.85	5
FA3	10	2.85	5
FA10	31	2.85	5

Dimensions in mm

## Polarity and marking of components



Manufacturer's logo

X = CeraLink FA type (e.g. FA2)

Y = Nominal capacitance

Z = Rated voltage

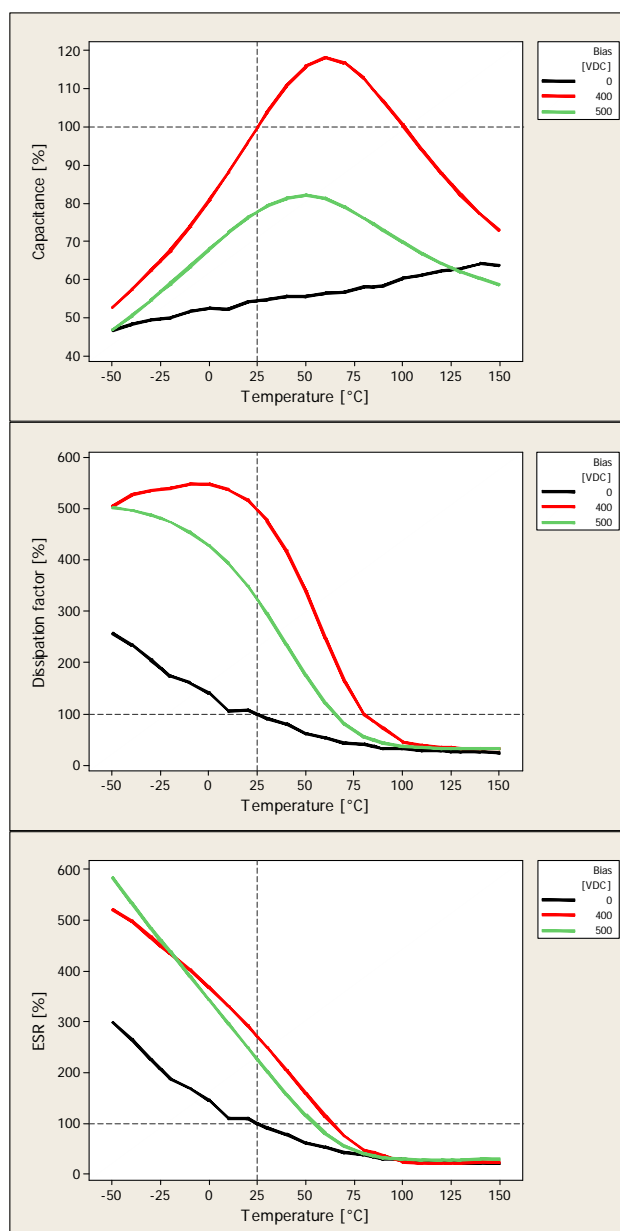
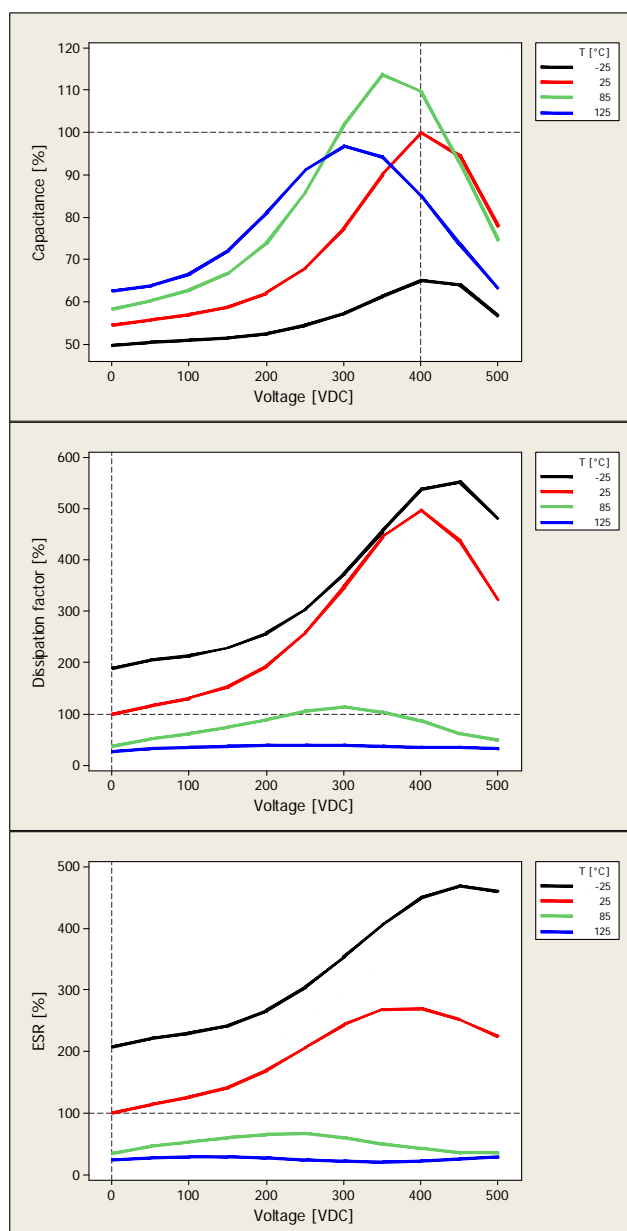
Note that polarity is only for incoming inspection purposes and it does not affect operation. If put under reverse rated voltage  $V_R$ , CeraLink is repoled and works identically.

# Typical characteristics as a function of temperature and voltage $V_R = 500\text{ V}$

( $V_{AC} = 0.5 V_{RMS}$ , frequency = 1 kHz)

All given temperatures are device temperatures.

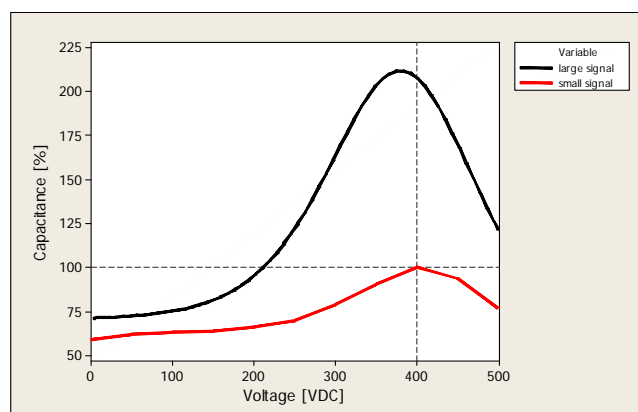
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to  $C_{eff, typ}$  and  $\tan \delta$  which are given on pages 2, 3 and 4 of this data sheet.



## Application Notes

Further typical electrical characteristics as a design reference for CeraLink applications.

### Typical capacitance values as a function of voltage $V_R = 500\text{ V}$ – valid for FA2, FA3 and FA10



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C

The nominal capacitance is defined as the large signal capacitance at  $V_{op}$ .

See glossary for further information.

Small signal capacitance:

0.5  $V_{RMS}$ , 1 kHz, +25 °C

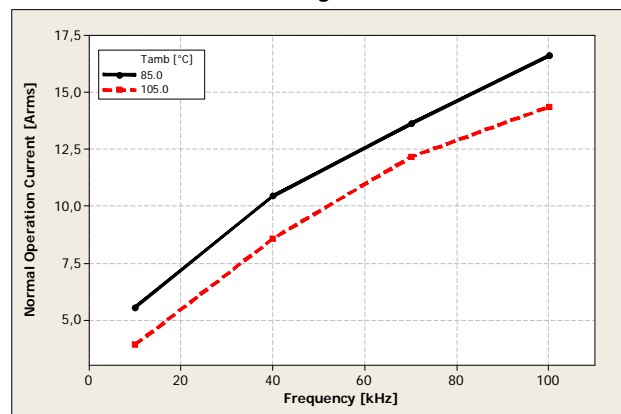
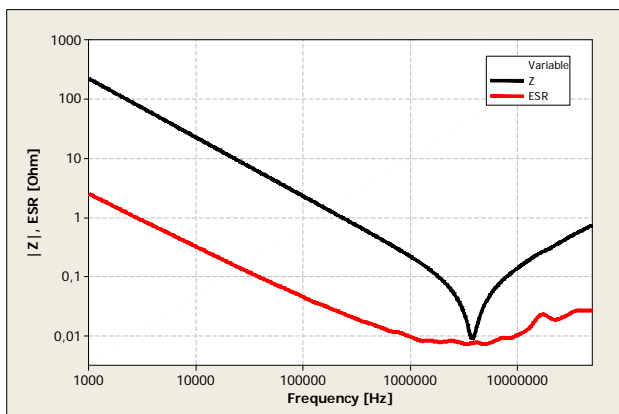
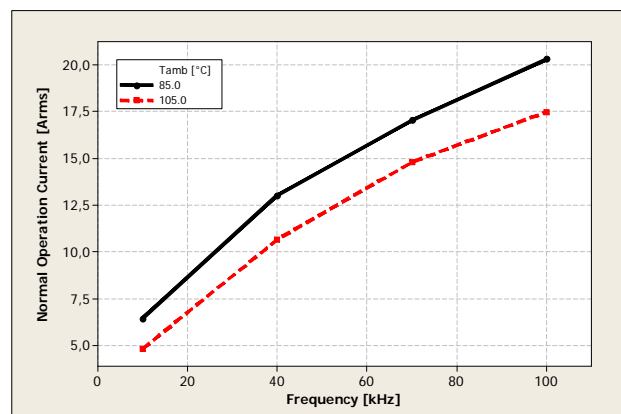
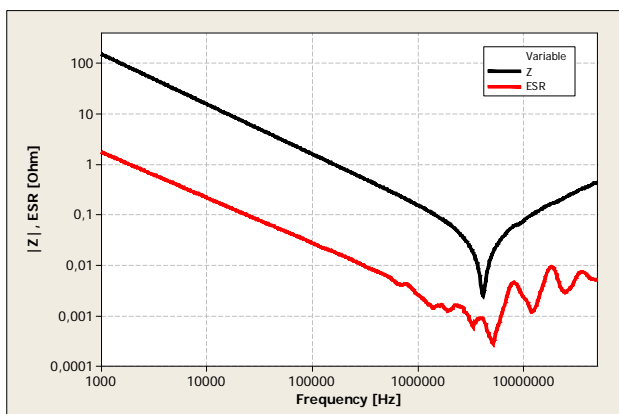
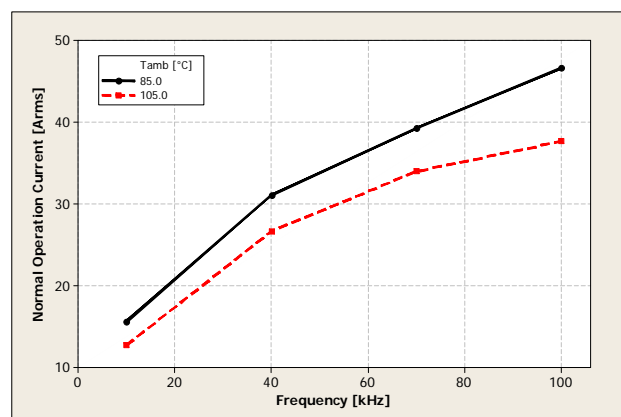
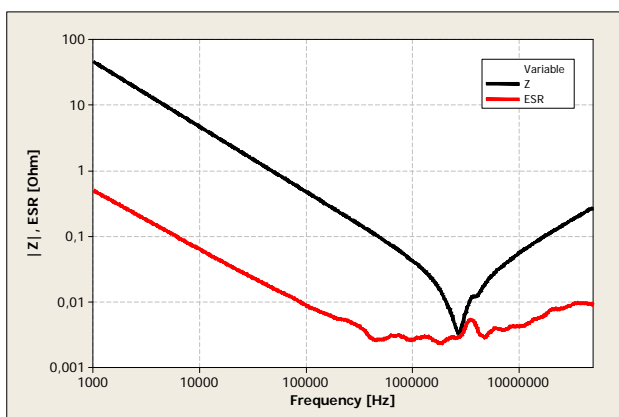
The effective capacitance is defined as the small signal capacitance at  $V_{op}$ .



**Typical impedance, ESR and permissible current as a function of frequency  $V_R = 500\text{ V}$** 

$V_{DC} = 0\text{ V}$ ,  
 $V_{AC} = 0.5\text{ V}_{RMS}$ ,  
 $T_{device} = +25\text{ °C}$

Measurements performed at  $V_{op}$ .  
 The values correspond to a device temperature of  $+150\text{ °C}$ . No forced cooling was used.

**FA2**

**FA3**

**FA10**

**Aging**

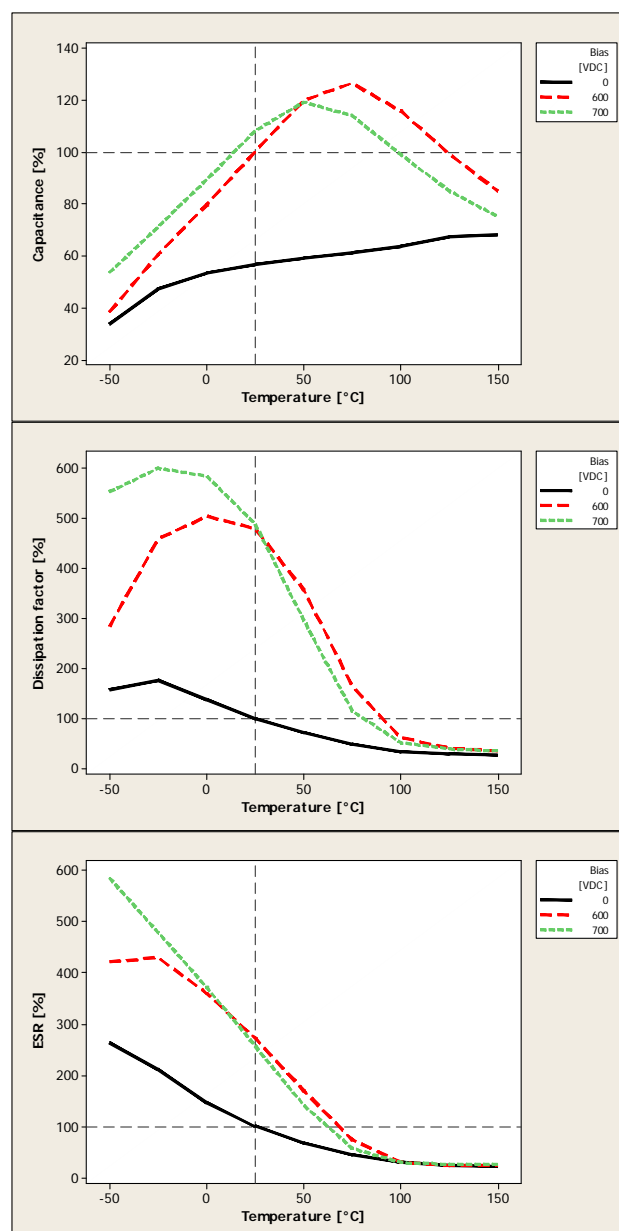
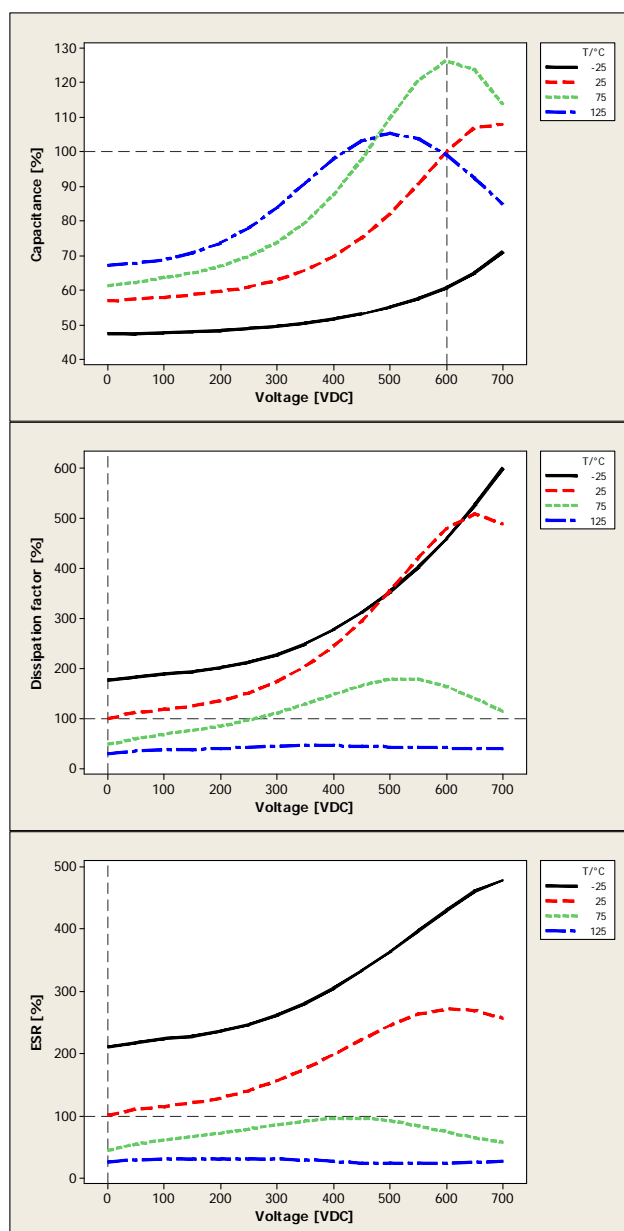
The capacitance has an aging behavior which shows a decrease of capacitance with time.  
 The typical aging rate is about 2.5% per logarithmic decade in hours.

# Typical characteristics as a function of temperature and voltage $V_R = 700\text{ V}$

( $V_{AC} = 0.5 V_{RMS}$ , frequency = 1 kHz)

All given temperatures are device temperatures.

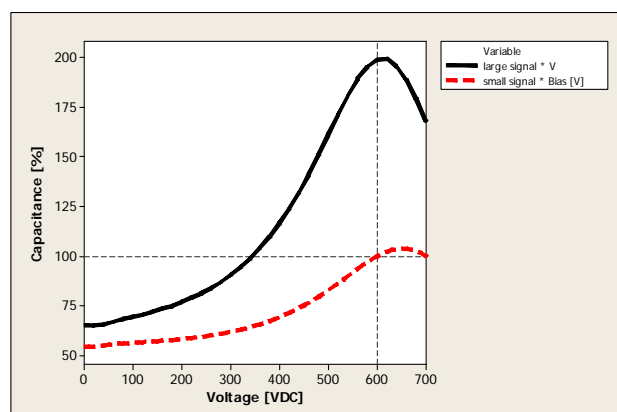
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to  $C_{eff, typ}$  and  $\tan \delta$  which are given on pages 2, 3 and 4 of this data sheet.



## Application Notes

Further typical electrical characteristics as a design reference for CeraLink applications.

### Typical capacitance values as a function of voltage $V_R = 700\text{ V}$ – valid for FA2, FA3 and FA10



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C

The nominal capacitance is defined as the large signal capacitance at  $V_{op}$ .

See glossary for further information.

Small signal capacitance:

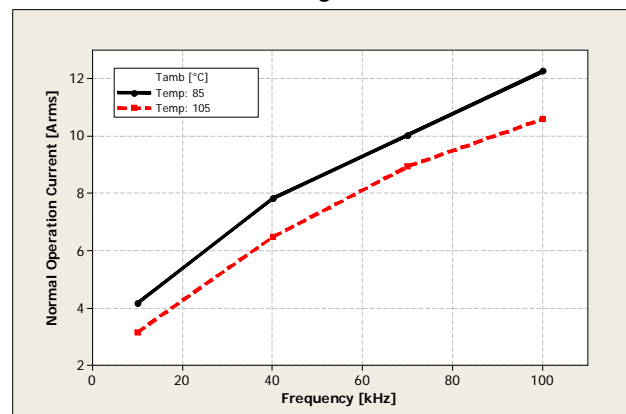
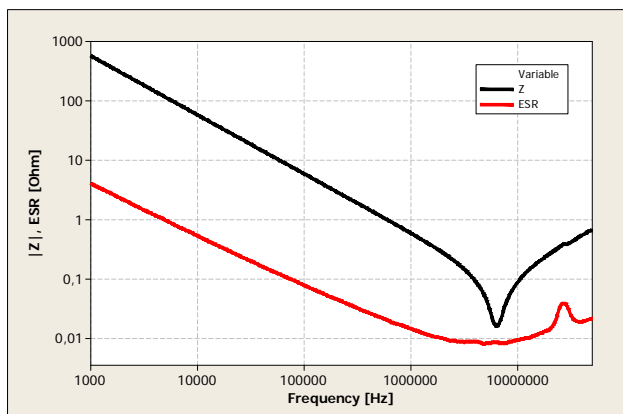
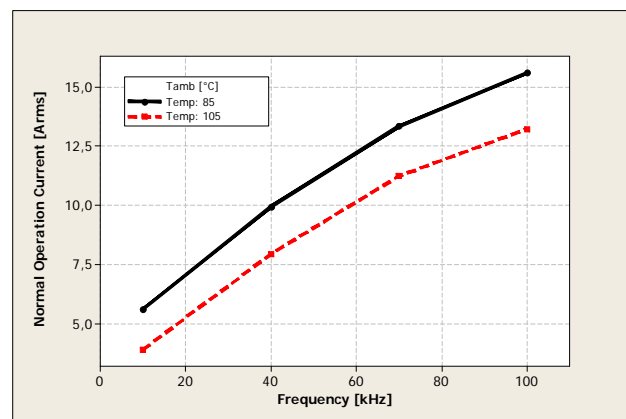
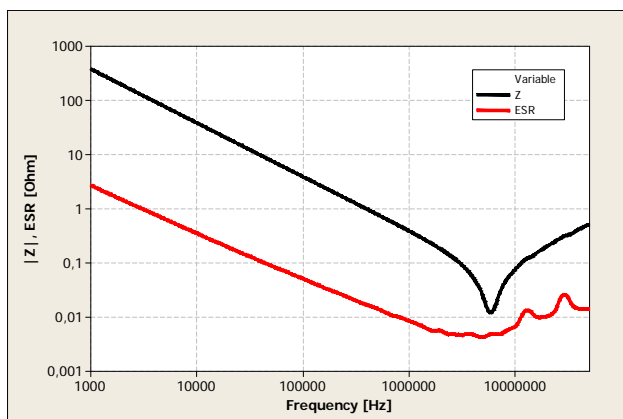
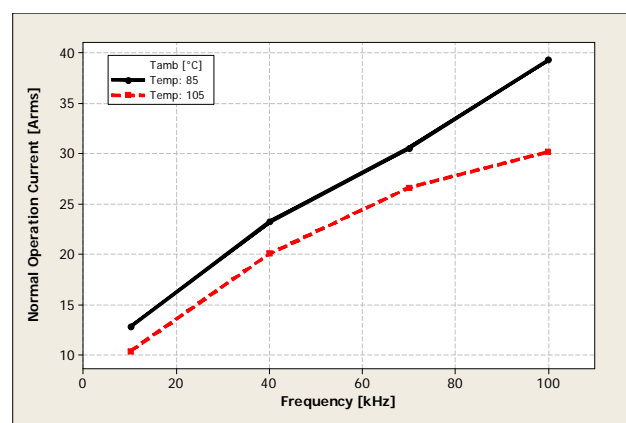
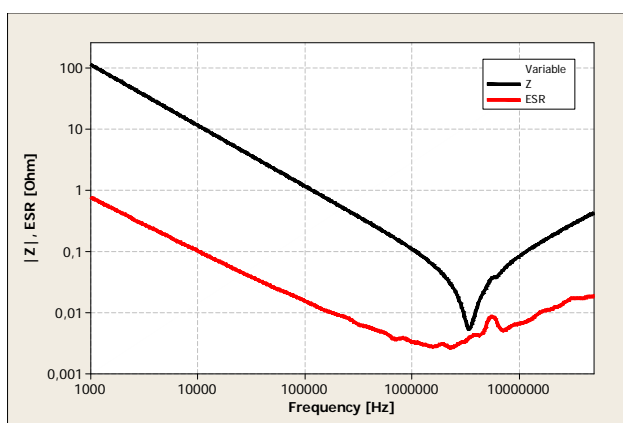
0.5  $V_{RMS}$ , 1 kHz, +25 °C

The effective capacitance is defined as the small signal capacitance at  $V_{op}$ .

**Typical impedance, ESR and permissible current as a function of frequency  $V_R = 700\text{ V}$** 

$V_{DC} = 0\text{ V}$ ,  
 $V_{AC} = 0.5\text{ V}_{RMS}$ ,  
 $T_{device} = +25\text{ }^{\circ}\text{C}$

Measurements performed at  $V_{op}$ .  
 The values correspond to a device temperature of  $+150\text{ }^{\circ}\text{C}$ . No forced cooling was used.

**FA2**

**FA3**

**FA10**

**Aging**

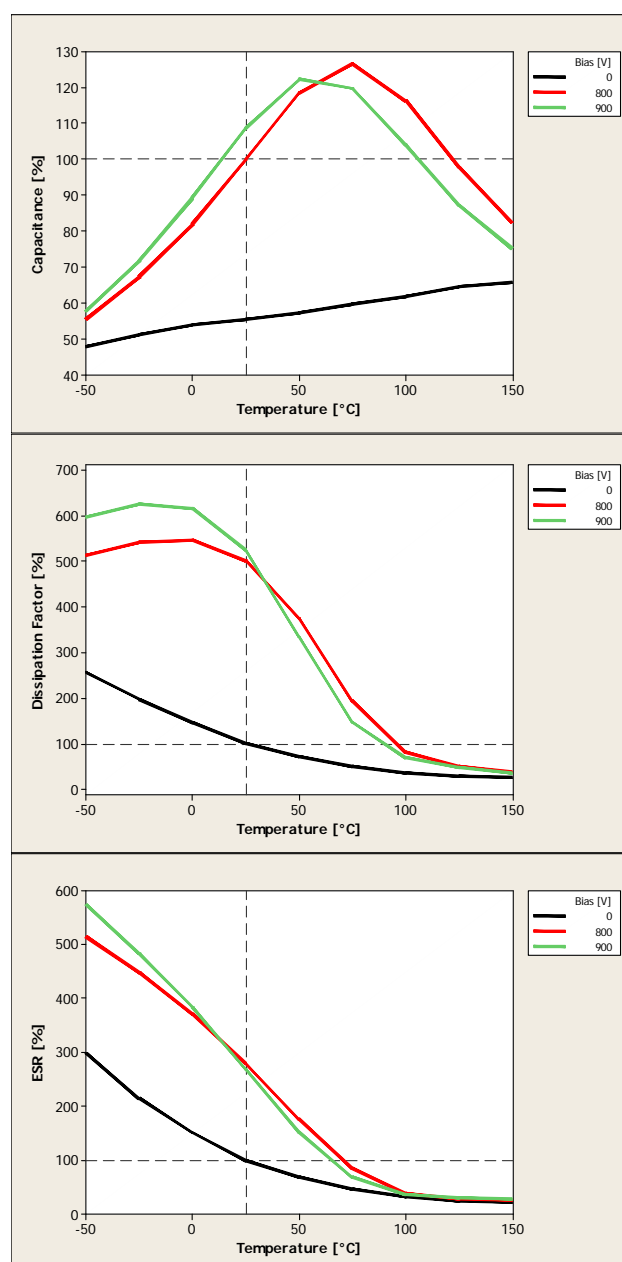
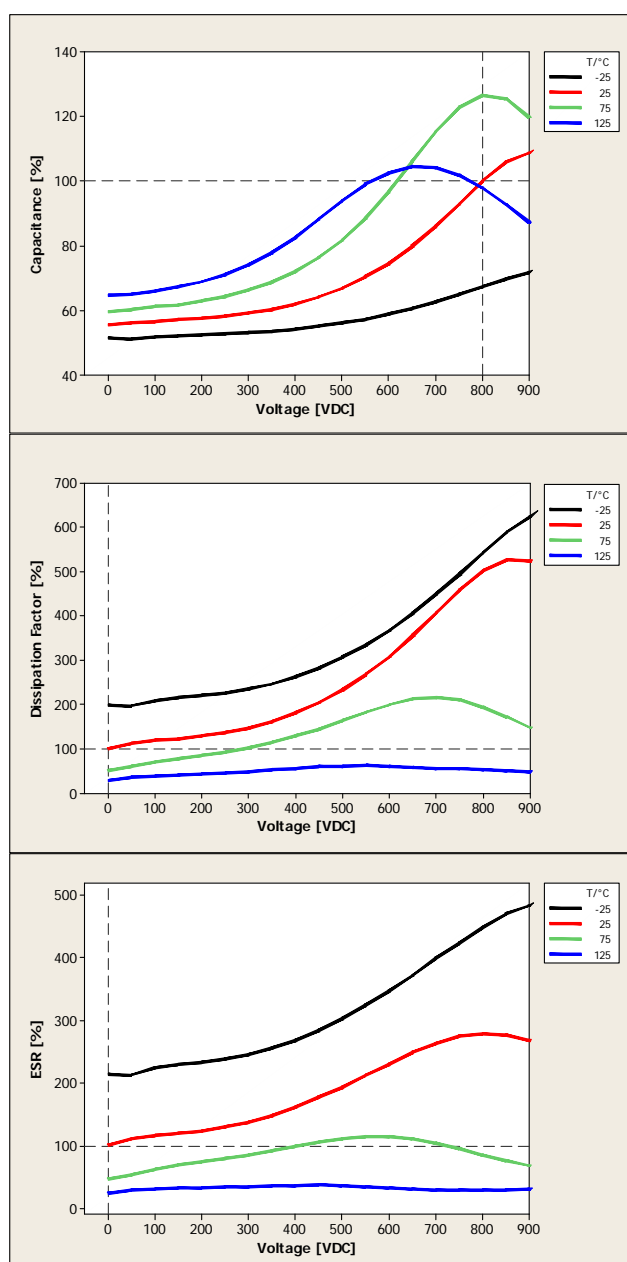
The capacitance has an aging behavior which shows a decrease of capacitance with time.  
 The typical aging rate is about 2.5% per logarithmic decade in hours.

# Typical characteristics as a function of temperature and voltage $V_R = 900\text{ V}$

( $V_{AC} = 0.5 V_{RMS}$ , frequency = 1 kHz)

All given temperatures are device temperatures.

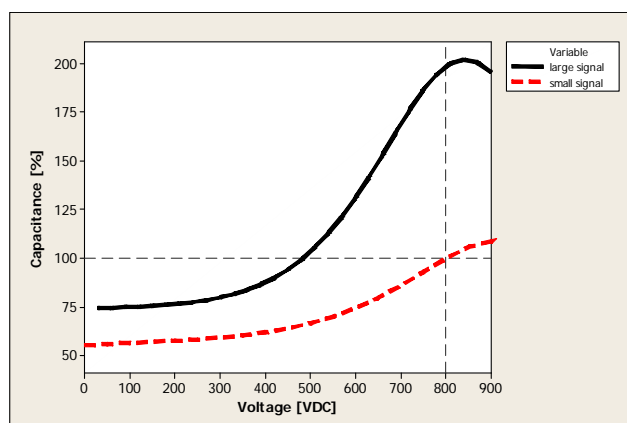
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to  $C_{eff, typ}$  and  $\tan \delta$  which are given on pages 2, 3 and 4 of this data sheet.



## Application Notes

Further typical electrical characteristics as a design reference for CeraLink applications.

### Typical capacitance values as a function of voltage $V_R = 900\text{ V}$ – valid for FA2, FA3 and FA10



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C

The nominal capacitance is defined as the large signal capacitance at  $V_{op}$ .

See glossary for further information.

Small signal capacitance:

0.5  $V_{RMS}$ , 1 kHz, +25 °C

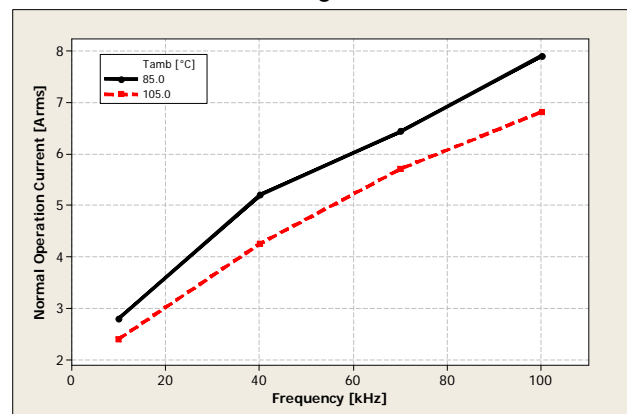
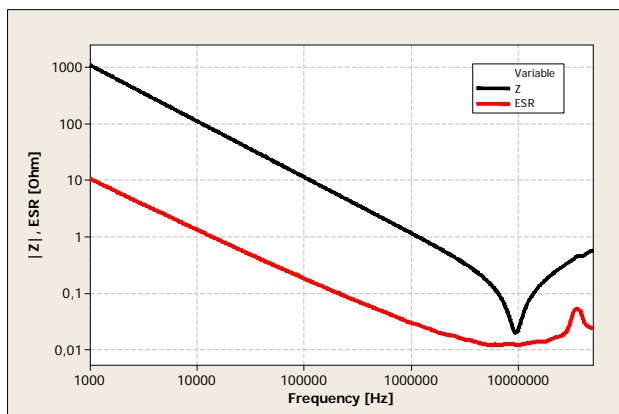
The effective capacitance is defined as the small signal capacitance at  $V_{op}$ .

## Typical impedance, ESR and permissible current as a function of frequency $V_R = 900\text{ V}$

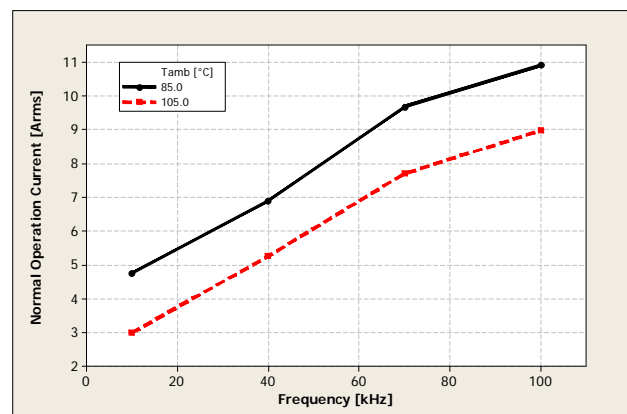
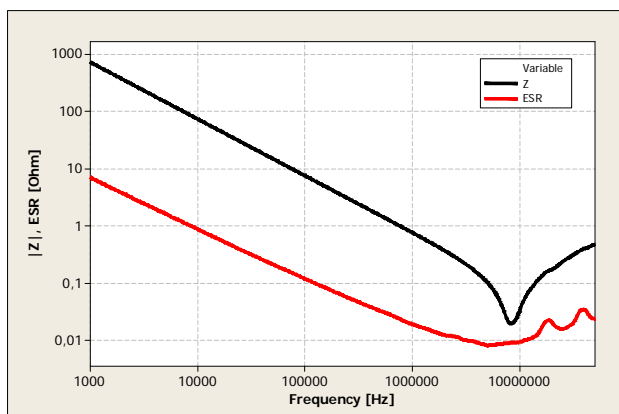
$V_{DC} = 0\text{ V}$ ,  
 $V_{AC} = 0.5\text{ V}_{RMS}$ ,  
 $T_{device} = +25\text{ }^{\circ}\text{C}$

Measurements performed at  $V_{op}$ .  
 The values correspond to a device temperature of  $+150\text{ }^{\circ}\text{C}$ . No forced cooling was used.

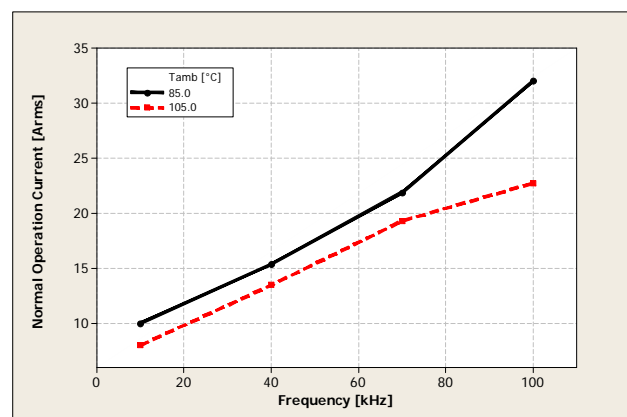
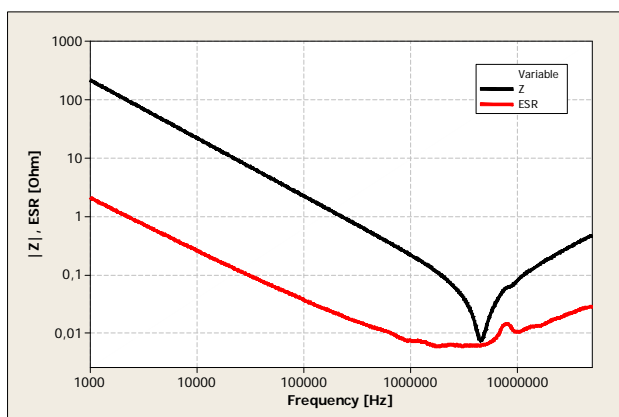
FA2



FA3



FA10



## Aging

The capacitance has an aging behavior which shows a decrease of capacitance with time.  
 The typical aging rate is about 2.5% per logarithmic decade in hours.

## Reliability

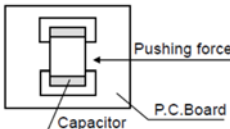
### A. Preconditioning:

- Reflow solder the capacitor on a PCB using the recommended soldering profile
- Check of external appearance
- Measurement of electrical parameters  $R_{ins}$ ,  $C_0$ ,  $\tan \delta$ 
  - Apply  $V_{pk,max}$  for 7 seconds and measure  $R_{ins}$  at room temperature:  
Isolation resistance (@  $V_{pk,max}$ , 7 s, 25 °C)  **$R_{ins} > 100 \text{ M}\Omega$**
  - Measure  $C_0$  and  $\tan \delta$  within 10 minutes to 1 hour afterwards:  
Initial capacitance (@ 0  $V_{DC}$ , 0.5  $V_{RMS}$ , 1 kHz, 25 °C)  
Dissipation factor (@ 0  $V_{DC}$ , 0.5  $V_{RMS}$ , 1 kHz, 25 °C)

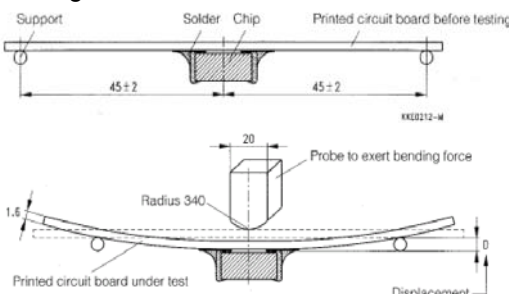
### B. Performance of a specific reliability test.

### C. After performing a specific test:

- Check the external appearance again
- Repeat the measurement of the electrical parameters
  - Apply  $V_{pk,max}$  for 7 seconds and measure  $R_{ins}$  at room temperature:  
Isolation resistance (@  $V_{pk,max}$ , 7 s, 25 °C)  **$R_{ins} > 10 \text{ M}\Omega$**
  - Measure  $C$  and  $\tan \delta$ :  
Change of initial capacitance (@ 0  $V_{DC}$ , 0.5  $V_{RMS}$ , 1 kHz, 25 °C)  **$|\Delta C_0 / C_0| < 15\%$**
  - Dissipation factor (@ 0  $V_{DC}$ , 0.5  $V_{RMS}$ , 1 kHz, 25 °C)  **$\tan \delta < 0.05$**

Test	Standard	Test conditions	Criteria
External appearance		Visual inspection with magnifying glass	No defects that might affect performance
High temperature operating life	MIL-STD-202, method 108	+150 °C, $V_R$ , 1000 hours	No mechanical damage $ \Delta C_0 / C_0 $ , $\tan \delta$ and $R_{ins}$ within defined limits
Biased humidity	MIL-STD-202, method 103	+85 °C, 85% rel. hum., $V_R$ , 1000 hours	No mechanical damage $ \Delta C_0 / C_0 $ , $\tan \delta$ and $R_{ins}$ within defined limits
Temperature shock	IEC 60384-9, 4.8	-55 °C to +150 °C 20 seconds transfer time 15 minutes dwell time 1000 cycles	No mechanical damage $ \Delta C_0 / C_0 $ , $\tan \delta$ and $R_{ins}$ within defined limits
Terminal strength test	AEC-Q200-005	Apply a force of 17.7 N for 60 seconds 	No detaching of termination. No rupture of ceramic $ \Delta C_0 / C_0 $ , $\tan \delta$ and $R_{ins}$ within defined limits



Test	Standard	Test conditions	Criteria
Board flex	AEC-Q200-005	Bending of 2 mm for 60 seconds  Dimensions in mm	No mechanical damage $ \Delta C_0 / C_0 $ , $\tan \delta$ and $R_{ins}$ within defined limits
Vibration	MIL-STD-202, method 204	5 g/ 20 min, 12 cycles, 3 axis 10 Hz to 2000 Hz	No mechanical damage $ \Delta C_0 / C_0 $ , $\tan \delta$ and $R_{ins}$ within defined limits
Mechanical shock	MIL-STD-202, method 213	Acceleration 400 m/s <sup>2</sup> Half sine pulse duration 6 milliseconds 4000 bumps	No mechanical damage $ \Delta C_0 / C_0 $ , $\tan \delta$ and $R_{ins}$ within defined limits
Reflow test		3 times recommended reflow soldering profile	No mechanical damage Proper solder coating of contact areas $ \Delta C_0 / C_0 $ , $\tan \delta$ and $R_{ins}$ within defined limits
Leaching test (lead frame only)	MIL-STD-202, method 210, condition B	Dip test of contact areas in solder bath (+260 °C for 10 seconds)	No damage of lead frame silver coating
Solderability (lead frame only)	J-STD-002, method A @ +235 °C, category 3	Dip test of contact areas in solder bath +(235 °C for 5 ± 0.5 seconds)	> 95% wettability of lead frame
Resistance to solvent		Dipping and cleaning with isopropanol	Marking must be legible $ \Delta C_0 / C_0 $ , $\tan \delta$ and $R_{ins}$ within defined limits
Geometry		Using a caliper	Within specified tolerance in the chapter construction

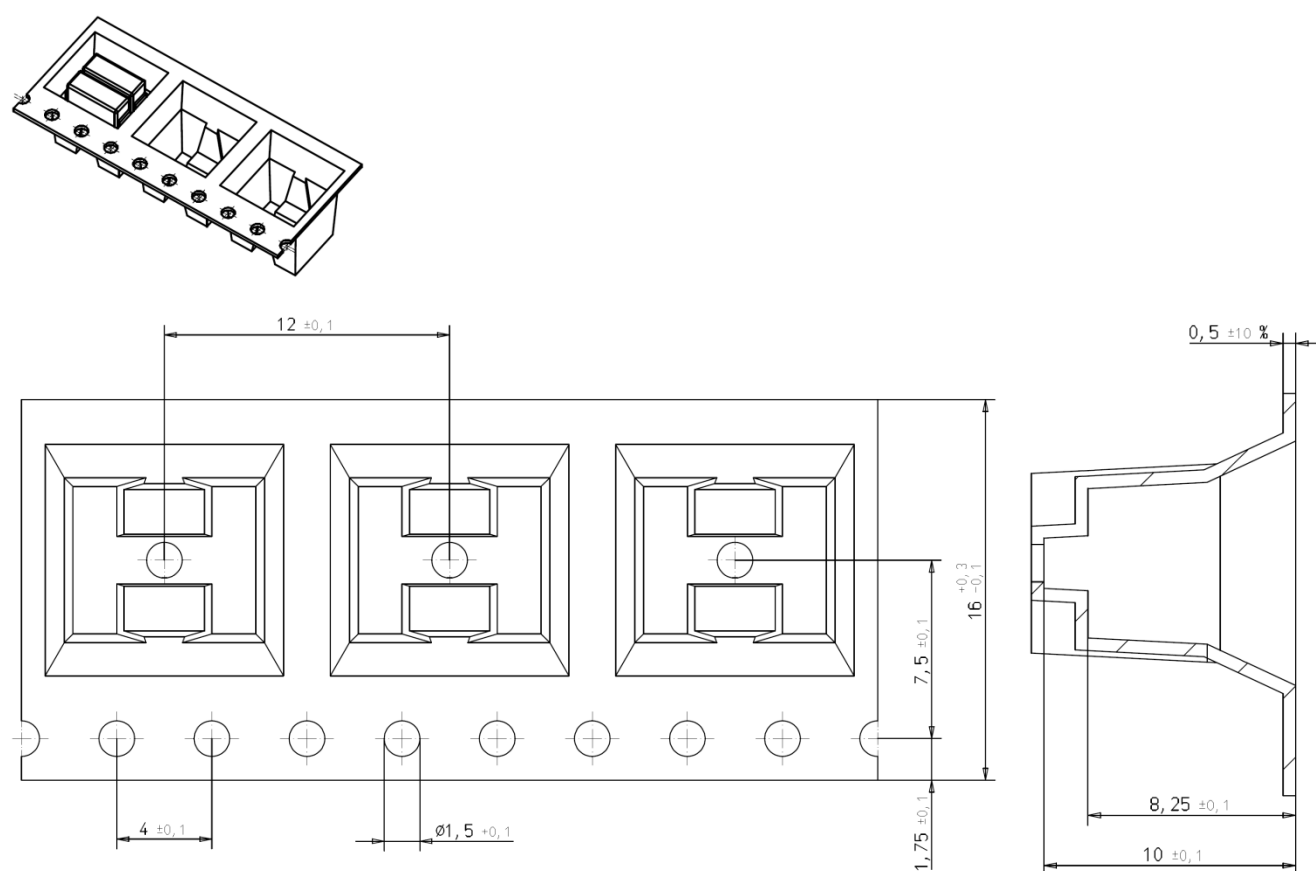
## Packaging

The CeraLink FA2 type is delivered in a blister tape (taping to IEC 60286-3, 180-mm / 330-mm reel available with 110 / 500 pieces per reel).

The CeraLink FA3 type is delivered in a blister tape (taping to IEC 60286-3, 180-mm / 330-mm reel available with 100 / 350 pieces per reel).

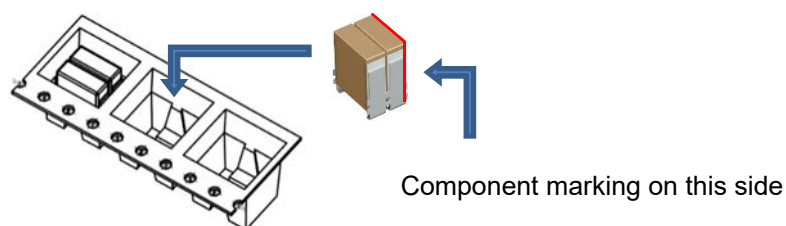
The CeraLink FA10 type is delivered in a cardboard box with 100 pieces per box.

### Blister tape for FA2

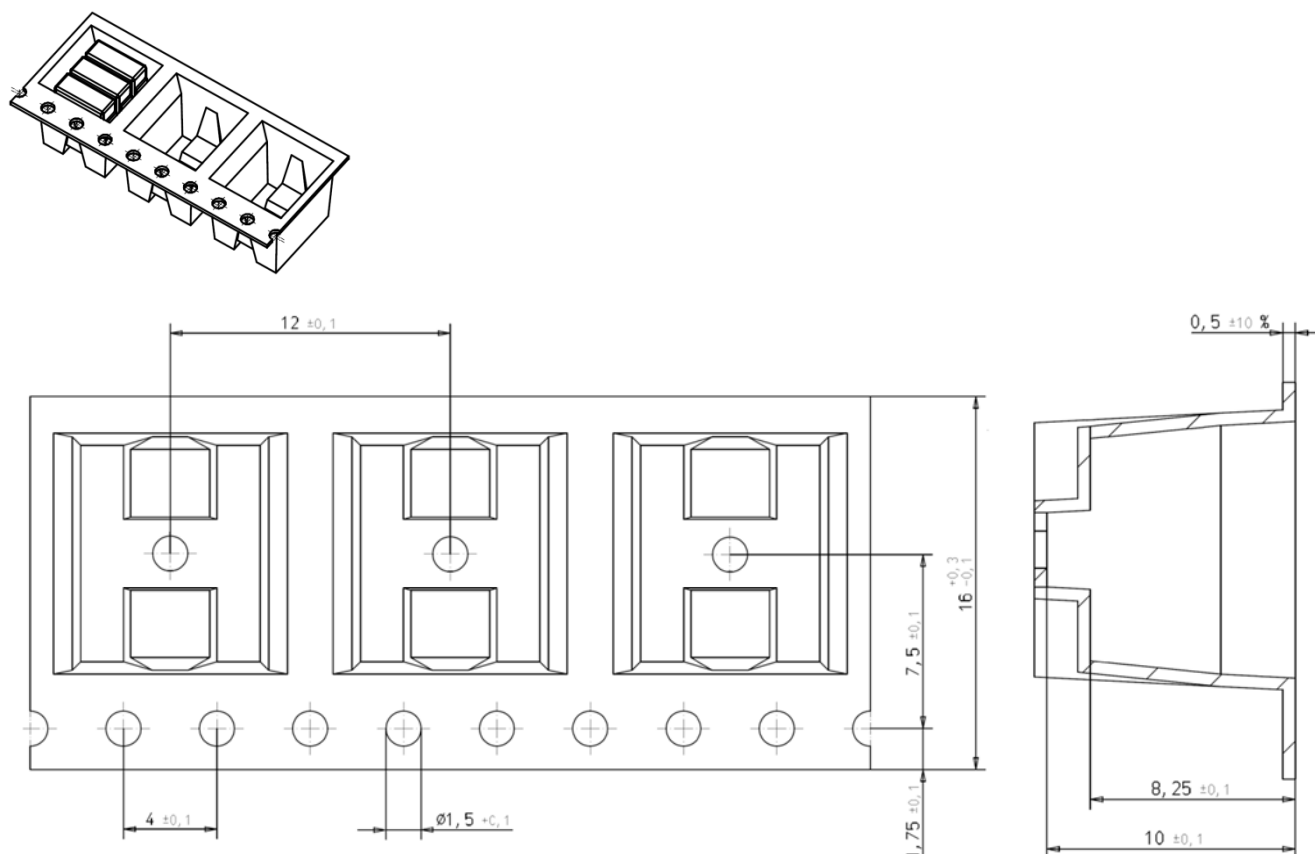


### Part orientation

The part-orientation/polarity is the same for all CeraLink FA2 capacitors within the blister tape.

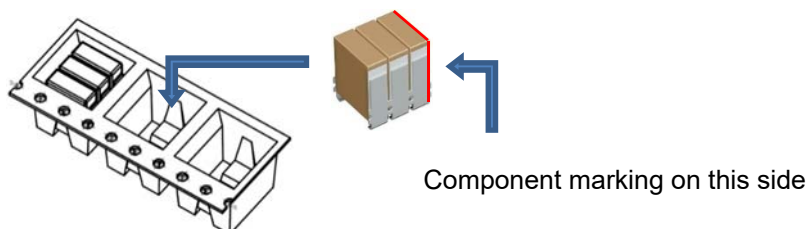


### Blister tape for FA3



## Part orientation

The part-orientation/polarity is the same for all CeraLink FA3 capacitors within the blister tape.

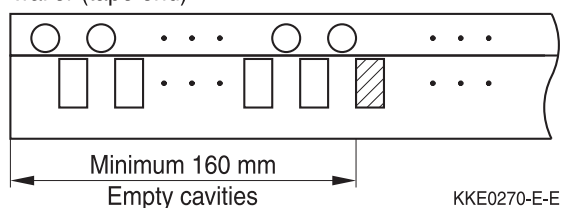


## Taping information

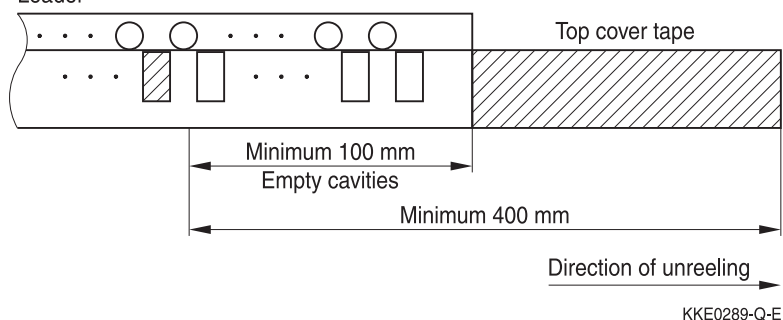
Trailer: There is a minimum of 160 mm of carrier tape with empty compartments and sealed by the cover tape.

Leader: There is a minimum of 400 mm of cover tape, which includes at least 100 mm of carrier tape with empty compartments.

Trailer (tape end)

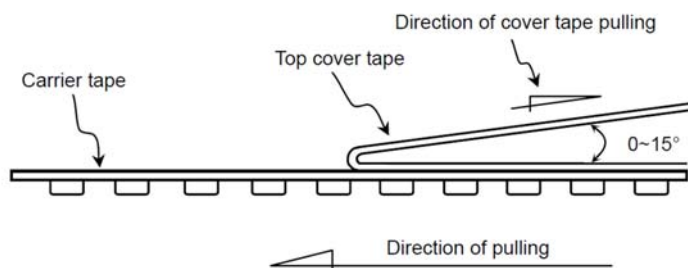


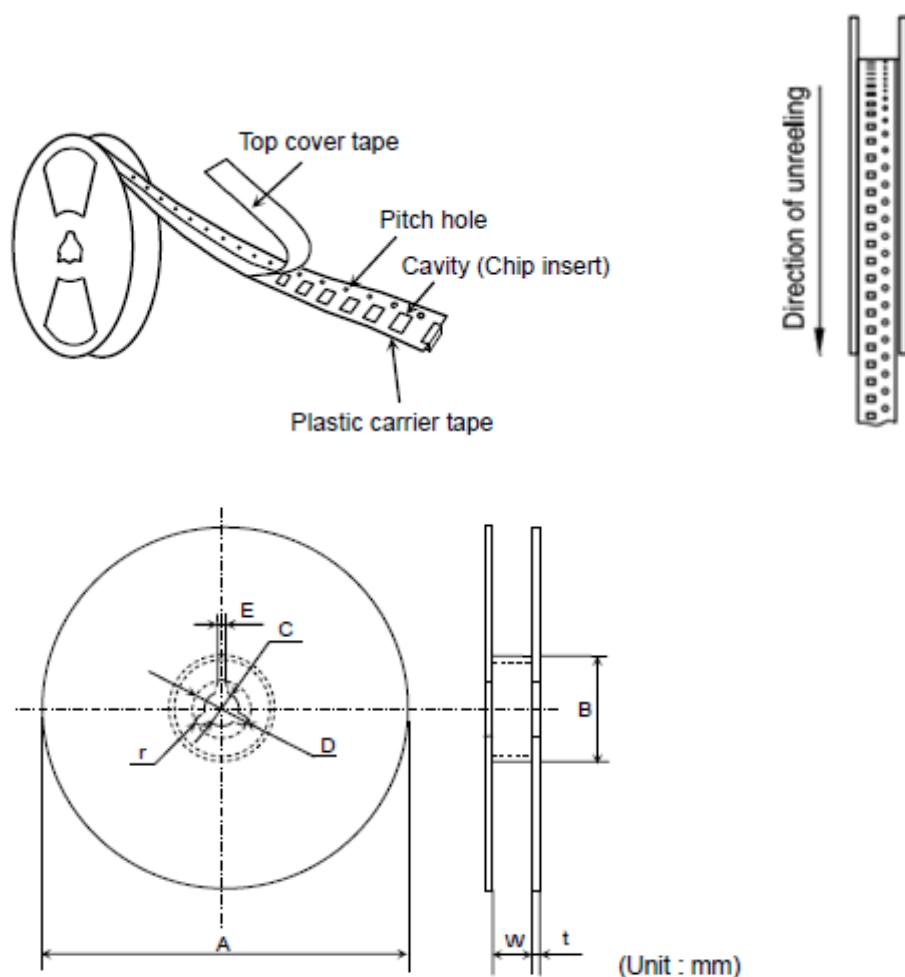
Leader



## Fixing peeling strength (top tape)

The peeling strength is 0.1 ... 1.3 N.

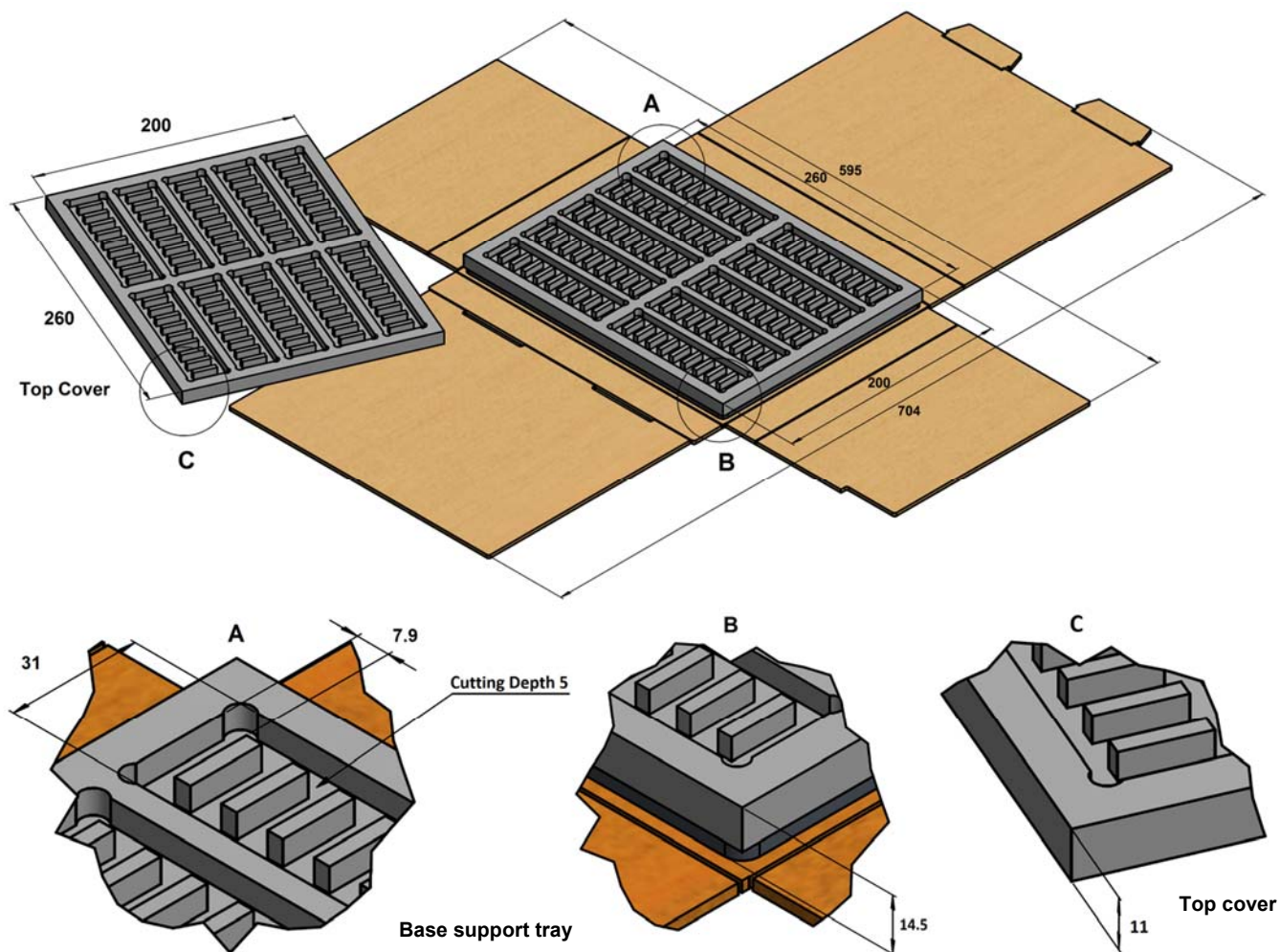


**Reel packing**


	FA2 & FA3 Type 330-mm reel	FA2 & FA3 Type 180-mm reel
A	330 ±2	180 ±3
B	62 ±1	62 ±1
C	12.8 +0.7	13.1 ±0.5
D	19.1 min.	19.1 min.
E	1.6 ±0.5	2.1 ±0.5
W	16.4 +2	17.0 -0.5 / +2

Dimensions in mm

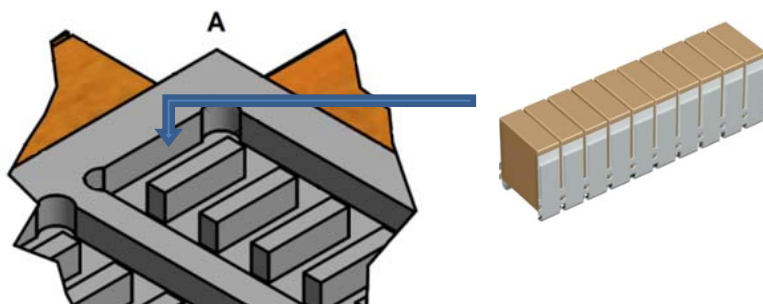
## Cardboard box for FA10



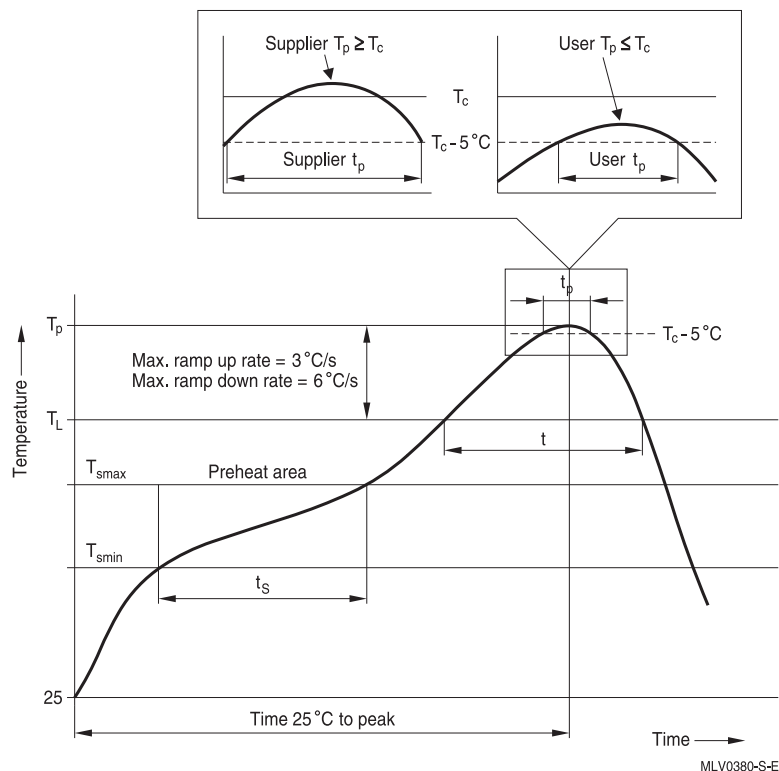
Dimensions in mm

## Part orientation

The part-orientation/polarity is the same for all CeraLink FA10 capacitors within the tray. Parts are placed with leadframes facing base support tray as shown.



## Recommended reflow soldering profile



Profile feature		SAC, Sn95.5Ag3.8Cu0.7 @ N <sub>2</sub> atmosphere
Preheat and soak		
- Temperature min	$T_{smin}$	+150 °C
- Temperature max	$T_{smax}$	+200 °C
- Time	$t_{smin}$ to $t_{smax}$	60 ... 120 seconds
Average ramp-up rate	$T_L$ to $T_p$	3 °C/ second max.
Liquidus temperature	$T_L$	+217 °C
Time at liquidus temperature	$t_L$	60 ... 150 seconds
Peak package body temperature	$T_p^{1)}$	245 °C ... 260 °C max. <sup>2)</sup>
Time ( $t_p$ ) <sup>3)</sup> within +5 °C of specified classification temperature ( $T_c$ )		30 seconds <sup>3)</sup>
Average ramp-down rate	$T_p$ to $T_L$	+6 °C/ second max.
Time +25 °C to peak temperature		maximum 8 minutes

1) Tolerance for peak profile temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.

2) Depending on package thickness (cf. JEDEC J-STD-020D).

3) Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.

### Notes:

All temperatures refer to topside of the package, measured on the package body surface.

Max. number of reflow cycles: 3

After the soldering process, the capacitance is lowered. Applying  $V_R$  to the device will re-establish the capacitance.

The proposed soldering profile is based on IEC 60068-2-58 (respectively JEDEC J-STD-020D) recommendations

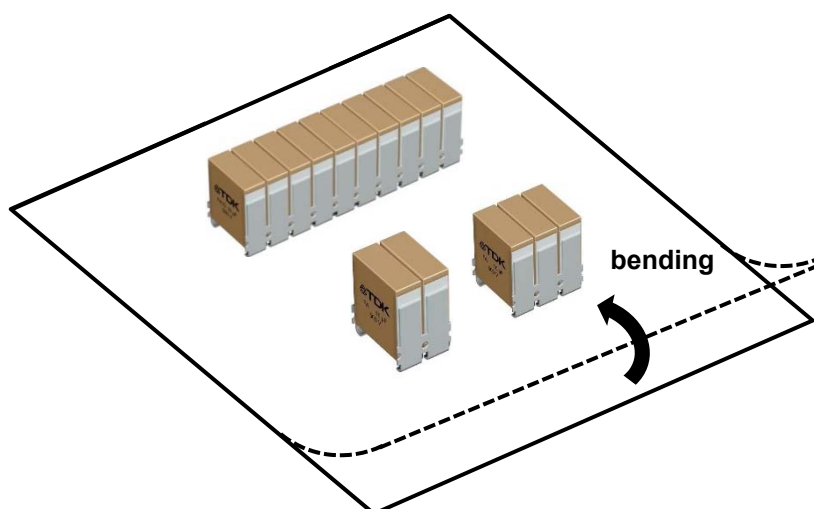
## General technical information

### Storage

- Only store CeraLink capacitors in their original packaging. Do not open the package prior to processing.
- Storage conditions in original packaging: temperature  $-25\text{ }^{\circ}\text{C}$  to  $+45\text{ }^{\circ}\text{C}$ , relative humidity  $\leq 75\%$  annual average, maximum 95%, dew precipitation is inadmissible.
- Do not store CeraLink capacitors where they are exposed to heat or direct sunlight. Otherwise the packaging material may be deformed or CeraLink may stick together, causing problems during mounting.
- Avoid contamination of the CeraLink surface during storage, handling and processing.
- Avoid storing CeraLink devices in harmful environments where they are exposed to corrosive gases (e.g. SO<sub>x</sub>, Cl).
- Use CeraLink as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- Solder CeraLink components within 6 months after shipment.

### Handling

- Do not drop CeraLink components or allow them to be chipped.
- Do not clamp CeraLink components on the face sides (e.g. during pick-and-place). A vacuum-based pick-and-place process picking the component on the top side is recommended.
- Do not touch CeraLink with your bare hands - gloves are recommended.
- Avoid contamination of the CeraLink surface during handling.
- The CeraLink FA series was tested to withstand the board flex test defined in the AEC-Q200 rev D, method 005.
- The CeraLink FA series uses copper-invar lead frames to prevent mechanical stress to the ceramic. Too much bending causes open mode. Avoid high mechanical stress like twisting after soldering on a PCB.



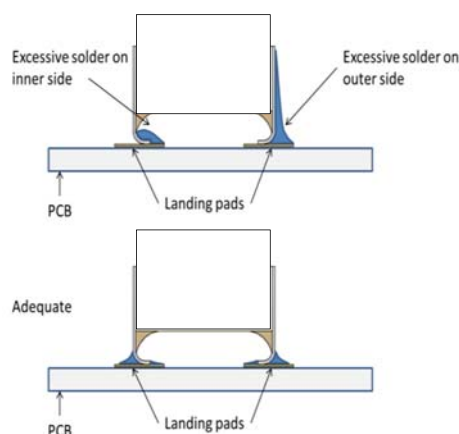


## Mounting

- Do not subject CeraLink devices to mechanical stress when encapsulating them with sealing material or overmolding with plastic material. Encapsulation may lead to worse heat dissipation too. Please ask for further information.
- Do not scratch the electrodes before, during or after the mounting process.
- Make sure contacts and housings used for assembly with CeraLink components are clean before mounting.
- The surface temperature of an operating CeraLink can be higher than the ambient temperature. Ensure that adjacent components are placed at a sufficient distance from a CeraLink to allow proper cooling.
- Avoid contamination of the CeraLink surface during processing.

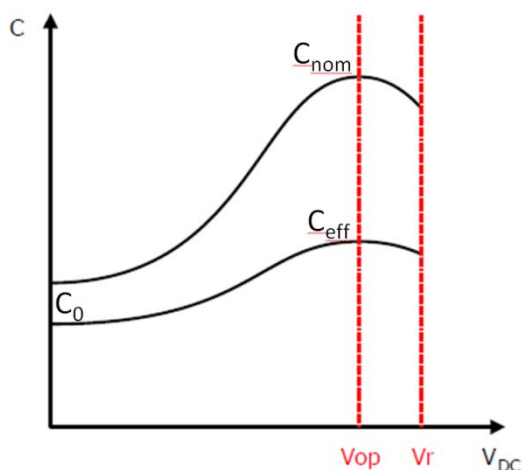
## Soldering guidelines

- The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.
- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.
- Excessive usage of solder paste can reduce the mechanical robustness of the device, whereas insufficient solder may cause the CeraLink to detach from the PCB. Use an adequate amount of solder paste, but on the landing pads only.



- If an unsuitable cleaning fluid is used, flux residue or foreign particles may stick to the CeraLink surface and deteriorate its insulation resistance. Insufficient or improper cleaning of the CeraLink may cause damage to the component.
- Excessive washing like ultrasonic cleaning, can affect the connection between the ceramic chip and the outer electrode. To avoid this, we give the following recommendation:
  - Power: 20 W/l max.
  - Frequency: 40 kHz max.
  - Washing time: 5 minutes max.

## Glossary



Initial capacitance  $C_0$ :

Is the value at the origin of the hysteresis without any applied direct voltage.

Effective capacitance  $C_{eff}$ :

Occurs at  $V_{op}$  and is measured with an applied ripple voltage of  $0.5 V_{RMS}$  and 1 kHz. The CeraLink is designed to have its highest capacitance value at the operating voltage  $V_{op}$ .

Nominal capacitance  $C_{nom}$ :

Is the value derived by the tangent of the mean hysteresis as the derivative of the mean hysteresis is  $dQ/dV \sim C$ .

## Symbols and terms

AC	Alternating current
$C_0$	Initial capacitance @ 0 V <sub>DC</sub> , 0.5 V <sub>RMS</sub> , 1 kHz, +25 °C
$C_{\text{eff,typ}}$	Typical effective capacitance @ V <sub>op</sub> , 0.5 V <sub>RMS</sub> , 1 kHz, +25 °C
$C_{\text{nom,typ}}$	Typical nominal capacitance @ V <sub>op</sub> , quasistatic, +25 °C. See glossary for definition of the nominal capacitance
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
I <sub>op</sub>	Operating ripple current, root mean square value of sinusoidal AC current
LP	Low profile
PCB	Printed circuit board
PLZT	Lead lanthanum zirconium titanate
R <sub>ins</sub>	Insulation resistance @ V <sub>pk,max</sub> , measurement time t = 7 s, +25 °C
R <sub>ins, typ</sub>	Insulation resistance @ V <sub>op</sub> , measurement time t > 240 s, +25 °C
SAC	Tin silver copper alloy; lead-free solder paste
T <sub>amb</sub>	Ambient temperature
tan δ	Dissipation factor @ 0 V <sub>DC</sub> , 0.5 V <sub>RMS</sub> , 1 kHz, +25 °C
T <sub>device</sub>	Device temperature. T <sub>device</sub> = T <sub>amb</sub> + ΔT (ΔT defines the self-heating of the device due to applied current).
V <sub>op</sub>	Operating voltage at maximum attenuation capability
V <sub>R</sub>	Rated voltage. Reference DC voltage for reliability tests.
V <sub>RMS</sub>	Root mean square value of sinusoidal AC voltage
V <sub>pk,max</sub>	Maximum peak operating voltage
ΔT	Increase of temperature during operation

## Cautions and warnings

### General

Not for use in resonant circuits, where a voltage of alternating polarity occurs.

Not for AC applications. Consult our local representative for further details.

If used in snubber circuits, ensure that the sum of all voltages remains at the same polarity.

Some parts of this publication contain statements about the suitability of our CeraLink components for certain areas of application, including recommendations about incorporation/design-in of these products into customer applications. The statements are based on our knowledge of typical requirements often made of our CeraLink devices in the particular areas. We nevertheless expressly point out that such statements cannot be regarded as binding statements about the suitability of our CeraLink components for a particular customer application. As a rule, TDK is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always incumbent on the customer to check and decide whether the CeraLink devices with the properties described in the product specification are suitable for use in a particular customer application.

- Do not use CeraLink components for purposes not identified in our specifications.
- Ensure the suitability of a CeraLink in particular by testing it for reliability during design-in. Always evaluate a CeraLink component under worst-case conditions.
- Pay special attention to the reliability of CeraLink devices intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).

### Design notes

- Consider derating at higher operating temperatures. As a rule, lower temperatures and voltages increase the life time of CeraLink devices.
- If steep surge current edges are to be expected, make sure your design is as low-inductive as possible.
- In some cases the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry, fuse or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraLink components that have not been subject to prior electrical, mechanical or thermal damage. The use of CeraLink devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures such as thermal fuses.

## Operation

- Use CeraLink only within the specified operating temperature range.
- Use CeraLink only within specified voltage and current ranges.
- The CeraLink has to be operated in a dry atmosphere, which must not contain any additional chemical vapors or substances.
- Environmental conditions must not harm the CeraLink. Use the capacitors under normal atmospheric conditions only. A reduction of the oxygen partial pressure to below 1 mbar is not permissible.
- Prevent a CeraLink from contacting liquids and solvents.
- Avoid dewing and condensation.
- During operation, the CeraLink can produce audible noise due to its piezoelectric characteristic.
- CeraLink components are mainly designed for encased applications. Under all circumstances avoid exposure to:
  - direct sunlight
  - rain or condensation
  - steam, saline spray
  - corrosive gases
  - atmosphere with reduced oxygen content

This listing does not claim to be complete, but merely reflects the experience of the manufacturer.

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## Important notes

The following applies to all products named in this publication:

1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application**. As a rule we are either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether a product with the properties described in the product specification is suitable for use in a particular customer application.
2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified**. In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.
3. **The warnings, cautions and product-specific notes must be observed.**
4. In order to satisfy certain technical requirements, **some of the products described in this publication may contain substances subject to restrictions in certain jurisdictions (e.g. because they are classed as hazardous)**. Useful information on this will be found in our Material Data Sheets on the Internet ([www.tdk-electronics.tdk.com/material](http://www.tdk-electronics.tdk.com/material)). Should you have any more detailed questions, please contact our sales offices.
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## Important notes

8. The trade names EPCOS, CeraCharge, CeraDiode, CeraLink, CeraPad, CeraPlas, CSMP, CTVS, DeltaCap, DigiSiMic, ExoCore, FilterCap, FormFit, LeaXield, MiniBlue, MiniCell, MKD, MKK, MotorCap, PCC, PhaseCap, PhaseCube, PhaseMod, PhiCap, PowerHap, PQSine, PQvar, SIFERRIT, SIFI, SIKOREL, SilverCap, SIMDAD, SiMic, SIMID, SineFormer, SIOV, ThermoFuse, WindCap are **trademarks registered or pending** in Europe and in other countries. Further information will be found on the Internet at [www.tdk-electronics.tdk.com/trademarks](http://www.tdk-electronics.tdk.com/trademarks).

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