



RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 87 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 1880 MHz.

1800 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 31.5$ Vdc, $I_{DQA} = 1080$ mA, $V_{GSB} = 0.25$ Vdc, $P_{out} = 87$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

| Frequency | G_{ps} (dB) | η_D (%) | Output PAR (dB) | ACPR (dBc) |
|-----------|---------------|--------------|-----------------|------------|
| 1805 MHz | 14.5 | 48.1 | 8.1 | -32.7 |
| 1840 MHz | 15.2 | 48.2 | 8.1 | -33.0 |
| 1880 MHz | 15.9 | 48.4 | 8.0 | -33.8 |

Features

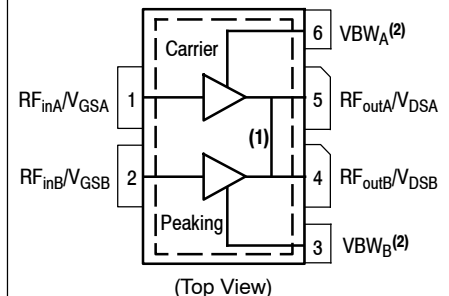
- Advanced High Performance In-Package Doherty
- High Thermal Conductivity Packaging Technology for Reduced Thermal Resistance
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Designed for Digital Predistortion Error Correction Systems

A2T18H455W23NR6

**1805–1880 MHz, 87 W AVG., 31.5 V
 AIRFAST RF POWER LDMOS
 TRANSISTOR**



**OM-1230-4L2S
 PLASTIC**



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

1. Pin connections 4 and 5 are DC coupled and RF independent.
2. Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.



Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|--|-----------|-------------|------|
| Drain-Source Voltage | V_{DSS} | -0.5, +65 | Vdc |
| Gate-Source Voltage | V_{GS} | -6.0, +10 | Vdc |
| Operating Voltage | V_{DD} | 32, +0 | Vdc |
| Storage Temperature Range | T_{stg} | -65 to +150 | °C |
| Case Operating Temperature Range | T_C | -40 to +125 | °C |
| Operating Junction Temperature Range (1,2) | T_J | -40 to +225 | °C |

Table 2. Thermal Characteristics

| Characteristic | Symbol | Value (2,3) | Unit |
|---|-----------------|-------------|------|
| Thermal Resistance, Junction to Case Case Temperature 77°C, 87 W Avg., W-CDMA, 31.5 Vdc, $I_{DQA} = 1080$ mA, $V_{GSB} = 0.25$ Vdc, 1840 MHz | $R_{\theta JC}$ | 0.23 | °C/W |

Table 3. ESD Protection Characteristics

| Test Methodology | Class |
|---------------------------------------|-------|
| Human Body Model (per JESD22-A114) | 2 |
| Machine Model (per EIA/JESD22-A115) | B |
| Charge Device Model (per JESD22-C101) | IV |

Table 4. Moisture Sensitivity Level

| Test Methodology | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3 | 260 | °C |

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Off Characteristics (4)

| | | | | | |
|---|-----------|---|---|----|-----------------|
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc) | I_{DSS} | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32$ Vdc, $V_{GS} = 0$ Vdc) | I_{DSS} | — | — | 5 | μAdc |
| Gate-Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc) | I_{GSS} | — | — | 1 | μAdc |

On Characteristics - Side A, Carrier

| | | | | | |
|---|--------------|------|------|-----|-----|
| Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 200$ μAdc) | $V_{GS(th)}$ | 1.05 | 1.2 | 2.2 | Vdc |
| Gate Quiescent Voltage ($V_{DD} = 31.5$ Vdc, $I_{DA} = 1080$ mAdc, Measured in Functional Test) | $V_{GSA(Q)}$ | 2.1 | 2.5 | 2.9 | Vdc |
| Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 2.0$ Adc) | $V_{DS(on)}$ | 0.05 | 0.15 | 0.3 | Vdc |

On Characteristics - Side B, Peaking

| | | | | | |
|--|--------------|------|------|-----|-----|
| Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 300$ μAdc) | $V_{GS(th)}$ | 0.8 | 1.2 | 1.6 | Vdc |
| Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 3$ Adc) | $V_{DS(on)}$ | 0.05 | 0.15 | 0.3 | Vdc |

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.nxp.com/RF/calculators>.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------|------|-------|-------|------|
| Functional Tests — 1805 MHz (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 31.5\text{ Vdc}$, $I_{DQA} = 1080\text{ mA}$, $V_{GSB} = 0.25\text{ Vdc}$, $P_{out} = 87\text{ W Avg.}$, $f = 1805\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset. | | | | | |
| Power Gain | G_{ps} | 14.0 | 14.5 | 17.0 | dB |
| Drain Efficiency | η_D | 43.0 | 48.1 | — | % |
| Output Peak-to-Average Ratio @ 0.01% Probability on CCDF | PAR | 7.3 | 8.1 | — | dB |
| Adjacent Channel Power Ratio | ACPR | — | -32.7 | -29.0 | dBc |

Functional Tests — 1880 MHz (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 31.5\text{ Vdc}$, $I_{DQA} = 1080\text{ mA}$, $V_{GSB} = 0.25\text{ Vdc}$, $P_{out} = 87\text{ W Avg.}$, $f = 1880\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.

| | | | | | |
|--|----------|------|-------|-------|-----|
| Power Gain | G_{ps} | 14.0 | 15.9 | 17.0 | dB |
| Drain Efficiency | η_D | 43.0 | 48.4 | — | % |
| Output Peak-to-Average Ratio @ 0.01% Probability on CCDF | PAR | 7.3 | 8.0 | — | dB |
| Adjacent Channel Power Ratio | ACPR | — | -33.8 | -29.0 | dBc |

Load Mismatch (3) (In Freescale Doherty Test Fixture, 50 ohm system) $I_{DQA} = 1080\text{ mA}$, $V_{GSB} = 0.25\text{ Vdc}$, $f = 1840\text{ MHz}$

| | |
|--|-----------------------|
| VSWR 10:1 at 32 Vdc, 575 W CW Output Power (3 dB Input Overdrive from 417 W CW Rated Power) | No Device Degradation |
|--|-----------------------|

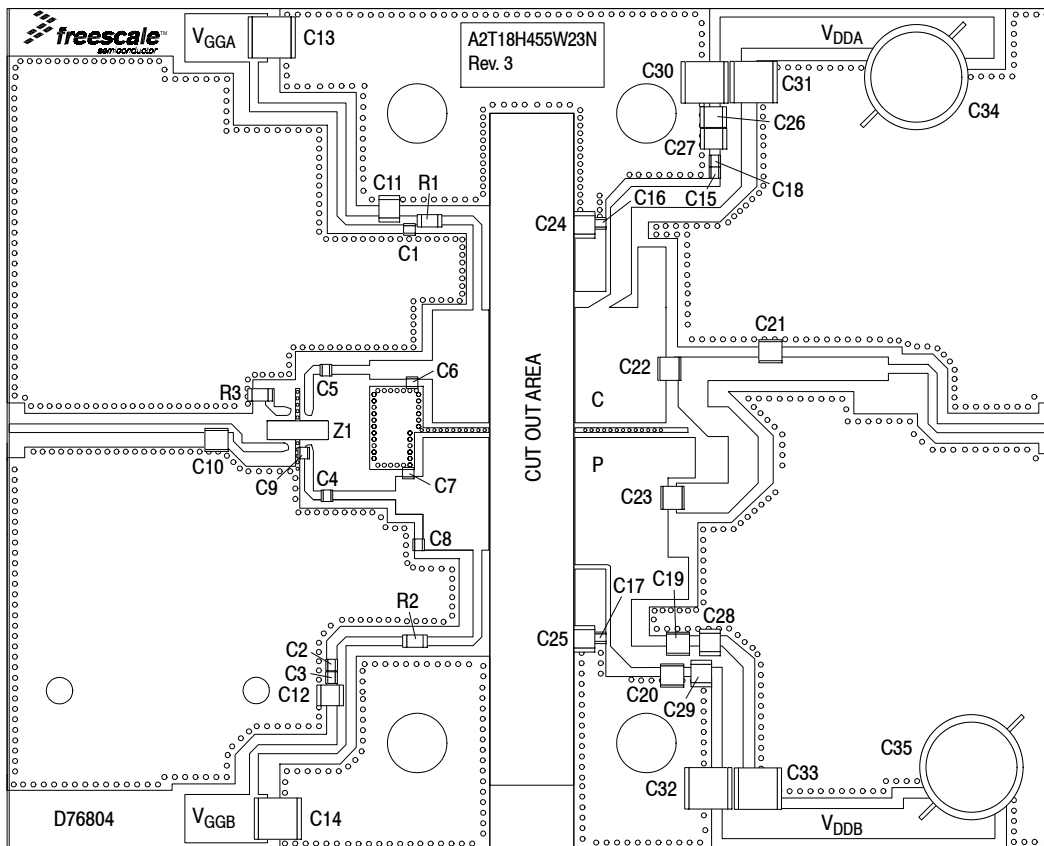
Typical Performance (3) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 31.5\text{ Vdc}$, $I_{DQA} = 1080\text{ mA}$, $V_{GSB} = 0.25$, 1805–1880 MHz Bandwidth

| | | | | | |
|--|---------------|---|-------|---|-------|
| P_{out} @ 1 dB Compression Point, CW | P1dB | — | 436 | — | W |
| P_{out} @ 3 dB Compression Point (4) | P3dB | — | 589 | — | W |
| AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz frequency range) | Φ | — | -21 | — | ° |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | VBW_{res} | — | 140 | — | MHz |
| Gain Flatness in 75 MHz Bandwidth @ $P_{out} = 87\text{ W Avg.}$ | G_F | — | 1.4 | — | dB |
| Gain Variation over Temperature (-30°C to +85°C) | ΔG | — | 0.012 | — | dB/°C |
| Output Power Variation over Temperature (-30°C to +85°C) | $\Delta P1dB$ | — | 0.007 | — | dB/°C |

Table 6. Ordering Information

| Device | Tape and Reel Information | Package |
|-----------------|---|--------------|
| A2T18H455W23NR6 | R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel | OM-1230-4L2S |

- V_{DDA} and V_{ddb} must be tied together and powered by a single DC power supply.
- Part internally matched both on input and output.
- Measurements made with device in an asymmetrical Doherty configuration.
- $P3dB = P_{avg} + 7.0\text{ dB}$ where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 1. A2T18H455W23NR6 Test Circuit Component Layout

Table 7. A2T18H455W23NR6 Test Circuit Component Designations and Values

| Part | Description | Part Number | Manufacturer |
|--|---|---------------------|--------------|
| C1, C2, C3, C4, C5, C15, C16, C17, C18 | 10 pF Chip Capacitors | GQM2195C2E100JB12D | Murata |
| C6 | 1 pF Chip Capacitor | GQM2195C2E1R0BB12D | Murata |
| C7 | 2.4 pF Chip Capacitor | GQM2195C2E2R4BB12D | Murata |
| C8 | 0.7 pF Chip Capacitor | GQM2195C2ER70BB12D | Murata |
| C9 | 1.3 pF Chip Capacitor | GQM2195C2E1R3BB12D | Murata |
| C10 | 0.2 pF Chip Capacitor | 800B0R2BT500XT | ATC |
| C11, C12, C24, C25, C26, C27, C28, C29 | 10 μ F Chip Capacitors | GRM32ER61H106KA12L | Murata |
| C13, C14, C30, C31, C32, C33 | 10 μ F Chip Capacitors | C5750X7S2A106M230KE | TDK |
| C19, C20 | 10 pF Chip Capacitors | ATC800B100JT500XT | ATC |
| C21 | 0.3 pF Chip Capacitor | ATC800B0R3BT500XT | ATC |
| C22 | 6.8 pF Chip Capacitor | ATC800B6R8BT500XT | ATC |
| C23 | 8.2 pF Chip Capacitor | ATC800B8R2BT500XT | ATC |
| C34, C35 | 470 μ F, 63 V Electrolytic Capacitors | MCGPR63V477M13X26 | Multicomp |
| R1, R2 | 3.3 Ω , 1/8 W Chip Resistors | WCR0805-3R3FI | Welwyn |
| R3 | 50 Ω , 10 W Termination | 060120A25X50-2 | Anaren |
| Z1 | 1800–2200 MHz Band, 90°, 2 dB Doherty Coupler | X3C20F1-02S | Anaren |
| PCB | Rogers RO4350B, 0.020", $\epsilon_r = 3.66$ | D76804 | MTL |

TYPICAL CHARACTERISTICS — 1805–1880 MHz

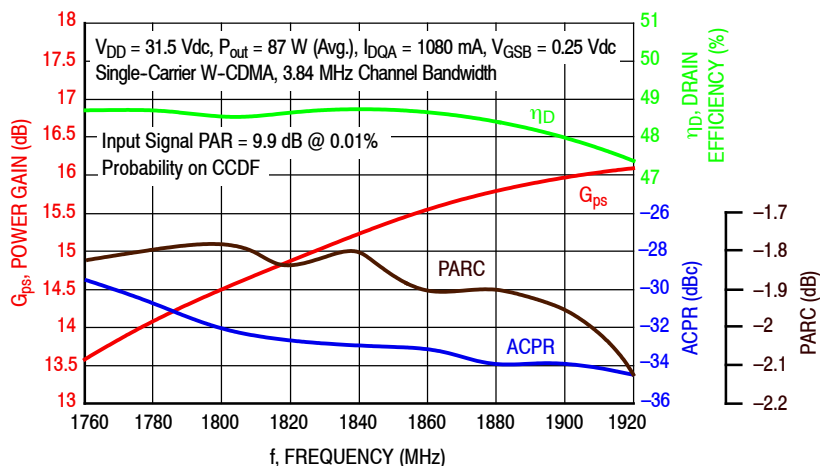


Figure 2. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 87$ Watts Avg.

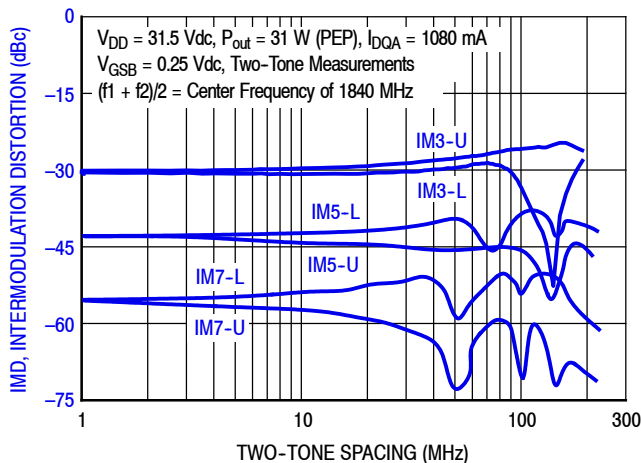


Figure 3. Intermodulation Distortion Products versus Two-Tone Spacing

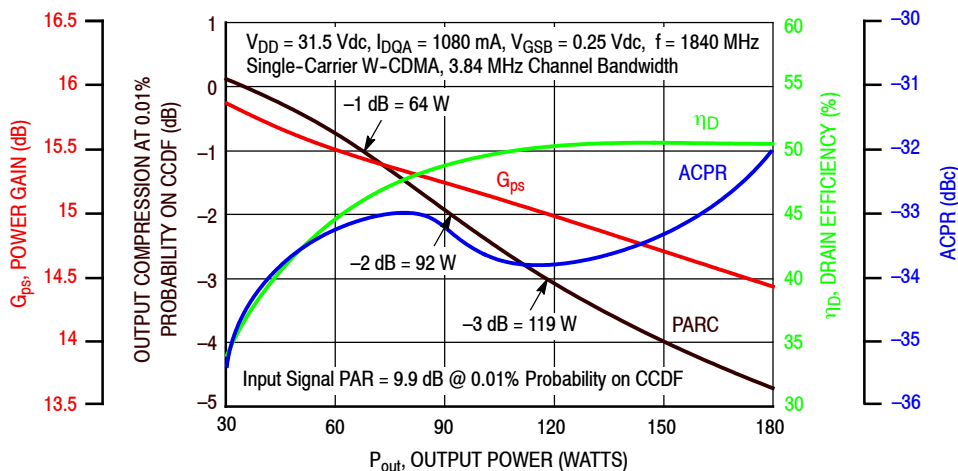


Figure 4. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1805–1880 MHz

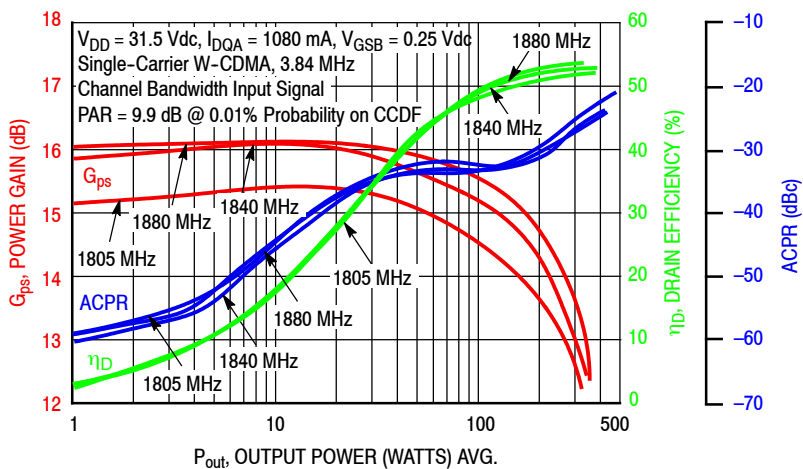


Figure 5. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

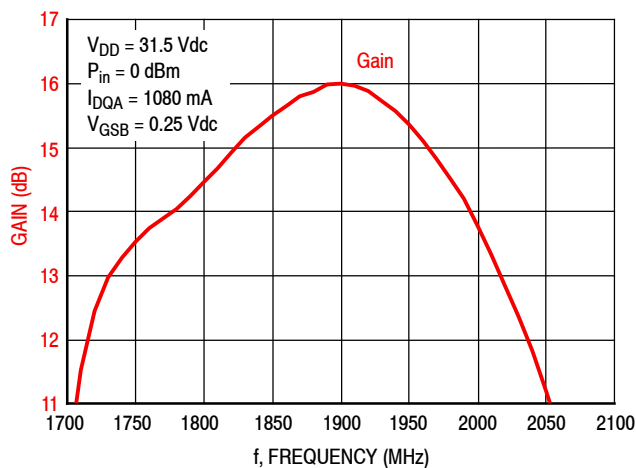


Figure 6. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning $V_{DD} = 31.5 \text{ Vdc}$, $I_{DQA} = 758 \text{ mA}$, Pulsed CW, $10 \mu\text{sec(on)}$, 10% Duty Cycle

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Output Power | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P1dB | | | | | |
| | | | $Z_{\text{load}}^{(1)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1800 | 1.95 – j6.68 | 2.39 + j6.81 | 1.02 – j2.85 | 17.3 | 52.6 | 184 | 53.9 | –14 |
| 1840 | 2.49 – j7.21 | 3.13 + j7.24 | 0.88 – j3.16 | 16.9 | 52.7 | 185 | 50.5 | –14 |
| 1880 | 3.51 – j8.21 | 4.17 + j7.60 | 0.84 – j3.24 | 17.2 | 52.6 | 183 | 50.3 | –16 |

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Output Power | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P3dB | | | | | |
| | | | $Z_{\text{load}}^{(2)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1800 | 1.95 – j6.68 | 2.26 + j7.13 | 0.96 – j3.04 | 14.9 | 53.4 | 218 | 53.0 | –19 |
| 1840 | 2.49 – j7.21 | 2.98 + j7.75 | 0.88 – j3.24 | 14.8 | 53.4 | 219 | 51.4 | –20 |
| 1880 | 3.51 – j8.21 | 4.21 + j8.41 | 0.84 – j3.36 | 15.0 | 53.3 | 214 | 50.4 | –21 |

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane. Z_{in} = Impedance as measured from gate contact to ground. Z_{load} = Measured impedance presented to the output of the device at the package reference plane.**Table 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning** $V_{DD} = 31.5 \text{ Vdc}$, $I_{DQA} = 758 \text{ mA}$, Pulsed CW, $10 \mu\text{sec(on)}$, 10% Duty Cycle

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Drain Efficiency | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P1dB | | | | | |
| | | | $Z_{\text{load}}^{(1)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1800 | 1.95 – j6.68 | 2.33 + j7.08 | 2.57 – j1.37 | 20.3 | 49.8 | 96 | 66.7 | –22 |
| 1840 | 2.49 – j7.21 | 3.15 + j7.49 | 2.25 – j1.61 | 20.2 | 49.9 | 97 | 65.2 | –22 |
| 1880 | 3.51 – j8.21 | 3.93 + j6.87 | 1.87 – j2.06 | 20.1 | 50.2 | 106 | 62.9 | –24 |

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Drain Efficiency | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P3dB | | | | | |
| | | | $Z_{\text{load}}^{(2)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1800 | 1.95 – j6.68 | 2.29 + j7.35 | 2.51 – j1.37 | 18.3 | 50.5 | 112 | 66.1 | –30 |
| 1840 | 2.49 – j7.21 | 3.04 + j7.85 | 1.93 – j1.94 | 17.9 | 51.2 | 132 | 65.0 | –28 |
| 1880 | 3.51 – j8.21 | 3.86 + j7.31 | 1.82 – j2.29 | 17.9 | 51.3 | 135 | 62.3 | –31 |

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

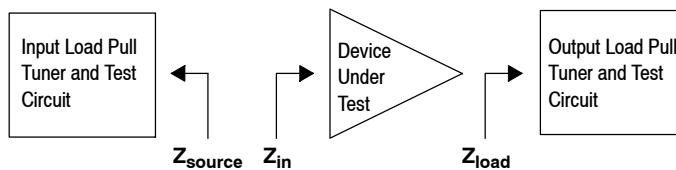
 Z_{source} = Measured impedance presented to the input of the device at the package reference plane. Z_{in} = Impedance as measured from gate contact to ground. Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

$V_{DD} = 31.5$ Vdc, $V_{GSB} = 0$ Vdc, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Output Power | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P1dB | | | | | |
| | | | $Z_{load}^{(1)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 1800 | 0.99 – j5.23 | 0.91 + j5.01 | 1.00 – j2.79 | 12.9 | 54.9 | 309 | 49.8 | –27 |
| 1840 | 1.13 – j5.22 | 1.04 + j5.21 | 0.98 – j2.99 | 13.4 | 54.9 | 307 | 49.6 | –28 |
| 1880 | 1.24 – j5.77 | 1.24 + j5.52 | 0.98 – j3.11 | 13.5 | 54.9 | 312 | 50.1 | –33 |

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Output Power | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P3dB | | | | | |
| | | | $Z_{load}^{(2)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 1800 | 0.99 – j5.23 | 0.90 + j5.14 | 1.04 – j2.95 | 10.8 | 55.6 | 365 | 52.8 | –34 |
| 1840 | 1.13 – j5.22 | 1.05 + j5.37 | 1.03 – j3.11 | 11.3 | 55.6 | 363 | 52.6 | –35 |
| 1880 | 1.24 – j5.77 | 1.27 + j5.73 | 1.03 – j3.24 | 11.5 | 55.6 | 366 | 52.7 | –40 |

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

$V_{DD} = 31.5$ Vdc, $V_{GSB} = 0$ Vdc, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Drain Efficiency | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P1dB | | | | | |
| | | | $Z_{load}^{(1)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 1800 | 0.99 – j5.23 | 0.83 + j5.01 | 2.93 – j2.55 | 14.2 | 53.5 | 223 | 62.9 | –34 |
| 1840 | 1.13 – j5.22 | 0.92 + j5.19 | 2.66 – j2.09 | 14.8 | 53.3 | 212 | 62.9 | –36 |
| 1880 | 1.24 – j5.77 | 1.10 + j5.49 | 2.13 – j2.13 | 14.8 | 53.5 | 226 | 63.1 | –39 |

| f (MHz) | Z_{source} (Ω) | Z_{in} (Ω) | Max Drain Efficiency | | | | | |
|---------|---------------------------|-----------------------|-------------------------------|-----------|-------|-----|--------------|--------------------|
| | | | P3dB | | | | | |
| | | | $Z_{load}^{(2)}$ (Ω) | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM ($^\circ$) |
| 1800 | 0.99 – j5.23 | 0.84 + j5.13 | 2.93 – j2.72 | 12.2 | 54.0 | 252 | 61.8 | –43 |
| 1840 | 1.13 – j5.22 | 0.95 + j5.35 | 2.72 – j2.18 | 12.7 | 53.8 | 239 | 61.9 | –46 |
| 1880 | 1.24 – j5.77 | 1.15 + j5.70 | 2.37 – j2.18 | 12.8 | 53.9 | 247 | 62.5 | –50 |

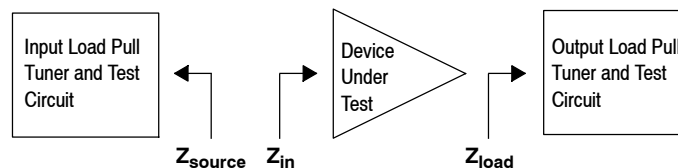
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

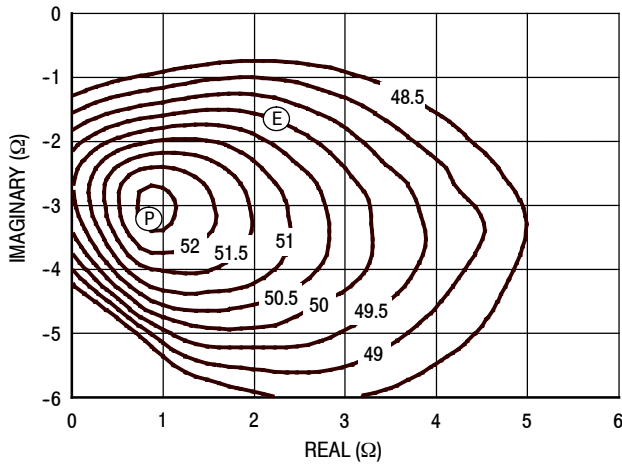


Figure 7. P1dB Load Pull Output Power Contours (dBm)

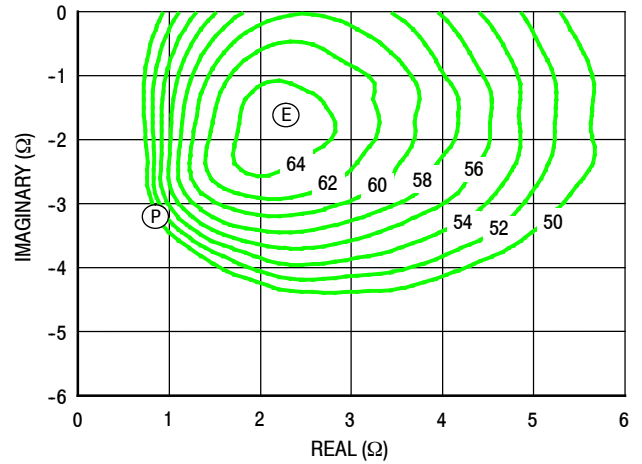


Figure 8. P1dB Load Pull Efficiency Contours (%)

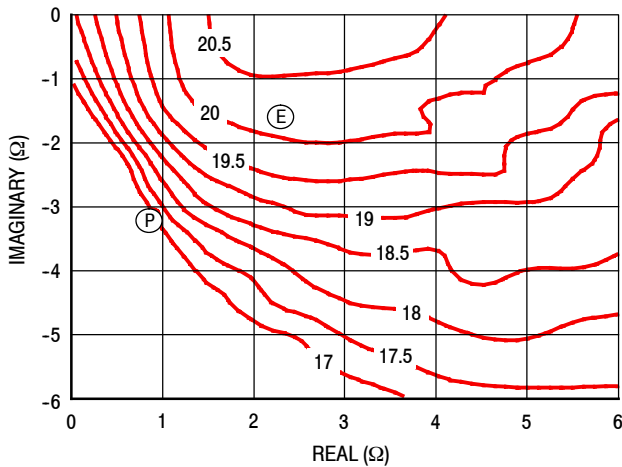


Figure 9. P1dB Load Pull Gain Contours (dB)

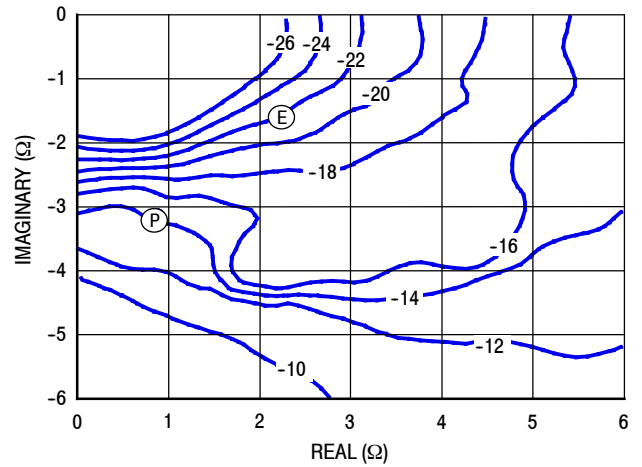


Figure 10. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

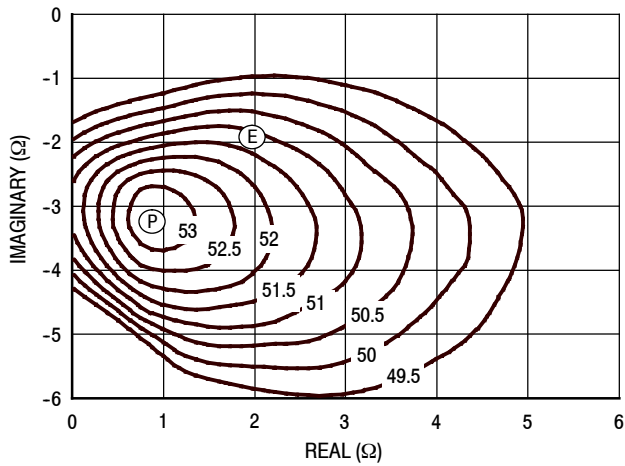


Figure 11. P3dB Load Pull Output Power Contours (dBm)

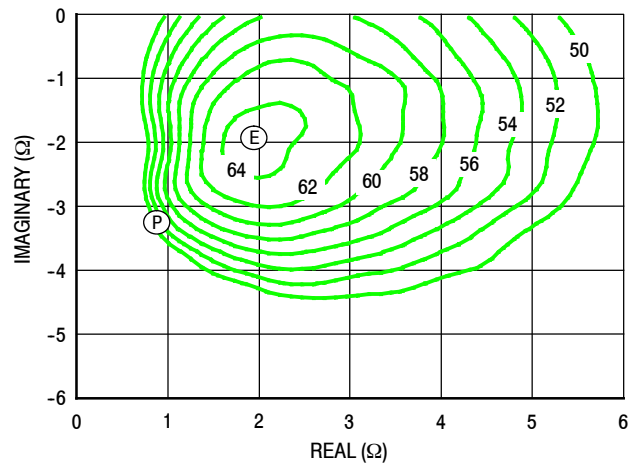


Figure 12. P3dB Load Pull Efficiency Contours (%)

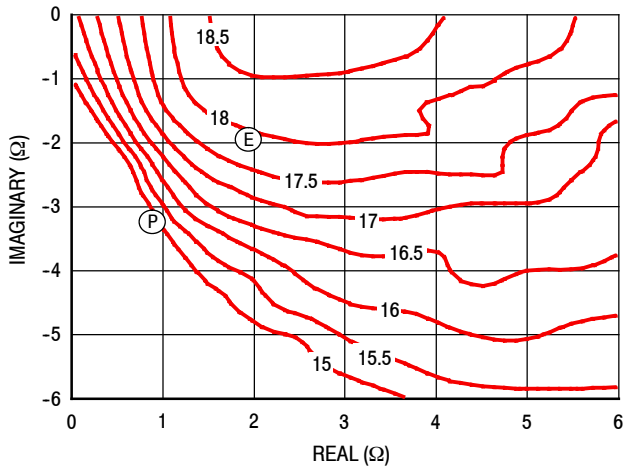


Figure 13. P3dB Load Pull Gain Contours (dB)

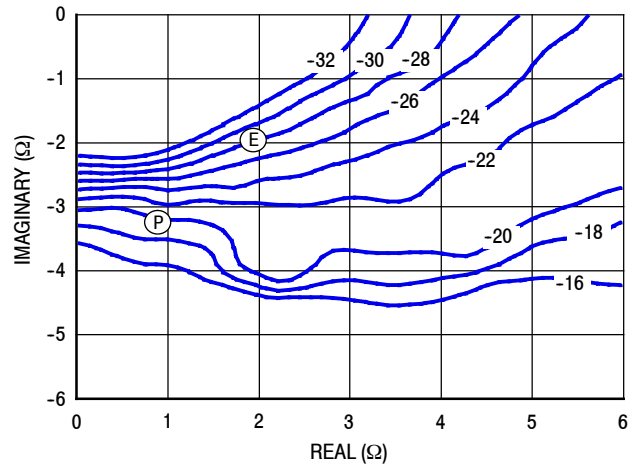


Figure 14. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

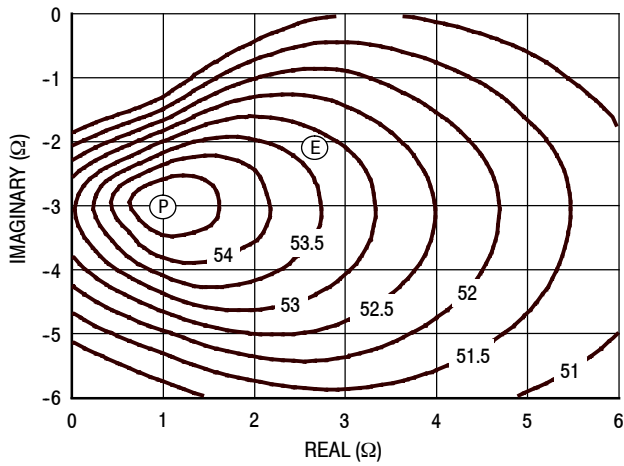


Figure 15. P1dB Load Pull Output Power Contours (dBm)

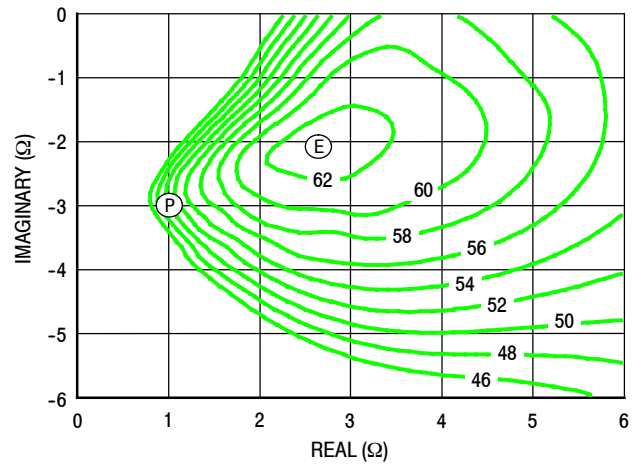


Figure 16. P1dB Load Pull Efficiency Contours (%)

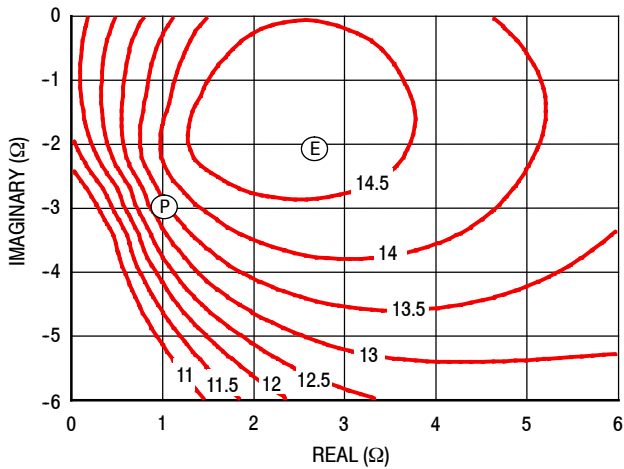


Figure 17. P1dB Load Pull Gain Contours (dB)

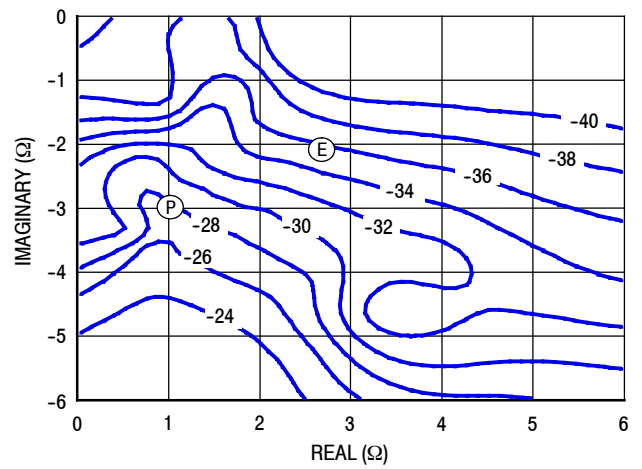


Figure 18. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

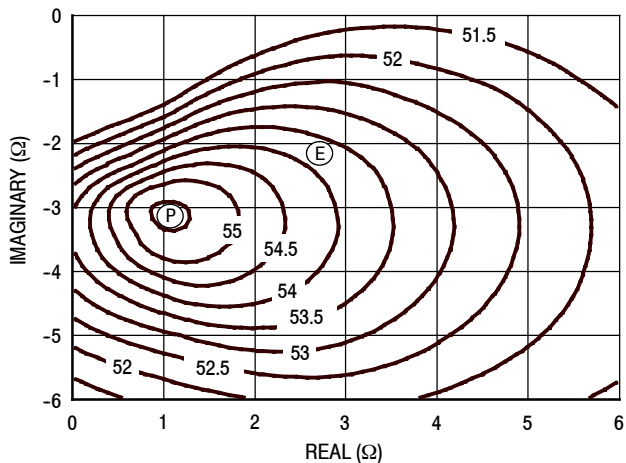


Figure 19. P3dB Load Pull Output Power Contours (dBm)

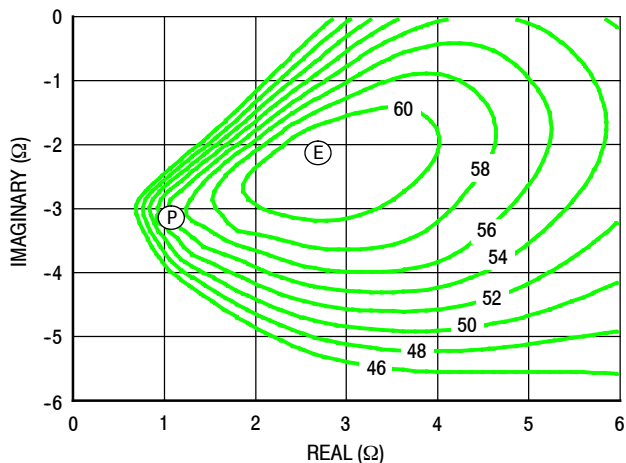


Figure 20. P3dB Load Pull Efficiency Contours (%)

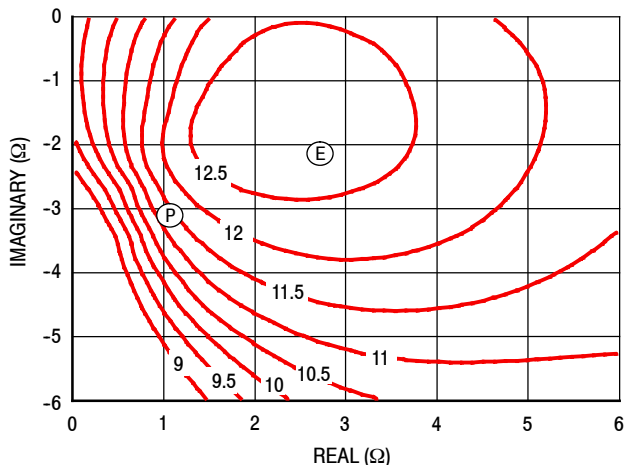


Figure 21. P3dB Load Pull Gain Contours (dB)

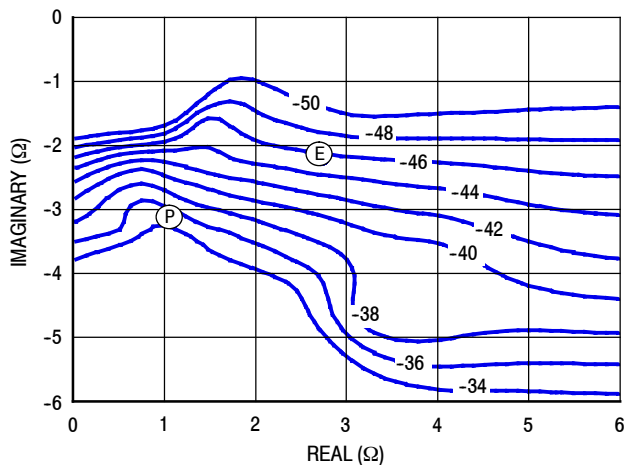
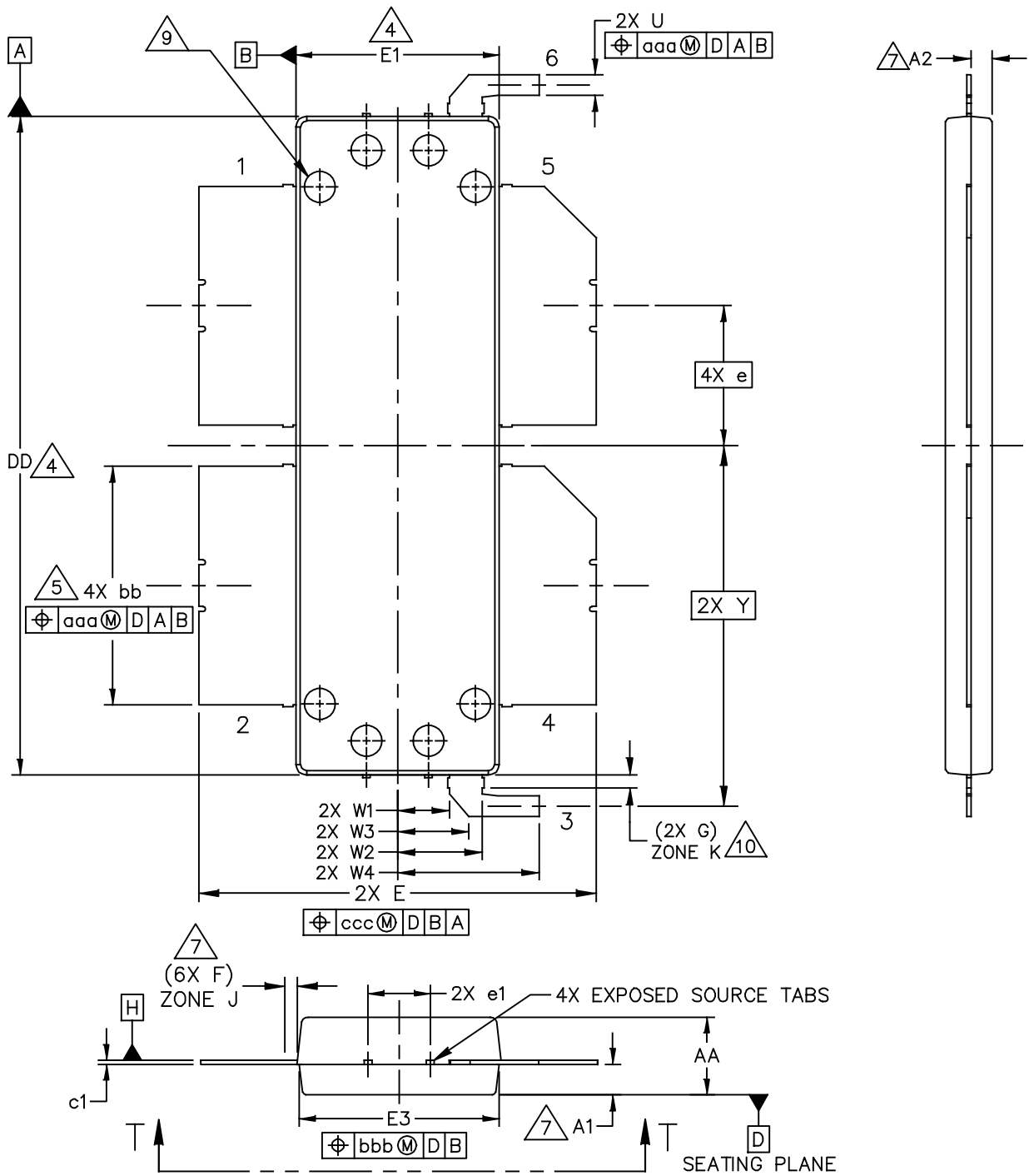


Figure 22. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
 (E) = Maximum Drain Efficiency

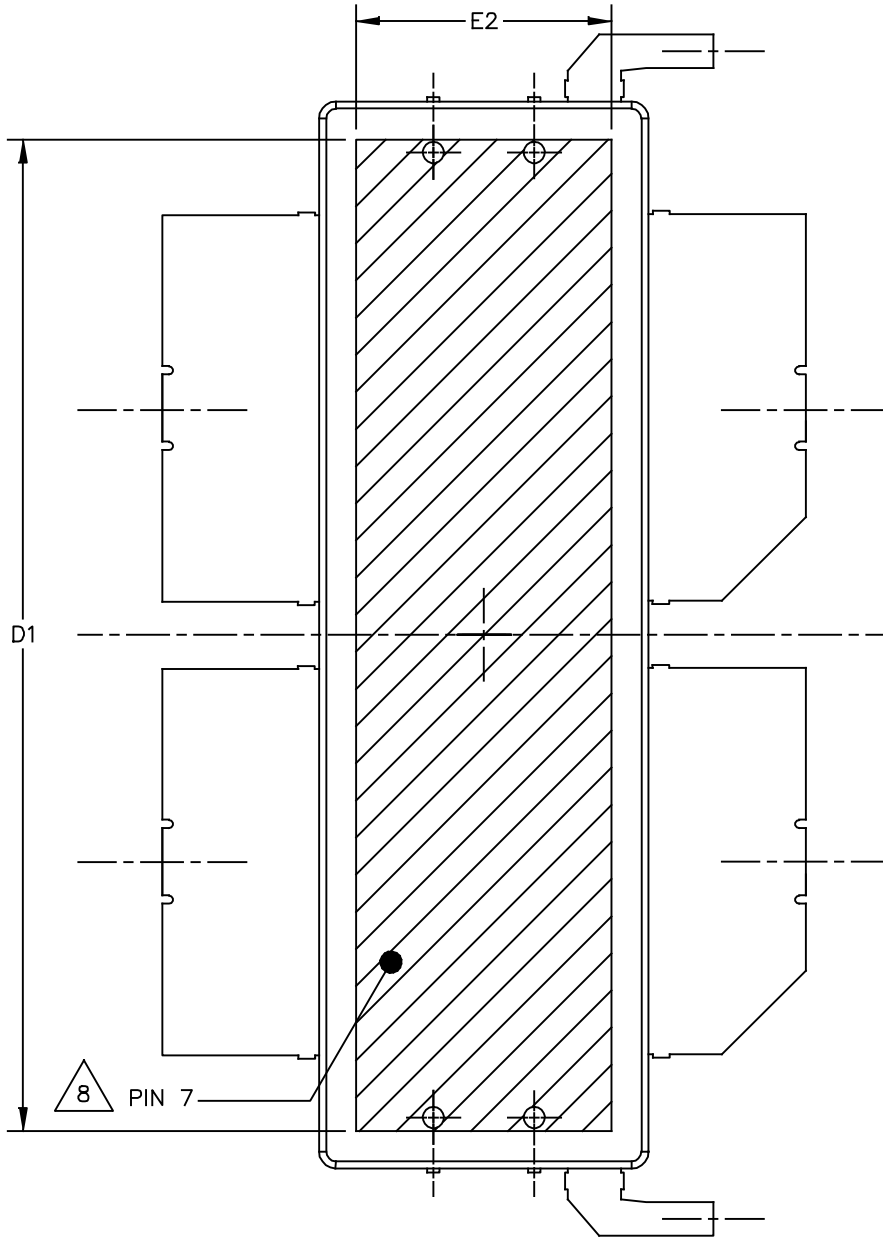
- Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



| | | |
|--|--------------------------|----------------------------|
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| | STANDARD: NON-JEDEC | |
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A2T18H455W23NR6



BOTTOM VIEW
VIEW T-T

| | | | |
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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSIONS A1 AND A2 APPLY WITHIN ZONE J ONLY. A1 APPLIES TO PINS 1, 2, 4 AND 5. A2 APPLIES TO PINS 3 AND 6.
8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.
10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

| DIM | INCH | | MILLIMETER | | DIM | INCH | | MILLIMETER | |
|-----|----------|-------|------------|-------|-----|----------|------|------------|-------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| AA | .148 | .152 | 3.76 | 3.86 | W2 | .158 | .168 | 4.01 | 4.27 |
| A1 | .059 | .065 | 1.50 | 1.65 | W3 | .132 | .142 | 3.35 | 3.61 |
| A2 | .056 | .068 | 1.42 | 1.73 | W4 | .265 | .281 | 6.73 | 7.14 |
| DD | 1.267 | 1.273 | 32.18 | 32.33 | U | .037 | .043 | 0.94 | 1.09 |
| D1 | 1.180 | ---- | 29.97 | ---- | Y | .695 BSC | | 17.65 BSC | |
| E | .762 | .770 | 19.35 | 19.56 | bb | .457 | .463 | 11.61 | 11.76 |
| E1 | .390 | .394 | 9.91 | 10.01 | c1 | .007 | .011 | 0.18 | 0.28 |
| E2 | .306 | ---- | 7.77 | ---- | e | .270 BSC | | 6.86 BSC | |
| E3 | .383 | .387 | 9.73 | 9.83 | e1 | .116 | .124 | 2.95 | 3.15 |
| F | .025 REF | | 0.64 REF | | aaa | .004 | | 0.10 | |
| G | .030 REF | | 0.76 REF | | bbb | .006 | | 0.15 | |
| W1 | .095 | .105 | 2.41 | 2.67 | ccc | .010 | | 0.25 | |

| | | | |
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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.nxp.com/RF>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|----------|---------------------------------|
| 0 | May 2016 | • Initial Release of Data Sheet |

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