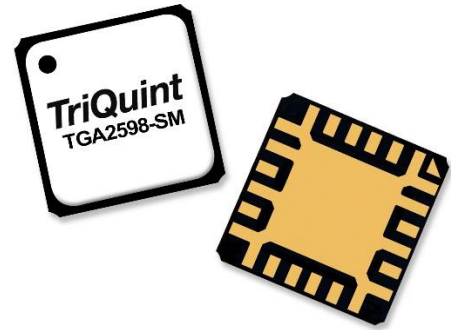


Product Description

Qorvo's TGA2598-SM is a packaged broadband driver amplifier fabricated on Qorvo's TQGaN25 0.25 um GaN on SiC process. Operating from 6 to 12 GHz, the TGA2598-SM achieves 2 W saturated output power with a power-added efficiency of > 25 %, and 25 dB small signal gain.

The TGA2598-SM is available in a low cost, 4x4 mm air-cavity ceramic QFN. The TGA2598-SM is an ideal choice to drive Qorvo's high performing GaN HPAs allowing the user to run both driver and HPA off the same voltage rail.

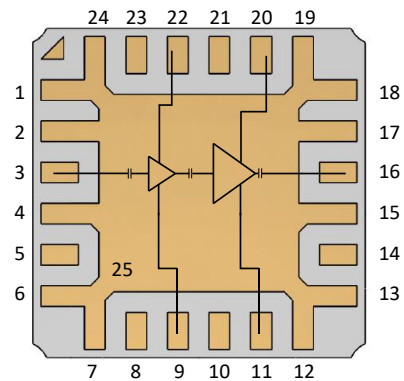
Both RF ports have integrated DC blocking capacitors and are fully matched to 50 Ohms.



Product Features

- Frequency Range: 6 - 12 GHz
- Small Signal Gain: 22 dB (mid-band)
- Pout: 33 dBm ($P_{IN} = 19$ dBm)
- PAE: > 25 % CW
- IM3: -22 dBc (23 dBm Pout/Tone)
- Input Return Loss: > 10 dB
- Output Return Loss: > 8 dB
- Bias: $V_D = 25$ V, $I_{DQ} = 100$ mA, $V_G = -2.5$ V Typical
- Package Dimensions: 4.0 x 4.0 x 1.5 mm

Functional Block Diagram



Top View

Applications

- Commercial and military radar
- Communications
- Electronic Warfare (EW)

Ordering Information

Part No.	Description
TGA2598-SM	6 – 12 GHz 2W GaN Driver Amplifier
TGA2598-SMTR7	Tape and Reel 7", Qty 250
TGA2598-SMEVB02	TGA2598-SM Evaluation Board



TGA2598-SM

6 – 12 GHz 2W GaN Driver Amplifier

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		25		V
Drain Current (I_{DQ})		100		mA
Drain Current Under RF Drive (I_{D_DRIVE})		See plots		mA
Gate Voltage (V_G)		-2.5		V
Gate Current Under RF Drive (I_{G_DRIVE})		See plots		mA
Temperature (T_{BASE})	-40		+85	°C

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	6		12	GHz
Small Signal Gain (from 6 to 10 GHz)	21	23		dB
Small Signal Gain (from 10 to 12 GHz)	19	21		dB
Input Return Loss		10		dB
Output Return Loss		8		dB
Output Power (at $P_{in} = 19$ dBm)	31	33		dBm
Power Added Efficiency (at $P_{in} = 19$ dBm)	20	25		%
IM3 (at $P_{out}/tone = 23$ dBm/Tone)		-22		dBc
IM5 (at $P_{out}/tone = 23$ dBm/Tone)		-37		dBc
Small Signal Gain Temperature Coefficient		-0.05		dB/°C
Gate Leakage Current ($V_D = 10$ V, $V_G = -3.7$ V)	-0.84			mA
Output Power Temperature Coefficient		-0.007		dBm/°C

Test conditions unless otherwise noted: $T_{BASE} = +25$ °C, $V_D = +25$ V, $I_{DQ} = 100$ mA, $V_G = -2.5$ V typical, CW Mode
Data de-embedded to reference planes

Absolute Maximum Ratings

Parameter	Range / Value	Units
Drain Voltage (V_D)	40	V
Gate Voltage Range (V_G)	-8 to 0	V
Drain Current (I_{D1})	128	mA
Drain Current (I_{D2})	260	mA
Gate Current (I_{G1}) at $T_{ch} = 200\text{ }^\circ\text{C}$	-0.2 to 1.4	mA
Gate Current (I_{G2}) at $T_{ch} = 200\text{ }^\circ\text{C}$	-0.6 to 2.8	mA
Power Dissipation (P_{DISS}), $85\text{ }^\circ\text{C}$	5.3	W
Input Power (P_{IN}), CW, $50\ \Omega$, $V_D=25\text{ V}$, $I_{DQ}=100\text{ mA}$, $85\text{ }^\circ\text{C}$,	30	dBm
Input Power (P_{IN}), CW, VSWR 10:1, $V_D=25\text{ V}$, $I_{DQ}=100\text{ mA}$, $85\text{ }^\circ\text{C}$	30	dBm
Mounting Temperature (30 Seconds)	260	$^\circ\text{C}$
Storage Temperature	-55 to 150	$^\circ\text{C}$

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Thermal and Reliability Information

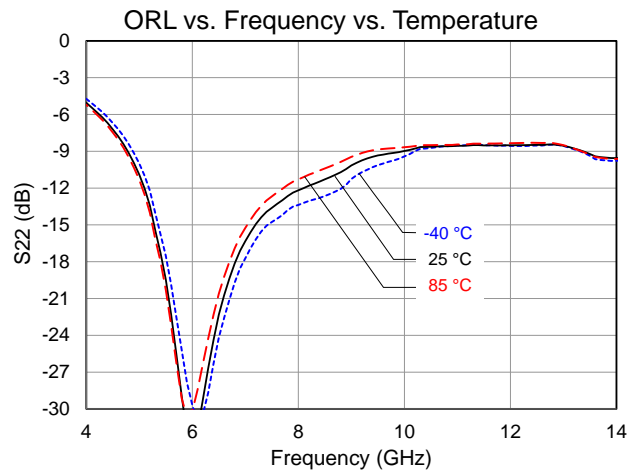
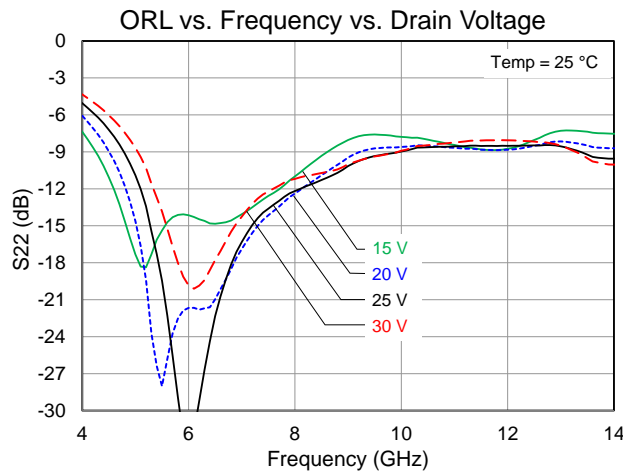
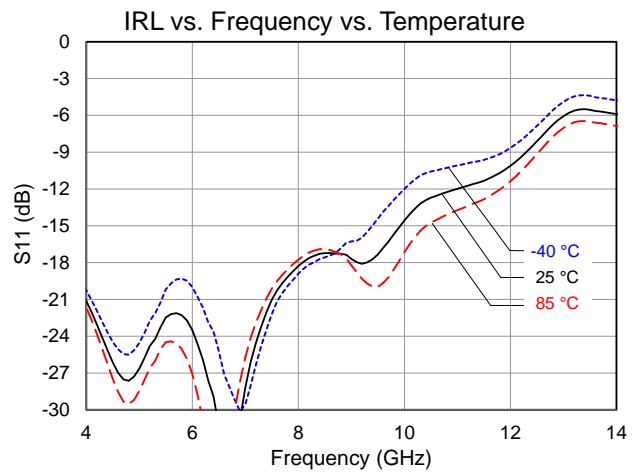
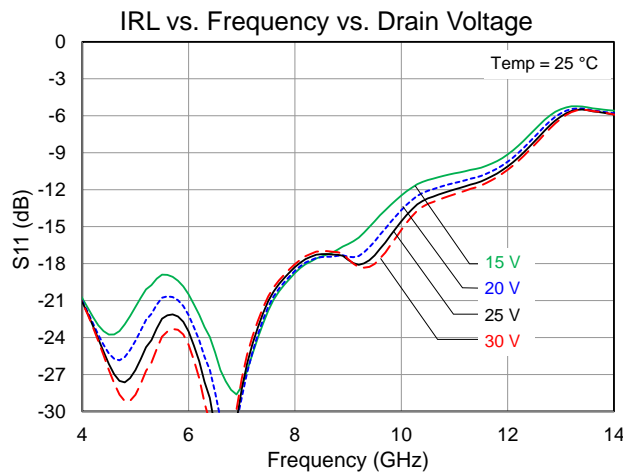
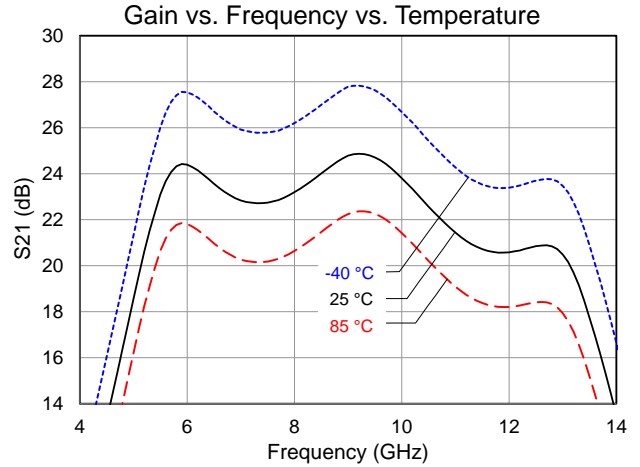
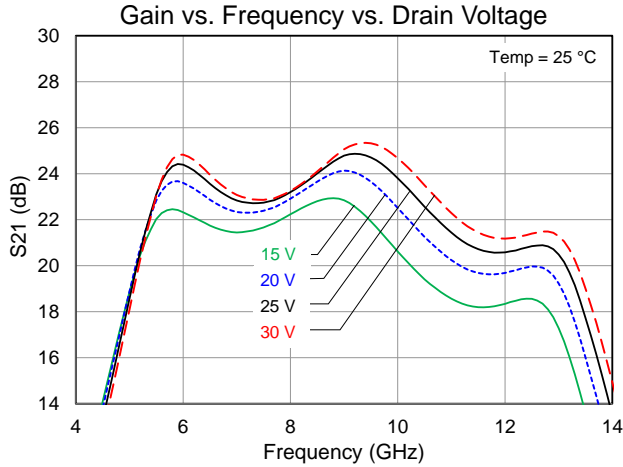
Parameter	Values	Units	Conditions
Under Drive, Thermal Resistance (θ_{JC}) ^(1,2,3)	16.83	$^\circ\text{C/W}$	$T_{BASE} = 85\text{ }^\circ\text{C}$, $V_D = +25\text{ V}$, CW Freq = 9 GHz, $I_{D_DRIVE} = 243\text{ mA}$ $P_{IN} = +16\text{ dBm}$, $P_{OUT} = +33\text{ dBm}$, $P_{DISS} = 4.1\text{ W}$
Channel Temperature (T_{CH})	154	$^\circ\text{C}$	

Notes:

1. Thermal resistance is measured to package backside
2. Base or ambient temperature is $85\text{ }^\circ\text{C}$
3. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

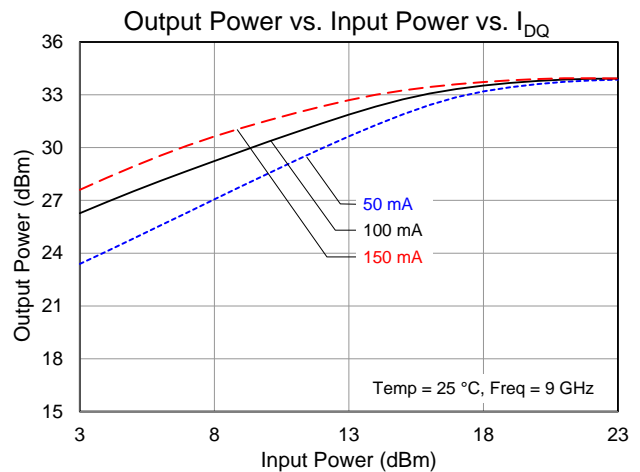
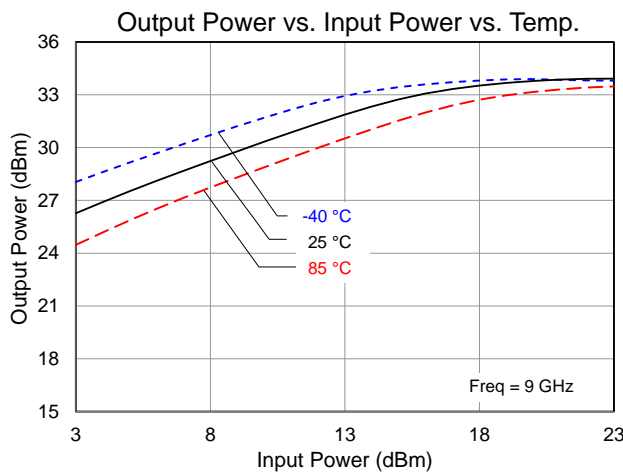
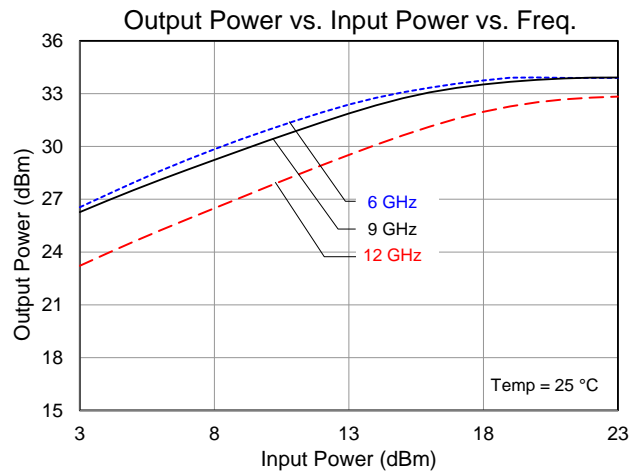
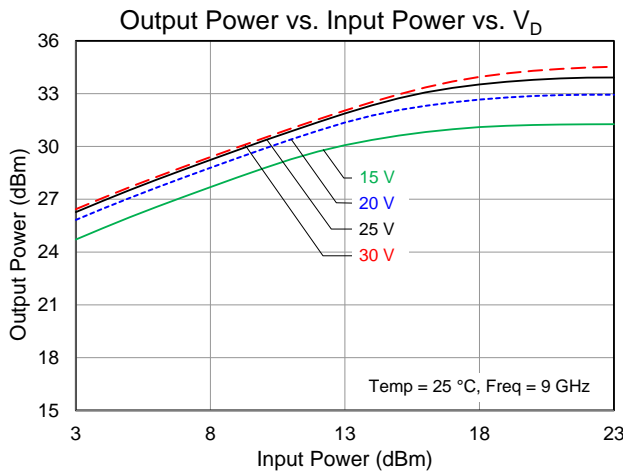
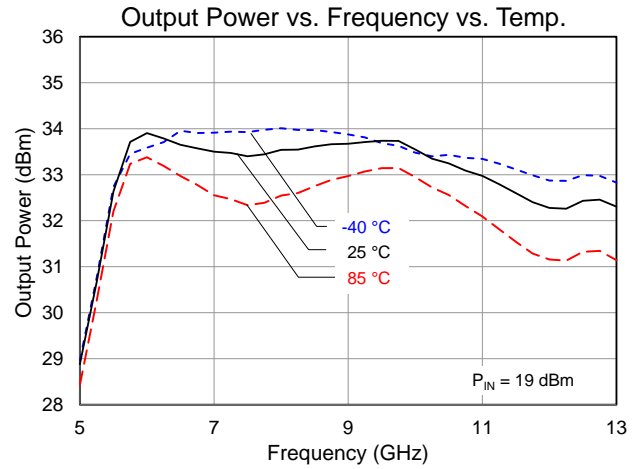
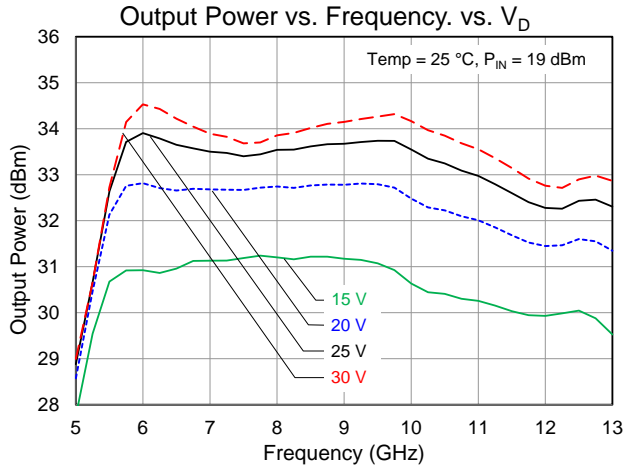
Performance Plots – Small Signal

Test conditions unless otherwise specified: $V_D = 25\text{ V}$, $I_{DQ} = 100\text{ mA}$, $V_G = -2.5\text{ V}$ Typical, CW, $25\text{ }^\circ\text{C}$



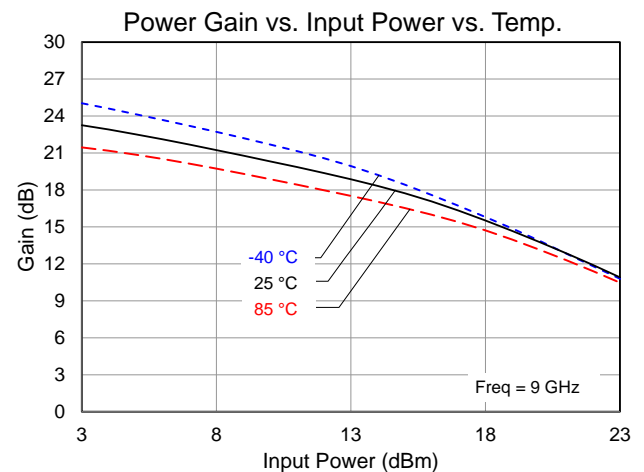
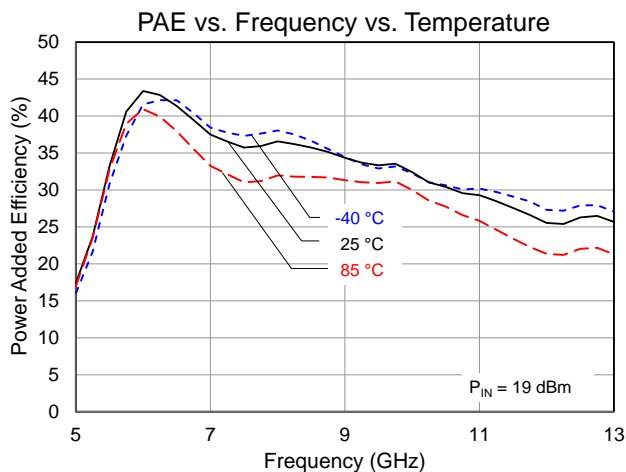
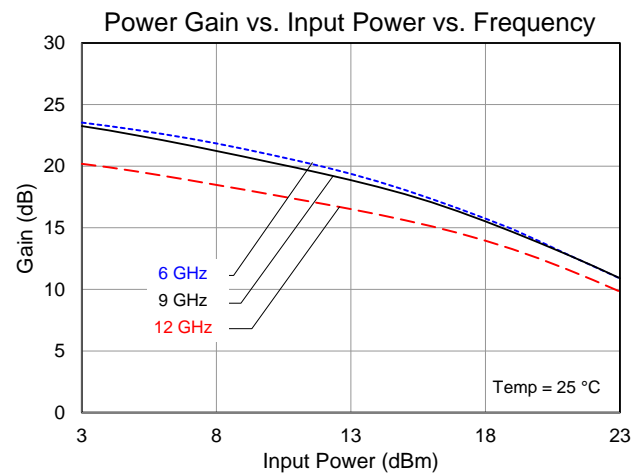
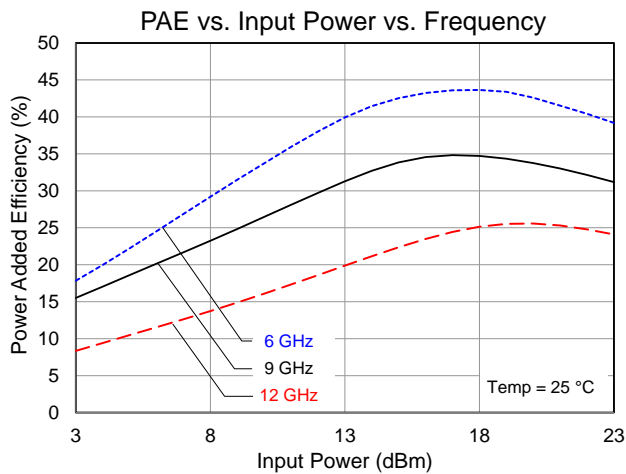
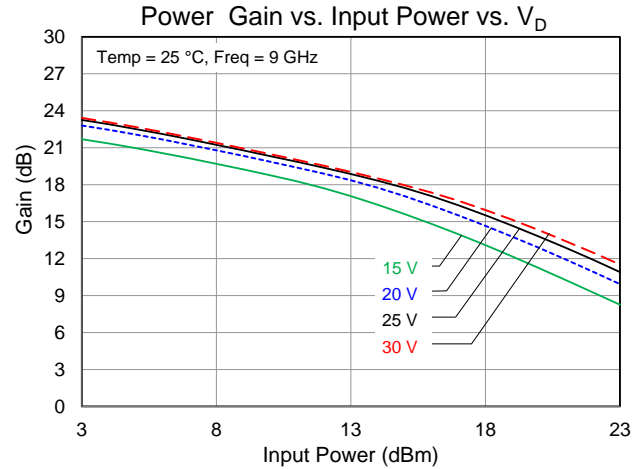
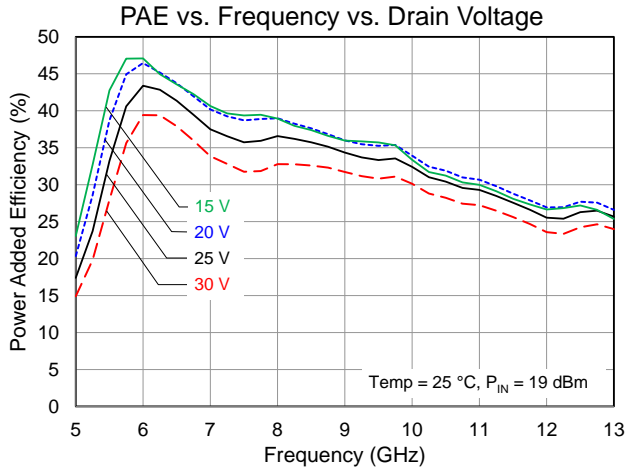
Performance Plots – Large Signal

Test conditions unless otherwise specified: $V_D = 25\text{ V}$, $I_{DQ} = 100\text{ mA}$, $V_G = -2.5\text{ V}$ Typical, CW, $25\text{ }^\circ\text{C}$



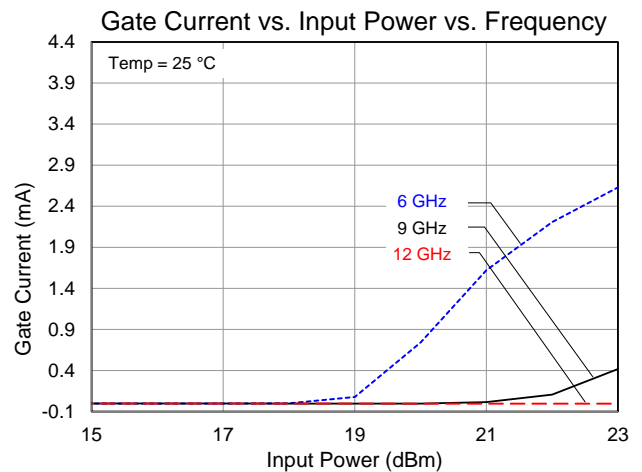
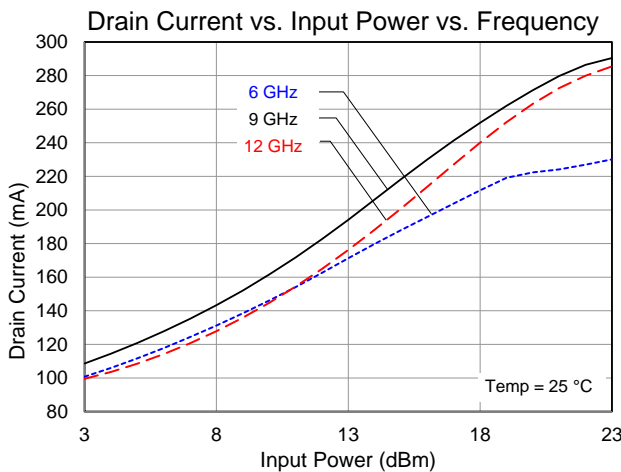
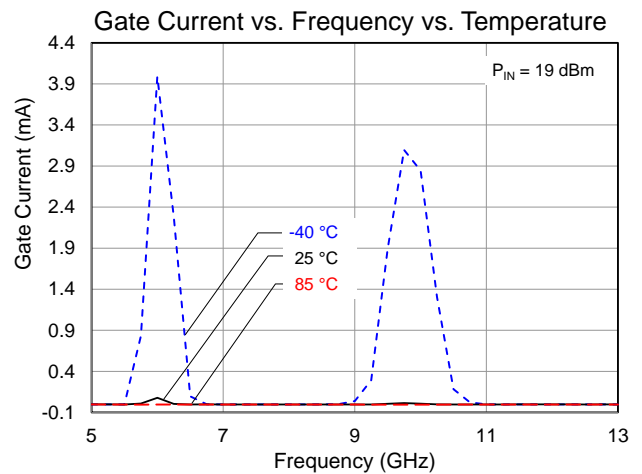
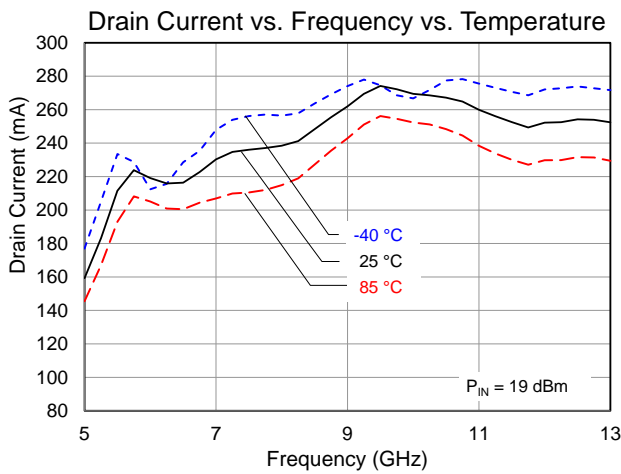
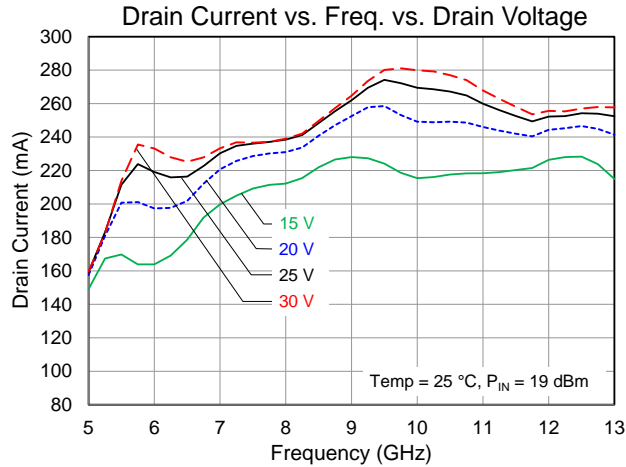
Performance Plots – Large Signal

Test conditions unless otherwise specified: $V_D = 25\text{ V}$, $I_{DQ} = 100\text{ mA}$, $V_G = -2.5\text{ V}$ Typical, CW, $25\text{ }^\circ\text{C}$



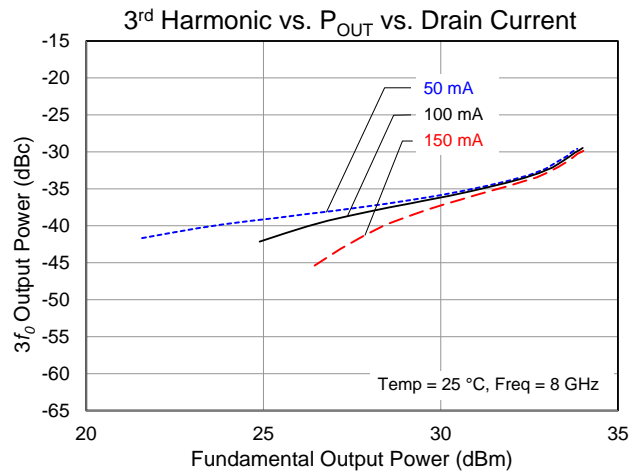
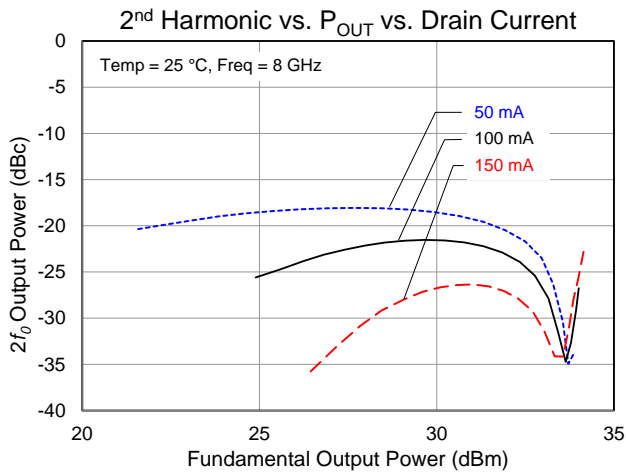
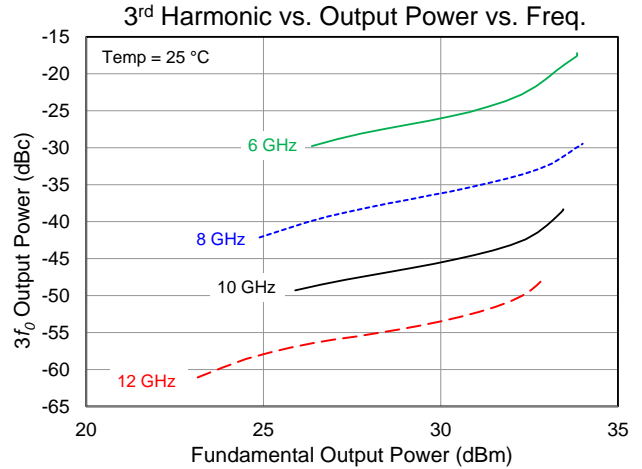
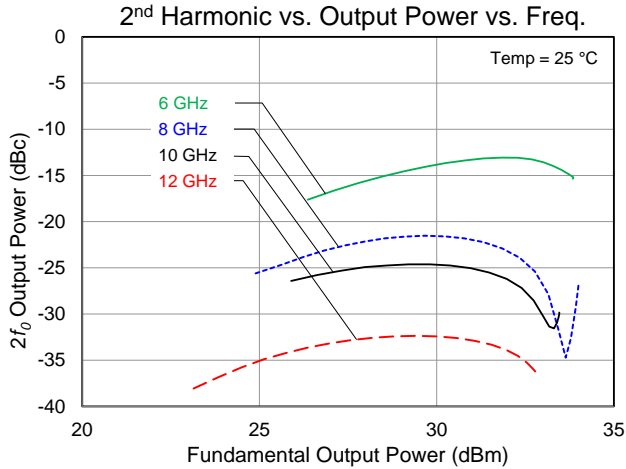
Performance Plots – Large Signal

Test conditions unless otherwise specified: $V_D = 25\text{ V}$, $I_{DQ} = 100\text{ mA}$, $V_G = -2.5\text{ V}$ Typical, CW, $25\text{ }^\circ\text{C}$



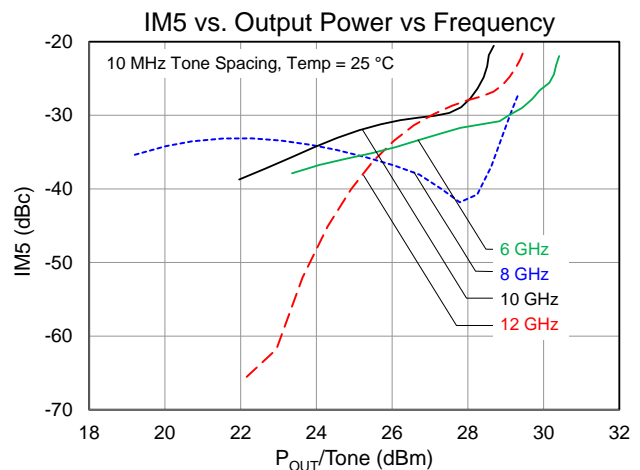
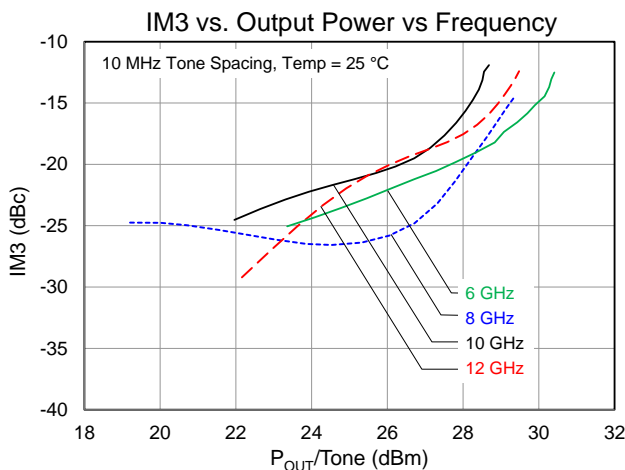
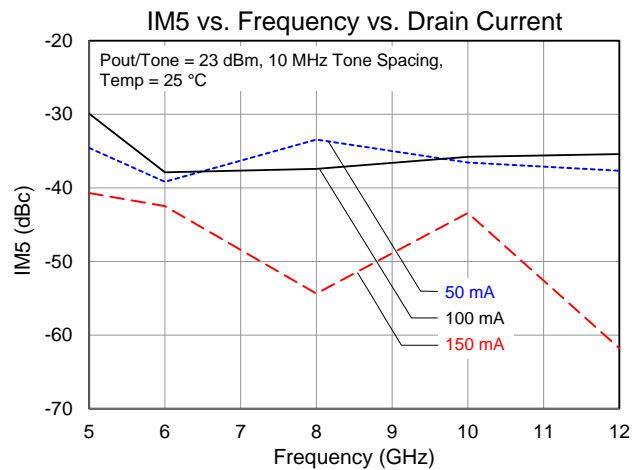
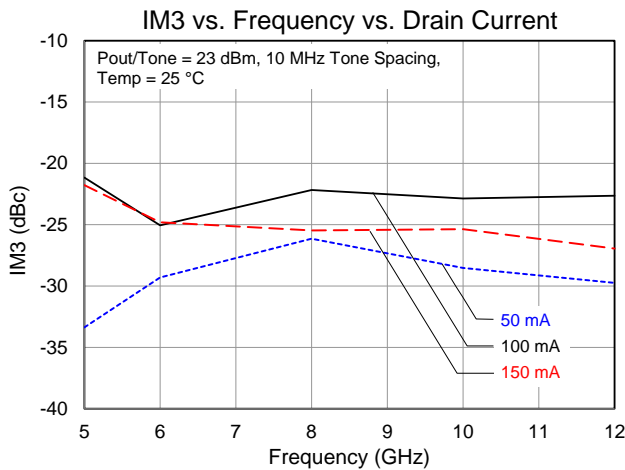
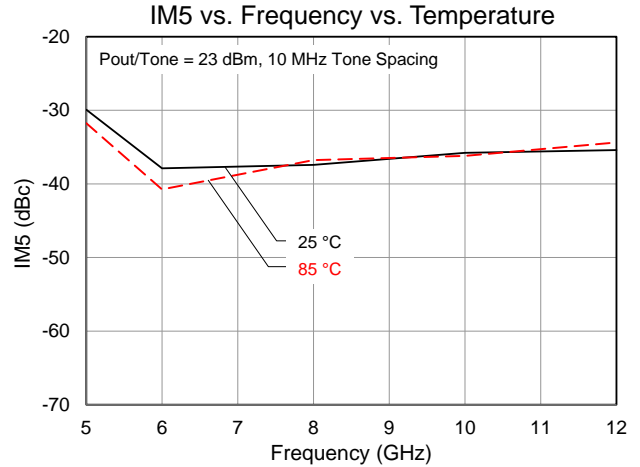
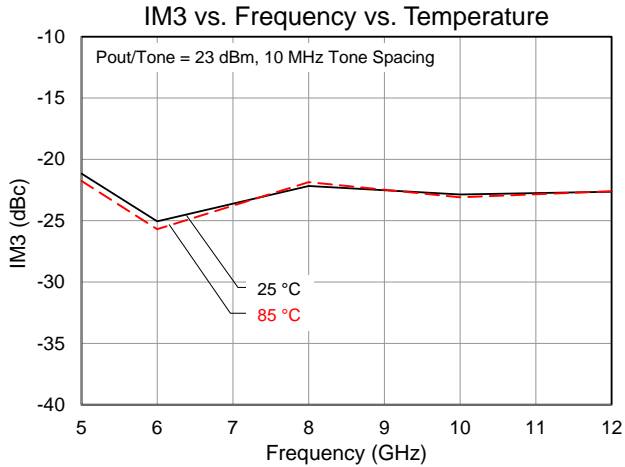
Performance Plots – Harmonics

Test conditions unless otherwise specified: $V_D = 25\text{ V}$, $I_{DQ} = 100\text{ mA}$, $V_G = -2.5\text{ V}$ Typical, CW, $25\text{ }^\circ\text{C}$

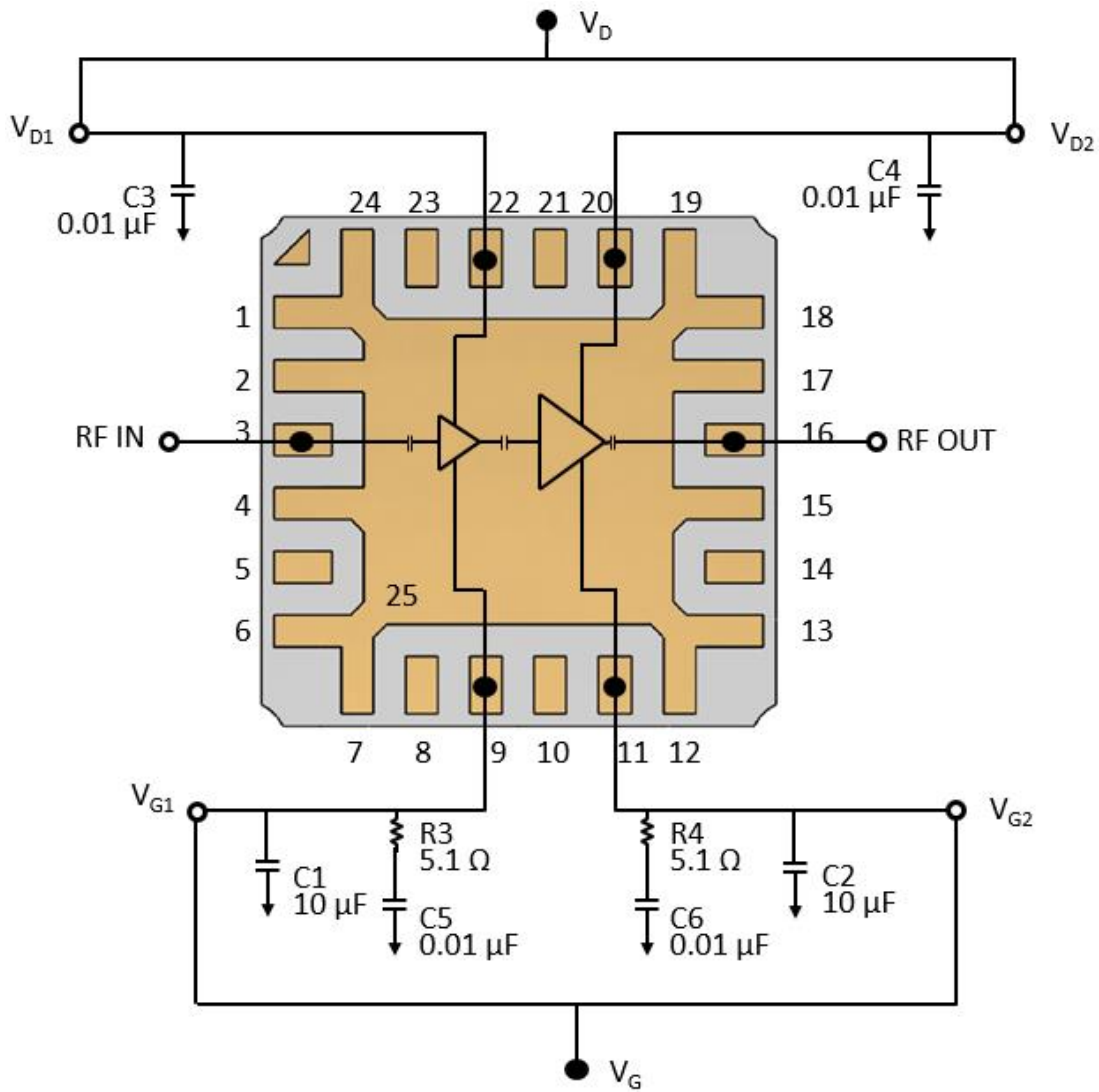


Performance Plots – Linearity

Test conditions unless otherwise specified: $V_D = 25\text{ V}$, $I_{DQ} = 100\text{ mA}$, $V_G = -2.5\text{ V}$ Typical, CW, $25\text{ }^\circ\text{C}$



Application Circuit



Note: Device shown is top view, Both V_{D1} and V_{D2} , and V_{G1} and V_{G2} must be biased

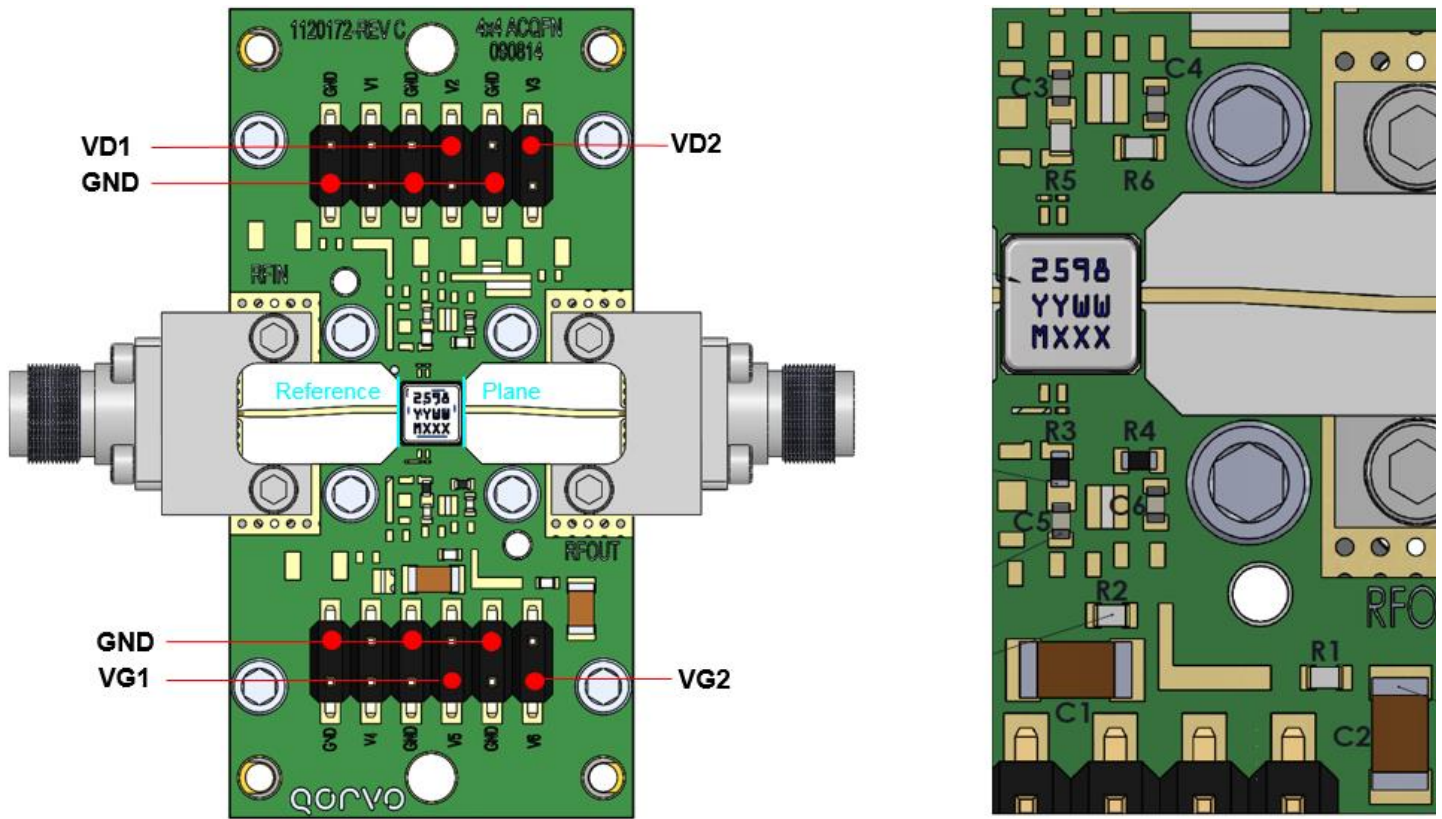
Bias Up Procedure

1. Set I_D limit to 320 mA, I_G limit to 4 mA
2. Apply -5 V to V_G
3. Apply $+25$ V to V_D ; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until $I_{DQ} = 100$ mA ($V_G \sim -2.5$ V Typ.).
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to -5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

EVB and BOM



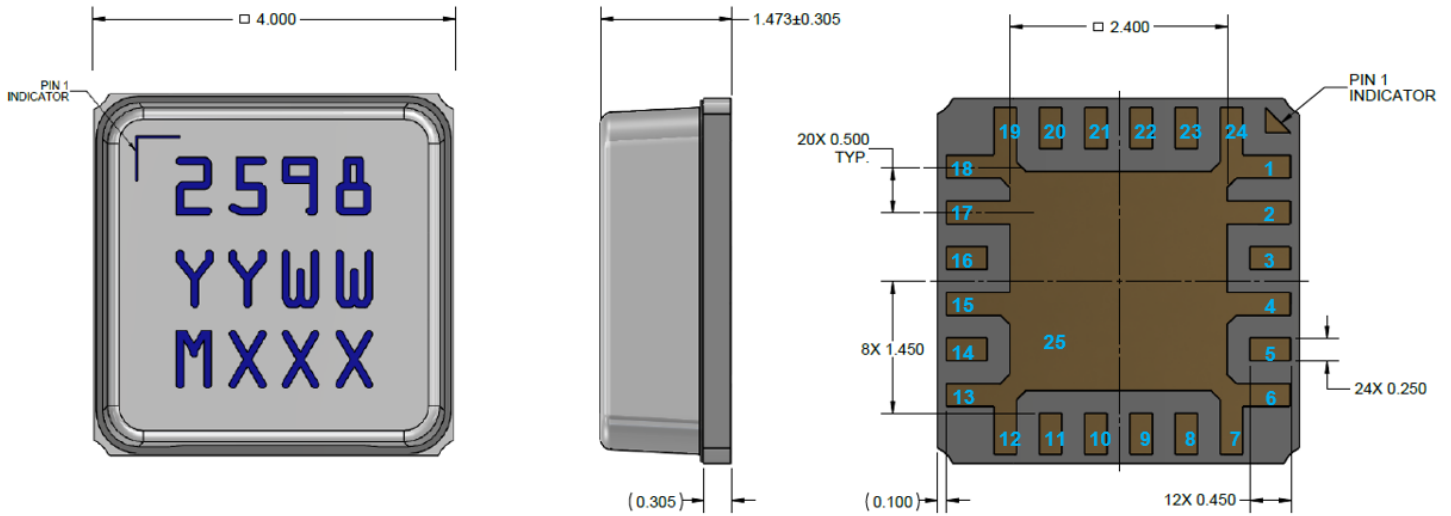
RF Layer is 0.008" thick Rogers Corp. RO4003C, $\epsilon_r = 3.38$. Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

The trace pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead tolerances. Since processes vary from company to company, careful process development is recommended

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2	10 μ F	Cap, 1206, X5R	Various	
C3, C4, C5, C6	0.01 μ F	Cap, 0402, X7R	Various	
R1, R2, R5, R6	0 Ohms	Resistor, 0402	Various	
R3, R4	5.1 Ohms	Resistor, 0402	Various	

Pin Configuration and Description



Dimensions in mm. Tolerance unless otherwise stated is +/- 0.127 μ m.
 Package lead finish: Ni / Au plating with minimum gold thickness of 0.5 μ m
 Materials: Base: Ceramic, Lid: Plastic, Part is epoxy sealed

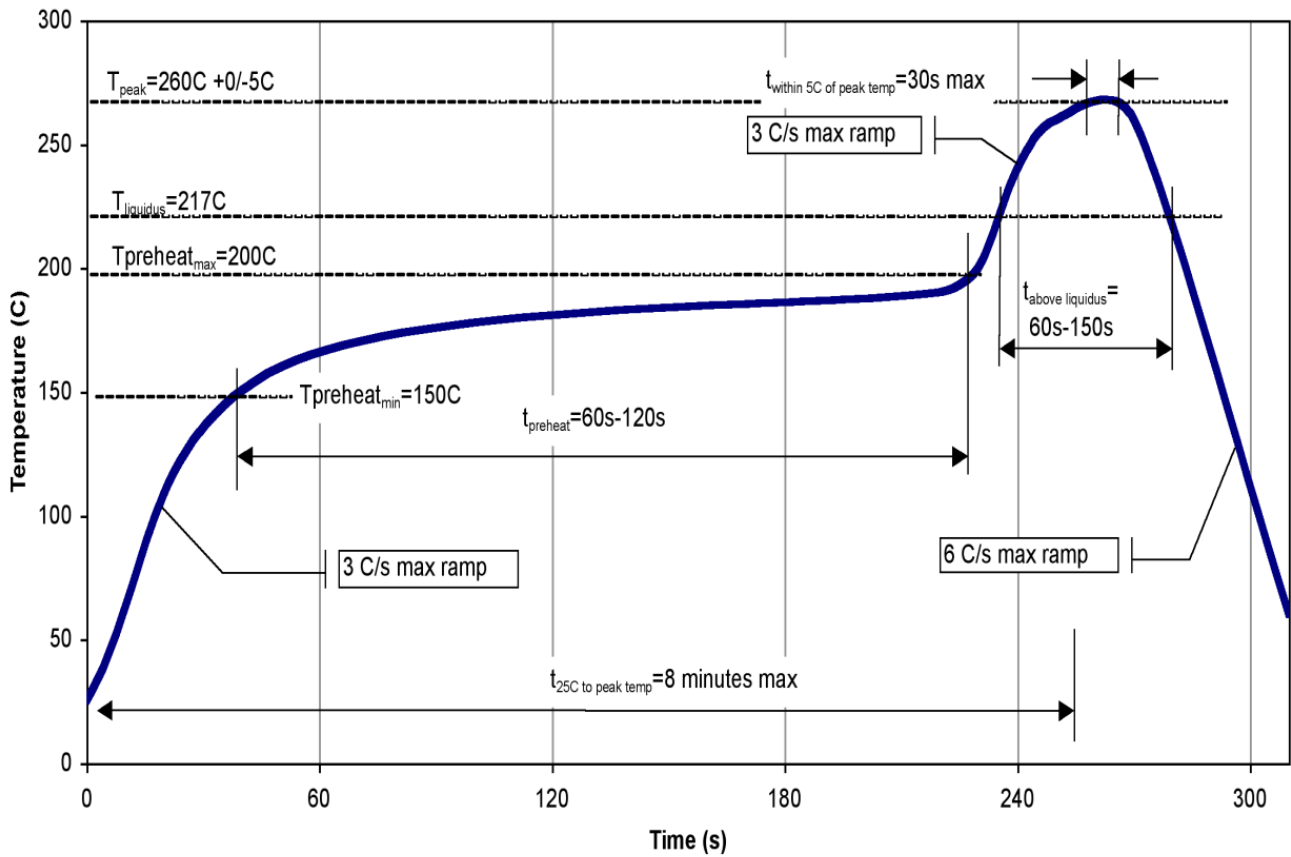
Part Marking: 2598: Part Number, YY = Part Assembly Year, WW = Part Assembly Week, MXXX = Batch ID

Pin No.	Label	Description
1, 2, 4, 6, 7, 12, 13, 15, 17-19, 24, 25	GND	Must be grounded on the PCB.
3	RF _{IN}	Input; matched to 50 Ω ; DC blocked
5, 8, 10, 14, 21, 23	NC	Not Connected
9	V _{G1}	Gate Voltage; Bias network required; see recommended Application Information above.
11	V _{G2}	Gate Voltage; Bias network is required; see recommended Application Information above.
16	RF _{OUT}	Output; matched to 50 Ω ; DC blocked
20	V _{D2}	Drain voltage; Bias network is required; see recommended Application Information above.
22	V _{D1}	Drain voltage; Bias network is required; see recommended Application Information above.

Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C.
2. This package is non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is recommended.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	0B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3	ESDA / JEDEC JS-002-2014
MSL – Convection Reflow 260 °C	3	JEDEC standard IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: 1-844-890-8163

Web: www.qorvo.com

Email: customer.support@qorvo.com

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<http://moschip.ru/get-element>

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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