

High Reliability Serial EEPROMs





BR25L010-W series, BR25L020-W series, BR25L040-W series, BR25L080-W series, BR25L160-W series, BR25L320-W series, BR25L640-W series

Description

BR25L - - W series is a serial EEPROM of SPI BUS interface method.

Features

- · High speed clock action up to 5MHz (Max.)
- · Wait function by HOLD terminal
- · Part or whole of memory arrays settable as read only memory area by program
- · 1.8 ~ 5.5V single power source action most suitable for battery use
- · Page write mode useful for initial value write at factory shipment
- · Highly reliable connection by Au pad and Au wire
- For SPI bus interface (CPOL, CPHA) = (0, 0), (1, 1)
- · Auto erase and auto end function at data rewrite
- · Low current consumption

At write action (5V) : 1.5mA (Typ.) At read action (5V) : 1.0mA (Typ.) At standby action (5V) : 0.1µA (Typ.)

- · Address auto increment function at read action
- · Write mistake prevention function

Write prohibition at power on

Write prohibition by command code (WRDI)

Write prohibition by WP pin

Write prohibition block setting by status registers (BP1, BP0)

Write mistake prevention function at low voltage

- SOP8, SOP-J8, SSOP-B8, TSSOP-B8, MSOP8 TSSOP-B8J package *1 *2
- · Data at shipment Memory array: FFh, status register WPEN, BP1, BP0:0
- · Data kept for 40 years
- Data rewrite up to 1,000,000 times

*1 BR25L080/160-W: SOP8, SOP-J8, SSOP-B8, TSSOP-B8

*2 BR25L320/640-W: SOP8, SOP-J8

Page write

Number of pages	16 Byte	32 Byte
Product number	BR25L010-W BR25L020-W BR25L040-W	BR25L080-W BR25L160-W BR25L320-W BR25L640-W

■ BR25L series

Capacity	Bit format	Туре	Power source voltage	SOP8 F	SOP-J8 FJ	SSOP-B8 FV	TSSOP-B8 FVT	MSOP8 FVM	TSSOP-B8J FVJ
1Kbit	128 X 8	BR25L010-W	1.8 ~ 5.5V	•	•	•	•	•	•
2Kbit	256 X 8	BR25L020-W	1.8 ~ 5.5V	•	•	•	•	•	•
4Kbit	512 X 8	BR25L040-W	1.8 ~ 5.5V	•	•	•	•	•	•
8Kbit	1K X 8	BR25L080-W	1.8 ~ 5.5V	•	•	•	•		
16Kbit	2K X 8	BR25L160-W	1.8 ~ 5.5V	•	•	•	•		
32Kbit	4K X 8	BR25L320-W	1.8 ~ 5.5V	•	•				
64Kbit	8K X 8	BR25L640-W	1.8 ~ 5.5V	•	•				

Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit			
Impressed voltage	Vcc	-0.3 ~ +6.5	V			
		450(SOP8) *1				
		450(SOP-J8) *2	mW			
Permissible dissipation	Pd	Pd 300(SSOP-B8) *3				
· .		330(TSSOP-B8) *4				
		310(MSOP8) *5				
		310(TSSOP-B8J)*6				
Storage temperature range	Tstg	-65 ~ +125	°C			
Operating temperature range	Topr	-40 ~ +85	°C			
Terminal voltage	_	-0.3 ~ Vcc+0.3	V			

[·]When using at Ta = 25°C or higher, 4.5mW (*1, *2), 3.0mW (*3), 3.3mW(*4), 3.1mW (*5, *6) to be reduced per 1°C

Recommended action conditions

Parameter	Symbol	Limits	Unit
Power source voltage	Vcc	1.8 ~ 5.5	\/
Input voltage	Vin	0 ~ Vcc	V

Memory cell characteristics (Ta=25°C, Vcc=1.8 ~ 5.5V)

Parameter		Limits				
Parameter	Min. Typ.		Max.	Unit		
Number of data rewrite times *1	1,000,000	-	_	Times		
Data hold years *1	40	_	_	Years		

^{*1:}Not 100% TESTED

Input / output capacity (Ta=25°C, frequency=5MHz)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Input capacity *1	Cin	VIN=GND	-	8	pF
Output capacity*1	Соит	Vout=GND	_	8	pF

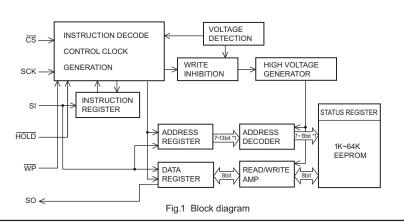
^{*1:}Not 100% TESTED

■ Electrical characteristics (Unless otherwise specified, Ta = -40 ~ +85°C, Vcc = 1.8 ~ 5.5V)

Parameter	Symbol Limits				Unit	Conditions		
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions		
"H" input voltage 1	VIH1	0.7x Vcc	ı	Vcc +0.3	V	1.8≤Vcc≤5.5V		
"L" input voltage 1	VIL1	-0.3	-	0.3x Vcc	V	1.8≤Vcc≤5.5V		
"L" output voltage 1	VOL1	0	_	0.4	V	IOL=2.1mA(Vcc=2.5V ~ 5.5V)		
"L" output voltage 2	VOL2	0	_	0.2	V	IOL=150μA(Vcc=1.8V ~ 2.5V)		
"H" output voltage 1	VOH1	Vcc -0.5	-	Vcc	V	IOH=-0.4mA(Vcc=2.5V ~ 5.5V)		
"H" output voltage 2	VOH2	Vcc -0.2	-	Vcc	V	IOH=-100μA(Vcc=1.8V ~ 2.5V)		
Input leak current	ILI	-1	-	1	μΑ	VIN=0 ~ VCC		
Output leak current	ILO	-1	_	1	μΑ	Vout=0 ~ Vcc, CS=Vcc		
	Icc1	_	-	1.0	mA	Vcc=1.8V,fSCK=2MHz,tE/W=5ms Byte write Page write Write status register		
Current consumption at write action	Icc2	_	-	2.0	mA	Vcc=2.5V,fSCK=5MHz,tE/W=5ms Byte write Page write Write status register		
	Icc3	_	_	3.0	mA	Vcc=5.5V,fSCK=5MHz,tE/W=5ms Byte write Page write Write status register		
Current consumption at read	Icc4	_	_	1.5	mA	Vcc=2.5V,fSCK=5MHz Read Read status register		
action	Icc5	_	_	2.0	mA	Vcc=5.5V,fSCK=5MHz Read Read status register		
Standby current	ISB	_	_	2	μА	Vcc=5.5V CS=HOLD=WP=Vcc,SCK=SI=Vcc or =GND,SO=OPEN		

[•] Radiation resistance design is not made.

Block diagram

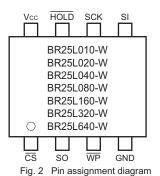


^{*1 7}bit : BR25L010-W

⁸bit : BR25L020-W 9bit : BR25L040-W 10bit : BR25L080-W 11bit : BR25L160-W 12bit : BR25L320-W

¹³bit : BR25L640-W

Pin assignment and description



Terminal name	Input/output	Function
Vcc	_	Power source to be connected
GND	_	All input / output reference voltage, 0V
CS	Input	Chip select input
SCK	Input	Serial clock input
SI	Input	Start bit, ope code, address, and serial data input
SO	Output	Serial data output
HOLD	Input	Hold input Command communications may be suspended temporarily (HOLD status).
WP	Input	Write protect input Write command is prohibited.*1 Write status register command is prohibited.

*1:BR25L010/020/040-W

Operating timing characteristics

(Ta = -40 ~ +85°C, unless otherwise specified, load capacity CL1 100pF)

	0 1 1		<u>'</u> ≤Vcc<2			 ≤Vcc<		' '
Parameter	Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
SCK frequency	fSCK	_	_	2	_	_	5	MHz
SCK high time	tSCKWH	200	_	_	85	_	_	ns
SCK low time	tSCKWL	200	_	_	85	_	_	ns
CS high time	tCS	200	_	_	85	_	_	ns
CS setup time	tCSS	200	_	_	90	_	_	ns
CS hold time	tCSH	200	_	_	85	_	_	ns
SCK setup time	tSCKS	200	_	_	90	_	_	ns
SCK hold time	tSCKH	200	ı	-	90	-	-	ns
SI setup time	tDIS	40	_	_	20	_	_	ns
SI hold time	tDIH	50	_	_	40	_	_	ns
Data output delay time 1	tPD1	-	ı	150	-	-	70	ns
Data output delay time 2 (CL2=30pF)	tPD2	_	-	145	_	_	55	ns
Output hold time	tOH	0	_	_	0	_	_	ns
Output disable time	tOZ	_	_	250	_	_	100	ns
HOLD setting setup time	tHFS	120	_	_	60	_	_	ns
HOLD setting hold time	tHFH	90	_	_	40	_	_	ns
HOLD release setup time	tHRS	120	_	_	60	_	_	ns
HOLD release hold time	tHRH	140	_	_	70	_	_	ns
Time from HOLD to output High-Z	tHOZ	_	_	250	_	_	100	ns
Time from HOLD to output change	tHPD	_	_	150	_	_	70	ns
SCK *1 rise time	tRC	_	_	1	_	_	1	μs
SCK *1 fall time	tFC	_	_	1	_	_	1	μs
OUTPUT *1 rise time	tRO	_	_	100	_	_	50	ns
OUTPUT *1 fall time	tFO	_	-	100	_	_	50	ns
Write time	tE/W	-	_	5	-	-	5	ms

*1NOT 100% TESTED

Sync data input / output timing

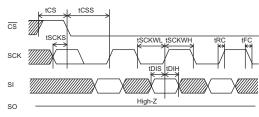


Fig. 3 Input timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the most significant bit MSB.

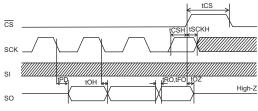


Fig. 4 Input / output timing

SO is output in sync with data fall edge of SCK. Data is output from the most significant bit MSB.

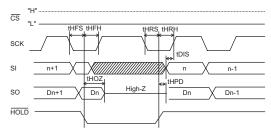


Fig. 5 HOLD timing

AC measurement conditions

AC measurement conditions								
Parameter	Symbol		Unit					
Farameter		Min.	Тур.	Max.	Unit			
Load capacity 1	C _{L1}	_	_	100	рF			
Load capacity 2	C _{L2}	-	_	30	рF			
Input rise time	_	_	_	50	ns			
Input fall time	_	_	_	50	ns			
Input voltage	_	0.2\	/cc/0.8	Vcc	V			
Input / output judgment voltage	_	0.3\	/cc/0.7	Vcc.	V			

Characteristic data (The following characteristic data are Typ. values.)

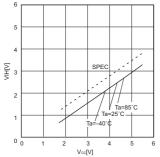


Fig.6 "H" input voltage VIH(CS,SCK,SI,HOLD,WP)

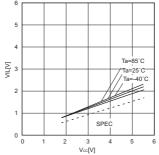


Fig.7 "L" input voltage VIL(CS,SCK,SI,HOLD,WP)

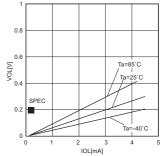


Fig.8 "L" output voltage VOL-IOL(Vcc=1.8V)

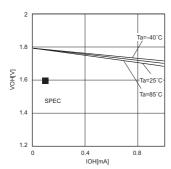


Fig.9 "H" output voltage VOH-IOH(Vcc=1.8V)

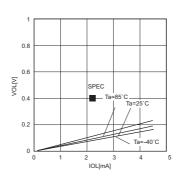


Fig.10 "L" output voltage VOL-IOL(Vcc=2.5V)

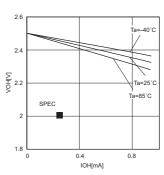


Fig.11 "H" output voltage VOH-IOH(Vcc=2.5V)

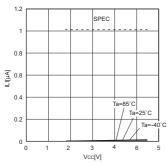


Fig.12 Input leak current $ILI(\overline{CS},SCK,SI,\overline{WP},\overline{HOLD})$

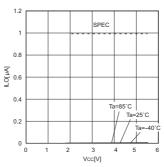


Fig.13 Output leak current ILO(SO)

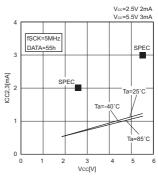


Fig.14 Current consumption at WRITE operation ICC1,2,3(WRITE,PAGE WRITE,WRSR,fSCK=5MHz) BR25L010-W,BR25L020-W,BR25L040-W

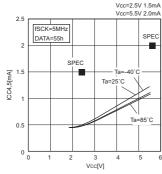


Fig.15 Consumption current at READ operation ICC4,5(READ,WRSR,fSK=5MHz)

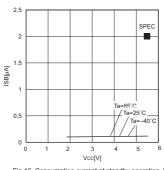


Fig.16 Consumption current at standby operation ISB

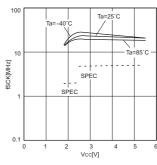
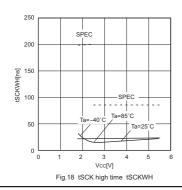
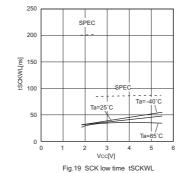
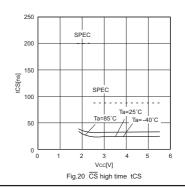
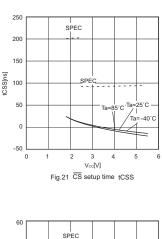


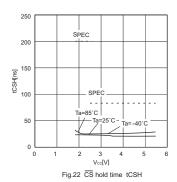
Fig.17 SCK frequency fSCK

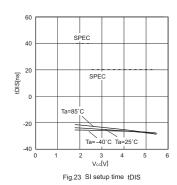


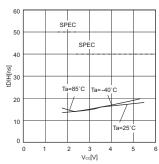


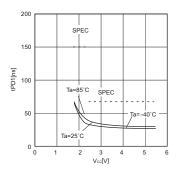












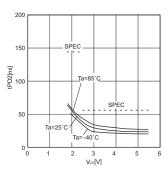
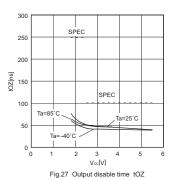
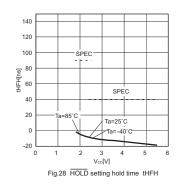


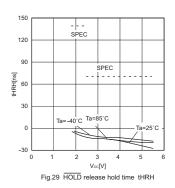


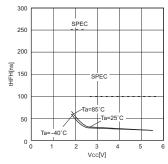
Fig.25 Data output delay time tPD1(CL=100pF)

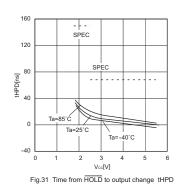
Fig.26 Data output delay time tPD2(CL=30pF)











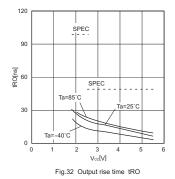
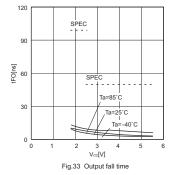


Fig.30 Time from $\overline{\text{HOLD}}$ to output High-Z tHOZ

10
8
8
SPEC
Ta=-40°C
Ta=85°C
Ta=25°C
Ta=25°C
Ta=25°C
Ta=25°C
Ta=25°C
Ta=25°C
Ta=25°C



Features

Status registers

This IC has status registers. The status registers are of 8 bits and express the following parameters.

BP0 and BP1 can be set by write status register command. These 2 bits are memorized into the EEPROM, therefore are valid even when power source is turned off.

Rewrite characteristics and data hold time are same as characteristics of the EEPROM.

WEN can be set by write enable command and write disable command. WEN becomes write disable status when power source is turned off. R/B is for write confirmation, therefore cannot be set externally.

The value of status register can be read by read status command.

Status registers

Product number	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR25L010-W								
BR25L020-W	1	1	1	1	BP1	BP0	WEN	R̄/B
BR25L040-W								
BR25L080-W								
BR25L160-W	WPEN	0	0	0	BP1	BP0	WEN	Ā/B
BR25L320-W	VVPEN	0	U	0	DP1	ן סרט	VV⊏IN	r/b
BR25L640-W								

bit	Memory location	Function	Contents
WPEN	EEPROM	WP pin enable / disable designation bit WPEN = 0 = invalid WPEN = 1 = valid	This enables / disables the functions of WP pin.
BP1 BP0	EEPROM	EEPROM write disable block designation bit	This designates the write disable area of EEPROM. Write designation areas of product numbers are shown below.
WEN	Register	Write and write status register write enable / disable status confirmation bit WEN = 0 = prohibited WEN = 1 = permitted	
R/B	Register	Write cycle status (READY / BUSY) status confirmation bit R/B=0=READY R/B=1=BUSY	

Write disable block setting

	·····g							
DD4	DDO			V	/rite disable bloc	k		
BP1	BP0	BR25L010-W	BR25L020-W	BR25L040-W	BR25L080-W	BR25L160-W	BR25L320-W	BR25L640-W
0	0	None	None	None	None	None	None	None
0	1	60h-7Fh	C0h-FFh	180h-1FFh	300h-3FFh	600h-7FFh	C00h-FFFh	1800h-1FFFh
1	0	40h-7Fh	80h-FFh	100h-1FFh	200h-3FFh	400h-7FFh	800h-FFFh	1000h-1FFFh
1	1	00h-7Fh	00h-FFh	000h-1FFh	000h-3FFh	000h-7FFh	000h-FFFh	0000h-1FFFh

\bigcirc $\overline{\text{WP}}$ pin

By setting \overline{WP} = LOW, write command is prohibited. As for BR25L080, 160, 320, 640-W, only when WPEN bit is set "1", the \overline{WP} pin functions become valid. And the write command to be disabled at this moment is WRSR. As for BR25L010, 020, 040-W, both WRITE and WRSR commands are prohibited.

However, when write cycle is in execution, no interruption can be made.

Product number	WRSR	WRITE	
BR25L010-W			
BR25L020-W	Prohibition possible	Prohibition possible	
BR25L040-W	possible	possible	
BR25L080-W			
BR25L160-W	Prohibition possible but	Prohibition	
BR25L320-W	WPEN bit "1"	impossible	
BR25L640-W			

\bigcirc $\overline{\text{HOLD}}$ pin

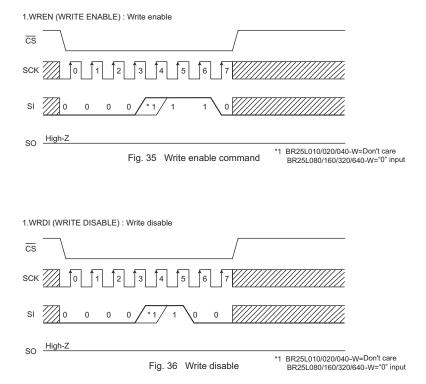
By \overline{HOLD} pin, data transfer can be interrupted. When SCK = "1", by making \overline{HOLD} from "1" into "0", data transfer to EEPROM is interrupted. When SCK = "0", by making \overline{HOLD} from "0" into "1", data transfer is restarted.

Command mode

			Ope code					
Command		Contents	BR25L010-W BR25L020-W		BR25L040-W		BR25L080-W BR25L160-W BR25L320-W BR25L640-W	
WREN	Write enable	Write enable command	0000	* 110	0000	* 110	0000	0110
WRDI	Write disable	Write disable command	0000	* 100	0000	* 100	0000	0100
READ Read		Read command	0000	* 011	0000	A8011	0000	0011
WRITE	Write	Write command	0000	* 010	0000	A8010	0000	0010
RDSR Read status register		Status register read command	0000	* 101	0000	* 101	0000	0101
WRSR Write status register		Status register write command	0000	* 001	0000	* 001	0000	0001

Timing chart

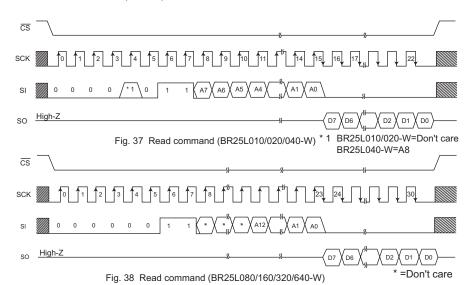
1. Write enable (WREN) / disable (WRDI) cycle



○ This IC has write enable status and write disable status. It is set to write enable status by write enable command, and it is set to write disable status by write disable command. As for these commands, set CS LOW, and then input the respective ope codes. The respective commands accept command at the 7-th clock rise. Even with input over 7 clocks, command becomes valid.

When to carry out write and write status register command, it is necessary to set write enable status by the write enable command. If write or write status register command is input in the write disable status, commands are cancelled. And even in the write enable status, once write and write status register command is executed once, it gets in the write disable status. After power on, this IC is in write disable status.

2. Read command (READ)

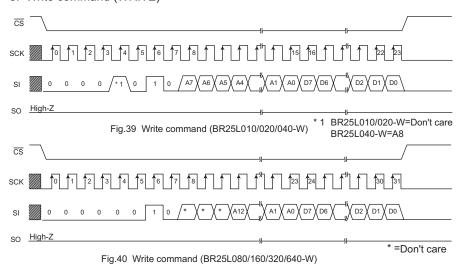


	oduct mber	Address length
BR25	L010-W	A6-A0
BR25	L020-W	A7-A0
BR25	L040-W	A8-A0

Product number	Address length
BR25L080-W	A9-A0
BR25L160-W	A10-A0
BR25L320-W	A11-A0
BR25L640-W	A12-A0

By read command, data of EEPROM can be read. As for this command, set $\overline{\text{CS}}$ LOW, then input address after read ope code. EEPROM starts data output of the designated address. Data output is started from SCK fall of 15/23^{*1} clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8 bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM. After reading data of the most significant address, by continuing increment read, data of the most insignificant address is read.

3. Write command (WRITE)



Product number	Address length
BR25L010-W	A6-A0
BR25L020-W	A7-A0
BR25L040-W	A8-A0

Product number	Address length
BR25L080-W	A9-A0
BR25L160-W	A10-A0
BR25L320-W	A11-A0
BR25L640-W	A12-A0

By write command, data of EEPROM can be written. As for this command, set \overline{CS} LOW, then input address and data after write ope code. Then, by making \overline{CS} HIGH, the EEPROM starts writing. The write time of EEPROM requires time of tE/W (Max 5ms). During tE/W, other than status read command is not accepted. Start \overline{CS} after taking the last data (D0), and before the next SCL clock starts. At other timing, write command is not executed, and this write command is cancelled. This IC has page write function, and after input of data for 1 byte (8 bits), by continuing data input without starting \overline{CS} , data up to $16/32^{*1}$ bytes can be written for one tE/W. In page write, the insignificant $4/5^{*2}$ bit of the designated address is incremented internally at every time when data of 1 byte is input, and data is written to respective addresses. When data of the maximum bytes or higher is input, address rolls over, and previously input data is overwritten.

- * 1 BR25L010/020/040-W=16 bytes at maximum BR25L080/160/320/640-W=32 bytes at maximum
- * 2 BR25L010/020/040-W=Insignificant 4 bits BR25L080/160/320/640-W=Insignificant 5 bits

4. Status register write / read command

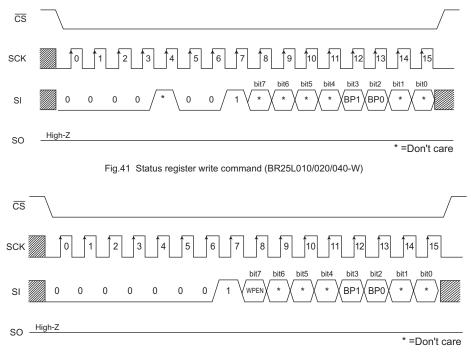


Fig.42 Status register write command (BR25L080/160/320/640-W)

Write status register command can write status register data. The data the can be written by this command are 2 bits *1, that is, BP1 (bit3) and BP0 (bit2) among 8 bits of status register. By BP1 and BP0, write disable block of EEPROM can be set. As for this command, set \overline{CS} LOW, and input ope code of write status register, and input data. Then, by making \overline{CS} HIGH, EEPROM starts writing. Write time requires time of tE/W as same as write. As for \overline{CS} rise, start \overline{CS} after taking the last data bit (bit0), and before the next SCK clock starts. At other timing, command is cancelled. Write disable block is determined by BP1 and BP0, and the block can be selected from 1/4 of memory array, 1/2, and entire memory array. (Refer to the write disable block setting table.) To the write disabled block, write cannot be made, and only read can be made.

* 3 bits including BR25L080, 160, 320, 640-W WPEN (bit7)

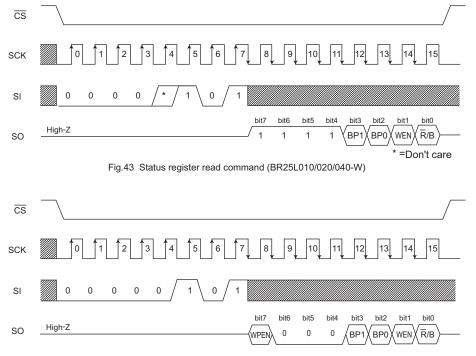


Fig.44 Status register read command (BR25L080/160/320/640-W)

At standby

- Current at standby
 - Set CS "H", and be sure to set SCK, SI, WP, HOLD input "L" or "H". Do not input intermediate electric potential.
- → Timing

As shown in Fig. 45, at standby, when SCK is "H", even if \overline{CS} is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of \overline{CS} . At standby and at power ON/OFF, set \overline{CS} "H" status.

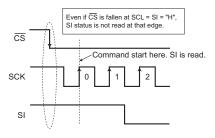


Fig.45 Operating timing

■ WP cancel valid area

 $\overline{\text{WP}}$ is normally fixed to "H" or "L" for use, but when $\overline{\text{WP}}$ is controlled so as to cancel write status register command and write command, pay attention to the following $\overline{\text{WP}}$ valid timing.

While write or write status register command is executed, by setting \overline{WP} = "L" in cancel valid area, command can be cancelled. The area from command ope code before \overline{CS} rise at internal automatic write start becomes the cancel valid area. However, once write is started, any input cannot be cancelled. \overline{WP} input becomes Don't Care, and cancellation becomes invalid.

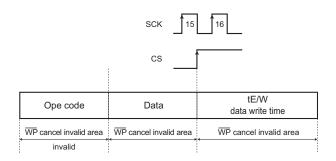


Fig.46 $\overline{\text{WP}}$ valid timing (WRSR)

Ope code	Address	Data	tE/W data write time
WP cancel invalid area	WP cancel	invalid area	WP cancel invalid area
invalid	va	lid	,

Fig.47 WP valid timing (WRITE)

■ HOLD pin

By HOLD pin, command communication can be stopped temporarily. (HOLD status) The HOLD pin carries out command communications normally when it is HIGH. To get in HOLD status, at command communication, when SCK = LOW, set the HOLD pin LOW. At HOLD status, SCK and SI become Don't Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the HOLD pin HIGH when SCK = LOW. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at read, after release of HOLD status, by starting A4 address input, read can be restarted. When in HOLD status, leave CS LOW. When it is set CS = HIGH in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

Method to cancel each command

○ READ

· Method to cancel : cancel by CS = "H"



Fig.48 READ cancel valid timing

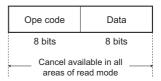


Fig.49 RDSR cancel valid timing

\bigcirc RDSR

Method to cancel: cancel by CS = "H"

OWRITE, PAGE WRITE

- a : Ope code, address input area.

 Cancellation is available by $\overline{\text{CS}}$ = "H".
- b : Data input area (D7 ~ D1 input area) Cancellation is available by \overline{CS} = "H".
- c : Data input area (D0 area)
 When \overline{CS} is started, write starts.
 After \overline{CS} rise, cancellation cannot be made by any means.

d: tE/W area

Cancellation is available by \overline{CS} = "H". However, when write starts (\overline{CS} is started) in the area c, cancellation cannot be made by any means. And, by inputting on SCK clock, cancellation cannot be made. In page write mode, there is write enable area at every 8 clocks.

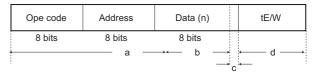
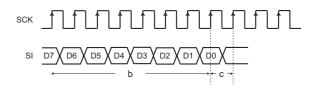


Fig.50 WRITE cancel valid timing



- Note 1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
- Note 2) If \overline{CS} is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is necessary to fall in SCK = "L" area. As for SCK rise, assure timing of tCSS / tCSH or higher.

○ WRSR

- a : From ope code to 15 clock rise Cancel by \overline{CS} = "H".
- b : From 15 clock rise to 16 clock rise (write enable area)
 When \overline{CS} is started, write starts.

 After \overline{CS} rise, cancellation cannot be made by any
- c: After 16 clock rise

means

Cancel by $\overline{\text{CS}}$ = "H". However, when write starts ($\overline{\text{CS}}$ is started) in the area b, cancellation cannot be made by any means. And, by inputting on SCK clock, cancellation cannot be made.

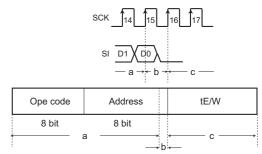


Fig.51 WRSR cancel valid timing

- Note 1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
- Note 2) If \overline{CS} is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is necessary to fall in SCK = "L" area. As for SCK rise, assure timing of tCSS/tCSH or higher.

○WREN/WRDI

- a: From ope code to clock rise, cancel by \overline{CS} = "H".
- b : Cancellation is not available when $\overline{\text{CS}}$ is started after 7 clock.

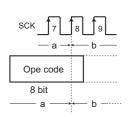


Fig.52 WREN / WRDI cancel valid timing

High speed operation

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

O Input pin pull up, pull down resistance

When to attach pull up, pull down resistance to EEPROM input pin, select an appropriate value for the microcontroller VOL, IOL from VIL characteristics of this IC.

O Pull up resistance

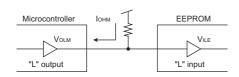


Fig.53 Pull up resistance

Example) When Vcc = 5V, VILM = 1.5V, VOLM = 0.4V, IOLM = 2mA, from the equation 1,

With the value of Rpu to satisfy the above equation, VoLM becomes 0.4V or higher, and with VILE (= 1.5V), the equation ② is also satisfied.

VILM: EEPROM VIH specifications
Volm: Microcontroller Vol. specifications
Iolm: Microcontroller Iol. specifications

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make $\overline{\text{CS}}$ pull up.

O Pull down resistance

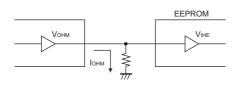


Fig.54 Pull down resistance

Example) When Vcc = 5V, VoHM = Vcc - 0.5V, IOHM = 0.4mA, VIHM = Vcc X 0.7V, from the equation ③,

R_{PD≥}
$$\frac{5-0.5}{0.4 \text{ X } 10^{-3}}$$

Further, by amplitude VIHE, VILE of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of VCC / GND level to input, more stable high speed operations can be realized. On the contrary, when amplitude of 0.8VCC / 0.2VCC is input, operation speed becomes slow.

In order to realize more stable high speed operation, it is recommended to make the values of RPU, RPD as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of VCC / GND level. (*1 At this moment, operating timing guaranteed value is guaranteed.)

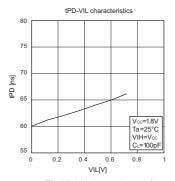
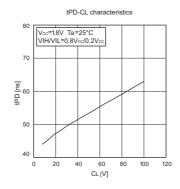


Fig.55 VIL dependency of data output delay time

O SO load capacity condition

Load capacity of SO output pin affects upon delay characteristic of SO output. (Data output delay time, time from HOLD to High-Z) In order to make output delay characteristic into higher speed, make SO load capacity small. In concrete, "Do not connect many devices to SO bus", "Make the wire between the controller and EEPROM short", and so forth.



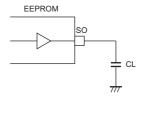


Fig.56 SO load dependency of data output delay time

Other cautions

Make the wire length from the microcontroller to EEPROM input signal same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

Equivalent circuitOutput circuit

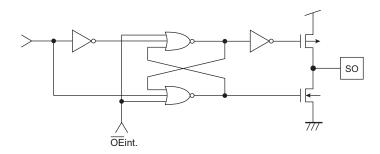


Fig.57 SO output equivalent circuit

Olnput circuit

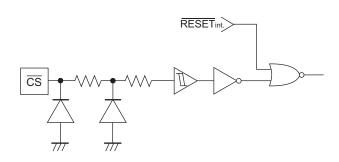


Fig.58 $\overline{\text{CS}}$ input equivalent circuit

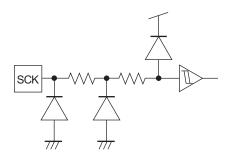


Fig.59 SCK input equivalent circuit

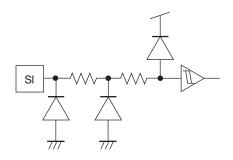


Fig.60 SI input equivalent circuit

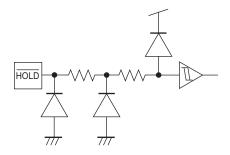


Fig.61 HOLD input equivalent circuit

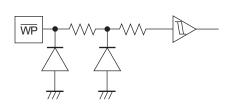


Fig.62 WP input equivalent circuit

Notes on power ON/OFF

At power ON/OFF, set CS "H" (= Vcc).

When \overline{CS} is "L", this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set \overline{CS} "H". (When \overline{CS} is in "H" status, all inputs are canceled.)

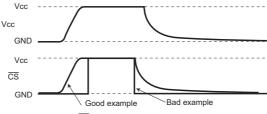


Fig.63 CS timing at power ON/OFF

(Good example) $\overline{\text{CS}}$ terminal is pulled up to Vcc.

At power OFF, take 10ms or higher before re supply. If power is turned on without observing this condition, the IC internal circuit may not be reset, which please note.

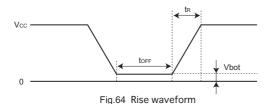
(Bad example) $\overline{\text{CS}}$ terminal is "L" at power ON/OFF.

In this case, CS always becomes "L" (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.

Even when CS input is High-Z, the status becomes like this case, which please note.

O PORcircuit

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following tR, tOFF, and Vbot are not satisfied, it may become write enable status owing to noises and the likes.



Recommended conditions of tR, tOFF, Vbot

tr	toff	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Noise countermeasures

○ Vcc noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor $(0.1\mu\text{F})$ between IC Vcc and GND. At that moment, attach it as close to IC as possible.

And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

OSCK noise

When the rise time (tR) of SCK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (tR) of SCK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

○ WP noise

During execution of write status register command, if there exist noises on \overline{WP} pin, mistake in recognition may occur and forcible cancellation may result, which please note. To avoid this, a Schmitt trigger circuit is built in \overline{WP} input. In the same manner, a Schmitt trigger circuit is built in SI input and \overline{HOLD} input too.

Cautions on use

- (1) Described numeric values and data are design representative values, and the values are not guaranteed.
- (2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.
- (3) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and operating temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

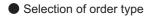
(5) Heat design

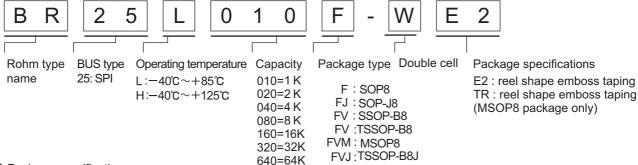
In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal short circuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of short circuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

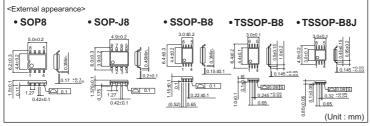
(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

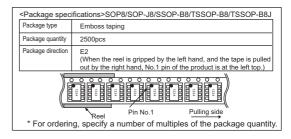


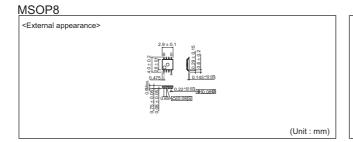


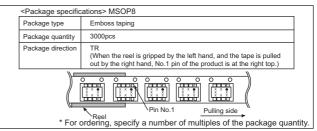
Package specifications

SOP8/SOP-J8/SSOP-B8/TSSOP-B8J









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 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
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- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- 2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
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http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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