

IS61WV20488ALL IS61/64WV20488BLL



2M x 8 HIGH-SPEED CMOS STATIC RAM

AUGUST 2010

FEATURES

- High-speed access times:
8, 10, 20 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with \overline{CE} and \overline{OE} options
- \overline{CE} power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single power supply
 - V_{DD} 1.65V to 2.2V (IS61WV20488ALL)
speed = 20ns for V_{cc} = 1.65V to 2.2V
 - V_{DD} 2.4V to 3.6V (IS61/64WV20488BLL)
speed = 10ns for V_{cc} = 2.4V to 3.6V
speed = 8ns for V_{cc} = 3.3V \pm 5%
- Packages available:
 - 48-ball miniBGA (9mm x 11mm)
 - 44-pin TSOP (Type II)
- Industrial and Automotive Temperature Support
- Lead-free available

DESCRIPTION

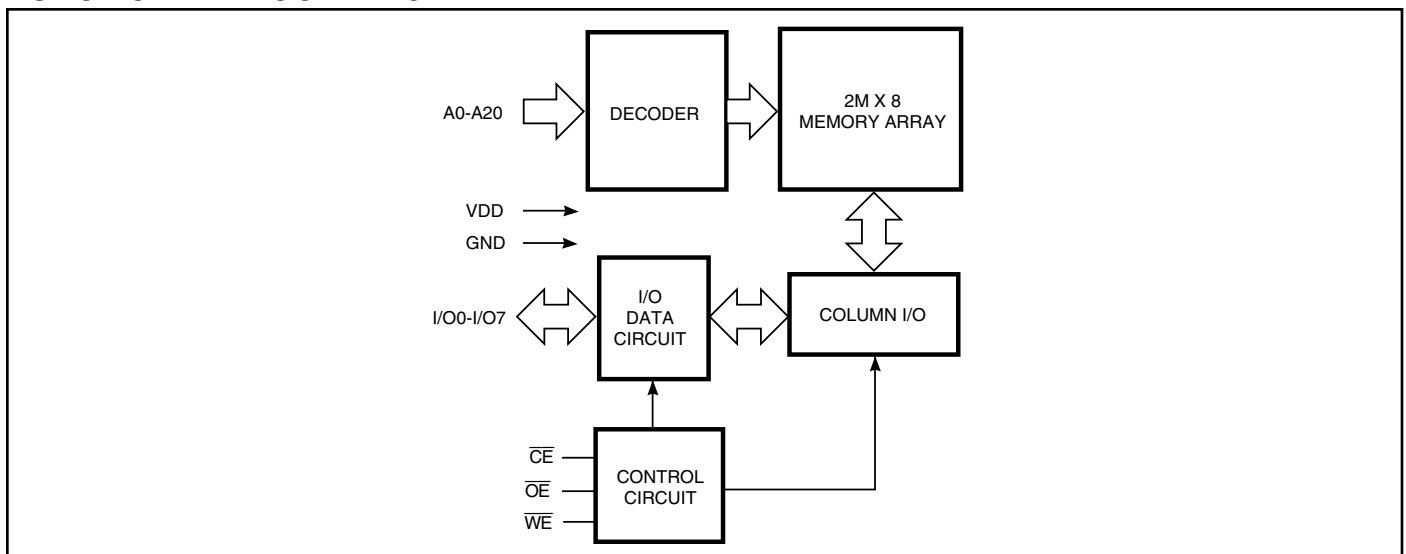
The *ISSI* IS61WV20488ALL/BLL and IS64WV20488BLL are very high-speed, low power, 2M-word by 8-bit CMOS static RAM. The IS61WV20488ALL/BLL and IS64WV20488BLL are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

The IS61WV20488ALL/BLL and IS64WV20488BLL operate from a single power supply and all inputs are TTL-compatible.

The IS61WV20488ALL/BLL and IS64WV20488BLL are available in 48 ball mini BGA and 44-pin TSOP (Type II) packages.

FUNCTIONAL BLOCK DIAGRAM



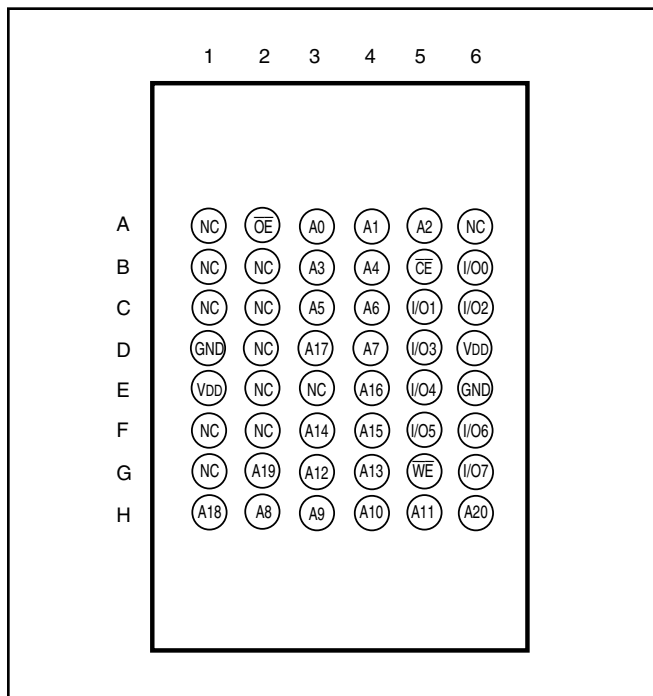
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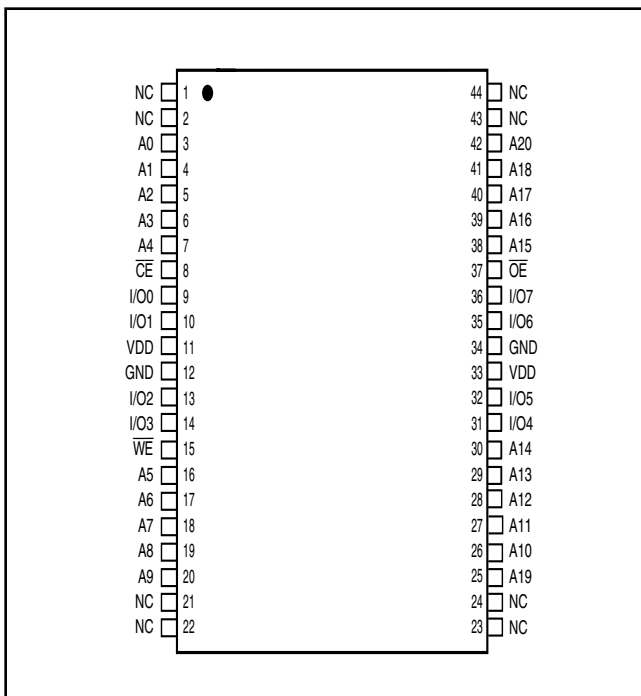
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATION

48-pin Mini BGA (M) (9mm x 11mm)



44-pin TSOP (Type II)



PIN DESCRIPTIONS

| | |
|-----------------|---------------------|
| A0-A20 | Address Inputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O0-I/O7 | Data Input / Output |
| VDD | Power |
| GND | Ground |
| NC | No Connection |

TRUTH TABLE

| Mode | \overline{WE} | \overline{CE} | \overline{OE} | I/O Operation | V _{DD} Current |
|------------------------------|-----------------|-----------------|-----------------|------------------|-------------------------------------|
| Not Selected (Power-down) | X | H | X | High-Z | I _{SB1} , I _{SB2} |
| Output Disabled | H | L | H | High-Z | I _{CC} |
| Read | H | L | L | D _{OUT} | I _{CC} |
| Write | L | L | X | D _{IN} | I _{CC} |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|-------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{DD} + 0.5 | V |
| V _{DD} | V _{DD} Relates to GND | -0.3 to 4.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{I/O} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

OPERATING RANGE (V_{DD}) (IS61WV20488ALL)

| Range | Ambient Temperature | V _{DD} (20 ns) |
|------------|---------------------|-------------------------|
| Commercial | 0°C to +70°C | 1.65V-2.2V |
| Industrial | -40°C to +85°C | 1.65V-2.2V |
| Automotive | -40°C to +125°C | 1.65V-2.2V |

OPERATING RANGE (V_{DD}) (IS61WV20488BLL)⁽¹⁾

| Range | Ambient Temperature | V _{DD} (8 ns) | V _{DD} (10 ns) |
|------------|---------------------|------------------------|-------------------------|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 2.4V-3.6V |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 2.4V-3.6V |

Note:

1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

OPERATING RANGE (V_{DD}) (IS64WV20488BLL)

| Range | Ambient Temperature | V _{DD} (10 ns) |
|------------|---------------------|-------------------------|
| Automotive | -40°C to +125°C | 2.4V-3.6V |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

 $V_{DD} = 3.3V \pm 5\%$

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------|----------------------------------|---|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $V_{DD} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | — | V |
| V_{OL} | Output LOW Voltage | $V_{DD} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$ | — | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I_{LI} | Input Leakage | $GND \leq V_{IN} \leq V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled | -1 | 1 | μA |

Note:

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

 $V_{DD} = 2.4V-3.6V$

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------|----------------------------------|---|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $V_{DD} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$ | 1.8 | — | V |
| V_{OL} | Output LOW Voltage | $V_{DD} = \text{Min.}, I_{OL} = 1.0 \text{ mA}$ | — | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.0 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I_{LI} | Input Leakage | $GND \leq V_{IN} \leq V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled | -1 | 1 | μA |

Note:

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

 $V_{DD} = 1.65V-2.2V$

| Symbol | Parameter | Test Conditions | V_{DD} | Min. | Max. | Unit |
|----------------|---------------------|---|-----------|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $I_{OH} = -0.1 \text{ mA}$ | 1.65-2.2V | 1.4 | — | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 0.1 \text{ mA}$ | 1.65-2.2V | — | 0.2 | V |
| V_{IH} | Input HIGH Voltage | | 1.65-2.2V | 1.4 | $V_{DD} + 0.2$ | V |
| $V_{IL}^{(1)}$ | Input LOW Voltage | | 1.65-2.2V | -0.2 | 0.4 | V |
| I_{LI} | Input Leakage | $GND \leq V_{IN} \leq V_{DD}$ | | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled | | -1 | 1 | μA |

Note:

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.

AC TEST CONDITIONS (HIGH SPEED)

| Parameter | Unit (2.4V-3.6V) | Unit (3.3V ± 5%) | Unit (1.65V-2.2V) |
|---|-------------------------------|-------------------------------|-------------------------------|
| Input Pulse Level | 0.4V to V _{DD} -0.3V | 0.4V to V _{DD} -0.3V | 0.4V to V _{DD} -0.2V |
| Input Rise and Fall Times | 1.5ns | 1.5ns | 1.5ns |
| Input and Output Timing and Reference Level (V _{Ref}) | V _{DD} /2 | V _{DD} /2 + 0.05 | V _{DD} /2 |
| Output Load | See Figures 1 and 2 | See Figures 1 and 2 | See Figures 1 and 2 |

AC TEST LOADS

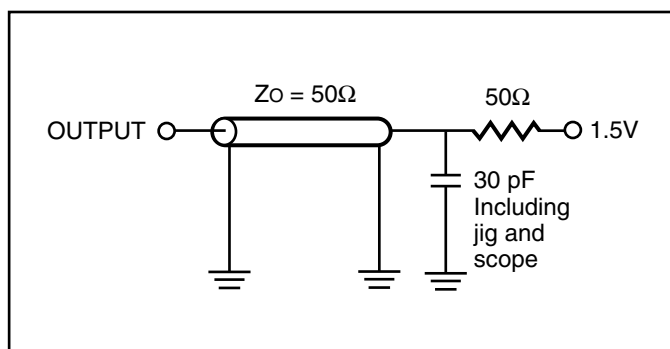


Figure 1.

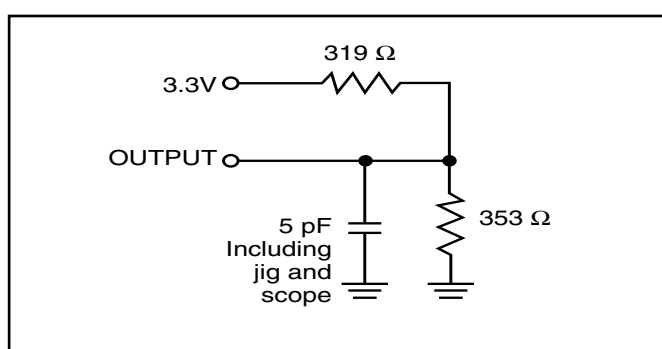


Figure 2.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -8 | | -10 | | -20 | | Unit |
|------------------|--|--|---------------------|------|------|------|------|------|------|------|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. | — | 120 | — | 95 | — | 90 | mA |
| | | | Ind. | — | 125 | — | 100 | — | 100 | |
| | | | Auto. | — | — | — | 140 | — | 140 | |
| | | | typ. ⁽²⁾ | | | 60 | | | | |
| I _{CC1} | Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = 0 | Com. | — | 35 | — | 30 | — | 30 | mA |
| | | | Ind. | — | 35 | — | 40 | — | 40 | |
| | | | Auto. | — | — | — | 60 | — | 70 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} CE ≥ V _{IH} , f = 0 | Com. | — | 30 | — | 30 | — | 30 | mA |
| | | | Ind. | — | 35 | — | 35 | — | 35 | |
| | | | Auto. | — | — | — | 70 | — | 70 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., CE ≥ V _{DD} - 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 20 | — | 20 | — | 15 | mA |
| | | | Ind. | — | 25 | — | 25 | — | 20 | |
| | | | Auto. | — | — | — | 70 | — | 70 | |
| | | | typ. ⁽²⁾ | | | 4 | | | | |

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | Unit |
|---------------------------------|---|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 8 | — | 10 | — | ns |
| t _{AA} | Address Access Time | — | 8 | — | 10 | ns |
| t _{OHA} | Output Hold Time | 2 | — | 2 | — | ns |
| t _{ACE} | $\overline{\text{CE}}$ Access Time | — | 8 | — | 10 | ns |
| t _{DOE} | $\overline{\text{OE}}$ Access Time | — | 5.5 | — | 6.5 | ns |
| t _{HZOE⁽²⁾} | $\overline{\text{OE}}$ to High-Z Output | — | 3 | — | 4 | ns |
| t _{LZOE⁽²⁾} | $\overline{\text{OE}}$ to Low-Z Output | 0 | — | 0 | — | ns |
| t _{HZCE⁽²⁾} | $\overline{\text{CE}}$ to High-Z Output | 0 | 3 | 0 | 4 | ns |
| t _{LZCE⁽²⁾} | $\overline{\text{CE}}$ to Low-Z Output | 3 | — | 3 | — | ns |
| t _{PU} | Power Up Time | 0 | — | 0 | — | ns |
| t _{PD} | Power Down Time | — | 8 | — | 10 | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

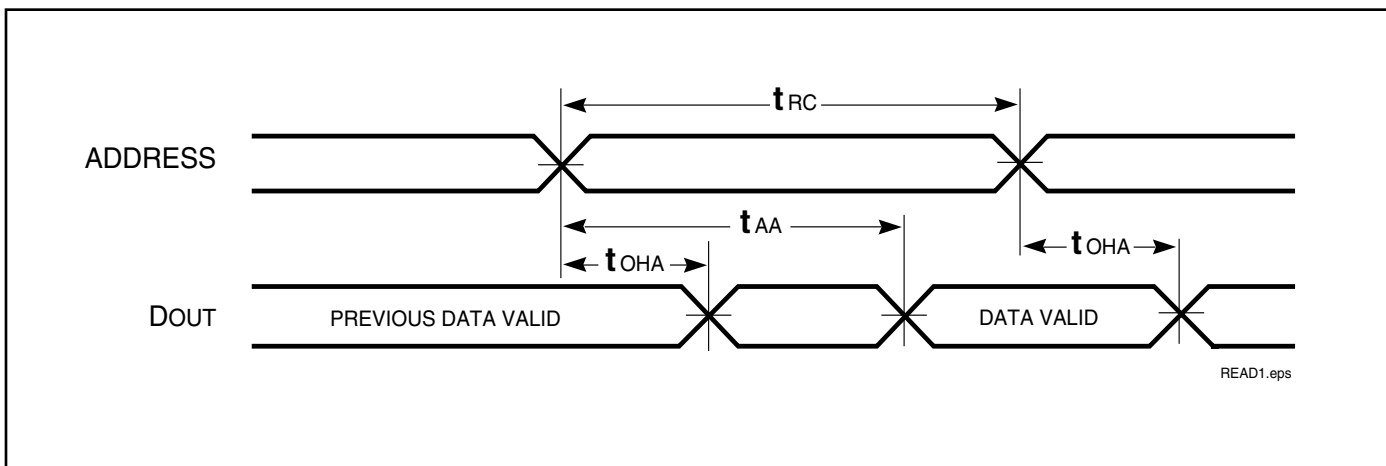
| Symbol | Parameter | -20 ns | | Unit |
|---------------------------------|----------------------------------|--------|------|------|
| | | Min. | Max. | |
| t _{RC} | Read Cycle Time | 20 | — | ns |
| t _{AA} | Address Access Time | — | 20 | ns |
| t _{OHA} | Output Hold Time | 2.5 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 20 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 8 | ns |
| t _{HZOE⁽²⁾} | \overline{OE} to High-Z Output | 0 | 8 | ns |
| t _{LZOE⁽²⁾} | \overline{OE} to Low-Z Output | 0 | — | ns |
| t _{HZCE⁽²⁾} | \overline{CE} to High-Z Output | 0 | 8 | ns |
| t _{LZCE⁽²⁾} | \overline{CE} to Low-Z Output | 3 | — | ns |
| t _{PU} | Power Up Time | 0 | — | ns |
| t _{PD} | Power Down Time | — | 20 | ns |

Notes:

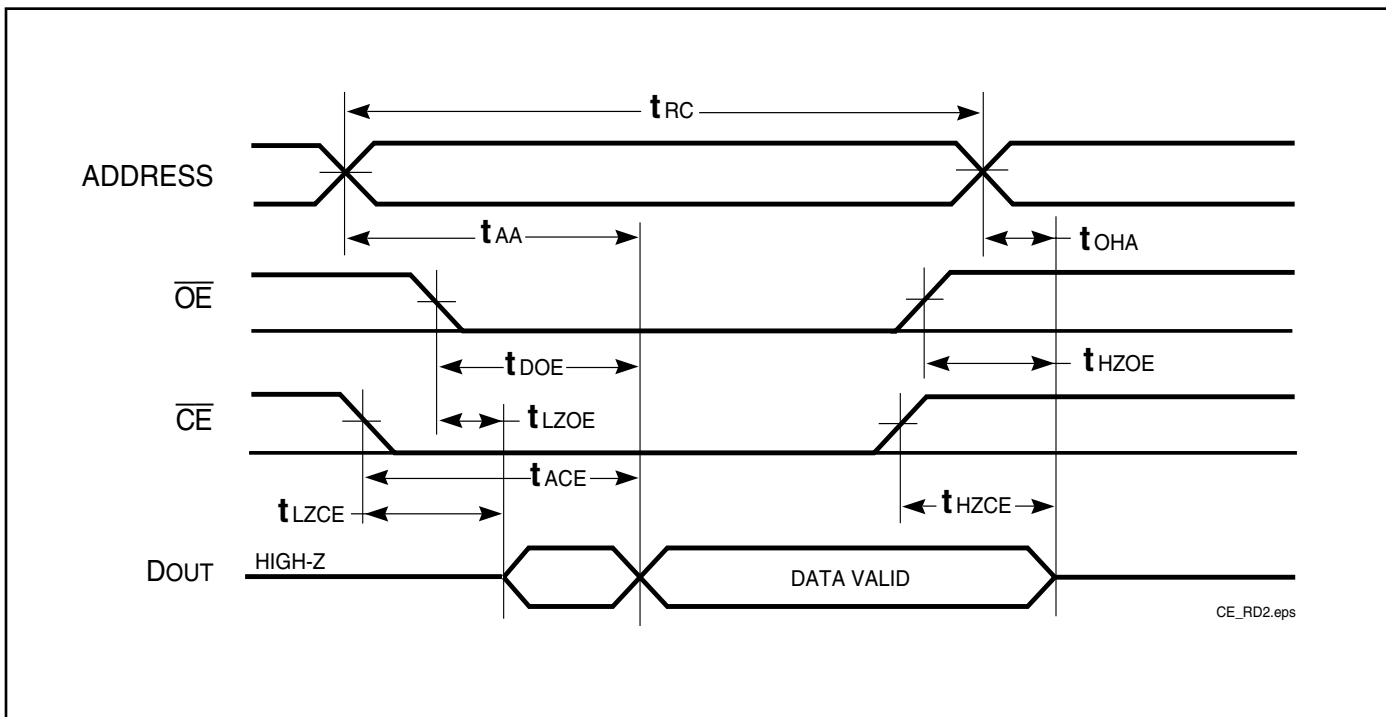
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)



READ CYCLE NO. 2^(1,3) (\overline{CE} and \overline{OE} Controlled)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | Unit |
|---------------------------------|---|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 8 | — | 10 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 6.5 | — | 8 | — | ns |
| t _{AW} | Address Setup Time to Write End | 6.5 | — | 8 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width (\overline{OE} = HIGH) | 6.5 | — | 8 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} = LOW) | 8.0 | — | 10 | — | ns |
| t _{SD} | Data Setup to Write End | 5 | — | 6 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | ns |
| t _{HZWE⁽²⁾} | \overline{WE} LOW to High-Z Output | — | 3.5 | — | 5 | ns |
| t _{LZWE⁽²⁾} | \overline{WE} HIGH to Low-Z Output | 2 | — | 2 | — | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

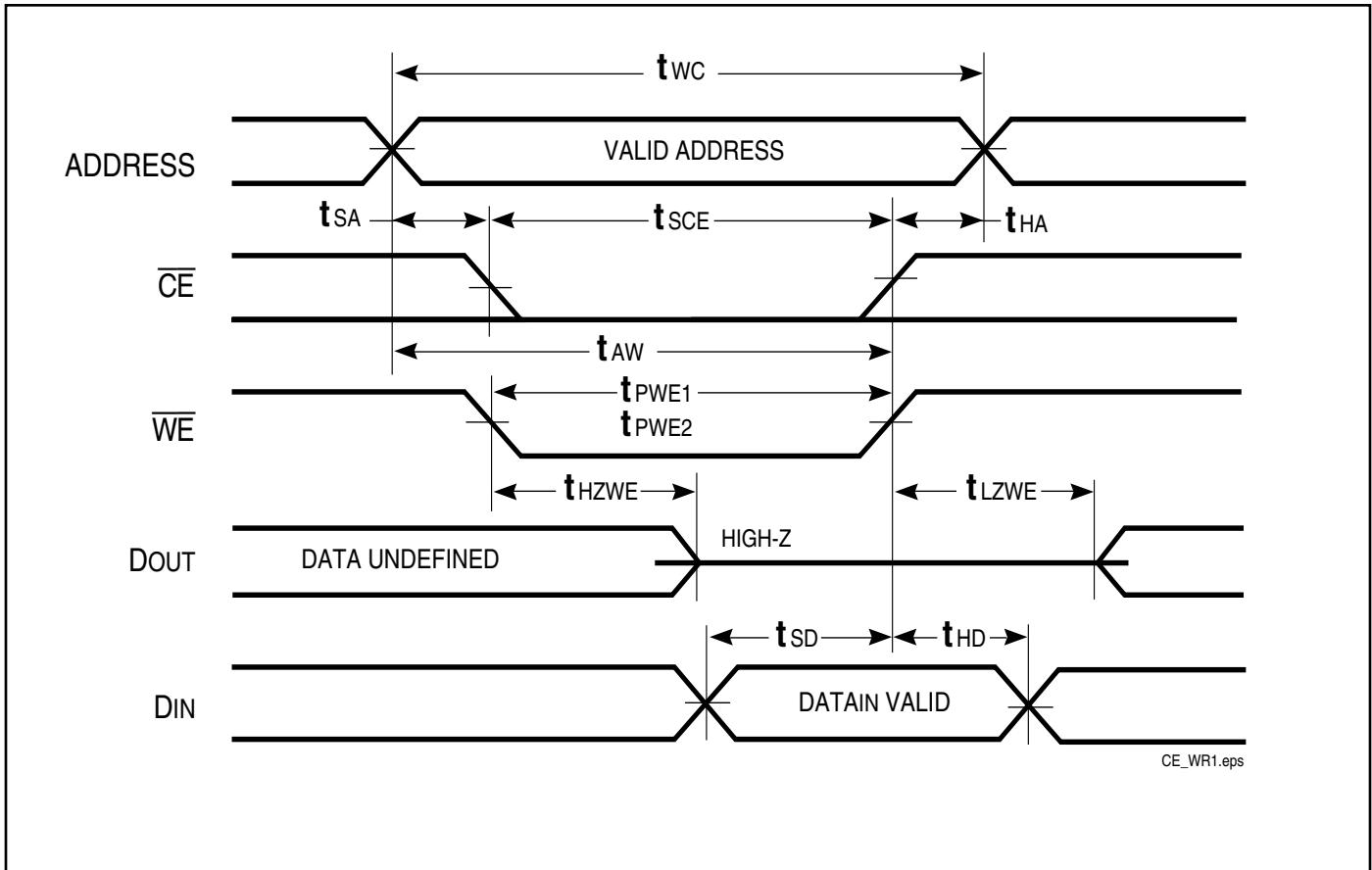
| Symbol | Parameter | -20 ns | | Unit |
|----------------------------------|---|--------|------|------|
| | | Min. | Max. | |
| t _{WC} | Write Cycle Time | 20 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 12 | — | ns |
| t _{AW} | Address Setup Time to Write End | 12 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width (\overline{OE} = HIGH) | 12 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} = LOW) | 17 | — | ns |
| t _{SD} | Data Setup to Write End | 9 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | ns |
| t _{HZWE} ⁽³⁾ | \overline{WE} LOW to High-Z Output | — | 9 | ns |
| t _{LZWE} ⁽³⁾ | \overline{WE} HIGH to Low-Z Output | 3 | — | ns |

Notes:

1. Test conditions assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

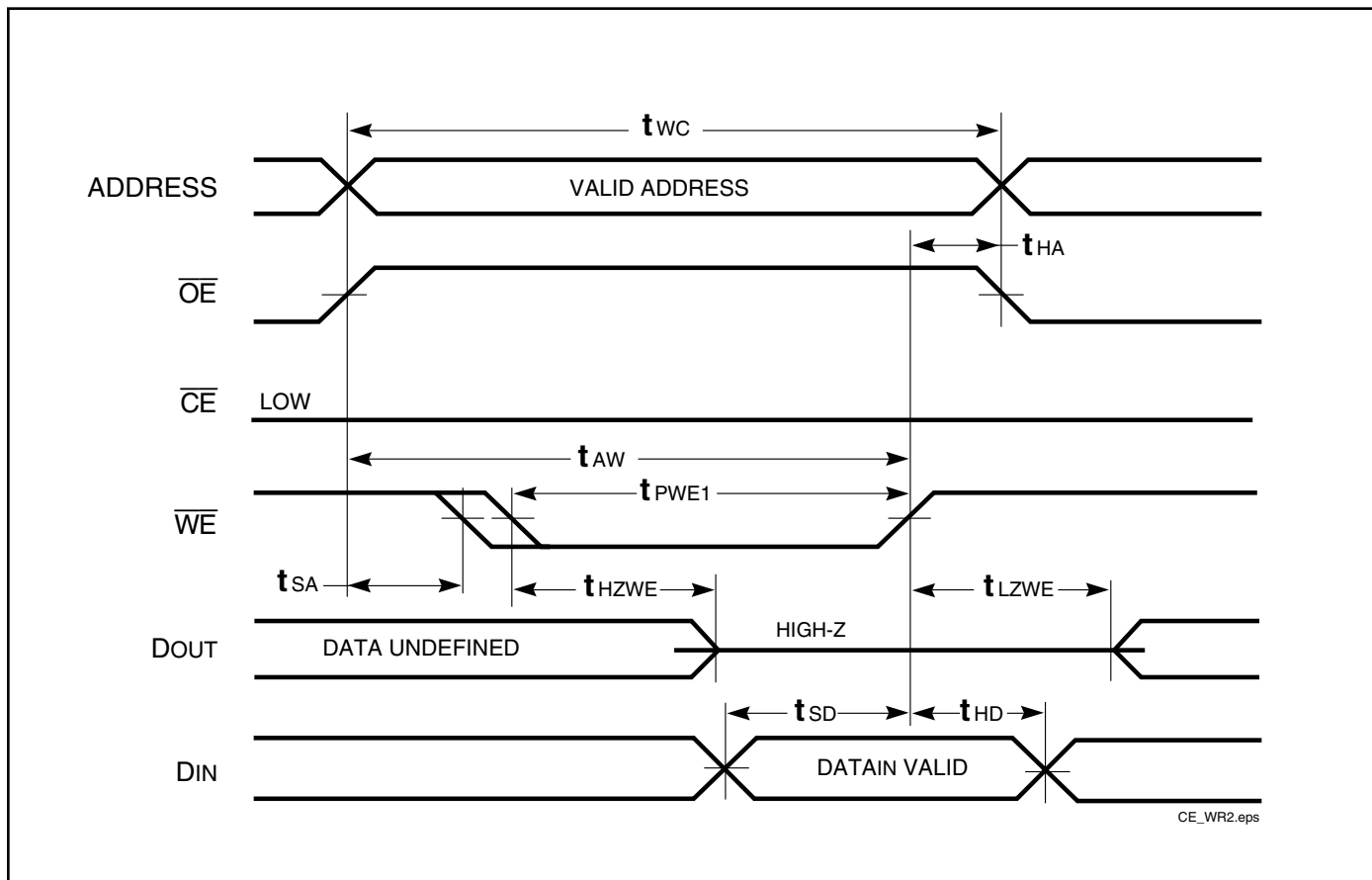
AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)



AC WAVEFORMS

WRITE CYCLE NO. 2^(1,2) (\overline{WE} Controlled: \overline{OE} is HIGH During Write Cycle)

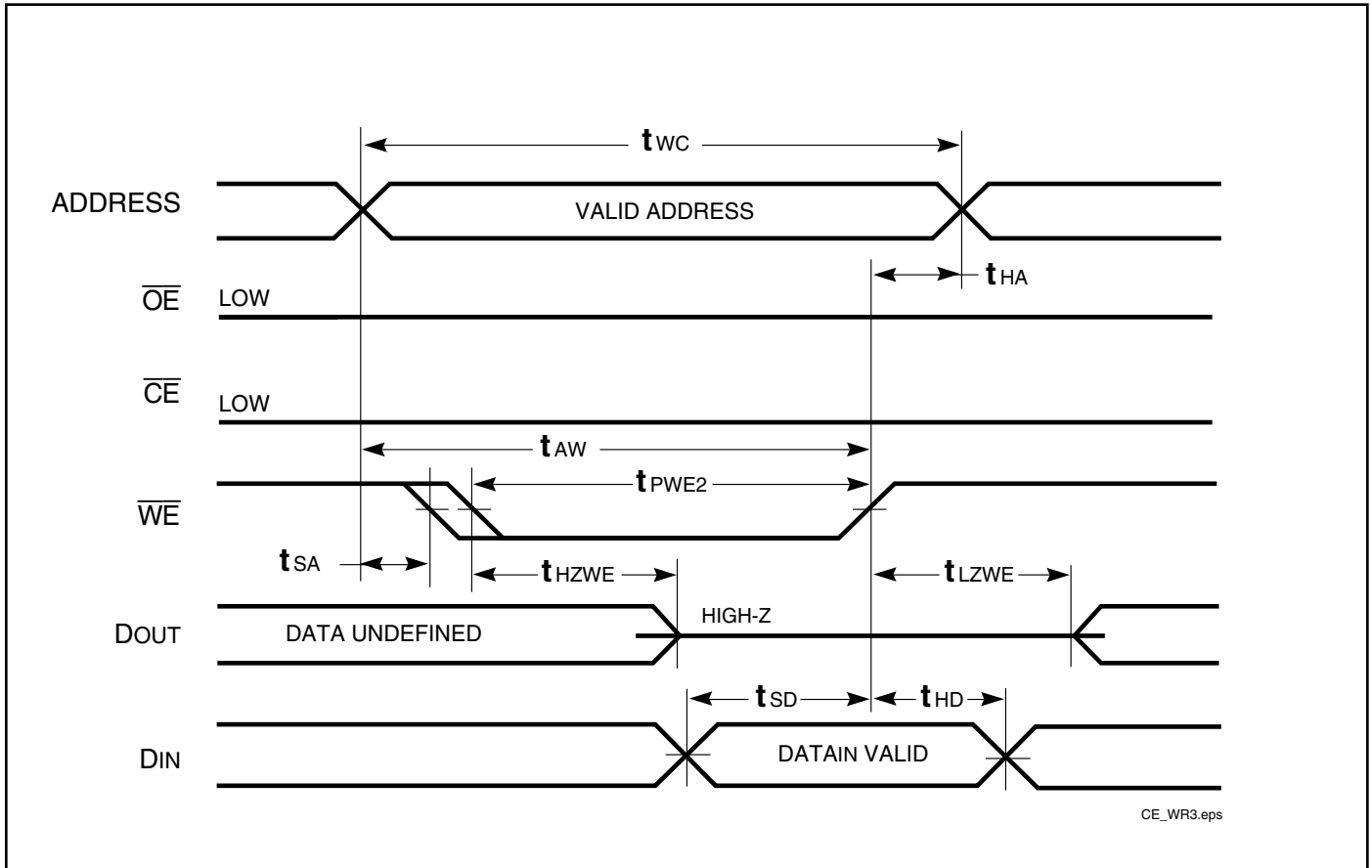


Notes:

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

AC WAVEFORMS

WRITE CYCLE NO. 3 (\overline{WE} Controlled: \overline{OE} is LOW During Write Cycle)



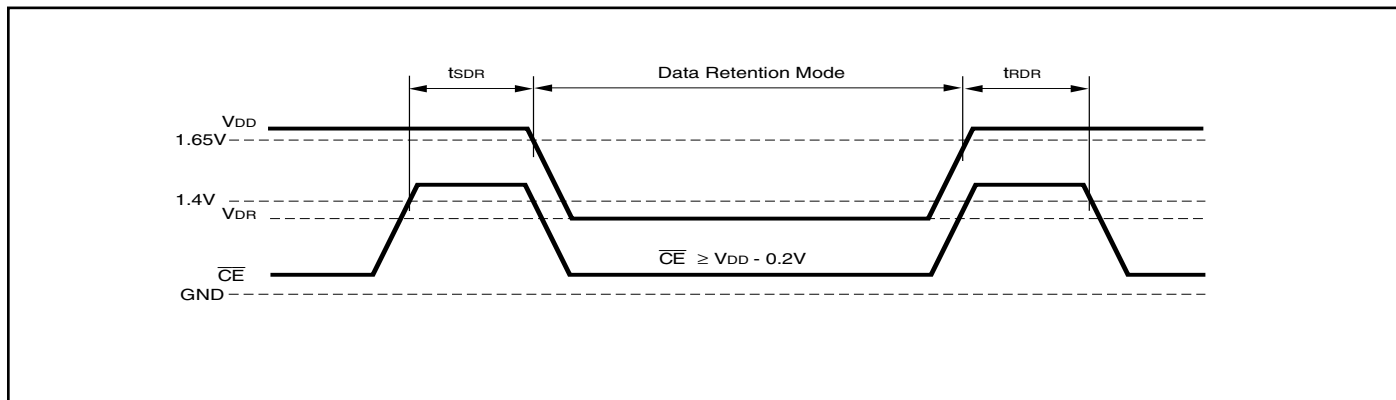
DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|------------------|------------------------------------|--|--------------------------------------|---------------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | 1.2 | 3.6 | V |
| I _{DR} | Data Retention Current | V _{DD} = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$ | Ind. Auto. typ. ⁽¹⁾ | 25 60 3 | mA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | 0 | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | t _{RC} | — | ns |

Note:

1. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



ORDERING INFORMATION
Industrial Range: -40°C to +85°C
Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|----------------------|----------------------|-------------------------------------|
| 10 (8 ¹) | IS61WV20488BLL-10MI | 48 mini BGA (9mm x 11mm) |
| | IS61WV20488BLL-10MLI | 48 mini BGA (9mm x 11mm), Lead-free |
| | IS61WV20488BLL-10TI | TSOP (Type II) |
| | IS61WV20488BLL-10TLI | TSOP (Type II), Lead-free |

Note:

 1. Speed = 8ns for V_{DD} = 3.3V ± 5%. Speed = 10ns for V_{DD} = 2.4V to 3.3V.

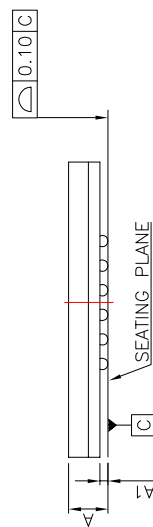
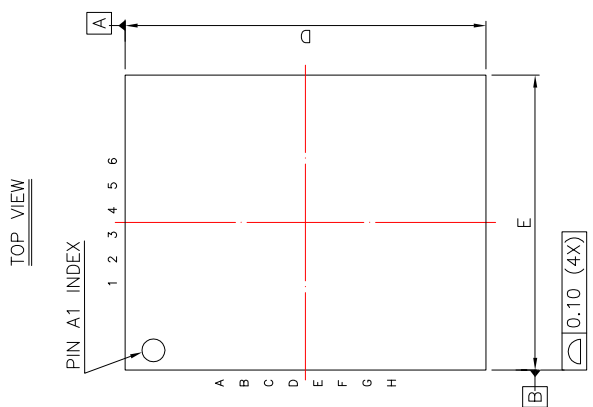
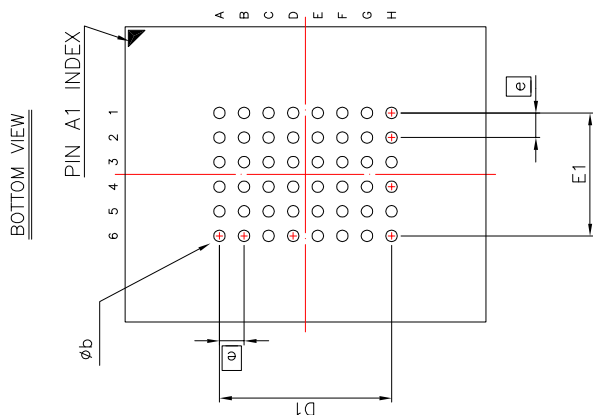
Industrial Range: -40°C to +85°C
Voltage Range: 1.65V to 2.2V

| Speed (ns) | Order Part No. | Package |
|------------|---------------------|--------------------------|
| 20 | IS61WV20488ALL-20MI | 48 mini BGA (9mm x 11mm) |
| | IS61WV20488ALL-20TI | TSOP (Type II) |

Automotive Range: -40°C to +125°C
Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|------------|-----------------------|-------------------------------------|
| 10 | IS64WV20488BLL-10MA3 | 48 mini BGA (9mm x 11mm) |
| | IS64WV20488BLL-10MLA3 | 48 mini BGA (9mm x 11mm), Lead-free |
| | IS64WV20488BLL-10TA3 | TSOP (Type II) |

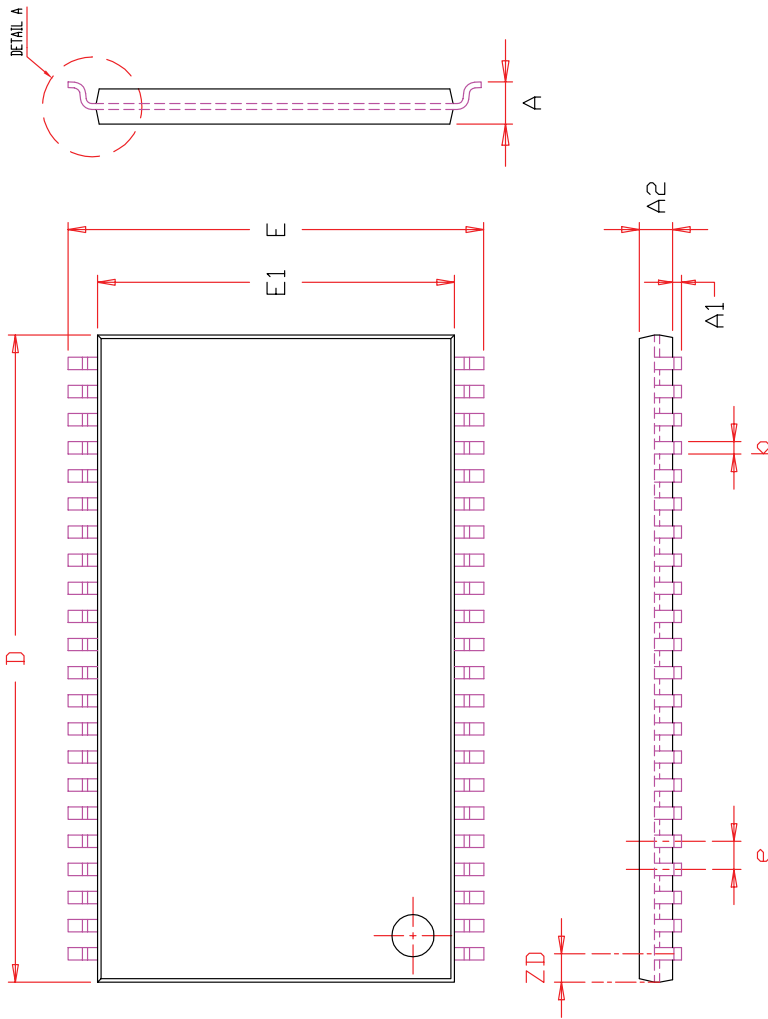
| SYM. | DIMENSION (mm) | | | DIMENSION (INCH) | | |
|------|----------------|-------|-------|------------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.20 | — | 0.30 | 0.008 | — | 0.012 |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| D | 10.90 | 11.00 | 11.10 | 0.429 | 0.433 | 0.437 |
| D1 | 5.25 | BSC | — | 0.207 | BSC | — |
| E | 8.90 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| E1 | — | 3.75 | BSC | — | 0.148 | BSC |
| Ⓜ | — | 0.75 | BSC | — | 0.030 | BSC |



NOTE :

1. CONTROLLING DIMENSION : MM.
2. Reference document : JEDEC MO-207

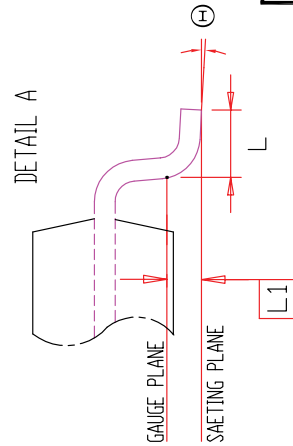
| | | | | | | |
|--|-------|-----------------------------------|------|---|------|------------|
| | TITLE | 48L 9x11mm TF-BGA Package Outline | REV. | B | DATE | 08/21/2008 |
|--|-------|-----------------------------------|------|---|------|------------|



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|-----------------|-------|-------|-------------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | | 1.20 | 0.039 | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.30 | | 0.45 | 0.012 | | 0.018 |
| D | 18.28 | 18.41 | 18.54 | 0.720 | 0.725 | 0.730 |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | 0.80 BSC. | | | 0.031 BSC. | | |
| L | 0.40 | | 0.69 | 0.016 | | 0.027 |
| L1 | 0.25 BSC. | | | 0.010 BSC. | | |
| ZD | 0.805 REF. | | | 0.032 REF. | | |
| ⊕ | 0 | | 8° | 0 | | 8° |

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



TITLE

44L 400mil TSOP-2
Package Outline

REV.

F

DATE

06/04/2008

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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