ISL6611A

Phase Doubler with Integrated Drivers and Phase Shedding Function

FN6881
Rev 1.00
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The ISL6611A utilizes Intersil's proprietary Phase Doubler scheme to modulate two-phase power trains with single PWM input. It doubles the number of phases that Intersil's ISL63xx multiphase controllers can support. At the same time, the PWM line can be pulled high to disable the corresponding phase or higher phase(s) when the enable pin (EN_PH) is pulled low. This simplifies the phase shedding implementation. For layout simplicity and improving system performance, the device integrates two 5V drivers (ISL6609) and current balance function.

The ISL6611A is designed to minimize the number of analog signals interfacing between the controller and drivers in high phase count and scalable applications. The common COMP signal, which is usually seen with conventional cascaded configuration, is not required; this improves noise immunity and simplifies the layout. Furthermore, the ISL6611A provides low part count and a low cost advantage over the conventional cascaded technique.

The IC is biased by a single low voltage supply (5V), minimizing driver switching losses in high MOSFET gate capacitance and high switching frequency applications. Bootstrapping of the upper gate driver is implemented via an internal low forward drop diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

The ISL6611A features 4A typical sink current for the lower gate driver, enhancing the lower MOSFET gate hold-down capability during PHASE node rising edge, preventing power loss caused by the self turn-on of the lower MOSFET due to the high dV/dt of the switching node.

The ISL6611A also features an input that recognizes a high-impedance state, working together with Intersil multiphase PWM controllers to prevent negative transients on the controlled output voltage when operation is suspended. This feature eliminates the need for the Schottky diode that may be utilized in a power system to protect the load from negative output voltage damage.

In addition, the ISL6611A's bootstrap function is designed to prevent the BOOT capacitor from overcharging, should excessively large negative swings occur at the transitions of the PHASE node.

Features

- Proprietary Phase Doubler Scheme with Phase Shedding Function (Patent Pending)
  - Enhanced Light to Full Load Efficiency
- Patented Current Balancing with $r_{DS(ON)}$ Current Sensing and Adjustable Gain
- Quad MOSFET Drives for Two Synchronous Rectified Bridge with Single PWM Input
- Channel Synchronization and Interleaving Options
- Adaptive Zero Shoot-Through Protection
- 0.4Ω On-Resistance and 4A Sink Current Capability
- 36V Internal Bootstrap Schottky Diode
- Bootstrap Capacitor Overcharging Prevention (ISL6611A)
- Supports High Switching Frequency (Up to 1MHz)
  - Fast Output Rise and Fall
- Tri-State PWM Input for Output Stage Shutdown
- Phase Enable Input and PWM Forced High Output to Interface with Intersil's Controller for Phase Shedding
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN-Quad Flat No Leads-Product Outline
  - Near Chip-Scale Package Footprint; Improves PCB Utilization, Thinner Profile
  - Pb-Free (RoHS Compliant)

Applications

- High Current Low Voltage DC/DC Converters
- High Frequency and High Efficiency VRM and VRD
- High Phase Count and Phase Shedding Applications

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Ordering Information

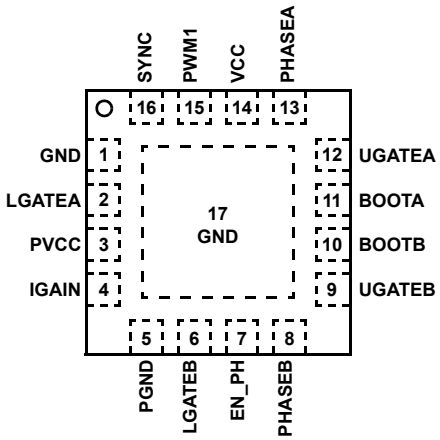
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6611ACRZ	66 11ACRZ	0 to +70	16 Ld 4x4 QFN	L16.4x4
ISL6611AIRZ*	66 11AIRZ	-40 to +85	16 Ld 4x4 QFN	L16.4x4

NOTES:

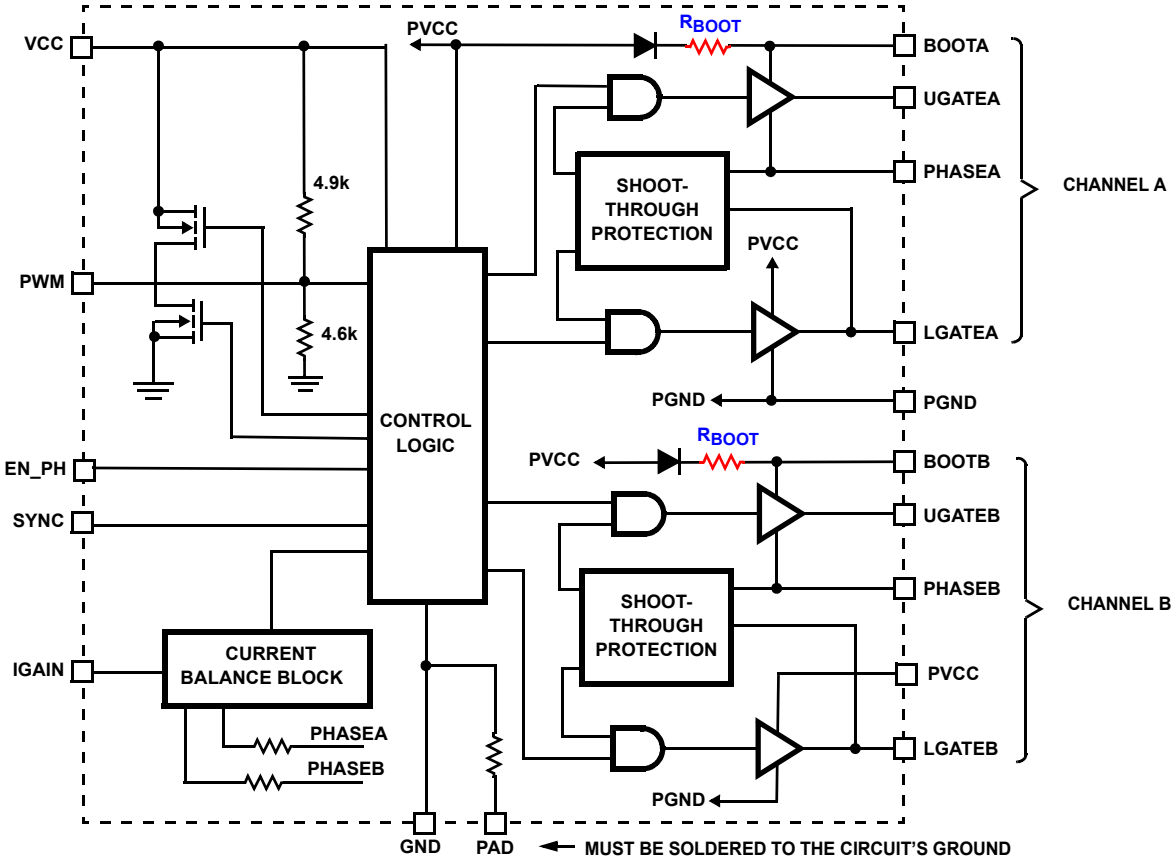
1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6611A. For more information on MSL please see techbrief TB363.

Pinout

ISL6611A
(16 LD QFN)
TOP VIEW



Block Diagram

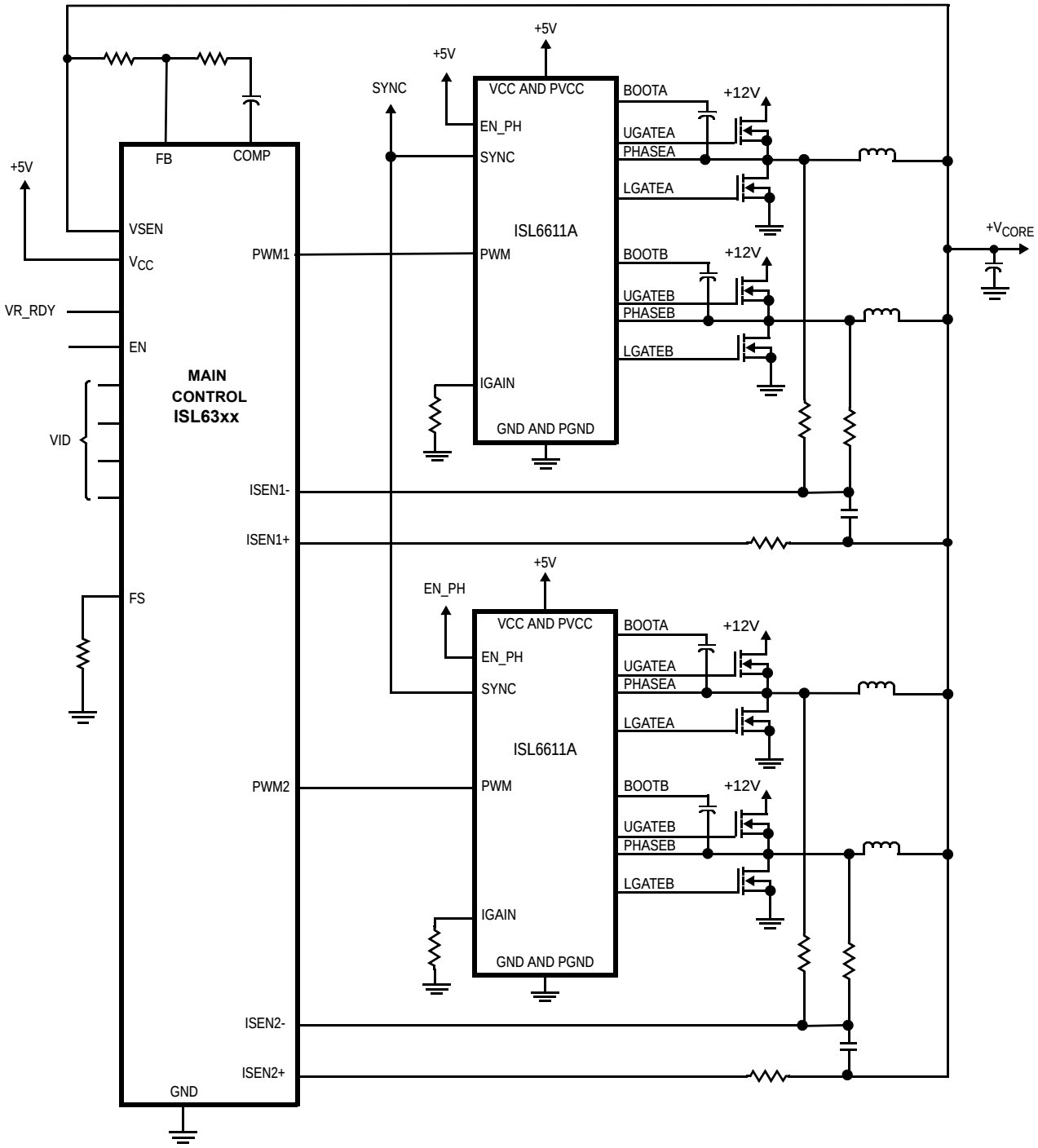


INTEGRATED 3Ω RESISTOR (R_{BOOT}) IN ISL6611A

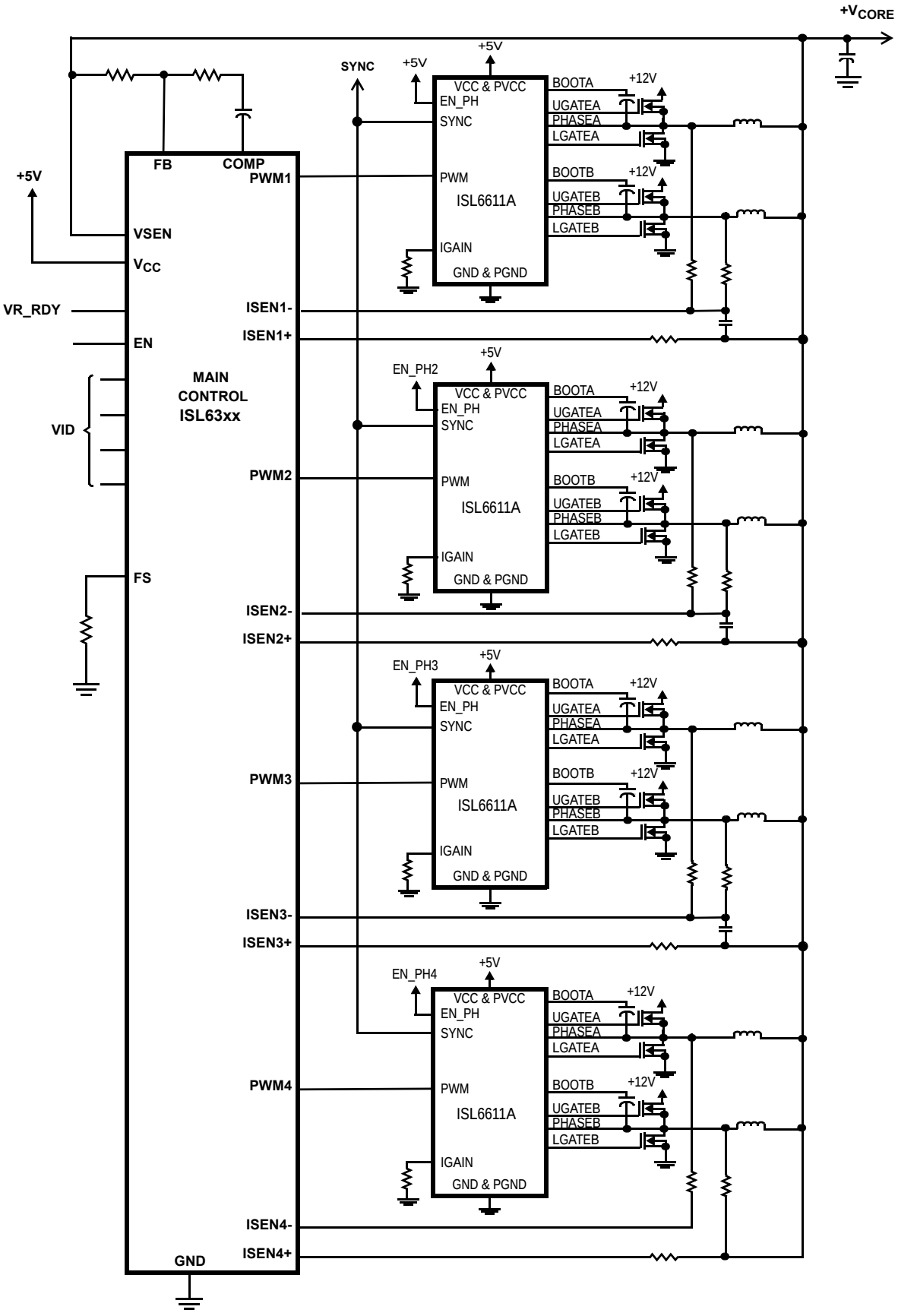
Functional Pin Descriptions

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	GND	Bias and reference ground. All signals are referenced to this node. It is also the return of the sample and hold of the $r_{DS(ON)}$ current sensing circuits. Place a high quality low ESR ceramic capacitor from this pin to VCC.
2	LGATEA	Lower gate drive output of Channel A. Connect to gate of the low-side power N-Channel MOSFET.
3	PVCC	This pin supplies power to both the lower and higher gate drives. Place a high quality low ESR ceramic capacitor from this pin to PGND.
4	IGAIN	A resistor from this pin to GND sets the current balance gain. See “Current Balance and Maximum Frequency” on page 11 for more details.
5	PGND	Power ground return of both low gate drivers. It is also the return of the phase node clamp circuits.
6	LGATEB	Lower gate drive output of Channel B. Connect to gate of the low-side power N-Channel MOSFET.
7	EN_PH	Driver Enable Input. A signal high input enables the driver at the PWM rising edge, a signal low input pulls PWM pin to VCC at the PWM falling edge and then enters tri-state.
8	PHASEB	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET in Channel B. This pin provides a return path for the upper gate drive.
9	UGATEB	Upper gate drive output of Channel B. Connect to gate of high-side power N-Channel MOSFET.
10	BOOTB	Floating bootstrap supply pin for the upper gate drive of Channel B. Connect the bootstrap capacitor between this pin and the PHASEB pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See“Bootstrap Considerations” on page 9 for guidance in choosing the capacitor value.
11	BOOTA	Floating bootstrap supply pin for the upper gate drive of Channel A. Connect the bootstrap capacitor between this pin and the PHASEA pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See “Bootstrap Considerations” on page 9 for guidance in choosing the capacitor value.
12	UGATEA	Upper gate drive output of Channel A. Connect to gate of high-side power N-Channel MOSFET.
13	PHASEA	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET in Channel A. This pin provides a return path for the upper gate drive.
14	VCC	Connect this pin to a +5V bias supply. It supplies power to internal analog circuits. Place a high quality low ESR ceramic capacitor from this pin to GND.
15	PWM	The PWM input signal triggers the J-K flip flop and alternates its input to channel A and B. Both channels are effectively modulated. The PWM signal can enter three distinct states during operation, see “Tri-State PWM Input” on page 9 for further details. Connect this pin to the PWM output of the controller. The pin is pulled to VCC when EN_PH is low and the PWM input starts transitioning low.
16	SYNC	A signal high synchronizes both channels with no phase shifted. A signal low interleaves both channels with 180° out-of-phase.
17	PAD	Connect this pad to the power ground plane (GND) via thermally enhanced connection.

Typical Application I (2-Phase Controller for 4-Phase Operation)



Typical Application II (4-Phase Controller to 8-Phase Operation)



Absolute Maximum Ratings

Supply Voltage (PVCC, VCC) . . . . . -0.3V to 6.7V
Input Voltage (V_{EN_PH}, V_{PWM}, V_{SYNC}) . . . . . -0.3V to VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . -0.3V to 27V (DC) or 36V (<200ns)
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V (DC)
-0.3V to 9V (<10ns)
PHASE Voltage . . . . . GND - 0.3V to 27V (DC)
GND -8V (<20ns Pulse Width, 10µJ) to 30V (<100ns)
UGATE Voltage . . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
V_{PHASE} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . . GND - 0.3V (DC) to VCC + 0.3V
GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA}(°C/W)	θ_{JC}(°C/W)
QFN Package (Notes 4, 5)	44	7

Ambient Temperature Range . . . . . -40°C to +125°C
Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature
ISL6611ACRZ . . . . . 0°C to +70°C
ISL6611AIRZ . . . . . -40°C to +85°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, VCC . . . . . 5V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

These specifications apply for recommended ambient temperature, unless otherwise noted. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT (Note 6)						
Bias Supply Current	$I_{VCC+PVCC}$	PWM pin floating, V_{VCC} = V_{PVCC} = 5V, EN_PH = 5V	-	1.25	-	mA
		PWM pin floating, V_{VCC} = V_{PVCC} = 5V, EN_PH = 0V	-	1.20	-	mA
		F_{PWM} = 600kHz, V_{VCC} = V_{PVCC} = 5V, EN_PH = 5V; SYNC = 0V	-	2.20	-	mA
		F_{PWM} = 300kHz, V_{VCC} = V_{PVCC} = 5V, EN_PH = 5V; SYNC = 5V	-	2.50	-	mA
BOOTSTRAP DIODE						
Forward Voltage	V_F	Forward bias current = 2mA T_A = 0°C to +70°C	0.30	0.60	0.70	V
		Forward bias current = 2mA T_A = -40°C to +85°C	0.30	0.60	0.75	V
POWER-ON RESET						
POR Rising			-	3.4	4.2	V
POR Falling			2.5	3.0	-	V
Hysteresis			-	400	-	mV
EN_PH INPUT						
EN_PH Minimum LOW Threshold			-	-	0.8	V
EN_PH Maximum HIGH Threshold			2.0	-	-	V
SYNC INPUT						
SYNC Minimum LOW Threshold			-	-	0.8	V
SYNC Maximum HIGH Threshold			2.0	-	-	V

Electrical Specifications These specifications apply for recommended ambient temperature, unless otherwise noted. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Minimum SYNC Pulse			-	-	40	ns
Synchronization Delay			-	50	-	ns
Interleaving Mode Phase Shift		SYNC = 5V, PWM = 300kHz, 10% Width	-	180	-	°
Synchronization Mode Phase Shift		SYNC = 0V, PWM = 300kHz, 10% Width	-	0	-	°
PWM INPUT						
Sinking Impedance	R_{PWM_SNK}		-	8.5	-	kΩ
Source Impedance	R_{PWM_SRC}		-	10	-	kΩ
Tri-State Rising Threshold		V_{VCC} = V_{PVCC} = 5V (250mV Hysteresis)	1.00	1.20	1.40	V
Tri-State Falling Threshold		V_{VCC} = V_{PVCC} = 5V (300mV Hysteresis)	3.10	3.40	3.70	V
PWM Pulled High Threshold		EN_PH = LOW, Ramping PWM low	-	3.4	-	V
SWITCHING TIME (Note 6, See Figure 1 on Page 9)						
UGATE Rise Time	t_{RU}	3nF Load	-	8.0	-	ns
LGATE Rise Time	t_{RL}	3nF Load	-	8.0	-	ns
UGATE Fall Time	t_{FU}	3nF Load	-	8.0	-	ns
LGATE Fall Time	t_{FL}	3nF Load	-	4.0	-	ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	Unloaded, Excluding Balance Extension	-	40	-	ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	Unloaded, Excluding Balance Extension	-	40	-	ns
UGATE Turn-On Propagation Delay	t_{PDHU}	Outputs Unloaded	-	25	-	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	Outputs Unloaded	-	20	-	ns
Tri-state to UG/LG Rising Propagation Delay	t_{PTS}	Outputs Unloaded	-	25	-	ns
Tri-State Shutdown Holdoff Time	t_{TSSHD}	Excluding Propagation Delay (t_{PDLU}, t_{PDLL})	-	25	-	ns
OUTPUT (Note 6)						
Upper Drive Source Resistance	R_{UG_SRC}	50mA Source Current	-	1.0	-	Ω
Upper Drive Sink Resistance	R_{UG_SNK}	50mA Sink Current	-	1.0	-	Ω
Lower Drive Source Resistance	R_{LG_SRC}	50mA Source Current	-	1.0	-	Ω
Lower Drive Sink Resistance	R_{LG_SNK}	50mA Sink Current	-	0.4	-	Ω

NOTE:

6. Limits established by characterization and are not production tested.

Timing Diagram

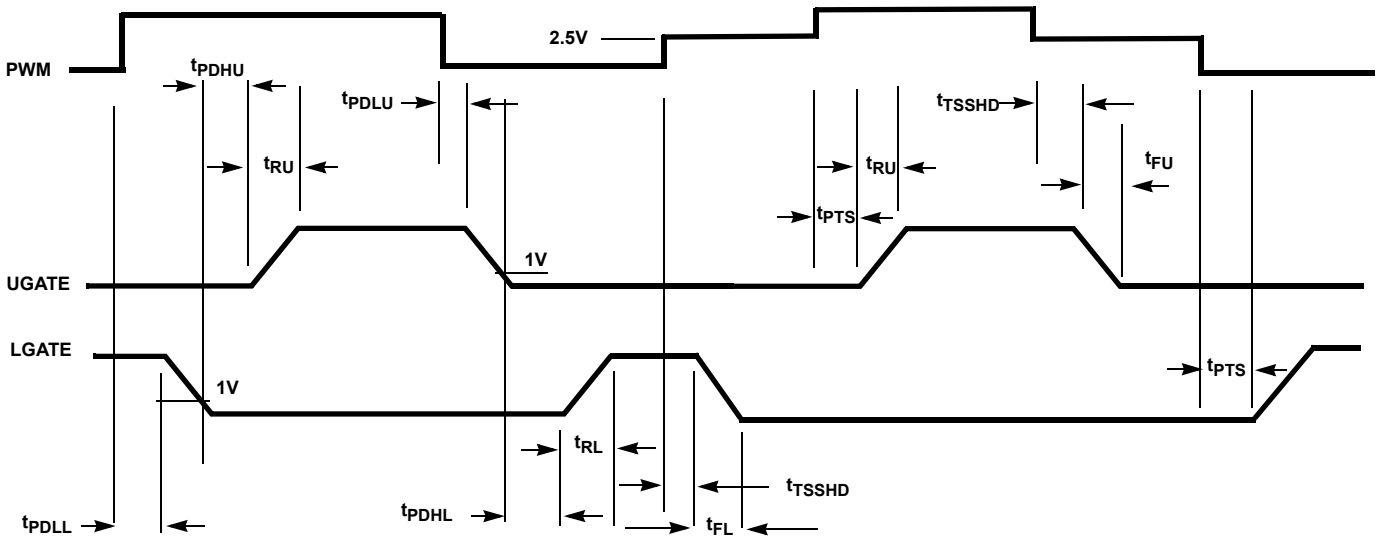


FIGURE 1. TIMING DIAGRAM

Operation and Adaptive Shoot-Through Protection

Designed for high speed switching, the ISL6611A MOSFET driver controls two-phase power trains' high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see Figure 1). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the "Electrical Specifications" on page 8. Adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time [t_{PDHU}] after the LGATE voltage drops below ~1V. The upper gate drive then begins to rise [t_{RU}] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. The upper gate begins to fall [t_{FU}] after a propagation delay [t_{PDLU}], which is modulated by the current balance circuits. The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET a short delay time, t_{PDHL}, after the upper MOSFET's gate voltage drops below 1V. The lower gate then rises [t_{RL}], turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

This driver is optimized for voltage regulators with large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.4Ω ON-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor (C_{GD}) of the lower MOSFET and help prevent shoot through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

Tri-State PWM Input

A unique feature of the ISL6611A is the adaptable tri-state PWM input. Once the PWM signal enters the shutdown window, either MOSFET previously conducting is turned off. If the PWM signal remains within the shutdown window for longer than 25ns of the previously conducting MOSFET, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. The PWM Tri-state rising and falling thresholds outlined in the "Electrical Specifications" on page 8 determine when the lower and upper gates are enabled. During normal operation in a typical application, the PWM rise and fall times through the shutdown window should not exceed either output's turn-off propagation delay plus the MOSFET gate discharge time to ~1V. Abnormally long PWM signal transition times through the shutdown window will simply introduce additional dead time between turn off and turn on of the synchronous bridge's MOSFETs. For optimal performance, no more than 100pF parasitic capacitive load should be present on the PWM line of ISL6611A (assuming an Intersil PWM controller is used).

Bootstrap Considerations

This driver features an internal bootstrap diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The ISL6611A's internal bootstrap resistor is designed to reduce the overcharging of the bootstrap capacitor when exposed to excessively large negative voltage swing at the PHASE node. Typically, such

large negative excursions occur in high current applications that use D^2-PAK and D-PAK MOSFETs or excessive layout parasitic inductance. Equation 1 helps select a proper bootstrap capacitor size:

$$C_{BOOT_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT_CAP}} \quad \text{(EQ. 1)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet PVCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

As an example, suppose two HAT2168 FETs are chosen as the upper MOSFETs. The gate charge, Q_G, from the data sheet is 12nC at 5V (V_{GS}) gate-source voltage. Then the Q_{GATE} is calculated to be 26.4nC at 5.5V PVCC level. We will assume a 100mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.264µF is required. The next larger standard value capacitance is 0.33µF. A good quality ceramic capacitor is recommended.

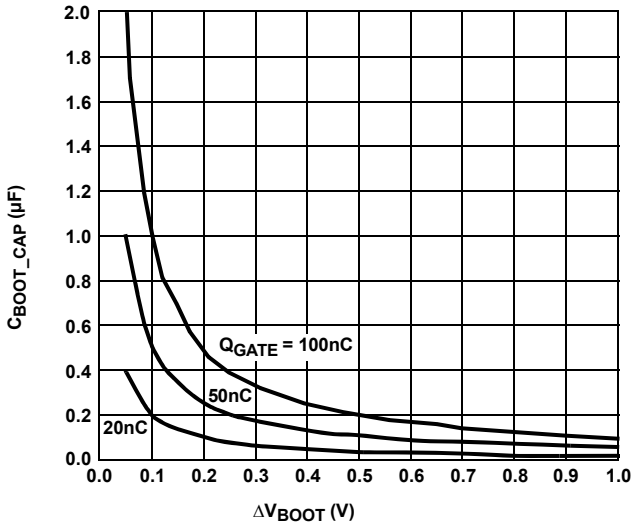


FIGURE 2. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the 4x4 QFN package, with an exposed heat escape pad, is around 2W. See "Layout Considerations" on page 12 for thermal transfer improvement suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with Equations 2 and 3, respectively,

$$P_{Qg_TOT} = 2 \bullet (P_{Qg_Q1} + P_{Qg_Q2}) + I_Q \bullet VCC \quad \text{(EQ. 2)}$$

$$P_{Qg_Q1} = \frac{Q_{G1} \bullet PVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg_Q2} = \frac{Q_{G2} \bullet PVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$I_{DR} = 2 \bullet \left(\frac{Q_{G1} \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet N_{Q2}}{V_{GS2}} \right) \bullet F_{SW} + I_Q \quad \text{(EQ. 3)}$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage ($V_{GS1}$and V_{GS2}) in the corresponding MOSFET datasheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively. The factor 2 is the number of active channels. The I_Q V_{CC} product is the quiescent power of the driver without capacitive load.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}, should be a short to avoid interfering with the operation shoot-through protection circuitry) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 3 and 4 show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated as Equation 4:

$$P_{DR} = 2 \bullet (P_{DR_UP} + P_{DR_LOW}) + I_Q \bullet VCC \quad \text{(EQ. 4)}$$

$$P_{DR_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}} \right) \bullet \frac{P_{Qg_Q1}}{2}$$

$$P_{DR_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}} \right) \bullet \frac{P_{Qg_Q2}}{2}$$

$$R_{EXT2} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

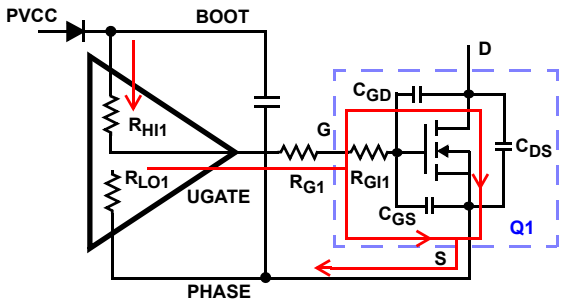


FIGURE 3. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

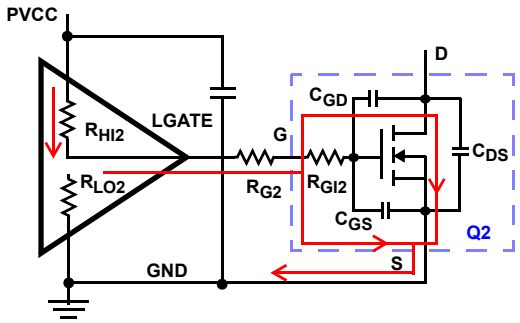


FIGURE 4. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

EN_PH Operation

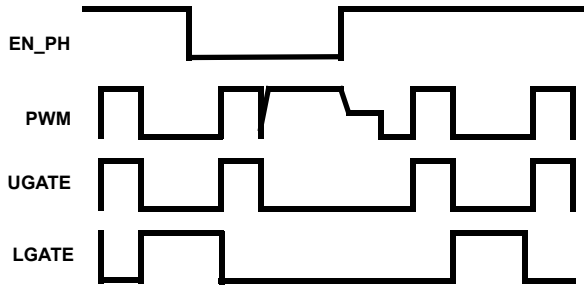


FIGURE 5. TYPICAL EN_PH OPERATION TIMING DIAGRAM

The ISL6611A disables the phase doubler operation when the EN_PH pin is pulled to ground and after it sees the PWM falling edge. The PWM pin is pulled to VCC at the PWM falling edge. With the PWM line pulled high, the controller will disable the corresponding phase and the higher number phases. When the EN_PH is pulled high, the phase doubler will pull the PWM line to tri-state and then will be enabled at the leading edge of PWM input. Prior to a leading edge of PWM, if the PWM is low, both LGATEA and LGATEB remain in tri-state unless the corresponding phase node (PHASEA, PHASEB) is higher than 80% of VCC. This provides additional protection if the doubler is enabled while the high-side MOSFET is shorted. However, this feature limits the
pre-charged output voltage to less than 80% of VCC. Note that the first doubler should always tie its EN_PH pin high since Intersil controllers do not allow PWM1 pulled high and this channel should remain ON to protect the system from an overvoltage event even when the controller is disabled.

SYNC Operation

The ISL6611A can be set to interleaving mode or synchronous mode by pulling the SYNC pin to GND or VCC, respectively. A synchronous pulse can be sent to the phase doubler during the load application to improve the voltage droop and current balance while it still can maintain interleaving operation at DC load conditions. However, an excessive ringback can occur; hence, the synchronous mode operation could have drawbacks. Figure 6 shows how to generate a synchronous pulse only when an transient load is applied. The comparator should be a fast comparator with a minimum delay.

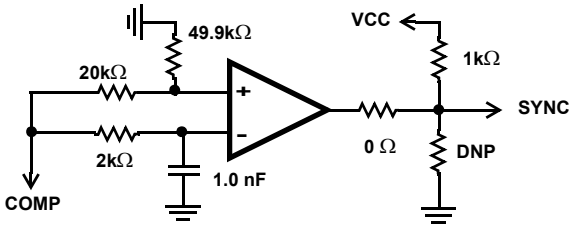


FIGURE 6. TYPICAL SYNC PULSE GENERATOR

Current Balance and Maximum Frequency

The ISL6611A utilizes $r_{DS(ON)}$ sensing technique to balance both channels, while the sample and hold circuits refer to GND pin. The phase current sensing resistors are integrated, while the current gain can be scaled by the impedance on the IGAIN pin, as shown in Table 1. In most applications, the default option should just work fine.

TABLE 1. CURRENT GAIN SELECTION

IMPEDANCE TO GND	CURRENT GAIN
OPEN	DEFAULT
0Ω	DEFAULT/2
49.9kΩ	DEFAULT/5

In addition to balancing the effective UGATE pulse width of phase A and phase B via standard $r_{DS(ON)}$ current sensing technique, a fast path is also added to swap both channels' firing order when one phase carries much higher current than the other phase. This improves the current balance between phase A and phase B during high frequency load transient events.

Each phase starts to sample current 200ns (t_{BLANK}) after LGATE falls and lasts for 400ns (t_{SAMP}) or ends at the rising edge of PWM if the available sampling time (t_{AVSAMP}) is < 400ns. The available sampling time (t_{AVSAMP}) depends upon the blanking time (t_{BLANK}), the duty cycle (D), the rising and falling time of low-side gate drive (t_{LR}, t_{LF}), the total propagation delay ($t_{PD} = t_{PDLL} + t_{PDLU}$), and the switching frequency (F_{SW}). As the switching frequency and the duty cycle increase, the available sampling time could be < 400ns. For a good current balance, it is recommended to keep at least

200ns sampling time, if not the full 400ns. Equations 5 and 6 show the maximum frequency of each channel in interleaving mode and synchronous mode, respectively. Assume 80ns each for t_{PD}, t_{LR}, t_{LF} and 200ns each for t_{AVSAMP}, t_{BLANK}, the maximum channel frequency can be set to no more than 500kHz at interleaving mode and 1MHz at synchronous mode, respectively, for an application with a maximum duty cycle of 20%. The maximum duty cycle occurs at the maximum output voltage (overvoltage trip level as needed) and at the minimum input voltage (undervoltage trip level as needed). The efficiency of the voltage regulator is also a factor in the theoretical approximation. Figure 7 shows the relationship between the maximum channel frequency and the maximum duty cycle in the previous assumed conditions.

For interleaving mode (SYNC = “0”),

$$F_{SW}(MAX) \approx \frac{1 - 2 \cdot D(MAX)}{(t_{AVSAMP} + t_{PD} + t_{LR} + t_{LF} + t_{BLANK}) \cdot 2} \quad \text{(EQ. 5)}$$

$$D(MAX) \approx \frac{VOUT(MAX)}{VIN(MIN) \cdot \eta}$$

For synchronous mode (SYNC = “1”),

$$F_{SW}(MAX) \approx \frac{1 - D(MAX)}{(t_{AVSAMP} + t_{PD} + t_{LR} + t_{LF} + t_{BLANK})} \quad \text{(EQ. 6)}$$

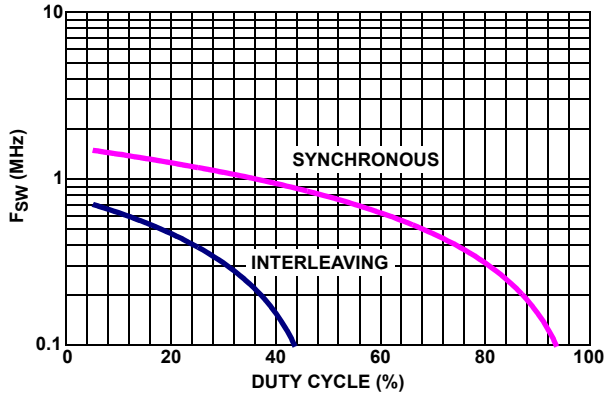


FIGURE 7. MAXIMUM CHANNEL SWITCHING FREQUENCY vs MAXIMUM DUTY CYCLE IN ASSUMED CONDITIONS

Note that the PWM controller should be set to 2 x F_{SW} for interleaving mode and the same switching frequency for the synchronous mode.

Application Information

MOSFET and Driver Selection

The parasitic inductances of the PCB and of the power devices’ packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding absolute maximum rating of the devices. The negative ringing at the edges of the PHASE node could increase the bootstrap capacitor voltage through the internal bootstrap diode, and in some cases, it may overstress the upper MOSFET driver. Careful layout, proper selection of MOSFETs and packaging, as well as the proper driver can go a long way toward minimizing such unwanted stress.

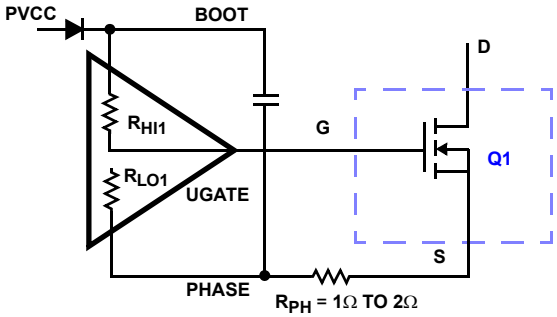


FIGURE 8. PHASE RESISTOR TO MINIMIZE SERIOUS NEGATIVE PHASE SPIKE IF NEEDED

The selection of D^2-PAK, or D-PAK packaged MOSFETs, is a much better match (for the reasons discussed) for the ISL6611A with a phase resistor (R_{PH}), as shown in Figure 8. Low-profile MOSFETs, such as Direct FETs and multi-source leads devices (SO-8, LFPAK, PowerPAK), have low parasitic lead inductances and can be driven by ISL6611A (assuming proper layout design) without the phase resistor (R_{PH}).

Layout Considerations

A good layout helps reduce the ringing on the switching node (PHASE) and significantly lower the stress applied to the output drives. The following advice is meant to lead to an optimized layout and performance:

- Keep decoupling loops (VCC-GND, PVCC-PGND and BOOT-PHASE) short and wide, at least 25 mils. Avoid using vias on decoupling components other than their ground terminals, which should be on a copper plane with at least two vias.
- Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, PGND, PVCC, VCC, GND) should be short and wide, at least 25 mils. Try to place power traces on a single layer, otherwise, two vias on interconnection are preferred where possible. For no connection (NC) pins on the QFN part,

connect it to the adjacent net (LGATE2/PHASE2) can reduce trace inductance.

- Shorten all gate drive loops (UGATE-PHASE and LGATE-PGND) and route them closely spaced.
- Minimize the inductance of the PHASE node. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.
- Avoid routing relatively high impedance nodes (such as PWM and ENABLE lines) close to high dV/dt UGATE and PHASE nodes.

In addition, connecting the thermal pad of the QFN package to the power ground through multiple vias, or placing a low noise copper plane (such as power ground) underneath the SOIC part is recommended. This is to improve heat dissipation and allow the part to achieve its full thermal potential.

Upper MOSFET Self Turn-On Effects At Start-up

Should the driver have insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, due to the self-coupling via the internal C_{GD} of the MOSFET, the UGATE could momentarily rise up to a level greater than the threshold voltage of the MOSFET. This could potentially turn on the upper switch and result in damaging in-rush energy. Therefore, if such a situation (when input bus powered up before the bias of the controller and driver is ready) could conceivably be encountered, it is common practice to place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the C_{GD}/C_{GS} ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower C_{DS}/C_{GS} ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated 20kΩ typically sufficient, not affecting normal performance and efficiency.

The coupling effect can be roughly estimated with the equations in Equation 7, which assume a fixed linear input ramp and neglect the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. These equations are provided for guidance purposes only. Thus, the actual coupling effect should be examined using a very high impedance (10MΩ or greater) probe to ensure a safe design margin.

$$V_{GS_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \quad \text{(EQ. 7)}$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

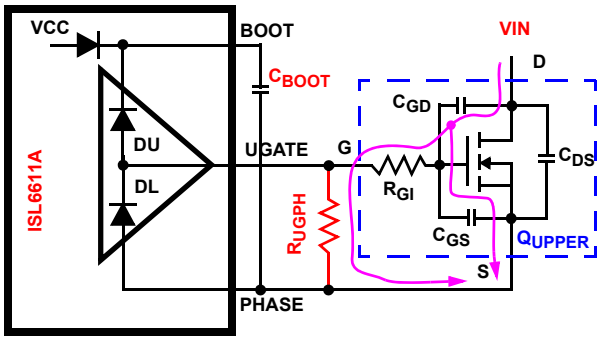


FIGURE 9. GATE TO SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

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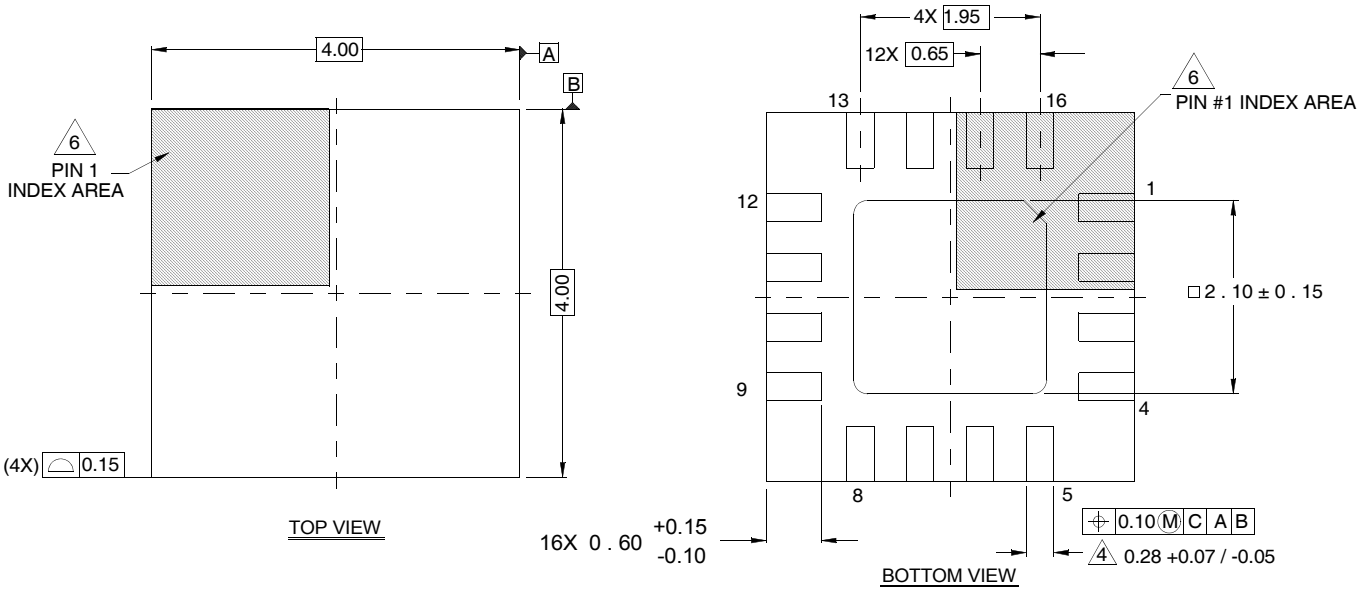
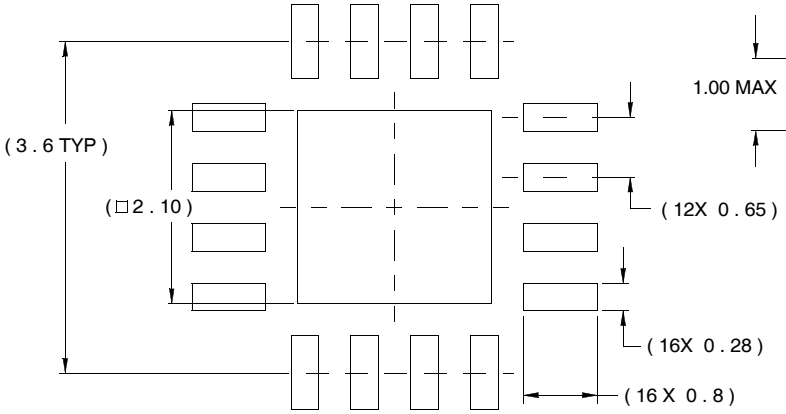
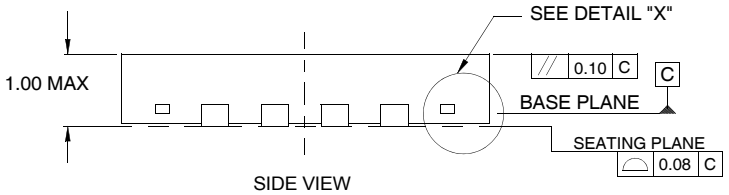
Package Outline Drawing

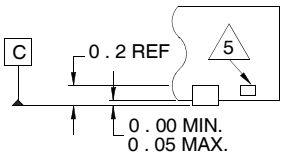
L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 6, 02/08









NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
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moschip.ru_9