A Microchip Technology Company

# 2 Mbit / 4 Mbit / 8 Mbit (x16) Multi-Purpose Flash

## SST39LF200A / SST39LF400A / SST39LF800A
## SST39VF200A / SST39VF400A / SST39VF800A

***Data Sheet***

*The SST39LF200A/400A/800A and SST39VF200A/400A/800A devices are 128K x16 / 256K x16 / 512K x16 CMOS Multi-Purpose Flash (MPF) manufactured with SST proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39LF200A/400A/800A write (Program or Erase) with a 3.0-3.6V power supply. The SST39VF200A/400A/800A write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pinouts for x16 memories.*

## Features:

- **Organized as 128K x16 / 256K x16 / 512K x16**
- **Single Voltage Read and Write Operations**
  - 3.0-3.6V for SST39LF200A/400A/800A
  - 2.7-3.6V for SST39VF200A/400A/800A
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption (typical values at 14 MHz)**
  - Active Current: 9 mA (typical)
  - Standby Current: 3 µA (typical)
- **Sector-Erase Capability**
  - Uniform 2 KWord sectors
- **Block-Erase Capability**
  - Uniform 32 KWord blocks
- **Fast Read Access Time**
  - 55 ns for SST39LF200A/400A/800A
  - 70 ns for SST39VF200A/400A/800A
- **Latched Address and Data**
- **Fast Erase and Word-Program**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Word-Program Time: 14 µs (typical)
  - Chip Rewrite Time:
    2 seconds (typical) for SST39LF/VF200A
    4 seconds (typical) for SST39LF/VF400A
    8 seconds (typical) for SST39LF/VF800A
- **Automatic Write Timing**
  - Internal $V_{PP}$ Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 48-lead TSOP (12mm x 20mm)
  - 48-ball TFBGA (6mm x 8mm)
  - 48-ball WFBGA (4mm x 6mm)
  - 48-bump XFLGA (4mm x 6mm) – 4 and 8Mbit
- **All non-Pb (lead-free) devices are RoHS compliant**

# Product Description

The SST39LF200A/400A/800A and SST39VF200A/400A/800A devices are 128K x16 / 256K x16 / 512K x16 CMOS Multi-Purpose Flash (MPF) manufactured with SST proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39LF200A/400A/800A write (Program or Erase) with a 3.0-3.6V power supply. The SST39VF200A/400A/800A write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pinouts for x16 memories.

Featuring high-performance Word-Program, the SST39LF200A/400A/800A and SST39VF200A/400A/800A devices provide a typical Word-Program time of 14 µsec. The devices use Toggle Bit or Data# Polling to detect the completion of the Program or Erase operation. To protect against inadvertent write, they have on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

The SST39LF200A/400A/800A and SST39VF200A/400A/800A devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during Erase and Program than alternative flash technologies. When programming a flash device, the total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet surface mount requirements, the SST39LF200A/400A/800A and SST39VF200A/400A/800A are offered in 48-lead TSOP packages and 48-ball TFBGA packages as well as Micro-Packages. See Figures 2, 3, and 4 for pin assignments.

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## Block Diagram

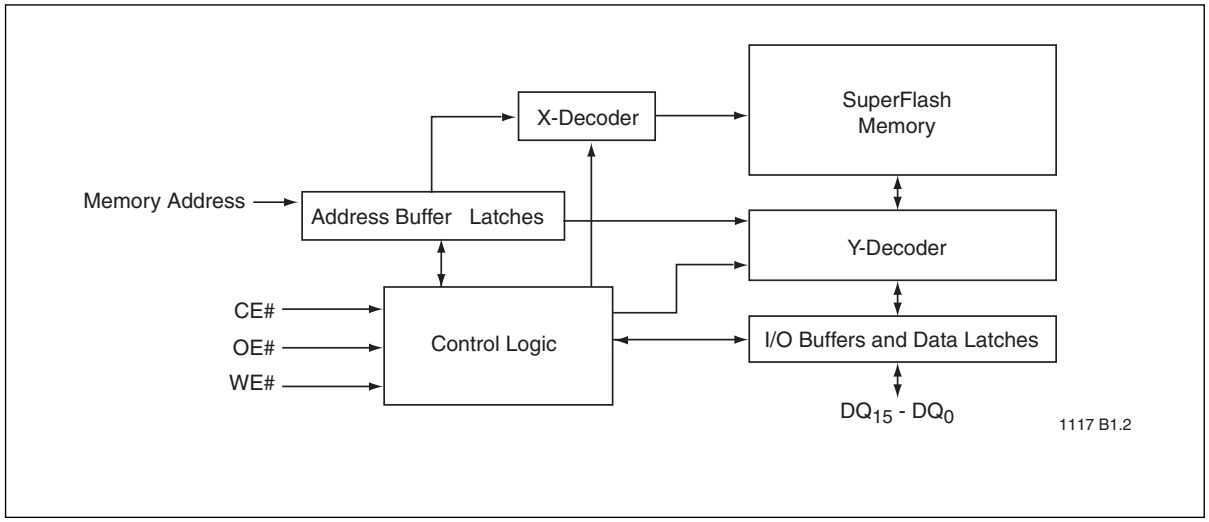


**Figure 1:** Functional Block Diagram

## Pin Assignments

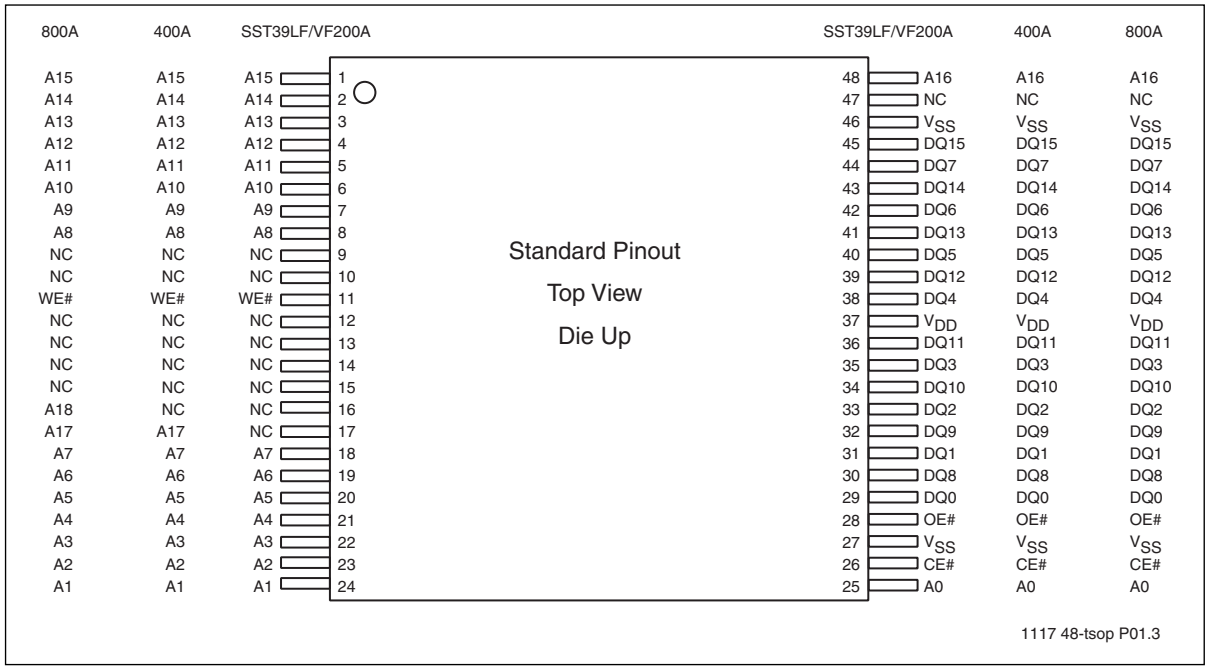


**Figure 2:** Pin Assignments for 48-Lead TSOP

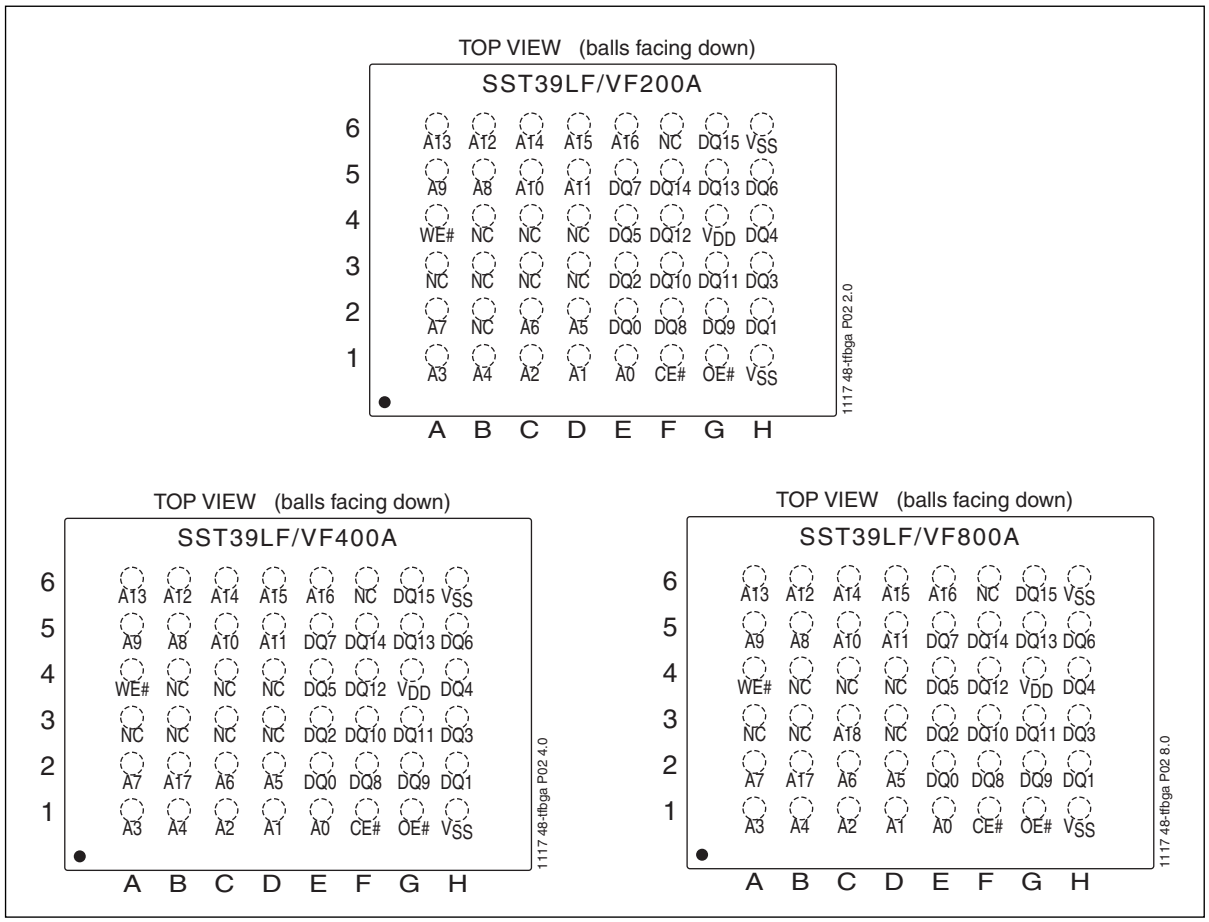


**Figure 3:** Pin Assignments for 48-Ball TFBGA

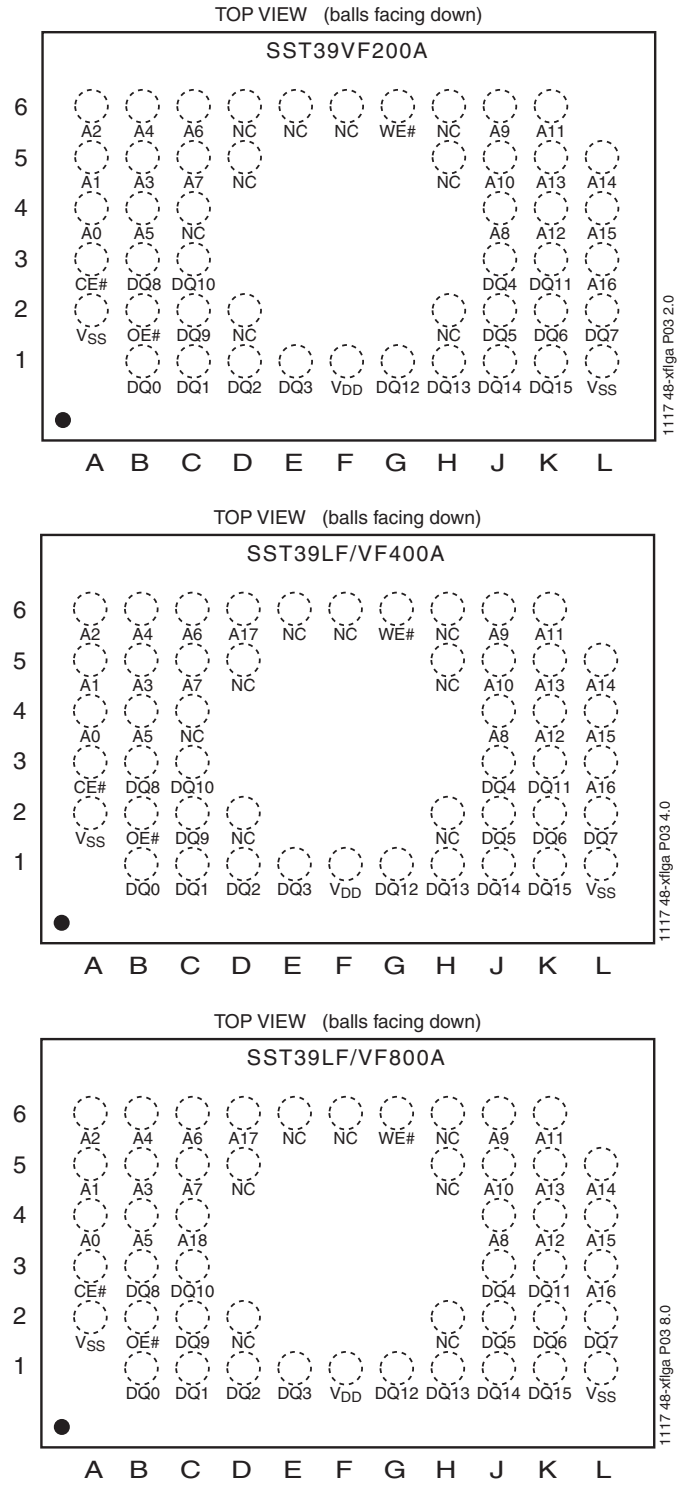


**Figure 4:** Pin Assignments for 48-Ball WFBGA and 48-Bump XFLGA

**Table 1:** Pin Description

| Symbol | Pin Name | Functions |
|---|---|---|
| $A_{MS}$[1]-$A_0$ | Address Inputs | To provide memory addresses. During Sector-Erase $A_{MS}$-$A_{11}$ address lines will select the sector. During Block-Erase $A_{MS}$-$A_{15}$ address lines will select the block. |
| $DQ_{15}$-$DQ_0$ | Data Input/output | To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high. |
| CE# | Chip Enable | To activate the device when CE# is low. |
| OE# | Output Enable | To gate the data output buffers. |
| WE# | Write Enable | To control the Write operations. |
| $V_{DD}$ | Power Supply | To provide power supply voltage: 3.0-3.6V for SST39LF200A/400A/800A<br>2.7-3.6V for SST39VF200A/400A/800A |
| $V_{SS}$ | Ground | |
| NC | No Connection | Unconnected pins. |

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1. $A_{MS}$ = Most significant address
   $A_{MS}$ = $A_{16}$ for SST39LF/VF200A, $A_{17}$ for SST39LF/VF400A, and $A_{18}$ for SST39LF/VF800A

# Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

## Read

The Read operation of the SST39LF200A/400A/800A and SST39VF200A/400A/800A is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 5).

## Word-Program Operation

The SST39LF200A/400A/800A and SST39VF200A/400A/800A are programmed on a word-by-word basis. Before programming, the sector where the word exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load word address and word data. During the Word-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 20 µs. See Figures 6 and 7 for WE# and CE# controlled Program operation timing diagrams and Figure 18 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored.

## Sector/Block-Erase Operation

The Sector- (or Block-) Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST39LF200A/400A/800A and SST39VF200A/400A/800A offers both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 2 KWord. The Block-Erase mode is based on uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figures 11 and 12 for timing waveforms. Any commands issued during the Sector- or Block-Erase operation are ignored.

## Chip-Erase Operation

The SST39LF200A/400A/800A and SST39VF200A/400A/800A provide a Chip-Erase operation, which allows the user to erase the entire memory array to the “1” state. This is useful when the entire device must be quickly erased.

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The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 10 for timing diagram, and Figure 21 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

## Write Operation Status Detection

The SST39LF200A/400A/800A and SST39VF200A/400A/800A provide two software means to detect the completion of a write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling ($DQ_7$) and Toggle Bit ($DQ_6$). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either $DQ_7$ or $DQ_6$. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

## Data# Polling ($DQ_7$)

When the SST39LF200A/400A/800A and SST39VF200A/400A/800A are in the internal Program operation, any attempt to read $DQ_7$ will produce the complement of the true data. Once the Program operation is completed, $DQ_7$ will produce true data. Note that even though $DQ_7$ may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read $DQ_7$ will produce a ‘0’. Once the internal Erase operation is completed, $DQ_7$ will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Data# Polling timing diagram and Figure 19 for a flowchart.

## Toggle Bit ($DQ_6$)

During the internal Program or Erase operation, any consecutive attempts to read $DQ_6$ will produce alternating 1s and 0s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the $DQ_6$ bit will stop toggling. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 9 for Toggle Bit timing diagram and Figure 19 for a flowchart.

## Data Protection

The SST39LF200A/400A/800A and SST39VF200A/400A/800A provide both hardware and software features to protect nonvolatile data from inadvertent writes.

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## Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

$V_{DD}$ Power Up/Down Detection: The Write operation is inhibited when $V_{DD}$ is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

## Software Data Protection (SDP)

The SST39LF200A/400A/800A and SST39VF200A/400A/800A provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. This group of devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within TRC. The contents of $DQ_{15}$-$DQ_8$ can be $V_{IL}$ or $V_{IH}$, but no other value, during any SDP command sequence.

## Common Flash Memory Interface (CFI)

The SST39LF200A/400A/800A and SST39VF200A/400A/800A also contain the CFI information to describe the characteristics of the device. In order to enter the CFI Query mode, the system must write three-byte sequence, same as Software ID Entry command with 98H (CFI Query command) to address 5555H in the last byte sequence. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 5 through 9. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

## Product Identification

The Product Identification mode identifies the devices as the SST39LF/VF200A, SST39LF/VF400A and SST39LF/VF800A and manufacturer as SST. This mode may be accessed by software operations. Users may use the Software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 4 for software operation, Figure 13 for the Software ID Entry and Read timing diagram, and Figure 20 for the Software ID Entry command sequence flowchart.

**Table 2:** Product Identification

| | Address | Data |
|---|---|---|
| Manufacturer's ID | 0000H | 00BFH |
| Device ID | | |
| SST39LF/VF200A | 0001H | 2789H |
| SST39LF/VF400A | 0001H | 2780H |
| SST39LF/VF800A | 0001H | 2781H |

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### Product Identification Mode Exit/CFI Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 15 for timing waveform, and Figure 20 for a flowchart.

## Operations

**Table 3:** Operation Modes Selection

| Mode | CE# | OE# | WE# | DQ | Address |
|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | $A_{IN}$ |
| Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $D_{IN}$ | $A_{IN}$ |
| Erase | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X[1] | Sector or Block address, XXH for Chip-Erase |
| Standby | $V_{IH}$ | X | X | High Z | X |
| Write Inhibit | X | $V_{IL}$ | X | High Z/ $D_{OUT}$ | X |
| | X | X | $V_{IH}$ | High Z/ $D_{OUT}$ | X |
| Product Identification | | | | | |
| Software Mode | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | | See Table 4 |

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1. X can be $V_{IL}$ or $V_{IH}$, but no other value.

**Table 4:** Software Command Sequence

| Command Sequence | 1st Bus Write Cycle | | 2nd Bus Write Cycle | | 3rd Bus Write Cycle | | 4th Bus Write Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Addr 1 | Data 2 | Addr[1] | Data 2 | Addr 1 | Data 2 | Addr 1 | Data 2 | Addr[1] | Data 2 | Addr 1 | Data 2 |
| Word-Program | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | WA[3] | Data | | | | |
| Sector-Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | $SA_X$[4] | 30H |
| Block-Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | $BA_X$[4] | 50H |
| Chip-Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| Software ID Entry[5,6] | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | | | | | | |
| CFI Query Entry[5] | 5555H | AAH | 2AAAH | 55H | 5555H | 98H | | | | | | |
| Software ID Exit[7]/ CFI Exit | XXH | F0H | | | | | | | | | | |
| Software ID Exit[7]/ CFI Exit | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | | | | | | |

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1. Address format $A_{14}$-$A_0$ (Hex), Addresses $A_{MS}$-$A_{15}$ can be $V_{IL}$ or $V_{IH}$, but no other value, for the Command sequence.
   $A_{MS}$ = Most significant address
   $A_{MS}$ = $A_{16}$ for SST39LF/VF200A, $A_{17}$ for SST39LF/VF400A, and $A_{18}$ for SST39LF/VF800A
2. $DQ_{15}$-$DQ_8$ can be $V_{IL}$ or $V_{IH}$, but no other value, for the Command sequence
3. WA = Program word address

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4. $SA_X$ for Sector-Erase; uses $A_{MS}$-$A_{11}$ address lines
   $BA_X$ for Block-Erase; uses $A_{MS}$-$A_{15}$ address lines
5. The device does not remain in Software Product ID mode if powered down.
6. With $A_{MS}$-$A_1$ = 0; SST Manufacturer's ID = 00BFH, is read with $A_0$ = 0,
   SST39LF/VF200A Device ID = 2789H, is read with $A_0$ = 1.
   SST39LF/VF400A Device ID = 2780H, is read with $A_0$ = 1.
   SST39LF/VF800A Device ID = 2781H, is read with $A_0$ = 1.
7. Both Software ID Exit operations are equivalent

**Table 5:** CFI Query Identification String[1] for SST39LF200A/400A/800A and SST39VF200A/400A/800A

| Address | Data | Data |
|---|---|---|
| 10H | 0051H | Query Unique ASCII string "QRY" |
| 11H | 0052H | |
| 12H | 0059H | |
| 13H | 0001H | Primary OEM command set |
| 14H | 0007H | |
| 15H | 0000H | Address for Primary Extended Table |
| 16H | 0000H | |
| 17H | 0000H | Alternate OEM command set (00H = none exists) |
| 18H | 0000H | |
| 19H | 0000H | Address for Alternate OEM extended Table (00H = none exits) |
| 1AH | 0000H | |

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1. Refer to CFI publication 100 for more details.

**Table 6:** System Interface Information for SST39LF200A/400A/800A and SST39VF200A/400A/800A

| Address | Data | Data |
|---|---|---|
| 1BH | 0027H[1] | $V_{DD}$ Min (Program/Erase) |
| | 0030H[1] | $DQ_7$-$DQ_4$: Volts, $DQ_3$-$DQ_0$: 100 millivolts |
| 1CH | 0036H | $V_{DD}$ Max (Program/Erase)<br>$DQ_7$-$DQ_4$: Volts, $DQ_3$-$DQ_0$: 100 millivolts |
| 1DH | 0000H | $V_{PP}$ min (00H = no $V_{PP}$ pin) |
| 1EH | 0000H | $V_{PP}$ max (00H = no $V_{PP}$ pin) |
| 1FH | 0004H | Typical time out for Word-Program $2^N$ µs ($2^4$ = 16 µs) |
| 20H | 0000H | Typical time out for min size buffer program $2^N$ µs (00H = not supported) |
| 21H | 0004H | Typical time out for individual Sector/Block-Erase $2^N$ ms ($2^4$ = 16 ms) |
| 22H | 0006H | Typical time out for Chip-Erase $2^N$ ms ($2^6$ = 64 ms) |
| 23H | 0001H | Maximum time out for Word-Program $2^N$ times typical ($2^1$ x $2^4$ = 32 µs) |
| 24H | 0000H | Maximum time out for buffer program $2^N$ times typical |
| 25H | 0001H | Maximum time out for individual Sector/Block-Erase $2^N$ times typical ($2^1$ x $2^4$ = 32 ms) |
| 26H | 0001H | Maximum time out for Chip-Erase $2^N$ times typical ($2^1$ x $2^6$ = 128 ms) |

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1. 0030H for SST39LF200A/400A/800A and 0027H for SST39VF200A/400A/800A

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**Table 7:** Device Geometry Information for SST39LF/VF200A

| Address | Data | Data |
|---|---|---|
| 27H | 0012H | Device size = $2^N$ Byte (12H = 18; $2^{18}$ = 256 KByte) |
| 28H | 0001H | Flash Device Interface description; 0001H = x16-only asynchronous interface |
| 29H | 0000H | |
| 2AH | 0000H | Maximum number of bytes in multi-byte write = $2^N$ (00H = not supported) |
| 2BH | | |
| 2CH | 0002H | Number of Erase Sector/Block sizes supported by device |
| 2DH | 003FH | Sector Information (y + 1 = Number of sectors; z x 256B = sector size) |
| 2EH | 0000H | y = 63 + 1 = 64 sectors (003FH = 63) |
| 2FH | 0010H | |
| 30H | 0000H | z = 16 x 256 Bytes = 4 KByte/sector (0010H = 16) |
| 31H | 0003H | Block Information (y + 1 = Number of blocks; z x 256B = block size) |
| 32H | 0000H | y = 3 + 1 = 4 blocks (0003H = 3) |
| 33H | 0000H | |
| 34H | 0001H | z = 256 x 256 Bytes = 64 KByte/block (0100H = 256) |

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**Table 8:** Device Geometry Information for SST39LF/VF400A

| Address | Data | Data |
|---|---|---|
| 27H | 0013H | Device size = $2^N$ Byte (13H = 19; $2^{19}$ = 512 KByte) |
| 28H | 0001H | Flash Device Interface description; 0001H = x16-only asynchronous interface |
| 29H | 0000H | |
| 2AH | 0000H | Maximum number of bytes in multi-byte write = $2^N$ (00H = not supported) |
| 2BH | 0000H | |
| 2CH | 0002H | Number of Erase Sector/Block sizes supported by device |
| 2DH | 007FH | Sector Information (y + 1 = Number of sectors; z x 256B = sector size) |
| 2EH | 0000H | y = 127 + 1 = 128 sectors (007FH = 127) |
| 2FH | 0010H | |
| 30H | 0000H | z = 16 x 256 Bytes = 4 KByte/sector (0010H = 16) |
| 31H | 0007H | Block Information (y + 1 = Number of blocks; z x 256B = block size) |
| 32H | 0000H | y = 7 + 1 = 8 blocks (0007H = 7) |
| 33H | 0000H | |
| 34H | 0001H | z = 256 x 256 Bytes = 64 KByte/block (0100H = 256) |

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**Table 9:** Device Geometry Information for SST39LF/VF800A

| Address | Data | Data |
|---|---|---|
| 27H | 0014H | Device size = $2^N$ Bytes (14H = 20; $2^{20}$ = 1 MByte) |
| 28H | 0001H | Flash Device Interface description; 0001H = x16-only asynchronous interface |
| 29H | 0000H | |
| 2AH | 0000H | Maximum number of bytes in multi-byte write = $2^N$ (00H = not supported) |
| 2BH | 0000H | |
| 2CH | 0002H | Number of Erase Sector/Block sizes supported by device |
| 2DH | 00FFH | Sector Information (y + 1 = Number of sectors; z x 256B = sector size) |
| 2EH | 0000H | y = 255 + 1 = 256 sectors (00FFH = 255) |
| 2FH | 0010H | |
| 30H | 0000H | z = 16 x 256 Bytes = 4 KByte/sector (0010H = 16) |
| 31H | 000FH | Block Information (y + 1 = Number of blocks; z x 256B = block size) |
| 32H | 0000H | y = 15 + 1 = 16 blocks (000FH = 15) |
| 33H | 0000H | |
| 34H | 0001H | z = 256 x 256 Bytes = 64 KByte/block (0100H = 256) |

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**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to $V_{DD}$+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to $V_{DD}$+2.0V
Voltage on $A_9$ Pin to Ground Potential . . . . . -0.5V to 13.2V
Package Power Dissipation Capability ($T_A$ = 25°C) . . . . . 1.0W
Surface Mount Solder Reflow Temperature[1] . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

**Operating Range: SST39LF200A/400A/800A**

| Range | Ambient Temp | $V_{DD}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 3.0-3.6V |

T9.1 25001

**Operating Range: SST39VF200A/400A/800A**

| Range | Ambient Temp | $V_{DD}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 2.7-3.6V |
| Industrial | -40°C to +85°C | 2.7-3.6V |

T9.1 25001

**Table 10:** AC Conditions of Test[1]

| Input Rise/Fall Time | Output Load SST39LF200A/400A/800A | Output Load SST39VF200A/400A/800A |
|---|---|---|
| 5ns | $C_L$ = 30 pF | $C_L$ = 100 pF |

T10.1 25001

1. See Figures 16 and 17

**Table 11:** DC Operating Characteristics –$V_{DD}$ = 3.0-3.6V for SST39LF200A/400A/800A and 2.7-3.6V for SST39VF200A/400A/800A[1]

| Symbol | Parameter | Limits | | | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | Units | |
| $I_{DD}$ | Power Supply Current | | | | Address input=$V_{ILT}$/$V_{IHT}$, at f=1/$T_{RC}$ Min, $V_{DD}$=$V_{DD}$ Max |
| | Read[2] | | 30 | mA | CE#=$V_{IL}$, OE#=WE#=$V_{IH}$, all I/Os open |
| | Program and Erase | | 30 | mA | CE#=WE#=$V_{IL}$, OE#=$V_{IH}$ |
| $I_{SB}$ | Standby $V_{DD}$ Current | | 20 | µA | CE#=$V_{IHC}$, $V_{DD}$=$V_{DD}$ Max |
| $I_{LI}$ | Input Leakage Current | | 1 | µA | $V_{IN}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $I_{LO}$ | Output Leakage Current | | 10 | µA | $V_{OUT}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $V_{IL}$ | Input Low Voltage | | 0.8 | | $V_{DD}$=$V_{DD}$ Min |
| $V_{IH}$ | Input High Voltage | 0.7$V_{DD}$ | | V | $V_{DD}$=$V_{DD}$ Max |
| $V_{IHC}$ | Input High Voltage (CMOS) | $V_{DD}$-0.3 | | V | $V_{DD}$=$V_{DD}$ Max |
| $V_{OL}$ | Output Low Voltage | | 0.2 | V | $I_{OL}$=100 µA, $V_{DD}$=$V_{DD}$ Min |
| $V_{OH}$ | Output High Voltage | $V_{DD}$-0.2 | | V | $I_{OH}$=-100 µA, $V_{DD}$=$V_{DD}$ Min |

T11.7 25001

1. Typical conditions for the Active Current shown on page 1 are average values at 25°C (room temperature), and $V_{DD}$ = 3V for VF devices. Not 100% tested.
2. Values are for 70 ns conditions. See the ***Multi-Purpose Flash Power Rating*** application note for further information.

**Table 12:** Recommended System Power-up Timings

| Symbol | Parameter | Minimum | Units |
|---|---|---|---|
| $T_{PU-READ}$[1] | Power-up to Read Operation | 100 | µs |
| $T_{PU-WRITE}$[1] | Power-up to Program/Erase Operation | 100 | µs |

T12.0 25001

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Table 13:** Capacitance ($T_A$ = 25°C, f=1 Mhz, other pins open)

| Parameter | Description | Test Condition | Maximum |
|---|---|---|---|
| $C_{I/O}$[1] | I/O Pin Capacitance | $V_{I/O}$ = 0V | 12 pF |
| $C_{IN}$[1] | Input Capacitance | $V_{IN}$ = 0V | 6 pF |

T13.0 25001

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Table 14:** Reliability Characteristics

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|---|---|---|---|---|
| $N_{END}$[1,2] | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| $T_{DR}$[1] | Data Retention | 100 | Years | JEDEC Standard A103 |
| $I_{LTH}$[1] | Latch Up | 100 + $I_{DD}$ | mA | JEDEC Standard 78 |

T14.2 25001

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. $N_{END}$ endurance rating is qualified as a 10,000 cycle minimum for the whole device. A sector- or block-level rating would result in a higher minimum specification.

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# AC Characteristics

**Table 15:** Read Cycle Timing Parameters $V_{DD}$ = 3.0-3.6V

| Symbol | Parameter | SST39LF200A/400A/800A-55 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{RC}$ | Read Cycle Time | 55 | | ns |
| $T_{CE}$ | Chip Enable Access Time | | 55 | ns |
| $T_{AA}$ | Address Access Time | | 55 | ns |
| $T_{OE}$ | Output Enable Access Time | | 30 | ns |
| $T_{CLZ}$[1] | CE# Low to Active Output | 0 | | ns |
| $T_{OLZ}$[1] | OE# Low to Active Output | 0 | | ns |
| $T_{CHZ}$[1] | CE# High to High-Z Output | | 15 | ns |
| $T_{OHZ}$[1] | OE# High to High-Z Output | | 15 | ns |
| $T_{OH}$[1] | Output Hold from Address Change | 0 | | ns |

T15.7 25001

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Table 16:** Read Cycle Timing Parameters $V_{DD}$ = 2.7-3.6V

| Symbol | Parameter | SST39VF200A/400A/800A-70 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{RC}$ | Read Cycle Time | 70 | | ns |
| $T_{CE}$ | Chip Enable Access Time | | 70 | ns |
| $T_{AA}$ | Address Access Time | | 70 | ns |
| $T_{OE}$ | Output Enable Access Time | | 35 | ns |
| $T_{CLZ}$[1] | CE# Low to Active Output | 0 | | ns |
| $T_{OLZ}$[1] | OE# Low to Active Output | 0 | | ns |
| $T_{CHZ}$[1] | CE# High to High-Z Output | | 20 | ns |
| $T_{OHZ}$[1] | OE# High to High-Z Output | | 20 | ns |
| $T_{OH}$[1] | Output Hold from Address Change | 0 | | ns |

T16.7 25001

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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**Table 17:** Program/Erase Cycle Timing Parameters

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{BP}$ | Word-Program Time | | 20 | µs |
| $T_{AS}$ | Address Setup Time | 0 | | ns |
| $T_{AH}$ | Address Hold Time | 30 | | ns |
| $T_{CS}$ | WE# and CE# Setup Time | 0 | | ns |
| $T_{CH}$ | WE# and CE# Hold Time | 0 | | ns |
| $T_{OES}$ | OE# High Setup Time | 0 | | ns |
| $T_{OEH}$ | OE# High Hold Time | 10 | | ns |
| $T_{CP}$ | CE# Pulse Width | 40 | | ns |
| $T_{WP}$ | WE# Pulse Width | 40 | | ns |
| $T_{WPH}$[1] | WE# Pulse Width High | 30 | | ns |
| $T_{CPH}$[1] | CE# Pulse Width High | 30 | | ns |
| $T_{DS}$ | Data Setup Time | 30 | | ns |
| $T_{DH}$[1] | Data Hold Time | 0 | | ns |
| $T_{IDA}$[1] | Software ID Access and Exit Time | 150 | | ns |
| $T_{SE}$ | Sector-Erase | | 25 | ms |
| $T_{BE}$ | Block-Erase | | 25 | ms |
| $T_{SCE}$ | Chip-Erase | | 100 | ms |

T17.0 25001

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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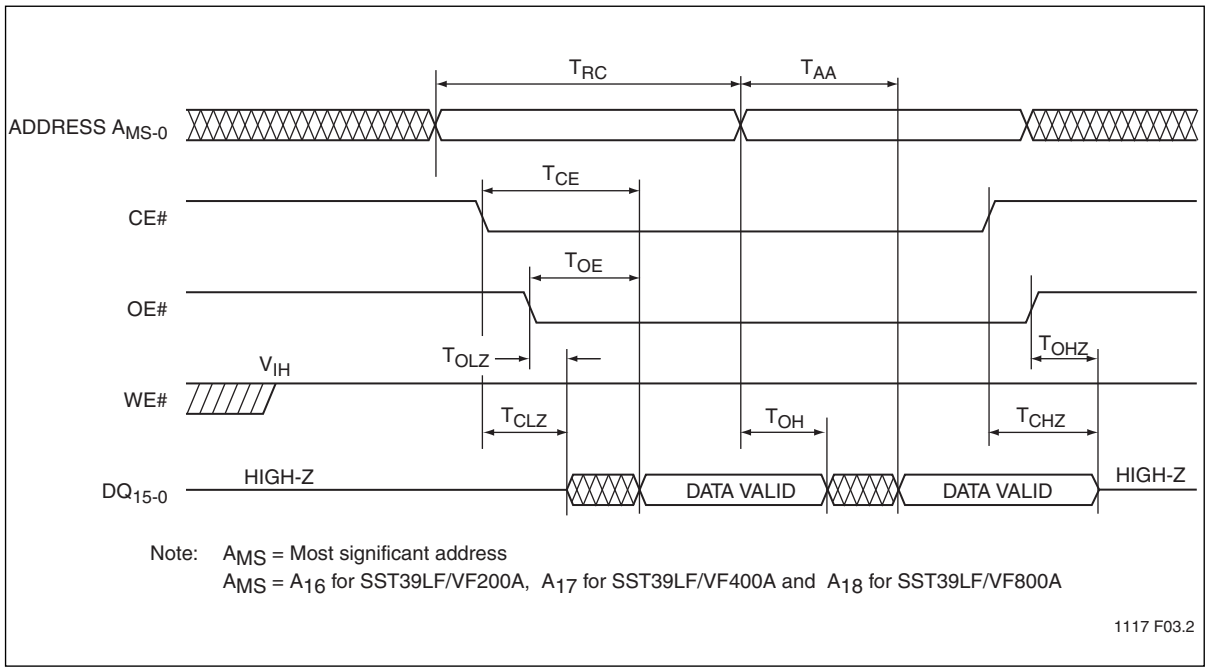



**Figure 5:** Read Cycle Timing Diagram

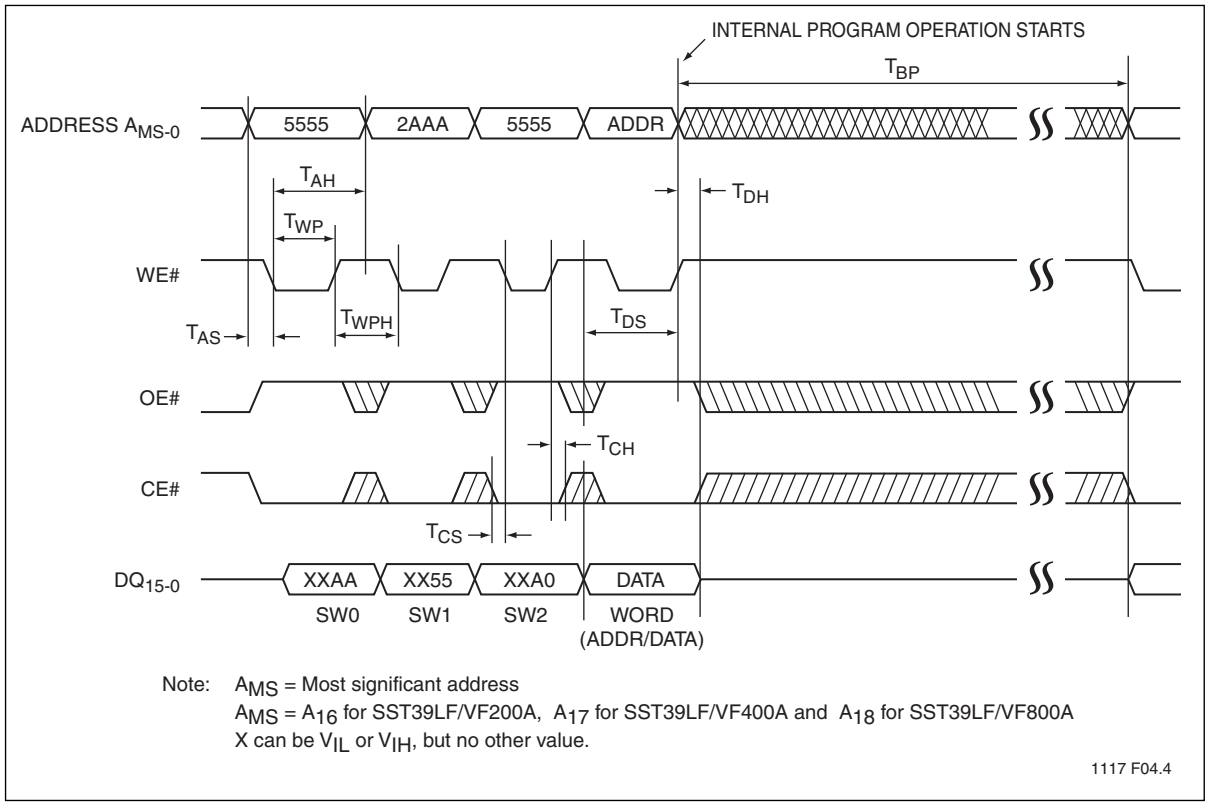



**Figure 6:** WE# Controlled Program Cycle Timing Diagram

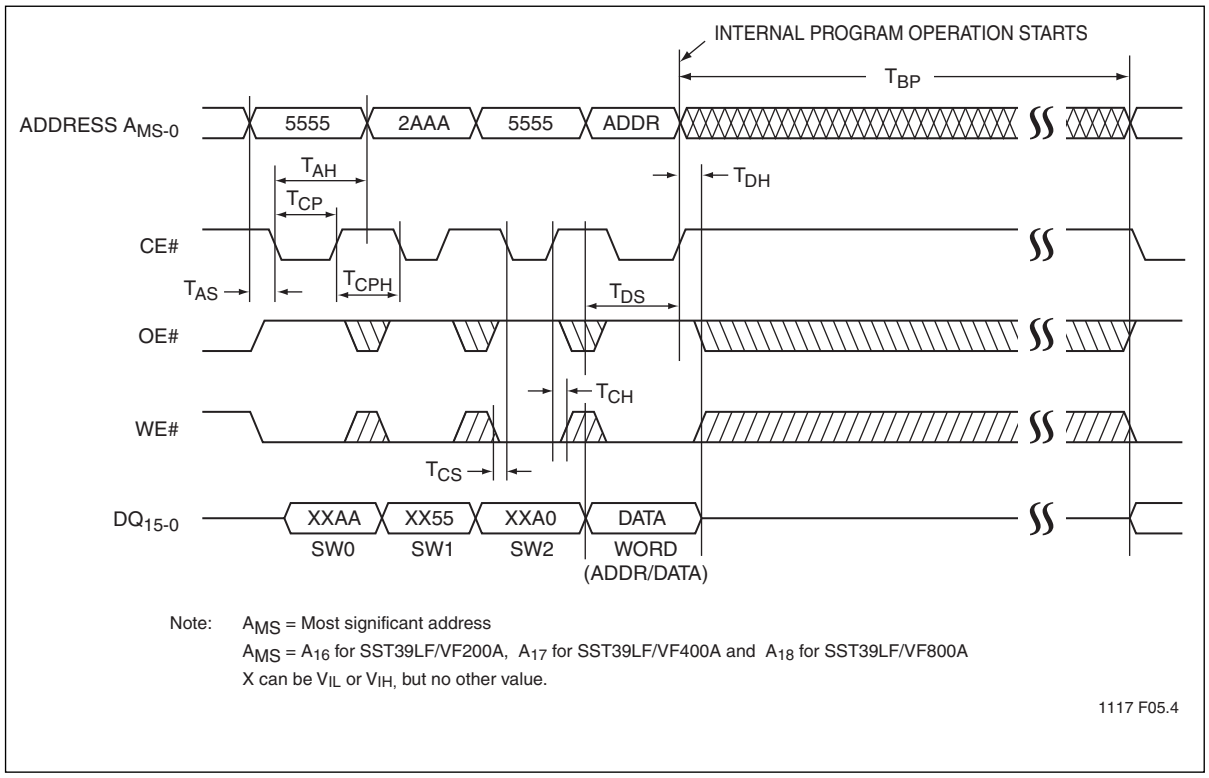



**Figure 7:** CE# Controlled Program Cycle Timing Diagram

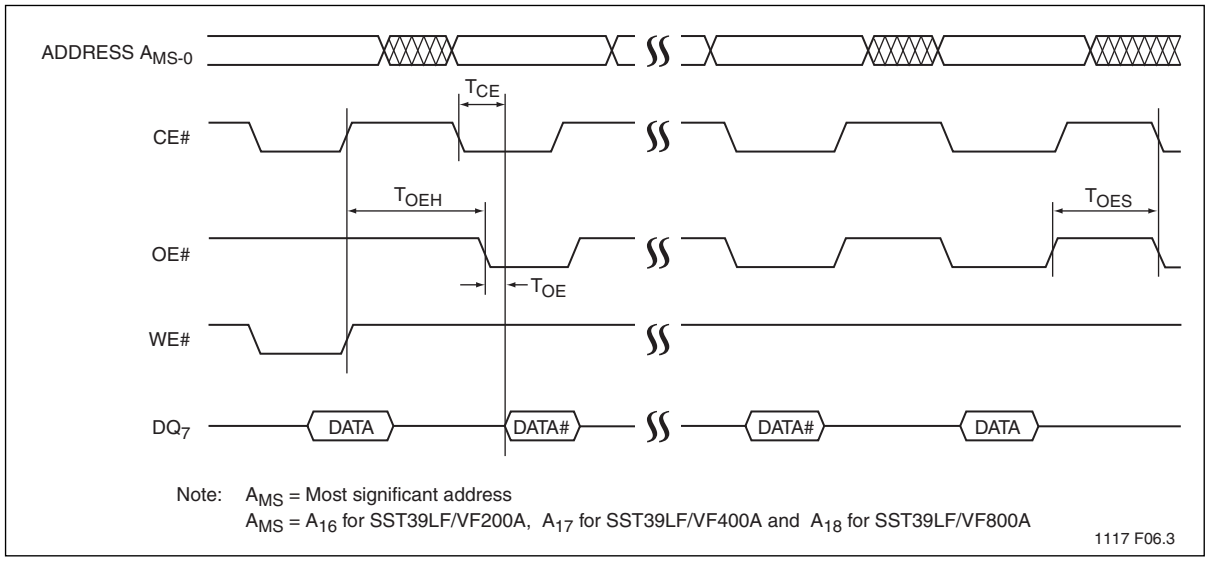
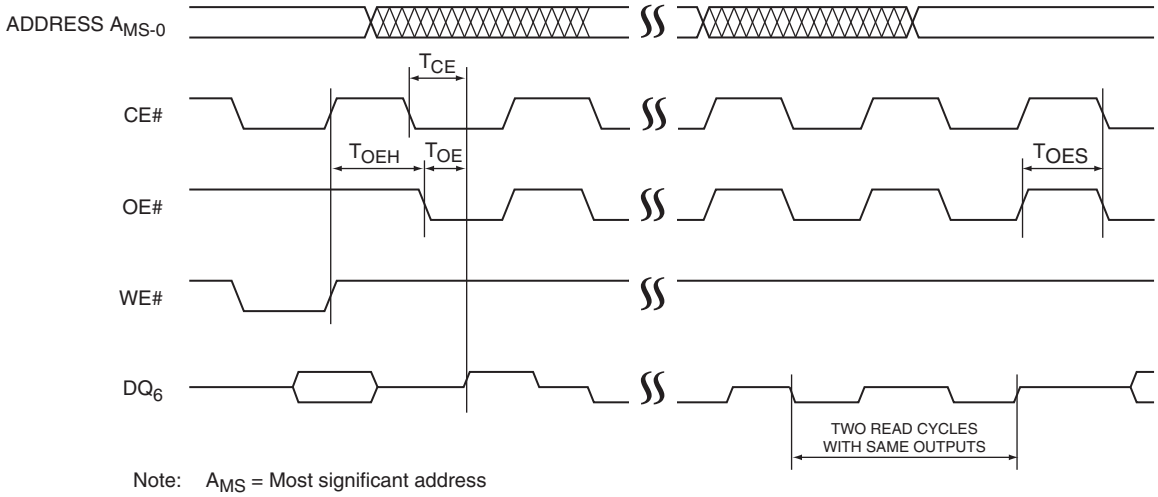


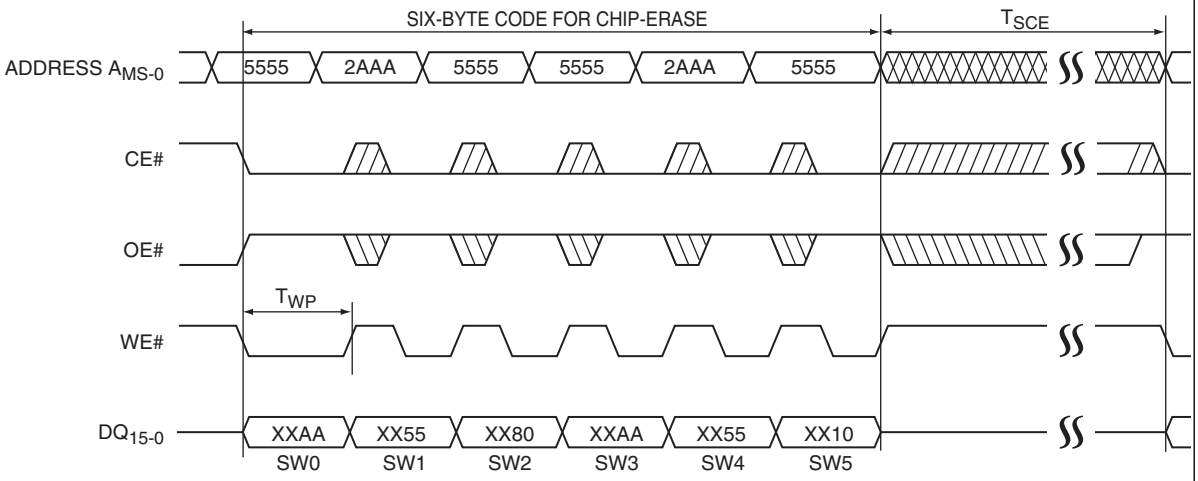

**Figure 8:** Data# Polling Timing Diagram




Note: $A_{MS}$ = Most significant address
$A_{MS} = A_{16}$ for SST39LF/VF200A, $A_{17}$ for SST39LF/VF400A and $A_{18}$ for SST39LF/VF800A

1117 F07.3

**Figure 9:** Toggle Bit Timing Diagram




Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 16)

$A_{MS}$ = Most significant address
$A_{MS} = A_{16}$ for SST39LF/VF200A, $A_{17}$ for SST39LF/VF400A and $A_{18}$ for SST39LF/VF800A
X can be $V_{IL}$ or $V_{IH}$, but no other value.

1117 F08.7

**Figure 10:** WE# Controlled Chip-Erase Timing Diagram

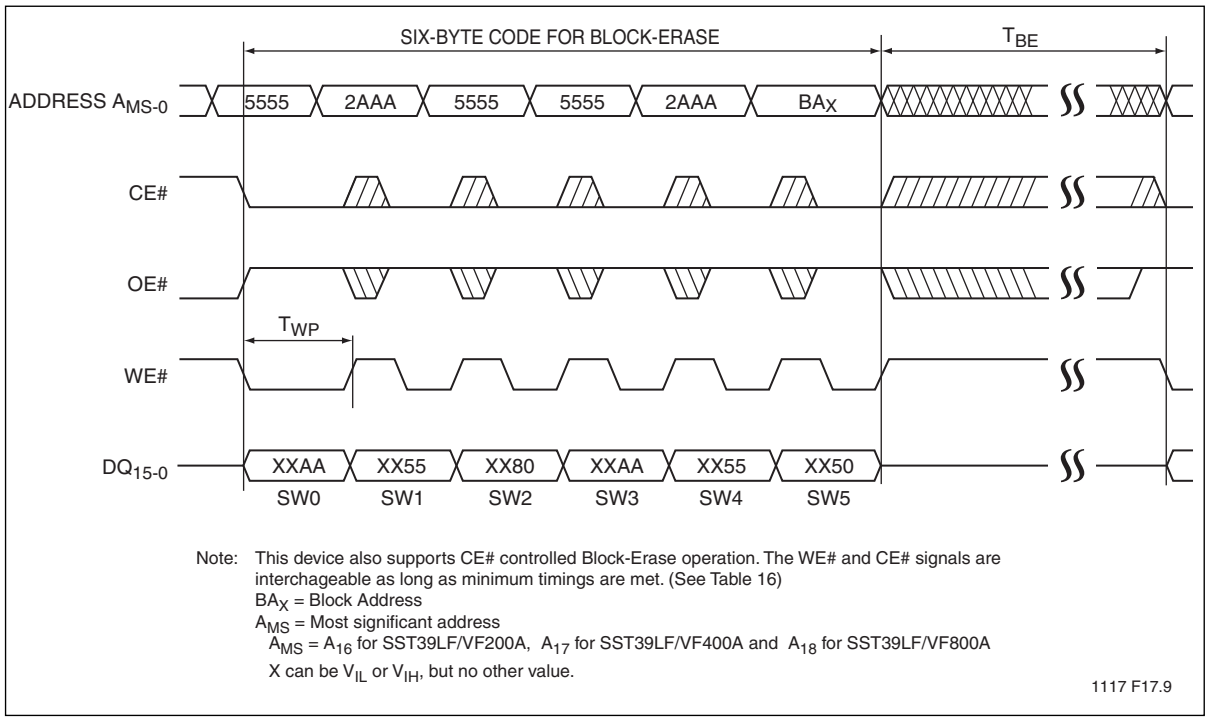



**Figure 11:** WE# Controlled Block-Erase Timing Diagram

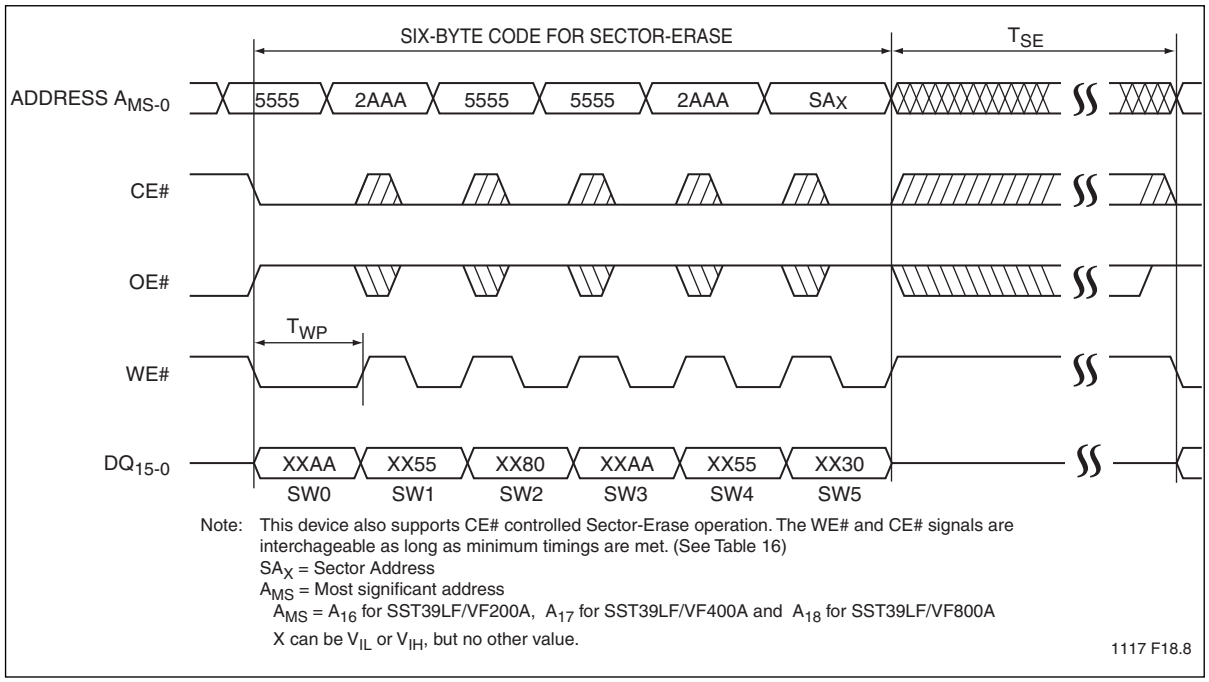



**Figure 12:** WE# Controlled Sector-Erase Timing Diagram

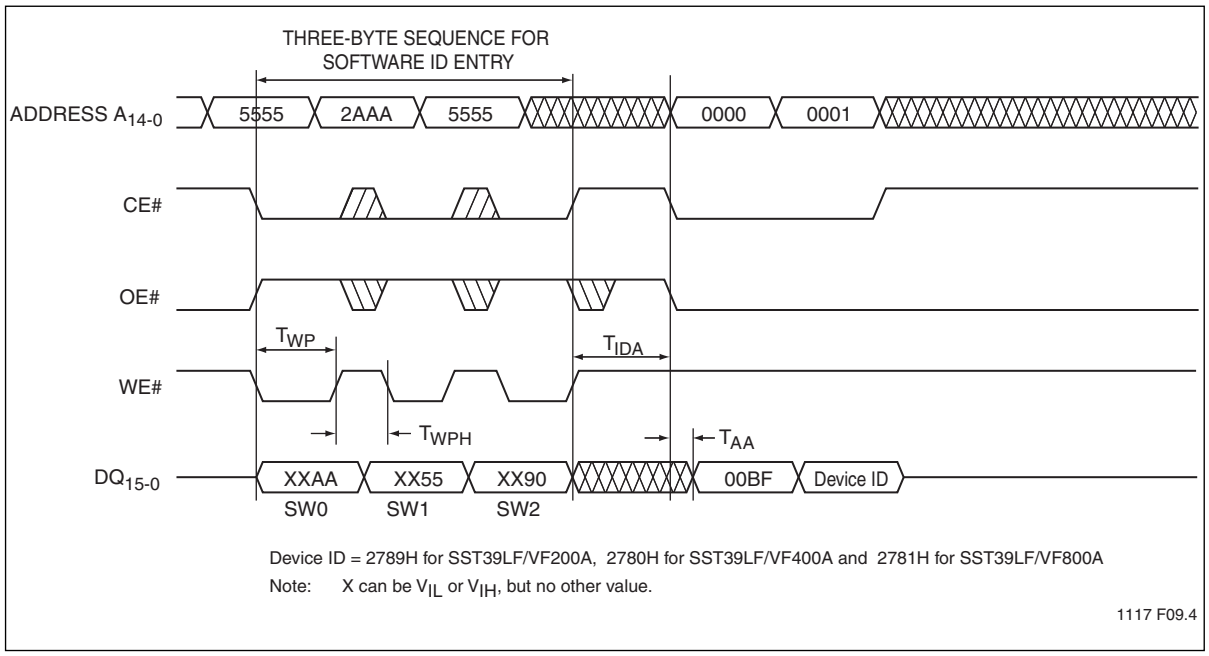



**Figure 13:** Software ID Entry and Read

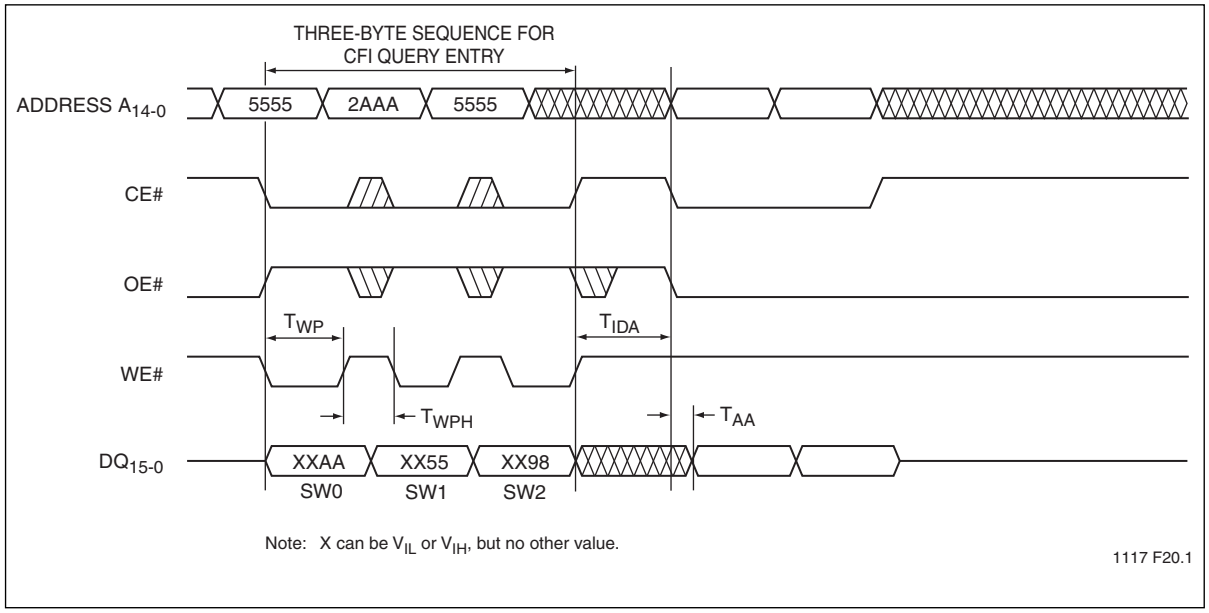



**Figure 14:** CFI Query Entry and Read

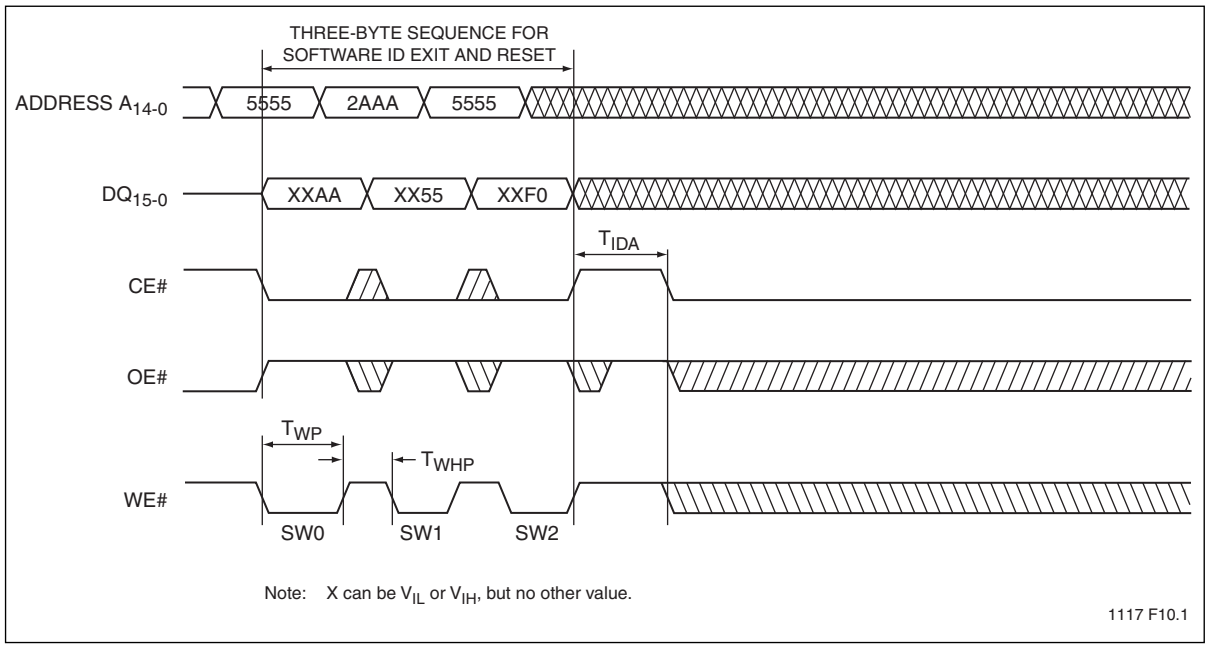
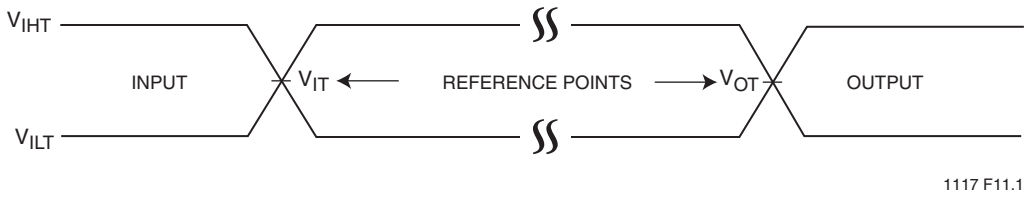



**Figure 15:** Software ID Exit/CFI Exit




AC test inputs are driven at $V_{IHT}$ (0.9 $V_{DD}$) for a logic "1" and $V_{ILT}$ (0.1 $V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are $V_{IT}$ (0.5 $V_{DD}$) and $V_{OT}$ (0.5 $V_{DD}$). Input rise and fall times (10% ↔ 90%) are <5 ns.

**Note:** $V_{IT}$ - $V_{INPUT}$ Test
$V_{OT}$ - $V_{OUTPUT}$ Test
$V_{IHT}$ - $V_{INPUT}$ HIGH Test
$V_{ILT}$ - $V_{INPUT}$ LOW Test

**Figure 16:** AC Input/Output Reference Waveforms

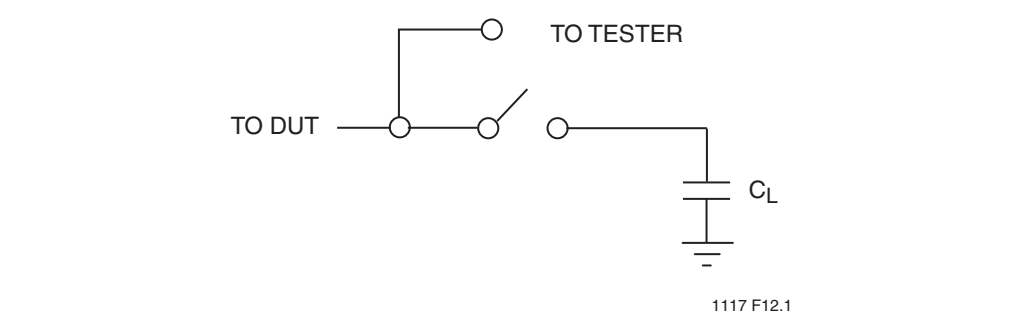



**Figure 17:** A Test Load Example

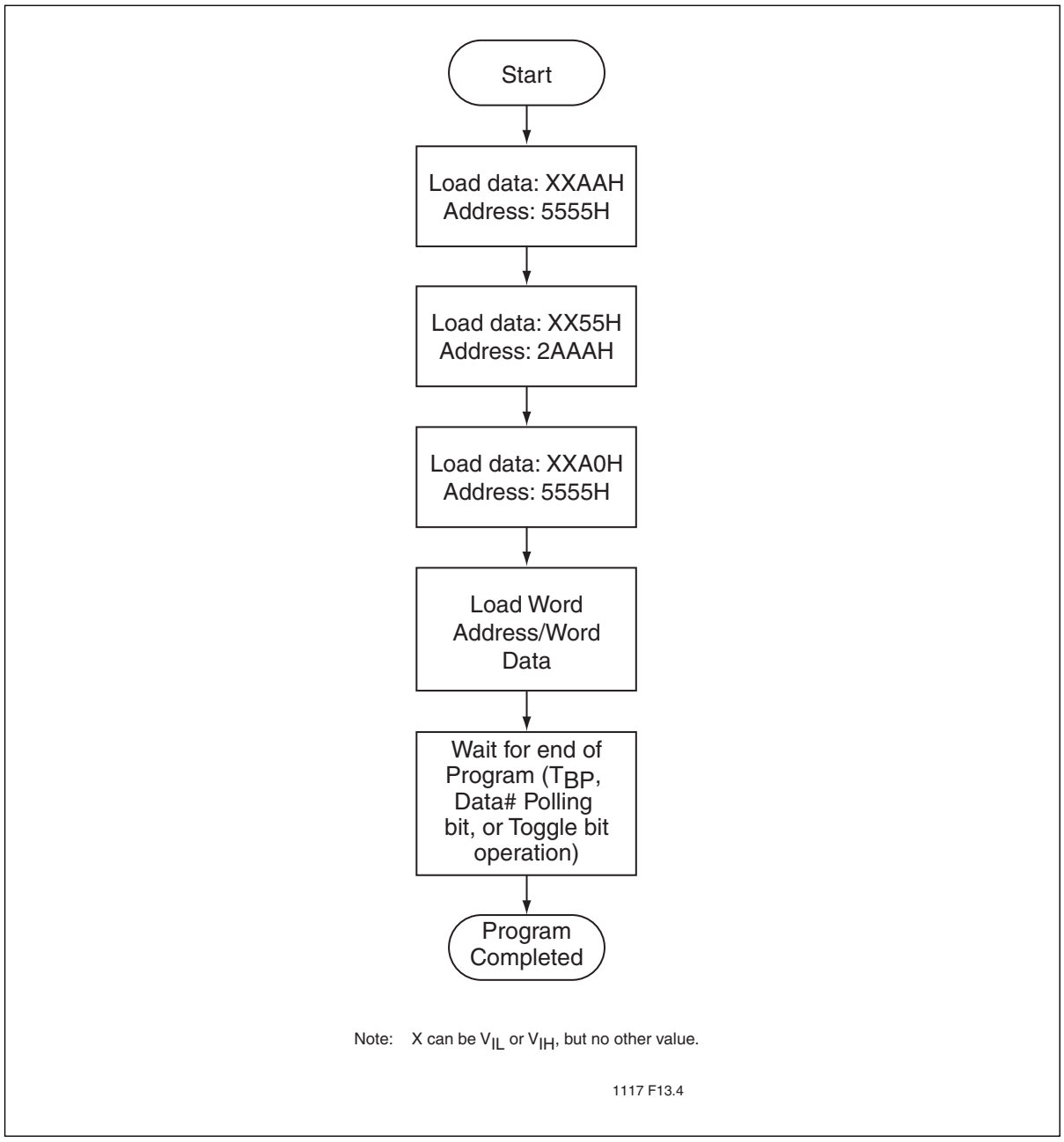



**Figure 18:** Word-Program Algorithm

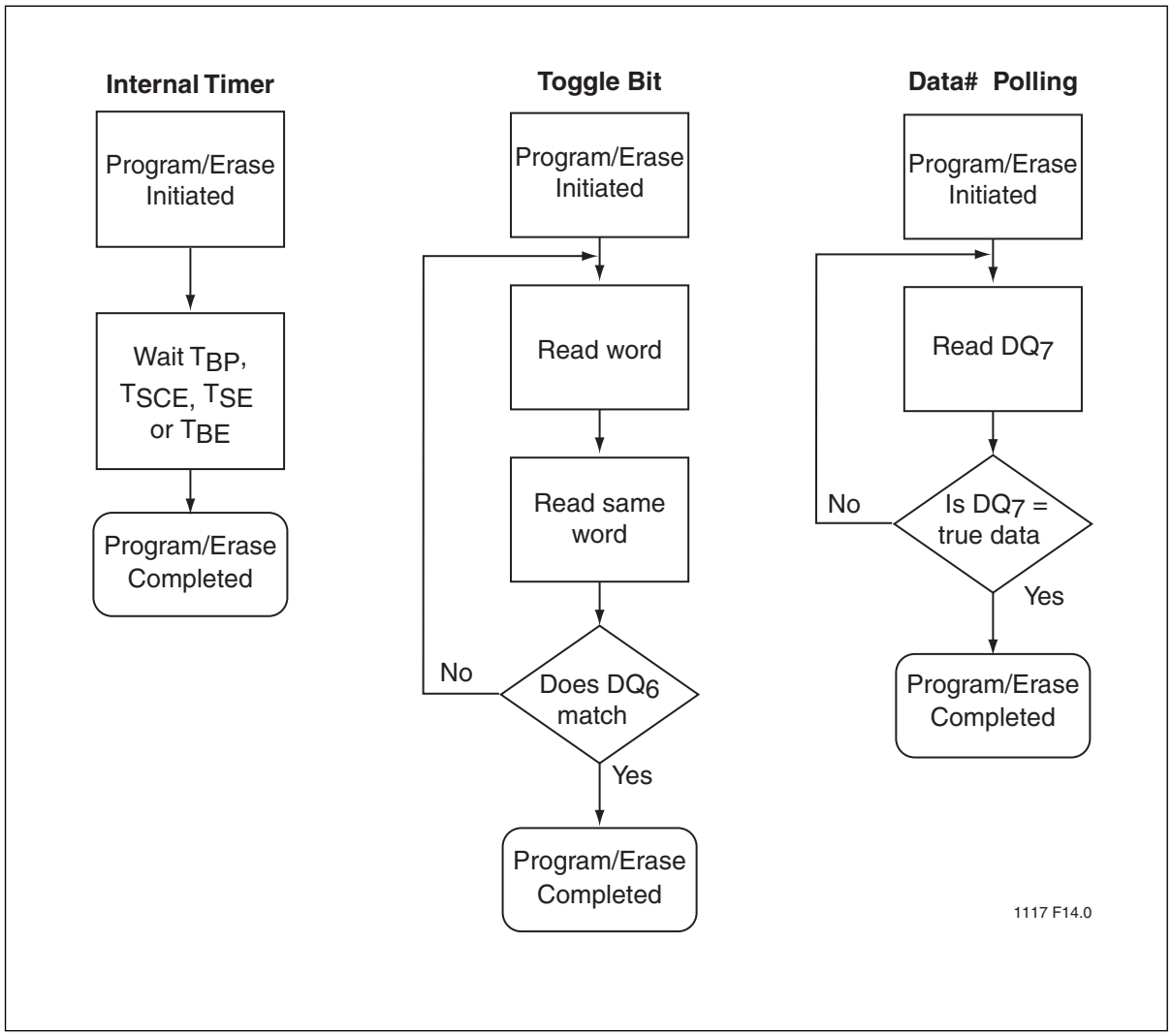



**Figure 19:** Wait Options

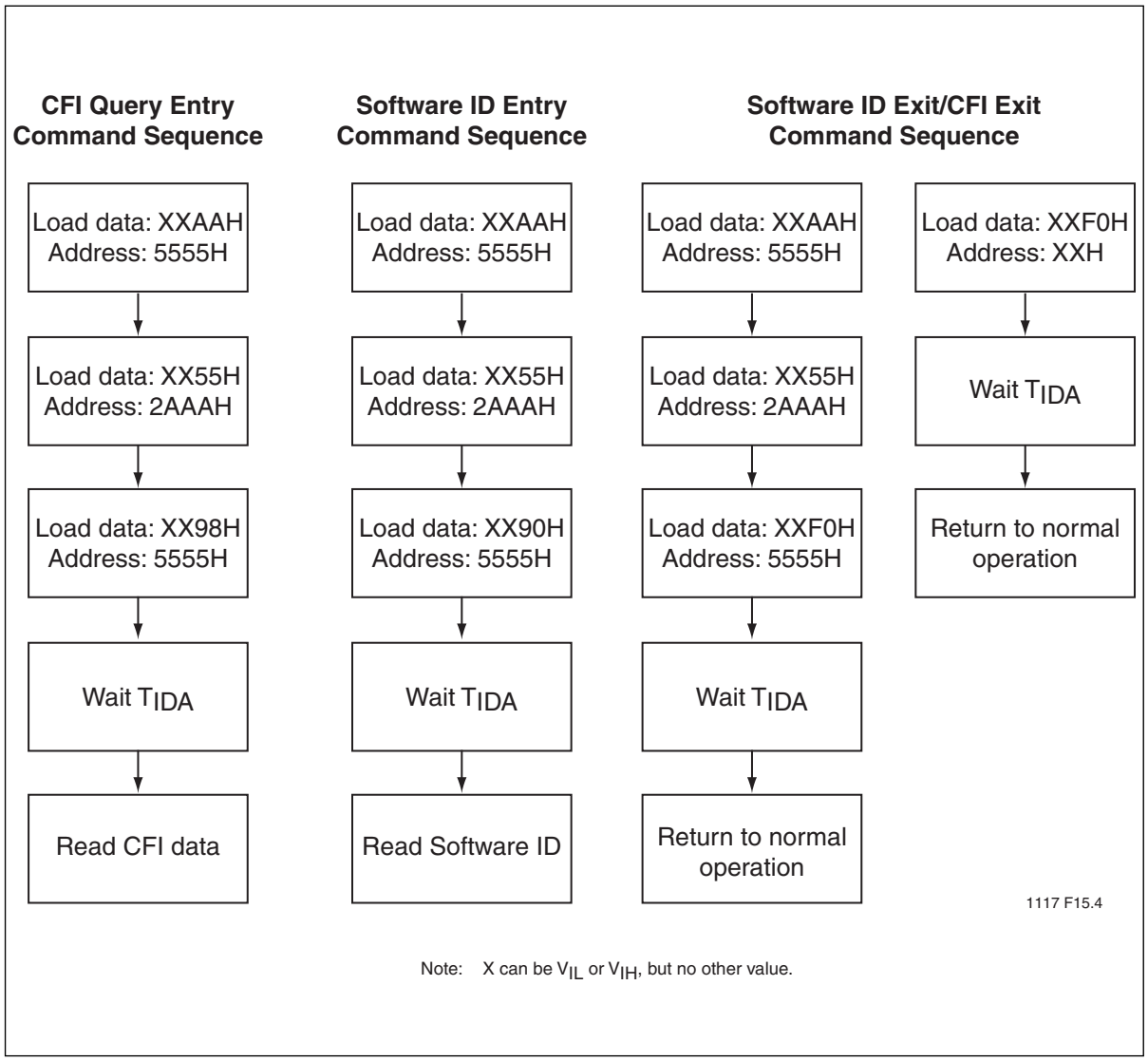



**Figure 20:** Software ID/CFI Command Flowcharts

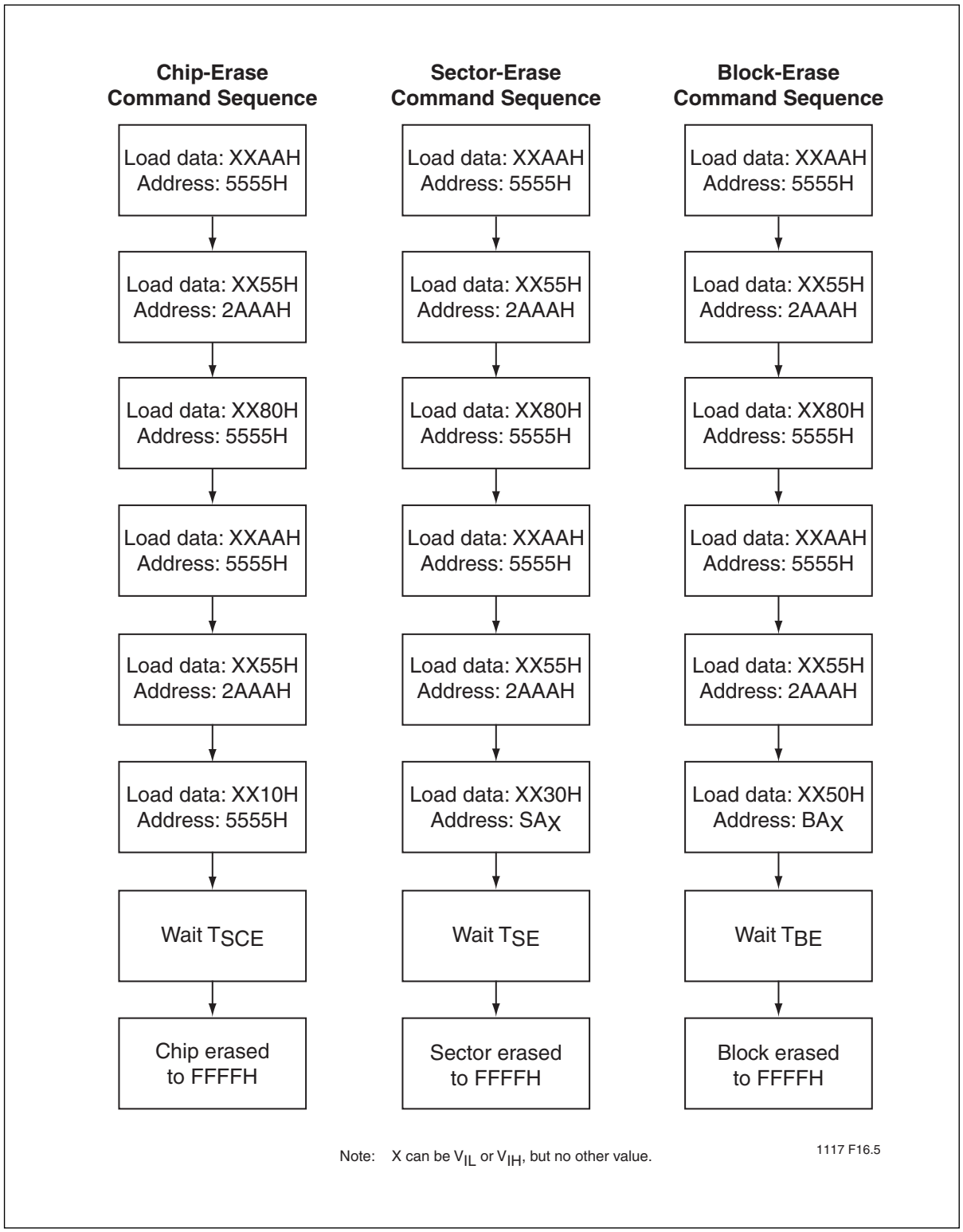
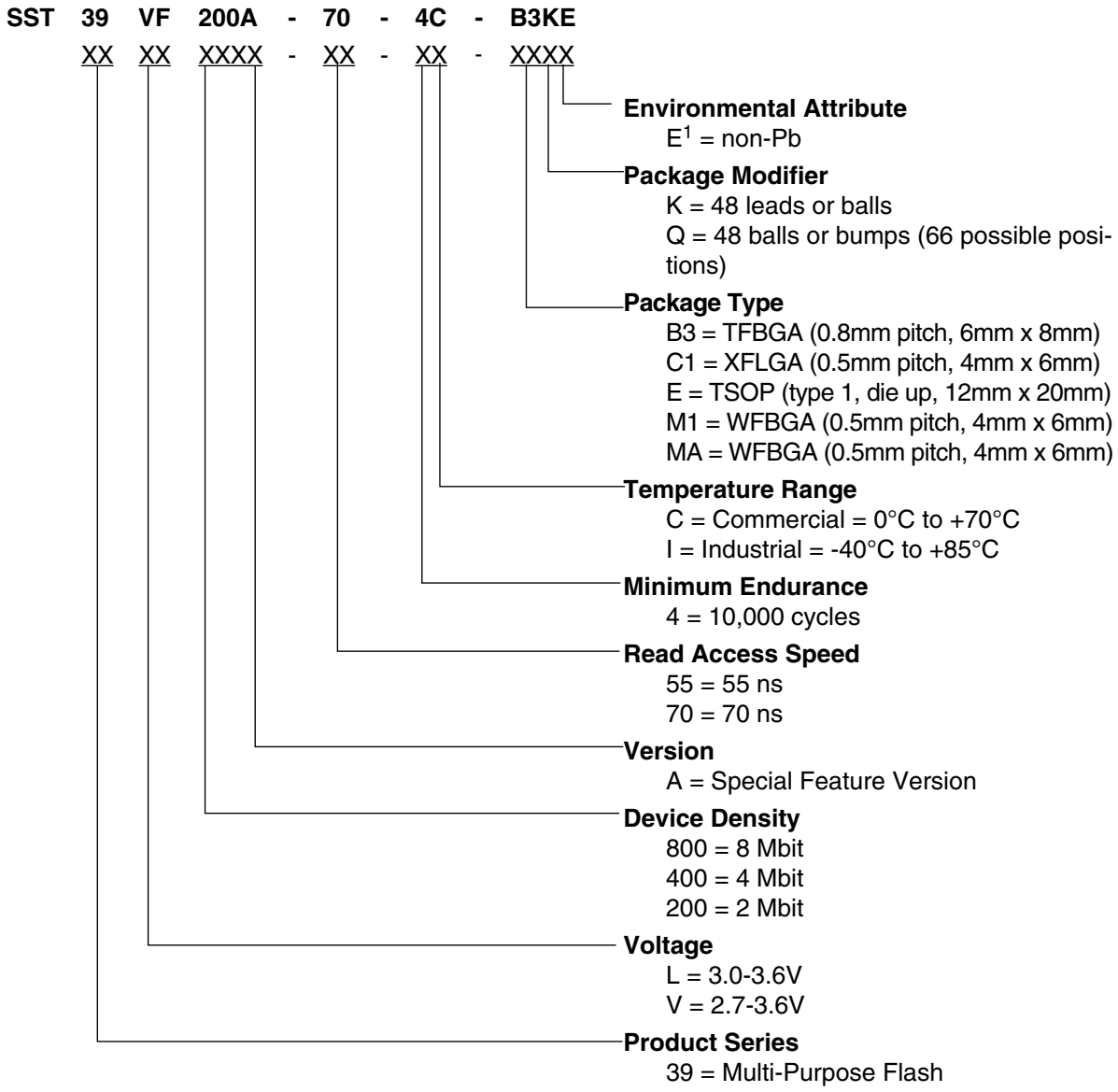



**Figure 21:** Erase Command Sequence

## Product Ordering Information




1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

### Valid combinations for SST39LF200A

SST39LF200A-55-4C-EKE SST39LF200A-55-4C-B3KE

### Valid combinations for SST39VF200A

SST39VF200A-70-4C-EKE SST39VF200A-70-4C-B3KE SST39VF200A-70-4C-M1QE
SST39VF200A-70-4C-MAQE
SST39VF200A-70-4I-EKE SST39VF200A-70-4I-B3KE SST39VF200A-70-4I-M1QE
SST39VF200A-70-4I-MAQE

### Valid combinations for SST39LF400A

SST39LF400A-55-4C-EKE SST39LF400A-55-4C-B3KE SST39LF400A-55-4C-MAQE

### Valid combinations for SST39VF400A

SST39VF400A-70-4C-EKE SST39VF400A-70-4C-B3KE SST39VF400A-70-4C-C1QE
ST39VF400A-70-4C-M1QE SST39VF400A-70-4C-MAQE
SST39VF400A-70-4I-EKE SST39VF400A-70-4I-B3KE SST39VF400A-70-4I-C1QE
SST39VF400A-70-4I-M1QE SST39VF400A-70-4I-MAQE

### Valid combinations for SST39LF800A

SST39LF800A-55-4C-EKE SST39LF800A-55-4C-B3KE SST39LF800A-55-4C-MAQE

### Valid combinations for SST39VF800A

SST39VF800A-70-4C-EKE SST39VF800A-70-4C-B3KE SST39VF800A-70-4C-C1QE
SST39VF800A-70-4C-M1QE SST39VF800A-70-4C-MAQE
SST39VF800A-70-4I-EKE SST39VF800A-70-4I-B3KE SST39VF800A-70-4I-C1QE
SST39VF800A-70-4I-M1QE SST39VF800A-70-4I-MAQE

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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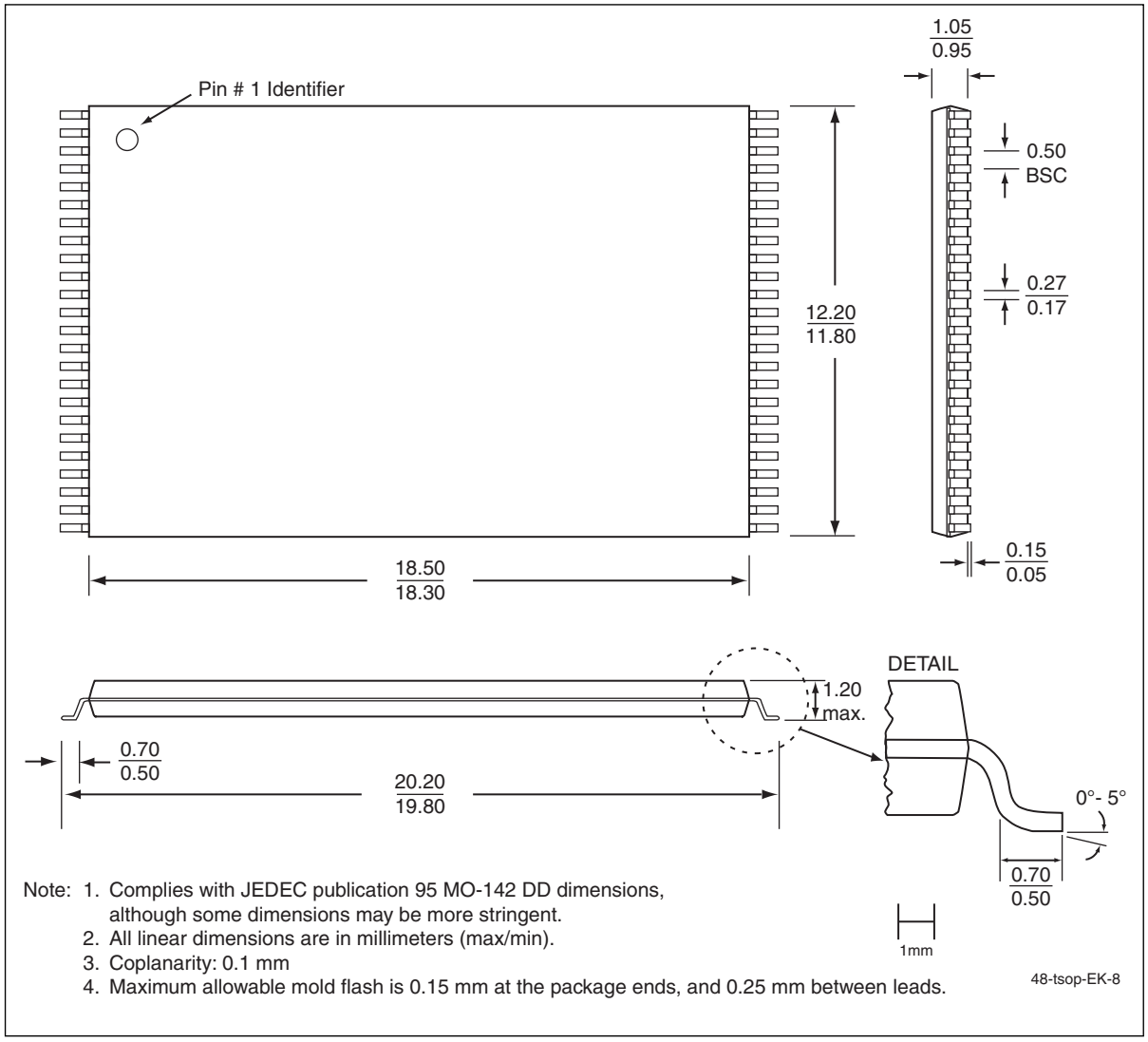
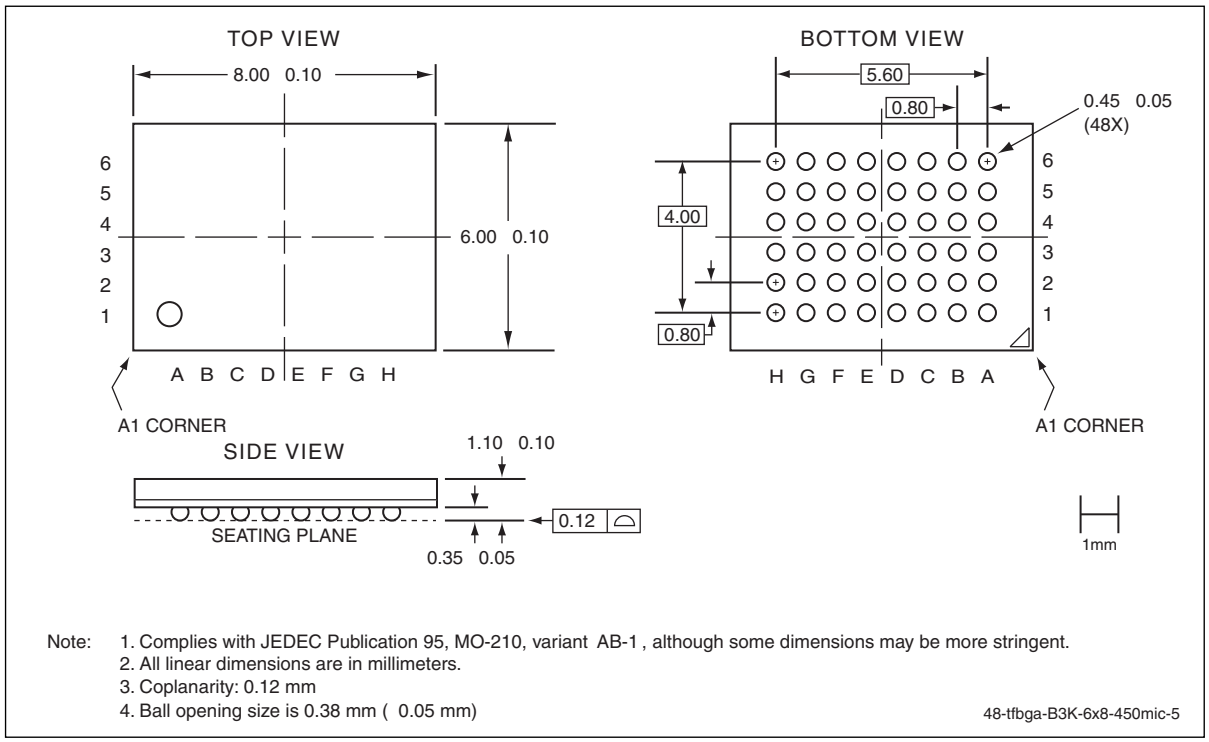
## Packaging Diagrams




Note: 1. Complies with JEDEC publication 95 MO-142 DD dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

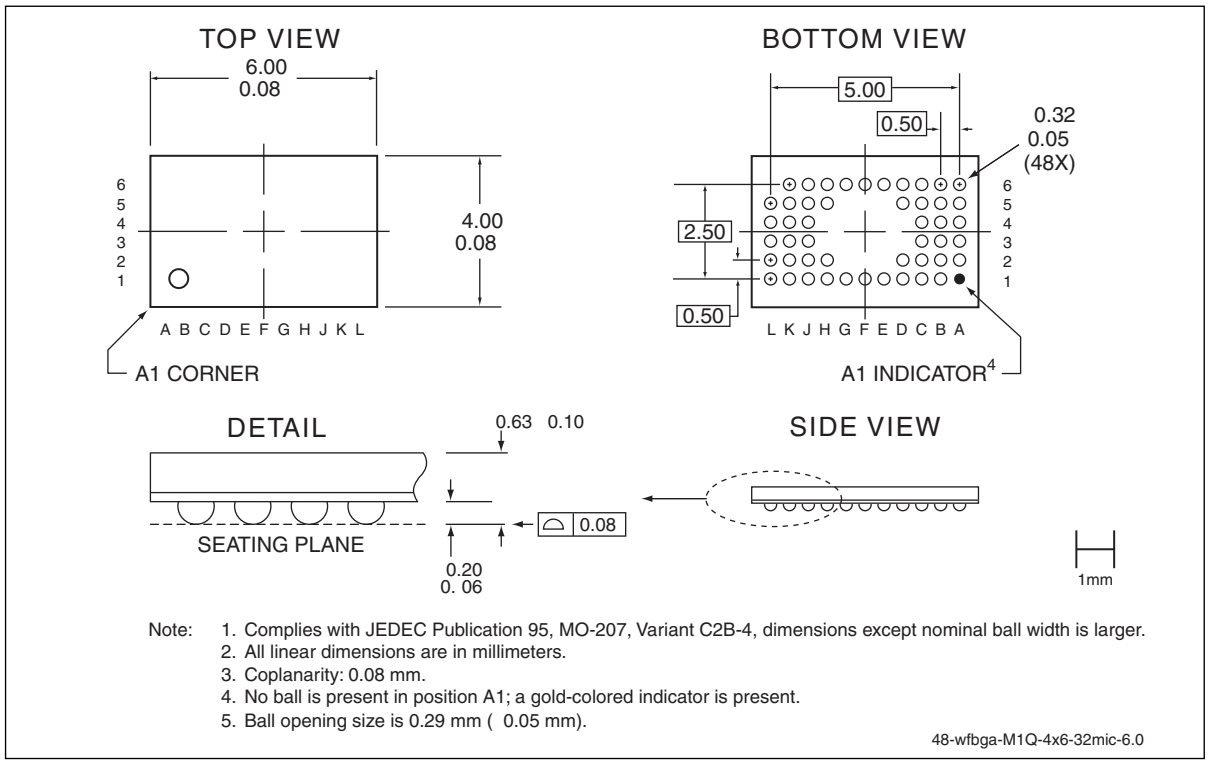
**Figure 22:** 48-Lead Thin Small Outline Package (TSOP) 12mm x 20mm
SST Package Code: EK




Note:
1. Complies with JEDEC Publication 95, MO-210, variant AB-1 , although some dimensions may be more stringent.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm ( 0.05 mm)

48-tfbga-B3K-6x8-450mic-5

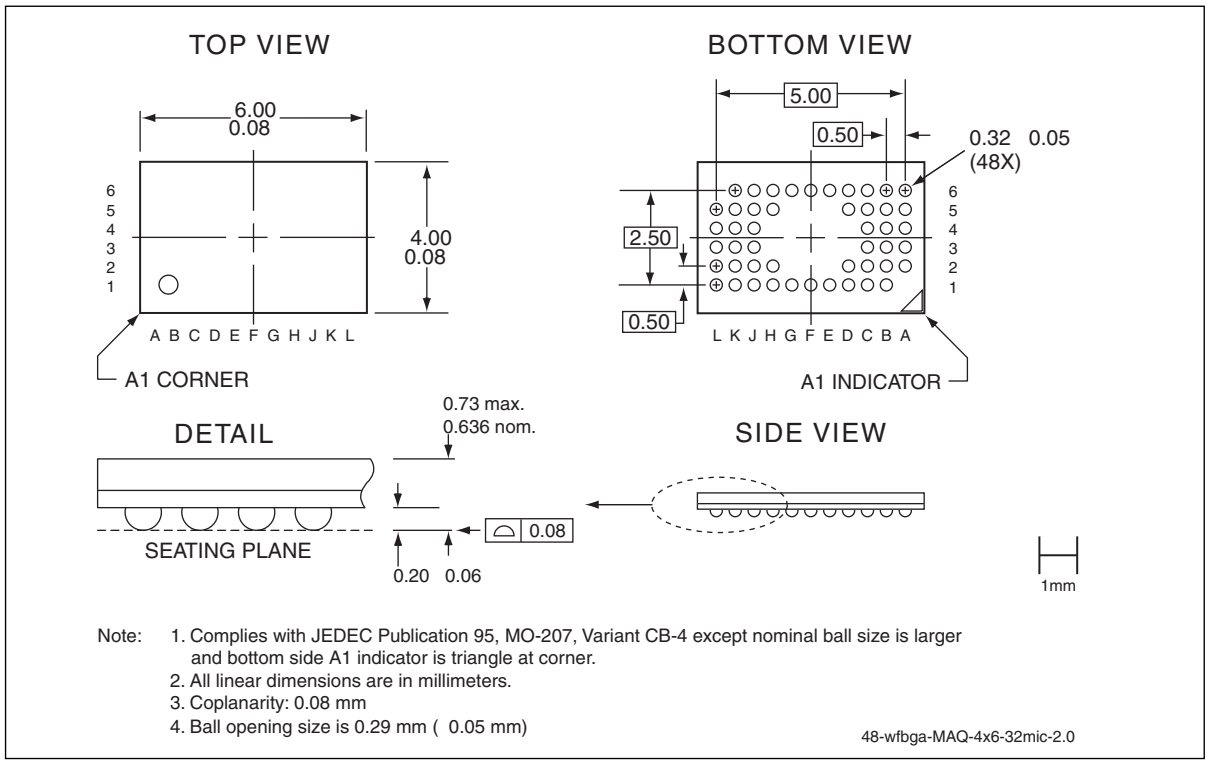
**Figure 23:** 48-Ball Thin-Profile, Fine-pitch Ball Grid Array (TFBGA) 6mm x 8mm
SST Package Code: B3K




Note:
1. Complies with JEDEC Publication 95, MO-207, Variant C2B-4, dimensions except nominal ball width is larger.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.08 mm.
4. No ball is present in position A1; a gold-colored indicator is present.
5. Ball opening size is 0.29 mm ( 0.05 mm).

48-wfbga-M1Q-4x6-32mic-6.0

**Figure 24:** 48-Ball Very-Very-Thin-Profile, Fine-Pitch Ball Grid Array (WFBGA) 4mm x 6mm
SST Package Code: M1Q




Note:
1. Complies with JEDEC Publication 95, MO-207, Variant CB-4 except nominal ball size is larger and bottom side A1 indicator is triangle at corner.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.08 mm
4. Ball opening size is 0.29 mm ( 0.05 mm)

48-wfbga-MAQ-4x6-32mic-2.0

**Figure 25:** 48-Ball Very-Very-Thin-Profile, Fine-Pitch Ball Grid Array (WFBGA) 4mm x 6mm
SST Package Code: MAQ

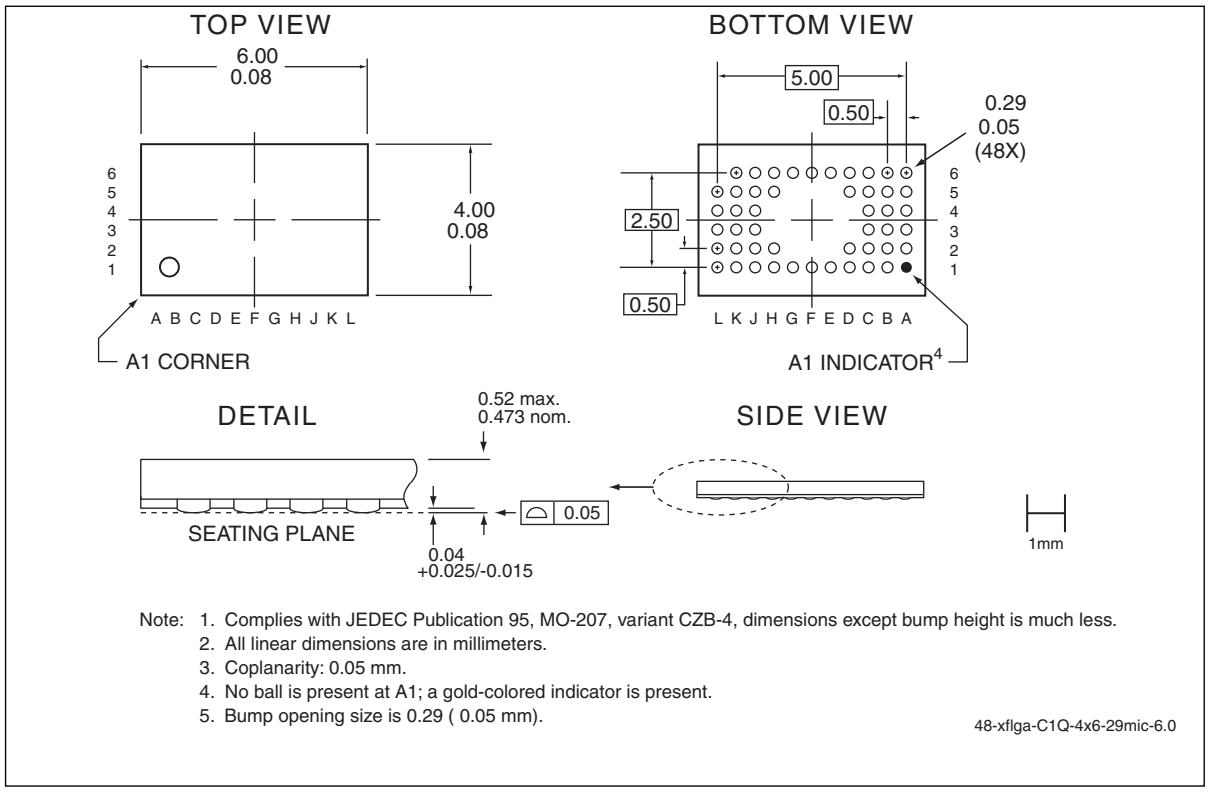



**Figure 26:** 48-Bump Extremely-Thin-Profile, Fine-Pitch Land Grid Array (XFLGA) 4mm x 6mm
SST Package Code: C1Q

**Table 18:** Revision History

| Revision | Description | Date |
|---|---|---|
| 04 | • 2002 Data Book | May 2002 |
| 05 | • Added footnotes for MPF power usage and Typical conditions to Table 11 on page 15<br>• Clarified the Test Conditions for Power Supply Current and Read parameters in Table 11 on page 15<br>• Part number changes - see page 30 for additional information<br>• New Micro-Package part numbers added for SST39VF400A and SST39VF800A | Mar 2003 |
| 06 | • New Micro-Package part numbers added for SST39VF400A / 800A (see page 30) | Oct 2003 |
| 07 | • 2004 Data Book<br>• Updated the B3K, M1Q, and C1Q package diagrams<br>• Added non-Pb MPNs and removed footnote (see page 30) | Nov 2003 |
| 08 | • Added M1Q/M1QE MPNs for the SSTVF200A device on page 30<br>• Removed 90ns MPNs and footnote for the SSTVFx00A devices on page 30<br>• Added RoHS compliance information on page 1 and in the “Product Ordering Information” on page 29<br>• Clarified the solder temperature profile under “Absolute Maximum Stress Ratings” on page 14. | Apr 2005 |
| 09 | • Removed valid combinations SST39LF400A-45-4C-EK, SST39LF400A-45-4C-B3K,<br>SST39LF400A-45-4C-EKE, and SST39LF400A-45-4C-B3KE due to EOL<br>• Applied new format styles. | Feb 2007 |
| 10 | • Add Y1QE package<br>• Removed all pb parts | Aug 2007 |
| 11 | • EOL of all Y1QE parts. Replacement parts are M1QE parts in this document. | Dec 2009 |
| 12 | • EOL of SST39LF200A-45-4C-EKE and SST39LF200A-45-4C-B3KE. See S71117(12). Replacement parts are SST39LF200A-55-4C-EKE and SST39LF200A-55-4C-B3KE found in this document. | Apr 2010 |
| 13 | • Added MAQE package information | Nov 2010 |
| A | • Applied new document format<br>• Released document under letter revision system.<br>• Updated Spec number from S71117 to DS25001.<br>• Updated $T_{IDA}$ value in Table 17 on page 17 from max 150 ns to min 150 ns. | Mar 2011 |

ISBN:978-1-61341-026-4

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