



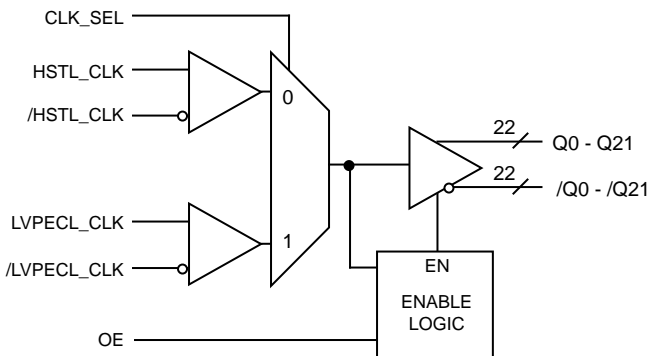
## FEATURES

- 22 differential HSTL (low-voltage swing) output pairs
- HSTL outputs drive 50Ω to ground with no offset voltage
- 3.3V core supply, 1.8V output supply for reduced power
- LVPECL and HSTL inputs
- Low part-to-part skew (200ps max.)
- Low pin-to-pin skew (50ps max.)
- Triple-buffered output enable (OE)
- -40°C to +85°C temperature range
- Available in a 64-pin EPAD-TQFP

## APPLICATIONS

- High-performance PCs
- Workstations
- Parallel processor-based systems
- Other high-performance computing
- Communications

## LOGIC SYMBOL



Precision Edge®

## DESCRIPTION

The SY89823L is a high-performance bus clock driver with 22 differential High-Speed Transceiver Logic (HSTL), 1.5V compatible output pairs. The device is designed for use in low-voltage (3.3V/1.8V) applications that require a large number of outputs to drive precisely aligned, ultra-low skew signals to their destination. The input is multiplexed from either HSTL or Low-Voltage Positive-Emitter-Coupled Logic (LVPECL) by the CLK\_SEL pin.

The Output Enable (OE) is synchronous and triple-buffered so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any potential of generating a runt clock pulse when the device is enabled/disabled, as can occur with an asynchronous control. The triple-buffering feature provides a three-clock delay from the time the OE input is asserted/de-asserted to when the clock appears at the outputs.

The SY89823L features low pin-to-pin skew (50ps max.) and low part-to-part skew (200ps max.), performance previously unachievable in a standard product having such a high number of outputs. The SY89823L is available in a single, space-saving package, enabling a lower overall cost solution.

All support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

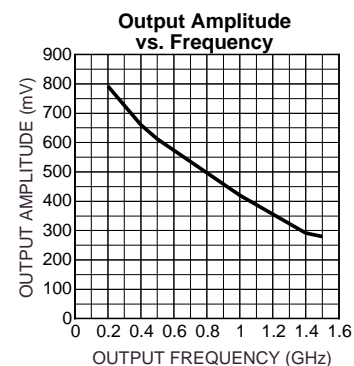
## TRUTH TABLE

OE <sup>(1)</sup>	CLK_SEL	Q <sub>0</sub> -Q <sub>21</sub>	/Q <sub>0</sub> -/Q <sub>21</sub>
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	HSTL_CLK	/HSTL_CLK
1	1	LVPECL_CLK	/LVPECL_CLK

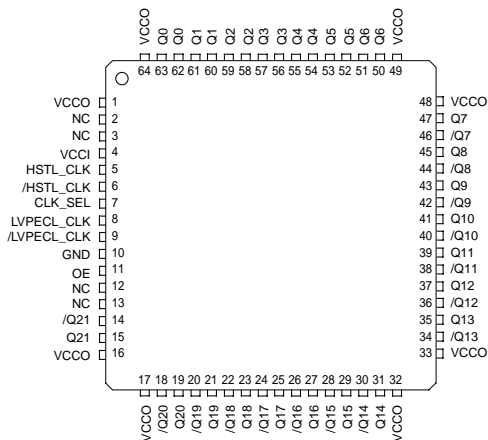
**Note:**

1. The output enable (OE) signal is synchronized with the low level of the HSTL\_CLK and LVPECL\_CLK signal.

## TYPICAL PERFORMANCE



**PACKAGE/ORDERING INFORMATION**



**64-Pin EPAD-TQFP (H64-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89823LHC	H64-1	Commercial	SY89823LHC	Sn-Pb
SY89823LHCTR <sup>(2)</sup>	H64-1	Commercial	SY89823LHC	Sn-Pb
SY89823LHZ <sup>(3)</sup>	H64-1	Commercial	SY89823LHZ with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89823LHZTR <sup>(2, 3)</sup>	H64-1	Commercial	SY89823LHZ with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89823LHI	H64-1	Industrial	SY89823LHI with Pb-Free bar-line indicator	Sn-Pb
SY89823LHITR <sup>(2, 3)</sup>	H64-1	Industrial	SY89823LHI with Pb-Free bar-line indicator	Sn-Pb
SY89823LHY <sup>(3)</sup>	H64-1	Industrial	SY89823LHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89823LHYTR <sup>(2, 3)</sup>	H64-1	Industrial	SY89823LHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

**PIN DESCRIPTION**

Pin Number	Pin Name	Type	Pin Function
5, 6	HSTL_CLK, /HSTL_CLK	HSTL Input	Differential clock input selected by CLK_SEL. Can be left floating if not selected. Floating input, if selected, produces an indeterminate output. HSTL input signal requires external termination 50Ω to GND.
8, 9	LVPECL_CLK, /LVPECL_CLK	LVPECL Input	Differential clock input selected by CLK_SEL. Can be left floating. Floating input, if selected, produces a LOW at the output. Requires external termination. 75kΩ pull-up.
7	CLK_SEL	LVTTL Input	Selects HSTL_CLK input when LOW and LVPECL_CLK output when HIGH. 11kΩ pull-up. Default condition selects LVPECL_CLK if left open.
11	OE	LVTTL Input	Enable input synchronized internally to prevent glitching of the Q0-Q21 and /Q0-/Q21 outputs. Must be a minimum of three clock periods wide if synchronous with the CLK inputs and must meet the t <sub>S</sub> and t <sub>H</sub> requirements (refer to “AC Electrical Characteristics” section). If asynchronous, must be a minimum of four clock periods wide. 11kΩ pull-up.
63, 61, 59, 57, 55, 53 51, 47, 45, 43, 41, 39 37, 35, 31, 29, 27 25, 23, 21, 19, 15	Q0-Q21	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. Q0-Q21 outputs are static LOW when OE = LOW. Unused output pairs may be left floating.
62, 60, 58, 56, 54, 52 50, 46, 44, 42, 40, 38 36, 34, 30, 28, 26 24, 22, 20, 18, 14	/Q0-/Q21	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. /Q0-/Q21 outputs are static HIGH when OE = LOW. Unused output pairs may be left floating.
4	VCCI	VCC Core	Core V <sub>CC</sub> connected to 3.3V supply. Bypass with 0.1μF in parallel with Power 0.01μF low ESR capacitors as close to V <sub>CCL</sub> pins as possible.
1, 16, 17, 32, 33, 48, 49, 64	VCCO	VCC Output Power	Output Buffer V <sub>CC</sub> connected to 1.8V supply. Bypass with 0.1μF in parallel with 0.01μF low ESR capacitors as close to V <sub>CCO</sub> pin as possible. All V <sub>CCO</sub> pins should be connected together on the PCB.
10	GND, Exposed Pad		Ground pin and exposed pad must be connected to the same ground plane.
2, 3, 12, 13	NC		No Connect.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{IN}$ )	-0.5V to $V_{CCI}$
$V_{CC}$ Pin Potential to Ground Pin	
$V_{CCI}, V_{CCO}$	-0.5V to +4.0V
DC Output Current, Output HIGH ( $I_{OUT}$ )	-50mA
Lead Temperature (soldering, 20 sec.)	260°C
Storage Temperature ( $T_S$ )	-65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage	
$V_{CCI}$	+3.15V to +3.45V
$V_{CCO}$	+1.6V to +2.0V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Package Thermal Resistance <sup>(3)</sup>	
EPAD-TQFP ( $\theta_{JA}$ ) with Die attach soldered to GND	
Still-Air	23°C/W
200lfpm	18°C/W
500lfpm	15°C/W
with Die attach NOT soldered to GND	
Still-Air	44°C/W
200lfpm	36°C/W
500lfpm	30°C/W
EPAD-TQFP ( $\theta_{JC}$ )	4.3°C/W

### DC ELECTRICAL CHARACTERISTICS<sup>(4)</sup>

**Power Supply**  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CCI}$	$V_{CC}$ Core		3.15	3.3	3.45	V
$V_{CCO}$	$V_{CC}$ Output		1.6	1.8	2.0	V
$I_{CCI}$	$I_{CC}$ Core	Max $V_{CC}$ , no load	—	115	170	mA

**HSTL**  $V_{CCI} = 3.3\text{V} \pm 5\%$ ;  $V_{CCO} = 1.8\text{V} \pm 10\%$ ;  $R_L = 50\Omega$  to GND;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage		1.0	—	1.2	V
$V_{OL}$	Output LOW Voltage		0.2	—	0.4	V
$V_{IH}$	Input HIGH Voltage		$V_X + 0.1$	—	1.6	V
$V_{IL}$	Input LOW Voltage		-0.3	—	$V_X - 0.1$	V
$V_X$	Input Crossover Voltage		0.68	—	0.9	V
$I_{IH}$	Input HIGH Current		+20	—	-350	$\mu\text{A}$
$I_{IL}$	Input LOW Current		—	—	-500	$\mu\text{A}$

**LVPECL**  $V_{CCI} = 3.3\text{V} \pm 5\%$ ;  $V_{CCO} = 1.8\text{V} \pm 10\%$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Max	Units
$V_{IH}$	Input HIGH Voltage		$V_{CCI} - 1.165$	$V_{CCI} - 0.880$	V
$V_{IL}$	Input LOW Voltage		$V_{CCI} - 1.810$	$V_{CCI} - 1.475$	V
$I_{IH}$	Input HIGH Current		—	+150	$\mu\text{A}$
$I_{IL}$	Input LOW Current		0.5	—	$\mu\text{A}$

**Notes:**

1. Permanent device damage may occur if the ratings in the "Absolute Maximum Ratings" section are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Valid for 4-layer board.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**DC ELECTRICAL CHARACTERISTICS<sup>(5)</sup>**LVCMOS/LVTTL  $V_{CCI} = 3.3V \pm 5\%$ ;  $V_{CCO} = 1.8V \pm 10\%$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		2.0	—	—	V
$V_{IL}$	Input LOW Voltage		—	—	0.8	V
$I_{IH}$	Input HIGH Current		+20	—	-250	$\mu\text{A}$
$I_{IL}$	Input LOW Current		—	—	-600	$\mu\text{A}$

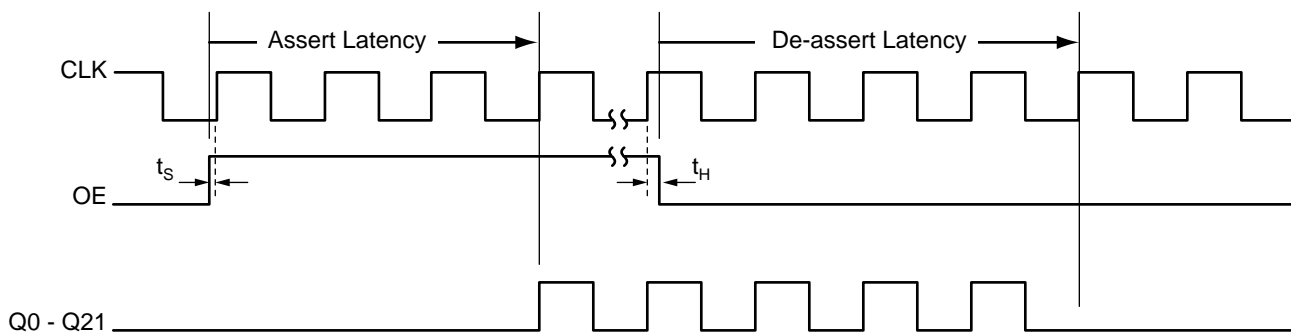
**AC ELECTRICAL CHARACTERISTICS<sup>(6)</sup>** $V_{CCI} = 3.3V \pm 5\%$ ;  $V_{CCO} = 1.8V \pm 10\%$ ; All outputs loaded with  $50\Omega$  to GND;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units	
$f_{MAX}$	Maximum Operating Frequency	$V_{OUT} \geq 450\text{mV}$	500	—	—	MHz	
$t_{pd}$	Propagation Delay	CLK-to-Q	<b>Note 7</b>	0.8	—	1.3	ns
		SEL-to-Q	<b>Note 7</b>	0.8	1.2	1.7	ns
$t_{SKEW}$	Within-Device Skew	<b>Note 8</b>	—	—	50	ps	
$t_{SKPP}$	Part-to-Part Skew	<b>Note 9</b>	—	—	200	ps	
$V_{pp}$	Minimum Input Swing LVPECL_CLK	<b>Note 10</b>	600	—	—	mV	
$V_{CMR}$	Common Mode Range LVPECL_CLK	<b>Note 11</b>	-1.5	—	-0.4	V	
$t_S$	OE Set-Up Time	<b>Note 12</b>	1.0	—	—	ns	
$t_H$	OE Hold Time		0.5	—	—	ns	
$t_r, t_f$	Output Rise/Fall Time (20% – 80%)		300	—	700	ps	
$t_{JITTER}$	Cycle-to-Cycle Jitter	<b>Note 13</b>			1	$\text{ps}_{RMS}$	

**Notes:**

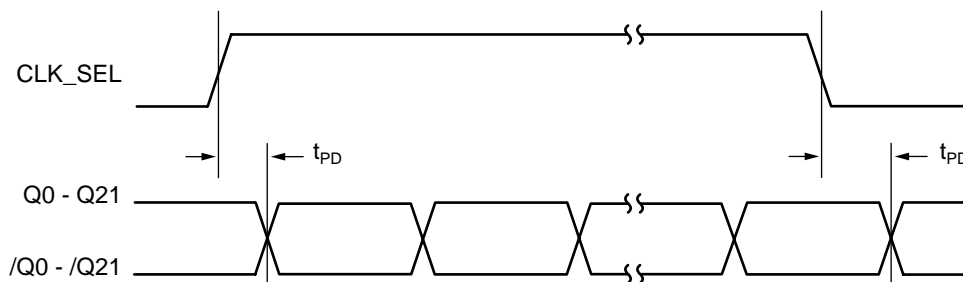
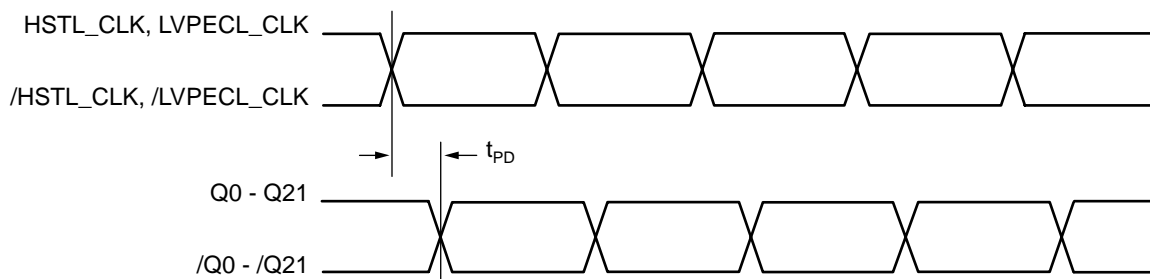
- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- High-frequency AC-parameters are guaranteed by design and characterization.
- Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.
- The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
- The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.
- The  $V_{pp}(\text{min})$  is defined as the minimum input differential voltage which will cause no increase in the propagation delay.
- $V_{CMR}$  is defined as the range within which the  $V_{IH}$  level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to  $V_{CCI}$ . The  $V_{IL}$  level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to  $V_{pp}(\text{min})$ . The lower end of the CMR range varies 1:1 with  $V_{CCI}$ . The  $V_{CMR}(\text{min})$  will be fixed at  $3.3V - |V_{CMR}(\text{min})|$ .
- OE set-up time is defined with respect to the rising edge of the clock. OE HIGH to LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW-to-HIGH transition enables normal operation of the next input clock.
- Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.

**TIMING DIAGRAMS**



**Notes:**

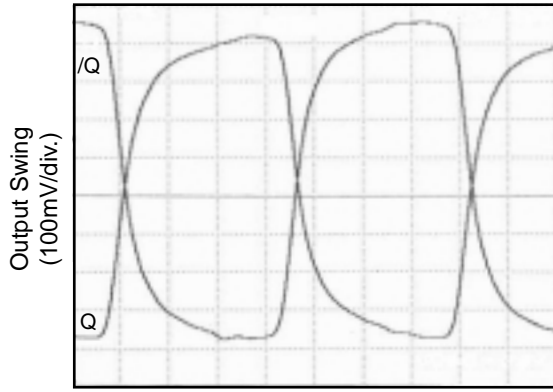
1. The OE input signal must be a minimum of 3 clock periods with width.
2. The internal enable is asserted and de-asserted on the falling edge of clock.
3. The internal enable occurs 2.5 clock cycles (plus the set-up time of OE with the rising edge of clock) after the rising edge of the external OE.
4. If OE does not meet the  $t_s$  of  $t_H$  specifications as in asynchronous applications, OE must be a minimum of 4 clock periods in width.



**TYPICAL OPERATING CHARACTERISTICS**

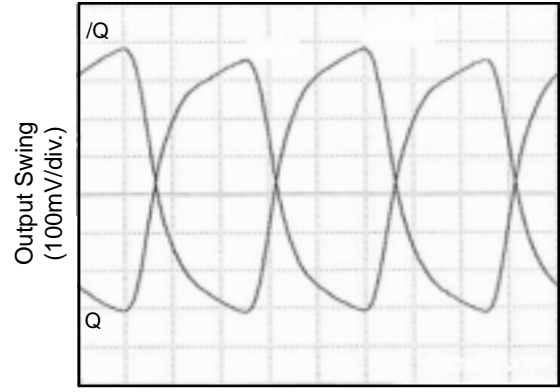
$V_{CCI} = 3.6V$ ,  $V_{CCO} = 2.0V$ ,  $T_A = 25^\circ C$ , unless otherwise stated.

**200MHz Output**



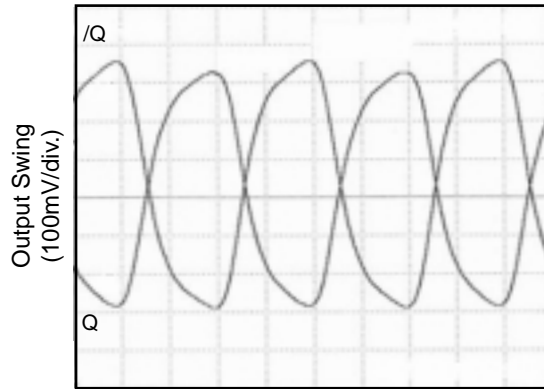
TIME (700ps/div)

**400MHz Output**



TIME (500ps/div)

**500MHz Output**



TIME (500ps/div)

**LVPECL/HSTL INPUTS**

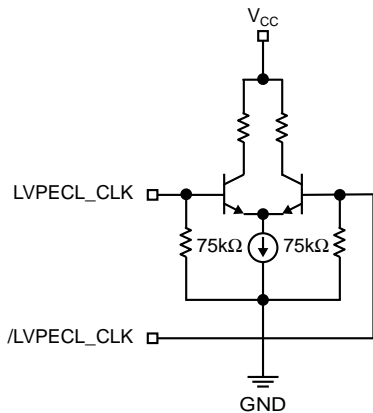


Figure 1. Simplified LVPECL Input Stage

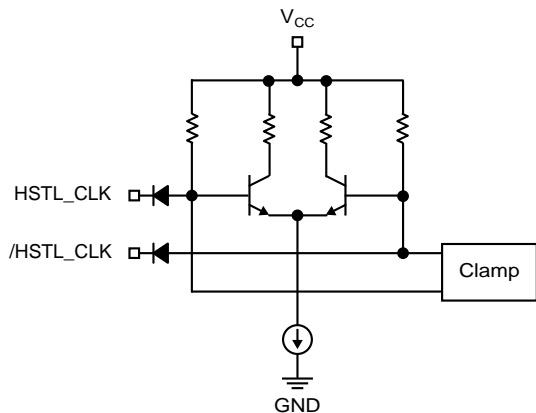


Figure 2. Simplified HSTL Input Stage

**HSTL OUTPUTS**

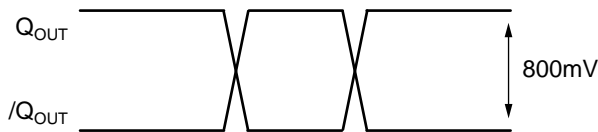


Figure 3. Output Driver Signal Levels (Single-Ended)

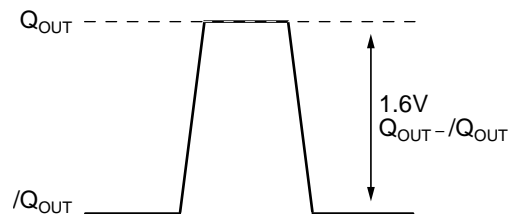
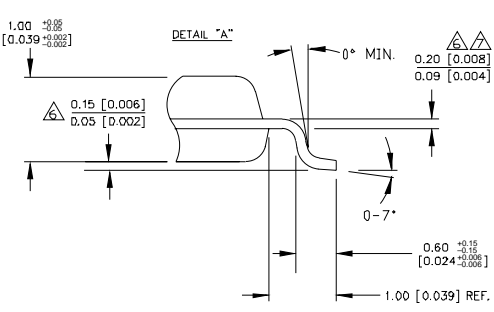
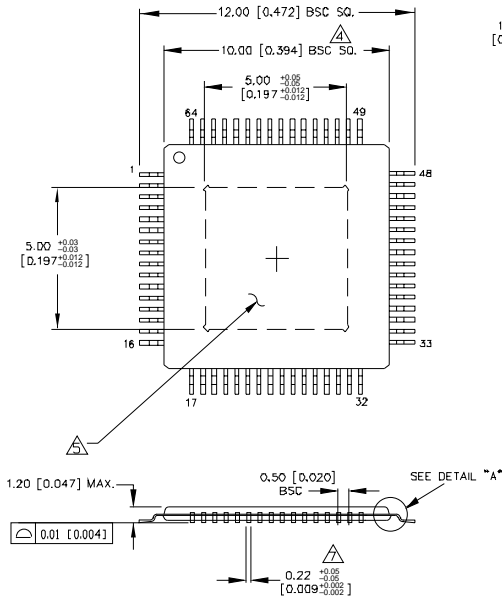


Figure 4. Output Driver Signal Levels (Differential)

**RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION**

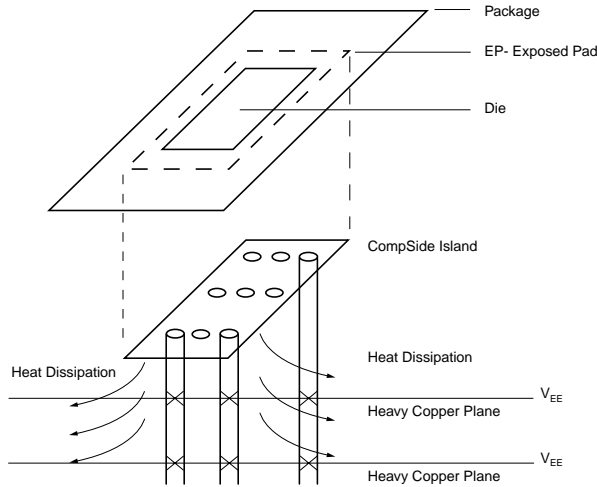
Part Number	Function	Data Sheet Link
SY89809L	3.3V 1:9 High-Performance, Low-Voltage Bus Clock Driver	<a href="http://www.micrel.com/product-info/products/sy89809l.shtml">http://www.micrel.com/product-info/products/sy89809l.shtml</a>
SY89808L	3.3V, 500MHz, 1:9 Differential HSTL (1.5V) Fanout Buffer Translator	<a href="http://www.micrel.com/product-info/products/sy89808l.shtml">http://www.micrel.com/product-info/products/sy89808l.shtml</a>
	Exposed Pad Application Note	<a href="http://www.amkor.com/products/notes_papers/epad.pdf">http://www.amkor.com/products/notes_papers/epad.pdf</a>
HBW Solutions	New Products and Applications	<a href="http://www.micrel.com/product-info/products/solutions.shtml">http://www.micrel.com/product-info/products/solutions.shtml</a>
MIC3775	750mA $\mu$ Cap Low-Voltage Low-Dropout Regulator	<a href="http://www.micrel.com/product-info/products/mic3775.shtml">http://www.micrel.com/product-info/products/mic3775.shtml</a>

**64-PIN EPAD-TQFP (DIE UP) (H64-1)**



- NOTES:  
 1. DIMENSIONS ARE IN MM[INCHES].  
 2. CONTROLLING DIMENSION: MM.  
 3. EXPOSED PAD: CU WITH Sn/Pb PLATING.  
 △ DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.  
 △ DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.  
 △ MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN  
 △ THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 02



**PCB Thermal Consideration for 64-Pin EPAD-TQFP Package  
(Always solder or equivalent the exposed pad to the PCB)**

- Package Notes:**
1. Package meets Level 2 qualification.
  2. All parts are dry-packaged before shipment.
  3. Exposed pads must be soldered to a ground for proper thermal management.

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