

# IS65WV12816ALL IS65WV12816BLL



## 128K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

NOVEMBER 2007

### FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation:
  - 36 mW (typical) operating
  - 9  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply:
  - 1.65V to 2.2V  $V_{DD}$  (65WV12816ALL)
  - 2.5V to 3.6V  $V_{DD}$  (65WV12816BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- 2CS Option Available
- Temperature Offerings:
  - Option A: 0 to 70°C
  - Option A1: -40 to +85°C
  - Option A2: -40 to +105°C
  - Option A3: -40 to +125°C
- Lead-free available

### DESCRIPTION

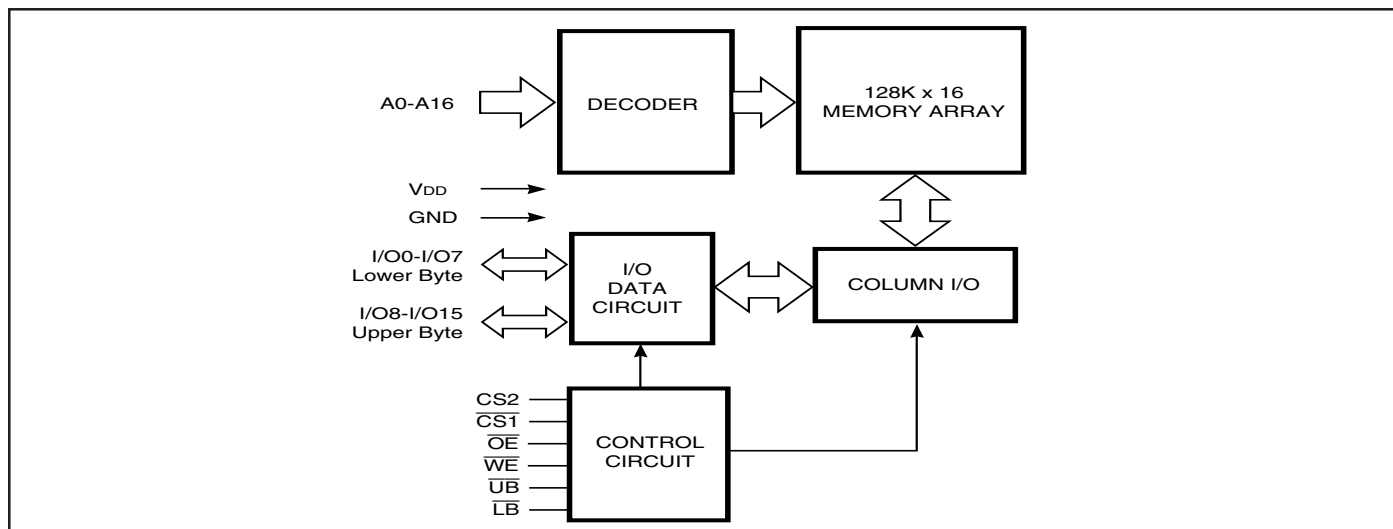
The *ISSI* IS65WV12816ALL/IS65WV12816BLL are high-speed, 2M bit static RAMs organized as 128K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when CS2 is LOW (deselected) or when  $\overline{CS1}$  is LOW, CS2 is HIGH and both  $\overline{LB}$  and  $\overline{UB}$  are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IS65WV12816ALL and IS65WV12816BLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II).

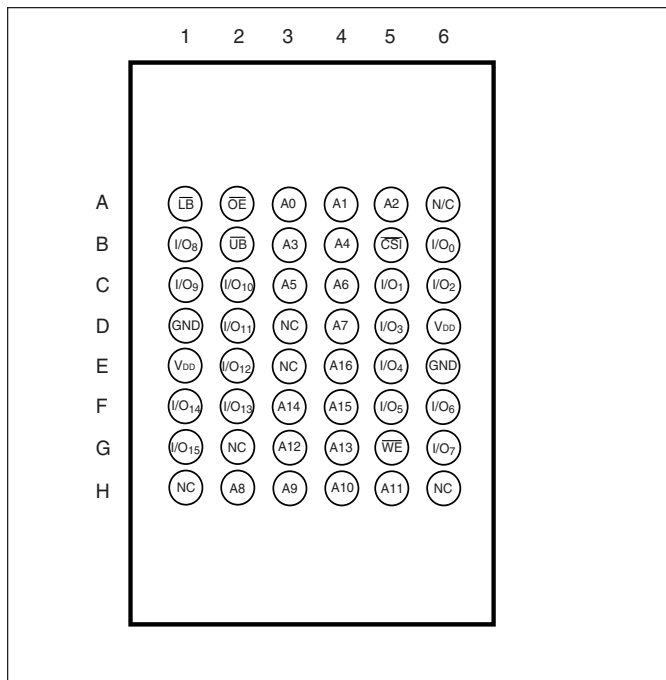
### FUNCTIONAL BLOCK DIAGRAM



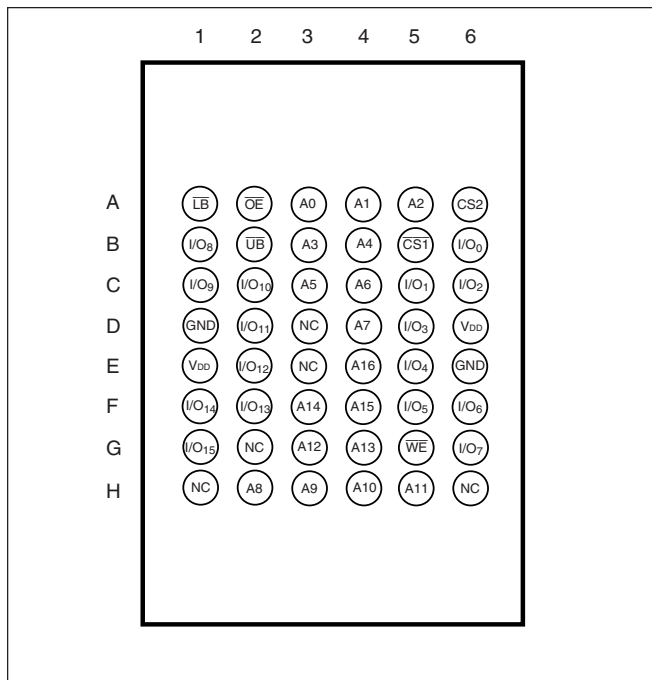
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**PIN CONFIGURATIONS**

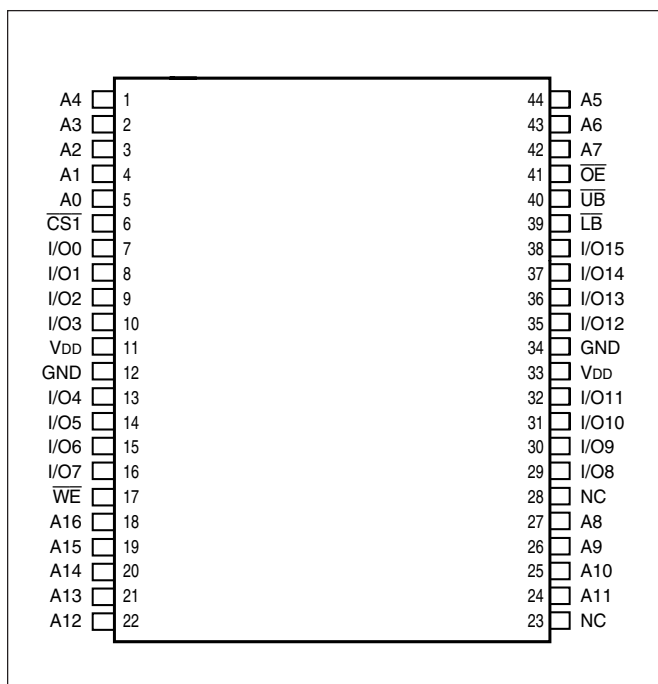
**48-Pin mini BGA (6mm x 8mm)  
(Package Code B)**



**48-Pin mini BGA (6mm x 8mm)  
2 CS Option (Package Code B2)**



**44-Pin mini TSOP (Type II)  
(Package Code T)**



**PIN DESCRIPTIONS**

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS1, CS2	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V <sub>DD</sub> Current
							I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	L	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	X	X	H	H	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I <sub>CC</sub>
	H	L	H	H	X	L	High-Z	High-Z	I <sub>CC</sub>
Read	H	L	H	L	L	H	D <sub>OUT</sub>	High-Z	I <sub>CC</sub>
	H	L	H	L	H	L	High-Z	D <sub>OUT</sub>	
	H	L	H	L	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	
Write	L	L	H	X	L	H	D <sub>IN</sub>	High-Z	I <sub>CC</sub>
	L	L	H	X	H	L	High-Z	D <sub>IN</sub>	
	L	L	H	X	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.2 to V <sub>DD</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

## Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V<sub>DD</sub>)

Option	Ambient Temperature	IS65WV12816ALL	IS65WV12816BLL
A	0°C to +70°C	1.65V - 2.2V	2.5V - 3.6V
A1	-40°C to +85°C	1.65V - 2.2V	2.5V - 3.6V
A2	-40°C to +105°C	1.65V - 2.2V	2.5V - 3.6V
A3	-40°C to +125°C	1.65V - 2.2V	2.5V - 3.6V

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions	Vdd	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	1.65-2.2V	1.4	—	V
		I <sub>OH</sub> = -1 mA	2.5-3.6V	2.2	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	1.65-2.2V	—	0.2	V
		I <sub>OL</sub> = 2.1 mA	2.5-3.6V	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		1.65-2.2V	1.4	V <sub>DD</sub> + 0.2	V
			2.5-3.6V	2.2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub> <sup>(1)</sup>	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
			2.5-3.6V	-0.2	0.6	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled		-1	1	μA

**Notes:**

- V<sub>IL</sub> (min.) = -1.0V for pulse width less than 10 ns.

**CAPACITANCE**<sup>(1)</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

**Note:**

- Tested initially and after any design or process changes that may affect these parameters.

**IS65WV12816ALL, POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	Test Conditions	Options	Max. -70 ns	Unit
loc	Vdd Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	A, A1 A2, A3	15 20	mA
loc1	Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 0	A, A1 A2, A3	7 7	mA
ISB1	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> , f = 1 MHz <b>OR</b>	A, A1 A2, A3	0.6 0.6	mA
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$			
ISB2	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CS1} \geq V_{DD} - 0.2V$ , CS2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0 <b>OR</b>	A, A1 A2 A3	15 20 50	μA
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB}/\overline{LB} = V_{DD} - 0.2V$			

**IS65WV12816BLL, POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	Test Conditions	Options	Max. -55 ns	Max. -70 ns	Unit
loc	Vdd Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	A, A1 A2, A3	25 30	20 25	mA
loc1	Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 0	A, A1 A2, A3	7 7	7 7	mA
ISB1	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> , f = 1 MHz <b>OR</b>	A, A1 A2, A3	0.6 0.6	0.6 0.6	mA
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$				
ISB2	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CS1} \geq V_{DD} - 0.2V$ , CS2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0 <b>OR</b>	A, A1 A2 A3	15 25 65	15 25 65	μA
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB}/\overline{LB} = V_{DD} - 0.2V$				

**Note:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**AC TEST CONDITIONS**

Parameter	65WV12816ALL (Unit)	65WV12816BLL (Unit)
Input Pulse Level	0.4V to $V_{DD}-0.2V$	0.4V to $V_{DD}-0.3V$
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	$V_{REF}$	$V_{REF}$
Output Load	See Figures 1 and 2	See Figures 1 and 2

	65WV12816ALL (1.65V-2.2V)	65WV12816BLL (2.5V - 3.6V)
<b>R1(<math>\Omega</math>)</b>	3070	3070
<b>R2(<math>\Omega</math>)</b>	3150	3150
<b><math>V_{REF}</math></b>	0.9V	1.5V
<b><math>V_{TM}</math></b>	1.8V	2.8V

**AC TEST LOADS**

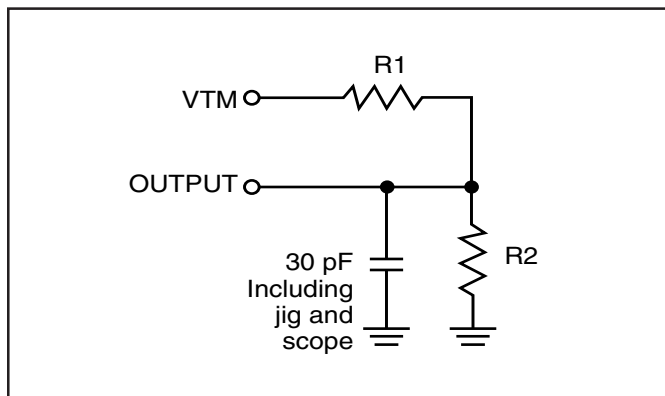


Figure 1

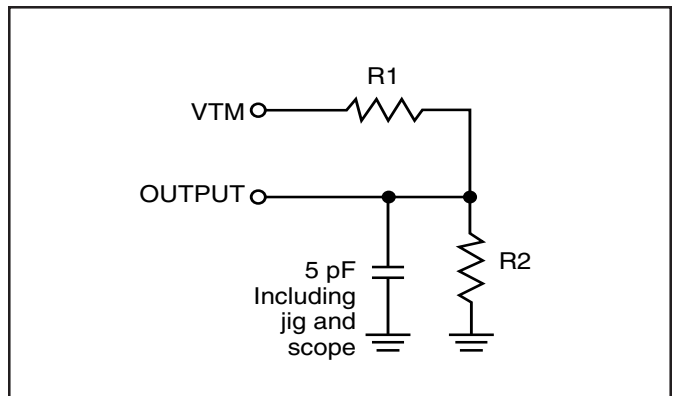


Figure 2

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

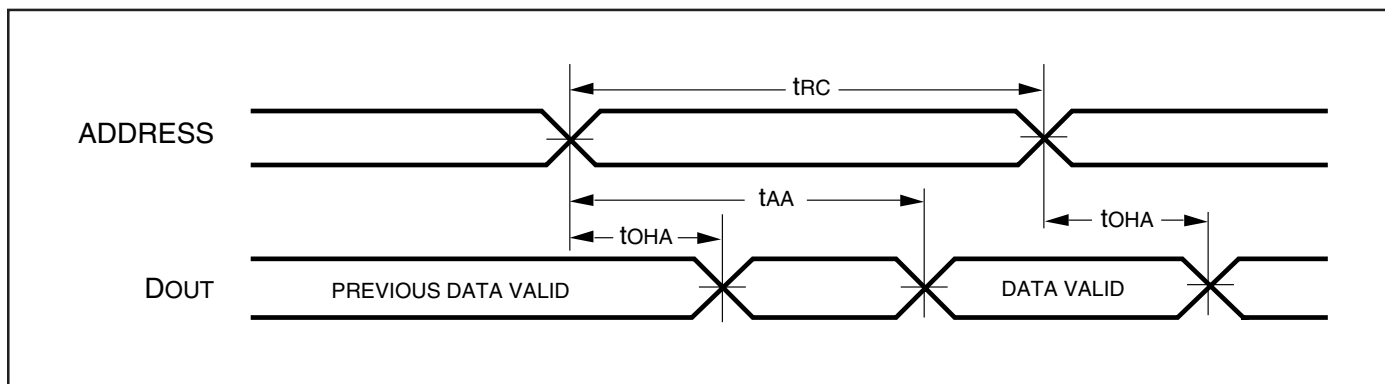
Symbol	Parameter	-55 ns		-70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	ns
t <sub>AA</sub>	Address Access Time	—	55	—	70	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	ns
t <sub>ACS1</sub> /t <sub>ACS2</sub>	$\overline{\text{CS1}}/\overline{\text{CS2}}$ Access Time	—	55	—	70	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ Access Time	—	25	—	35	ns
t <sub>HZOE</sub> <sup>(2)</sup>	$\overline{\text{OE}}$ to High-Z Output	—	20	—	25	ns
t <sub>LZOE</sub> <sup>(2)</sup>	$\overline{\text{OE}}$ to Low-Z Output	5	—	5	—	ns
t <sub>HZCS1</sub> /t <sub>HZCS2</sub> <sup>(2)</sup>	$\overline{\text{CS1}}/\overline{\text{CS2}}$ to High-Z Output	0	20	0	25	ns
t <sub>LZCS1</sub> /t <sub>LZCS2</sub> <sup>(2)</sup>	$\overline{\text{CS1}}/\overline{\text{CS2}}$ to Low-Z Output	10	—	10	—	ns
t <sub>BA</sub>	$\overline{\text{LB}}, \overline{\text{UB}}$ Access Time	—	55	—	70	ns
t <sub>HZB</sub>	$\overline{\text{LB}}, \overline{\text{UB}}$ to High-Z Output	0	20	0	25	ns
t <sub>LZB</sub>	$\overline{\text{LB}}, \overline{\text{UB}}$ to Low-Z Output	0	—	0	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

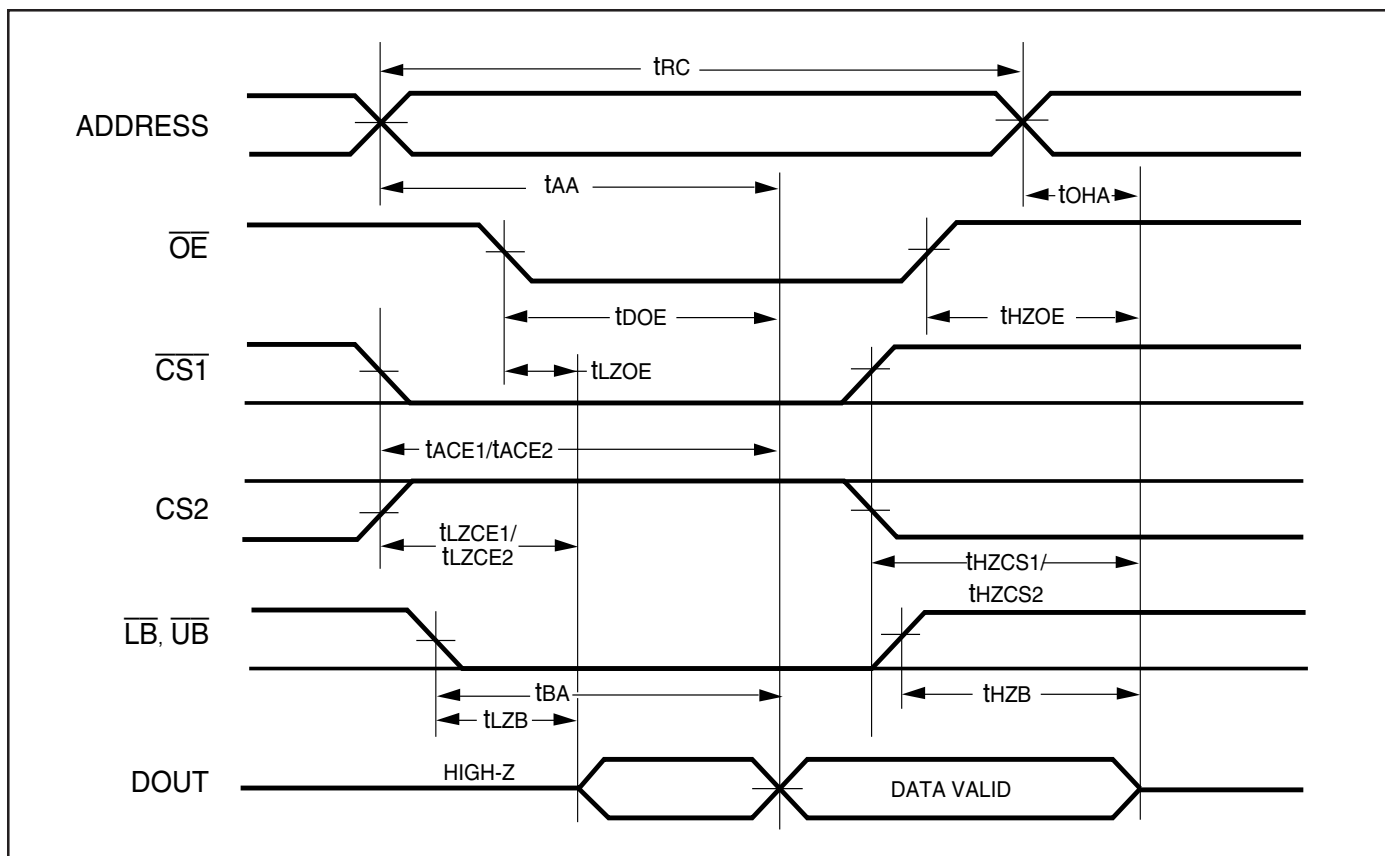
**AC WAVEFORMS**

**READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ ,  $\overline{CS2} = \overline{WE} = V_{IH}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ )



**AC WAVEFORMS**

**READ CYCLE NO. 2<sup>(1,3)</sup>** ( $\overline{CS1}$ ,  $\overline{CS2}$ ,  $\overline{OE}$ , AND  $\overline{UB/LB}$  Controlled)



**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1}$ ,  $\overline{UB}$ , or  $\overline{LB} = V_{IL}$ .  $CS2 = \overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW transition.



**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

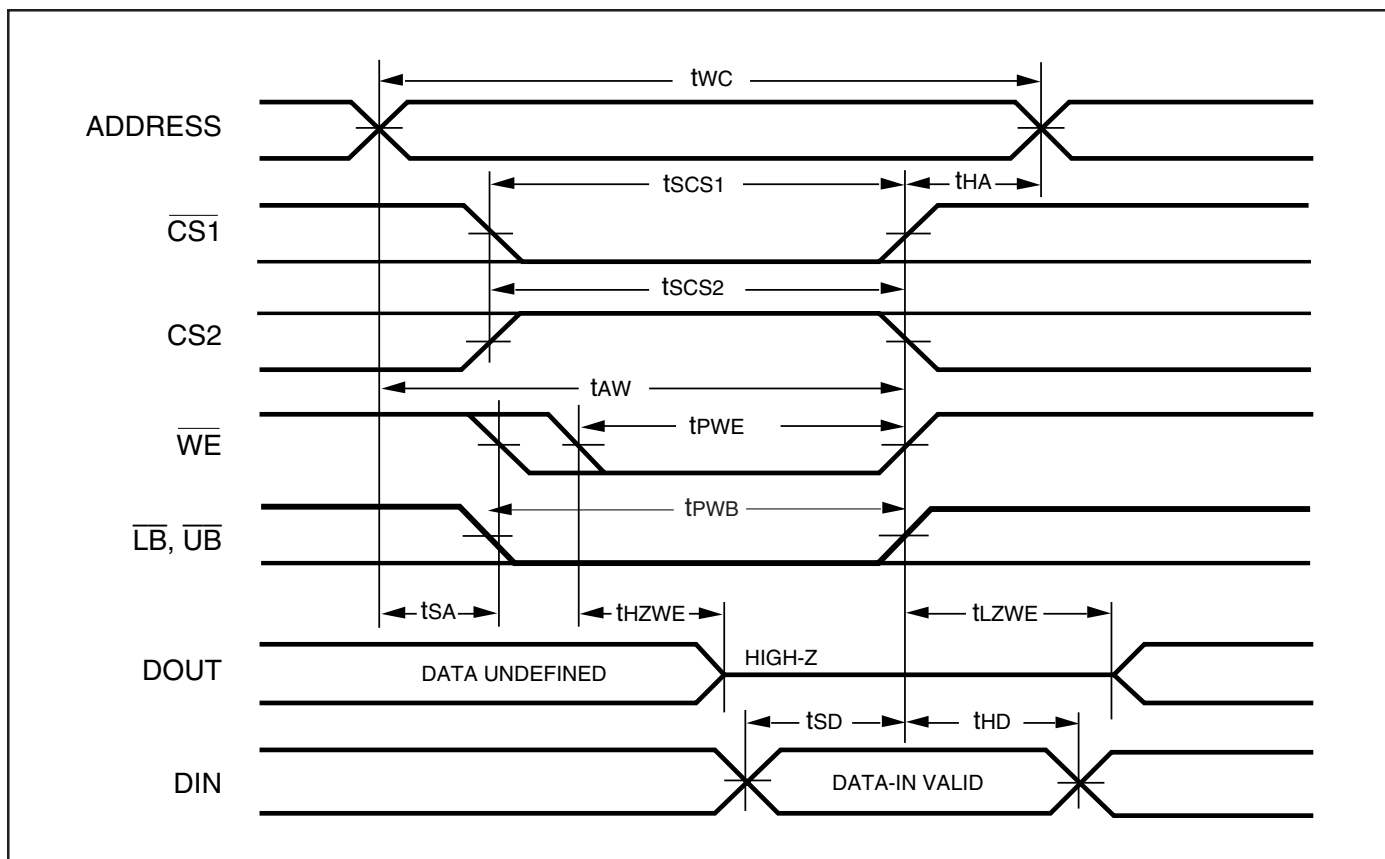
Symbol	Parameter	-55 ns		-70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	55	—	70	—	ns
t <sub>SCS1</sub> /t <sub>SCS2</sub>	$\overline{\text{CS1}}$ / $\overline{\text{CS2}}$ to Write End	45	—	60	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	45	—	60	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PWB</sub>	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ Valid to End of Write	45	—	60	—	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	40	—	50	—	ns
t <sub>SD</sub>	Data Setup to Write End	25	—	30	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE</sub> <sup>(3)</sup>	$\overline{\text{WE}}$ LOW to High-Z Output	—	20	—	20	ns
t <sub>LZWE</sub> <sup>(3)</sup>	$\overline{\text{WE}}$ HIGH to Low-Z Output	5	—	5	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{\text{CS1}}$  LOW, CS2 HIGH and  $\overline{\text{UB}}$  or  $\overline{\text{LB}}$ , and  $\overline{\text{WE}}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS**

**WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CS1}$  Controlled,  $\overline{OE}$  = HIGH or LOW)**

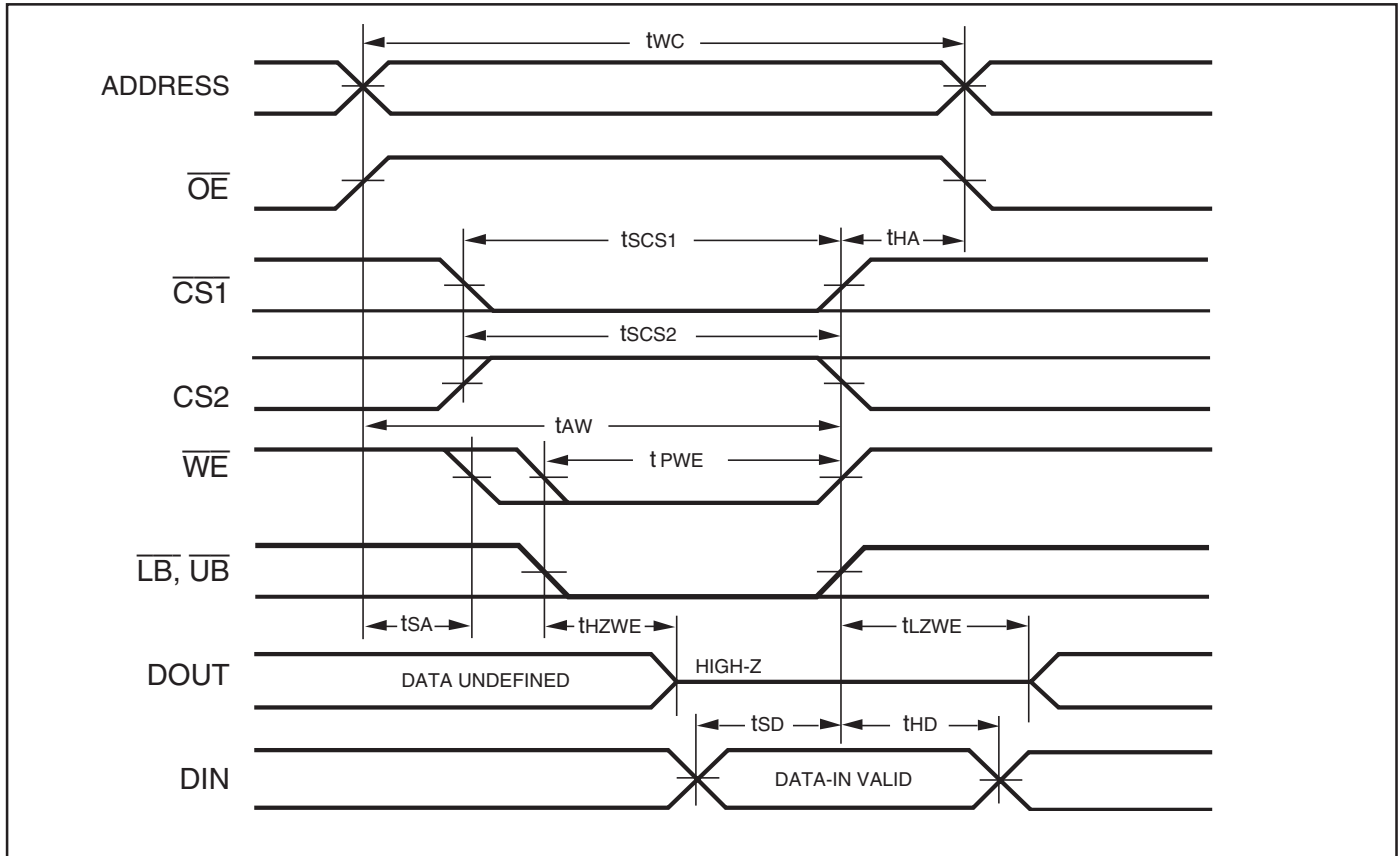


**Notes:**

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{WE}$  inputs and at least one of the  $\overline{LB}$  and  $\overline{UB}$  inputs being in the LOW state.
2. WRITE = ( $\overline{CS1}$ ) [ ( $\overline{LB}$ ) = ( $\overline{UB}$ ) ] ( $\overline{WE}$ ).

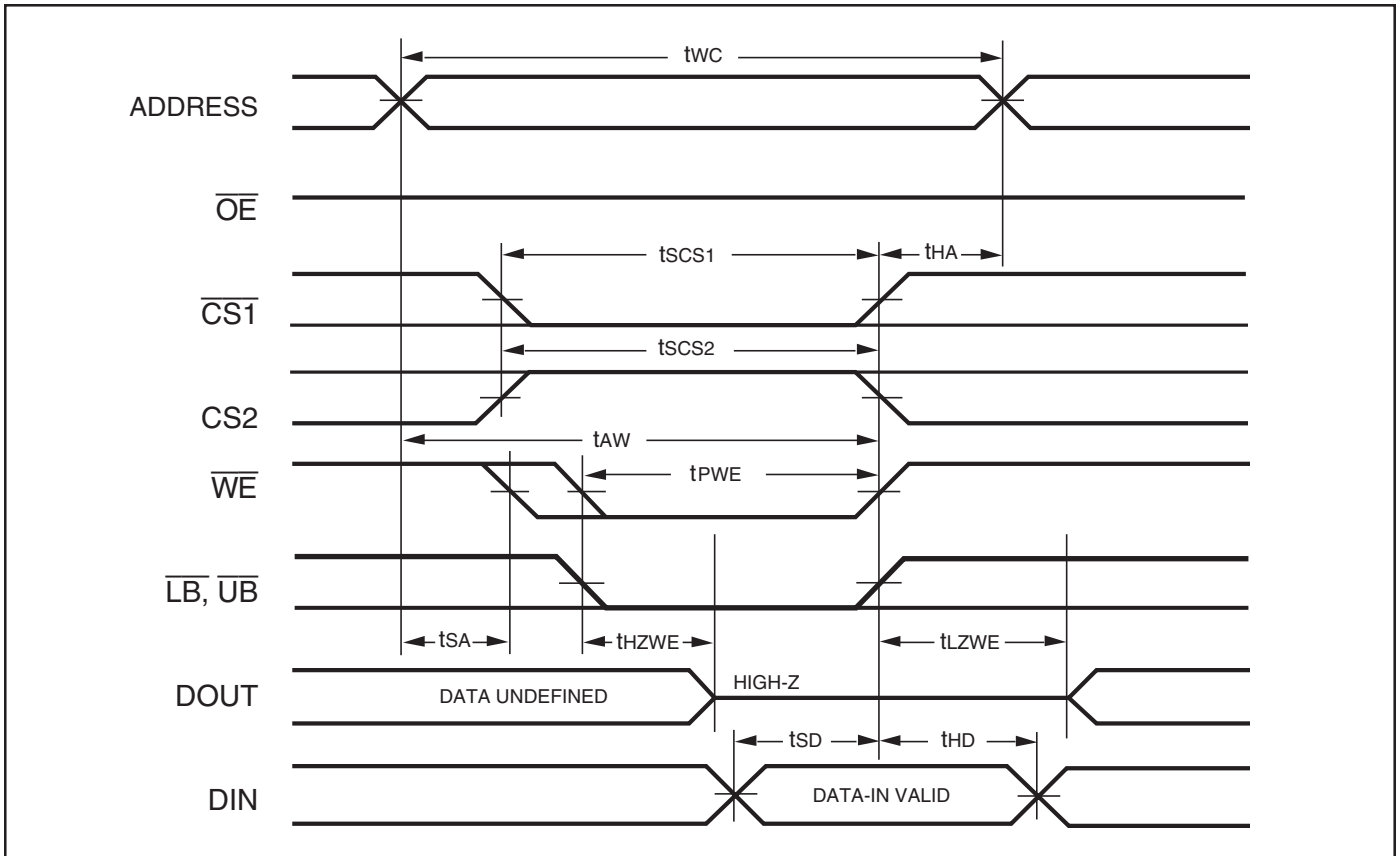
**AC WAVEFORMS**

**WRITE CYCLE NO. 2 ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)**



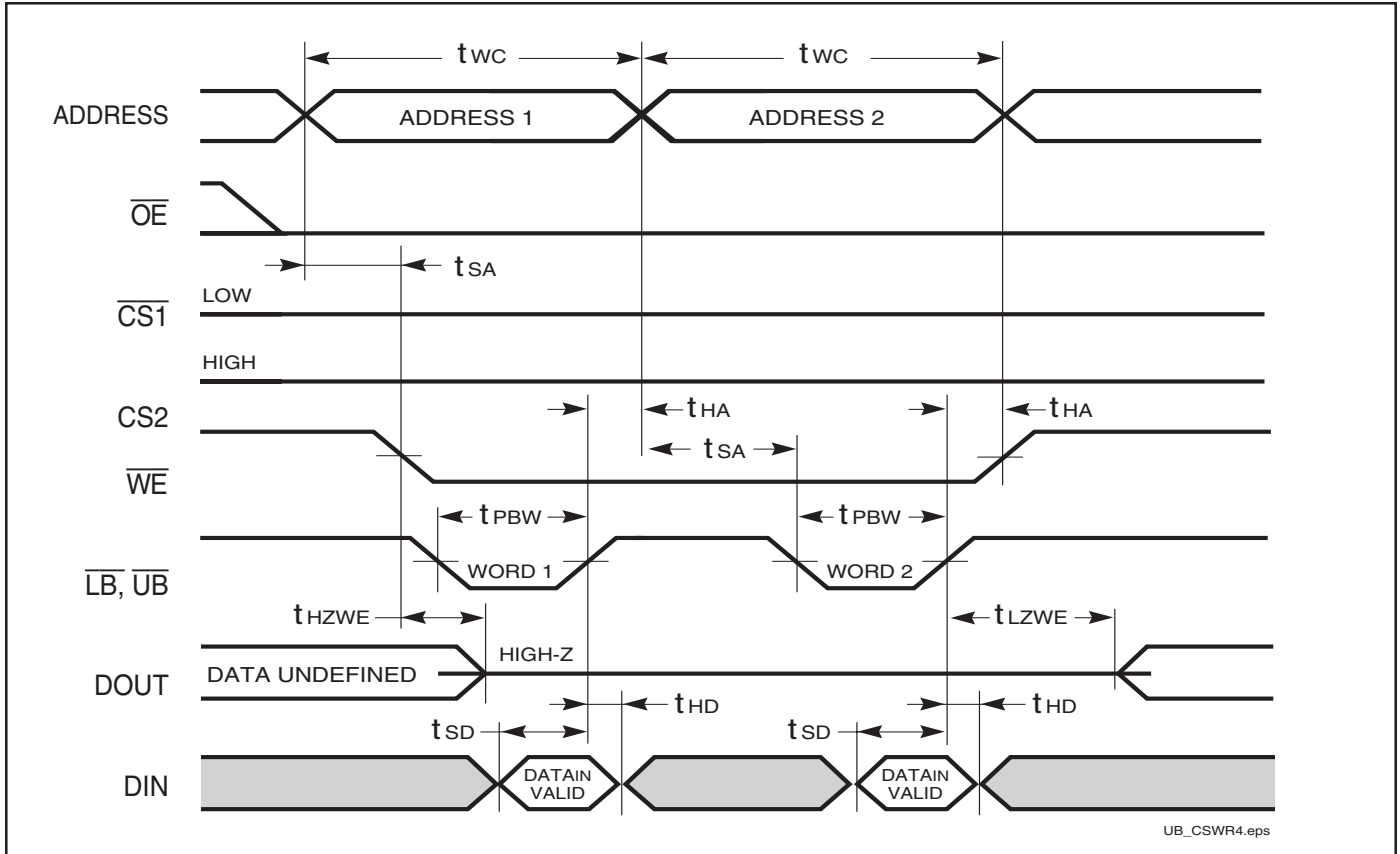
**AC WAVEFORMS**

**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



AC WAVEFORMS

WRITE CYCLE NO. 4 ( $\overline{UB}/\overline{LB}$  Controlled)

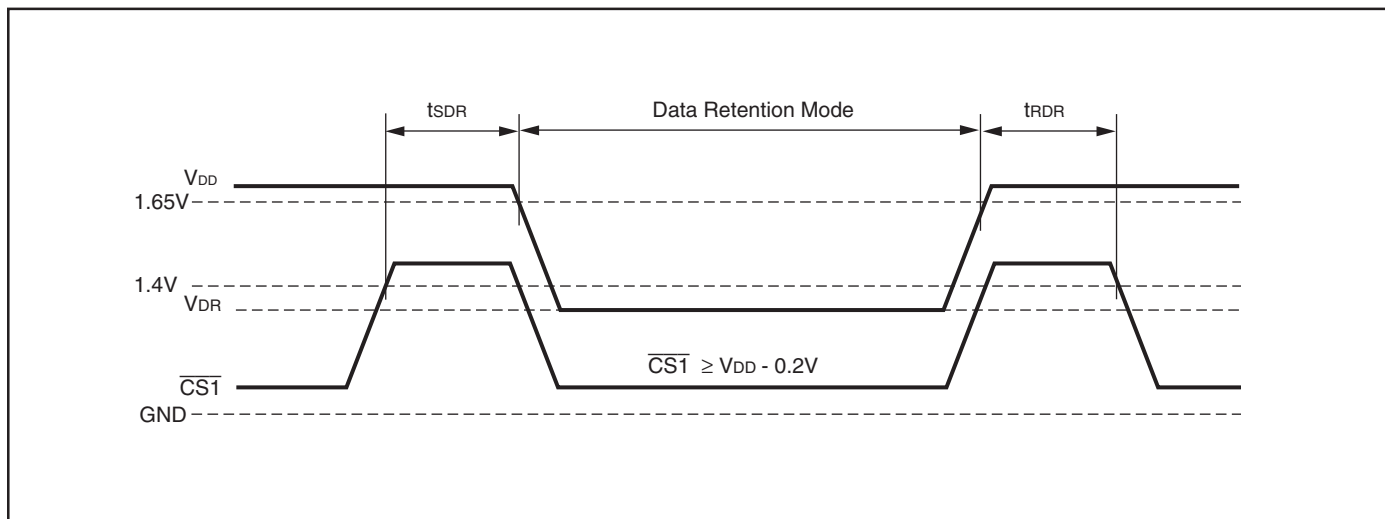


**DATA RETENTION SWITCHING CHARACTERISTICS (LL)**

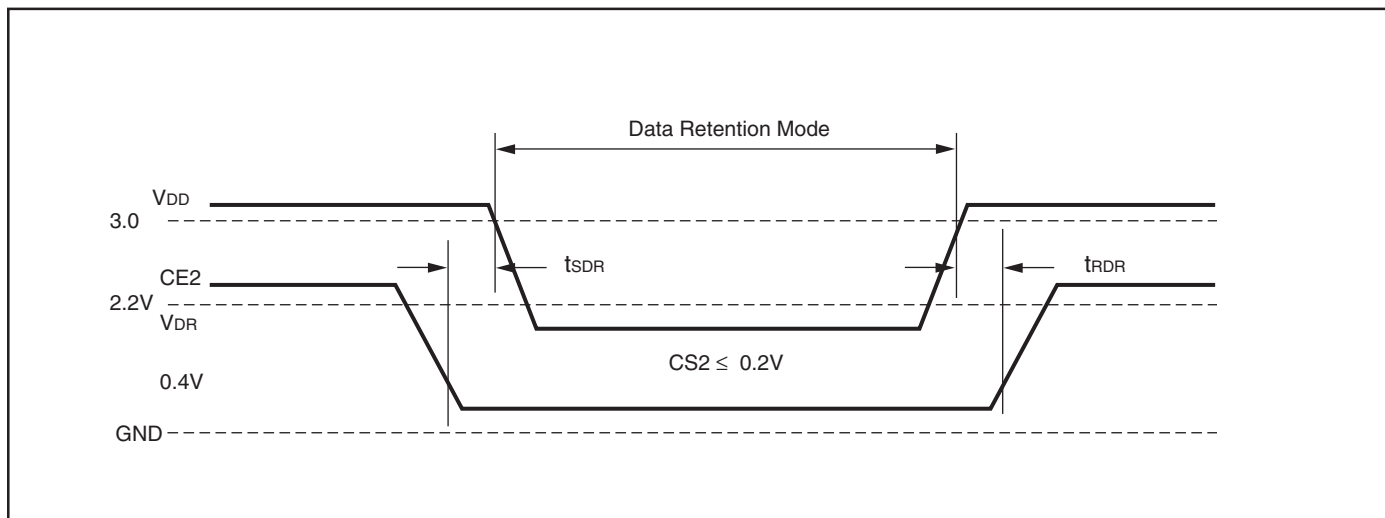
Symbol	Parameter	Test Condition	Options	Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>dd</sub> = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$	A, A1 A2 A3	—	5 — —	15 25 65	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform		t <sub>RC</sub>	—	—	ns

**Note 1:** Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

**DATA RETENTION WAVEFORM ( $\overline{CS1}$  Controlled)**



**DATA RETENTION WAVEFORM (CS2 Controlled)**



**ORDERING INFORMATION**
**IS65WV12816ALL (1.65V - 2.2V)**
**Temperature Range (A): 0°C to +70°C**

Speed (ns)	Order Part No.	Package
70	IS65WV12816ALL-70TA	TSOP
	IS65WV12816ALL-70BA	mini BGA (6mm x 8mm)
	IS65WV12816ALL-70B2A	mini BGA (6mm x 8mm), 2 CS Option

**Temperature Range (A1): -40°C to +85°C**

Speed (ns)	Order Part No.	Package
70	IS65WV12816ALL-70TA1	TSOP
	IS65WV12816ALL-70BA1	mini BGA (6mm x 8mm)
	IS65WV12816ALL-70B2A1	mini BGA (6mm x 8mm), 2 CS Option

**Temperature Range (A2): -40°C to +105°C**

Speed (ns)	Order Part No.	Package
70	IS65WV12816ALL-70TA2	TSOP
	IS65WV12816ALL-70BA2	mini BGA (6mm x 8mm)
	IS65WV12816ALL-70B2A2	mini BGA (6mm x 8mm), 2 CS Option

**Temperature Range (A3): -40°C to +125°C**

Speed (ns)	Order Part No.	Package
70	IS65WV12816ALL-70TA3	TSOP
	IS65WV12816ALL-70BA3	mini BGA (6mm x 8mm)
	IS65WV12816ALL-70B2A3	mini BGA (6mm x 8mm), 2 CS Option

## ORDERING INFORMATION

## IS65WV12816BLL (2.5V - 3.6V)

## Temperature Range (A): 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IS65WV12816BLL-55TA	TSOP
	IS65WV12816BLL-55BA	mini BGA (6mm x 8mm)
	IS65WV12816BLL-55B2A	mini BGA (6mm x 8mm), 2 CS Option
70	IS65WV12816BLL-70TA	TSOP
	IS65WV12816BLL-70BA	mini BGA (6mm x 8mm)
	IS65WV12816BLL-70B2A	mini BGA (6mm x 8mm), 2 CS Option

## Temperature Range (A1): -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS65WV12816BLL-55TA1	TSOP
	IS65WV12816BLL-55BA1	mini BGA (6mm x 8mm)
	IS65WV12816BLL-55B2A1	mini BGA (6mm x 8mm), 2 CS Option
70	IS65WV12816BLL-70TA1	TSOP
	IS65WV12816BLL-70BA1	mini BGA (6mm x 8mm)
	IS65WV12816BLL-70B2A1	mini BGA (6mm x 8mm), 2 CS Option



## ORDERING INFORMATION (continual)

## IS65WV12816BLL (2.5V - 3.6V)

## TEMPERATURE RANGE (A2): -40°C TO +105°C

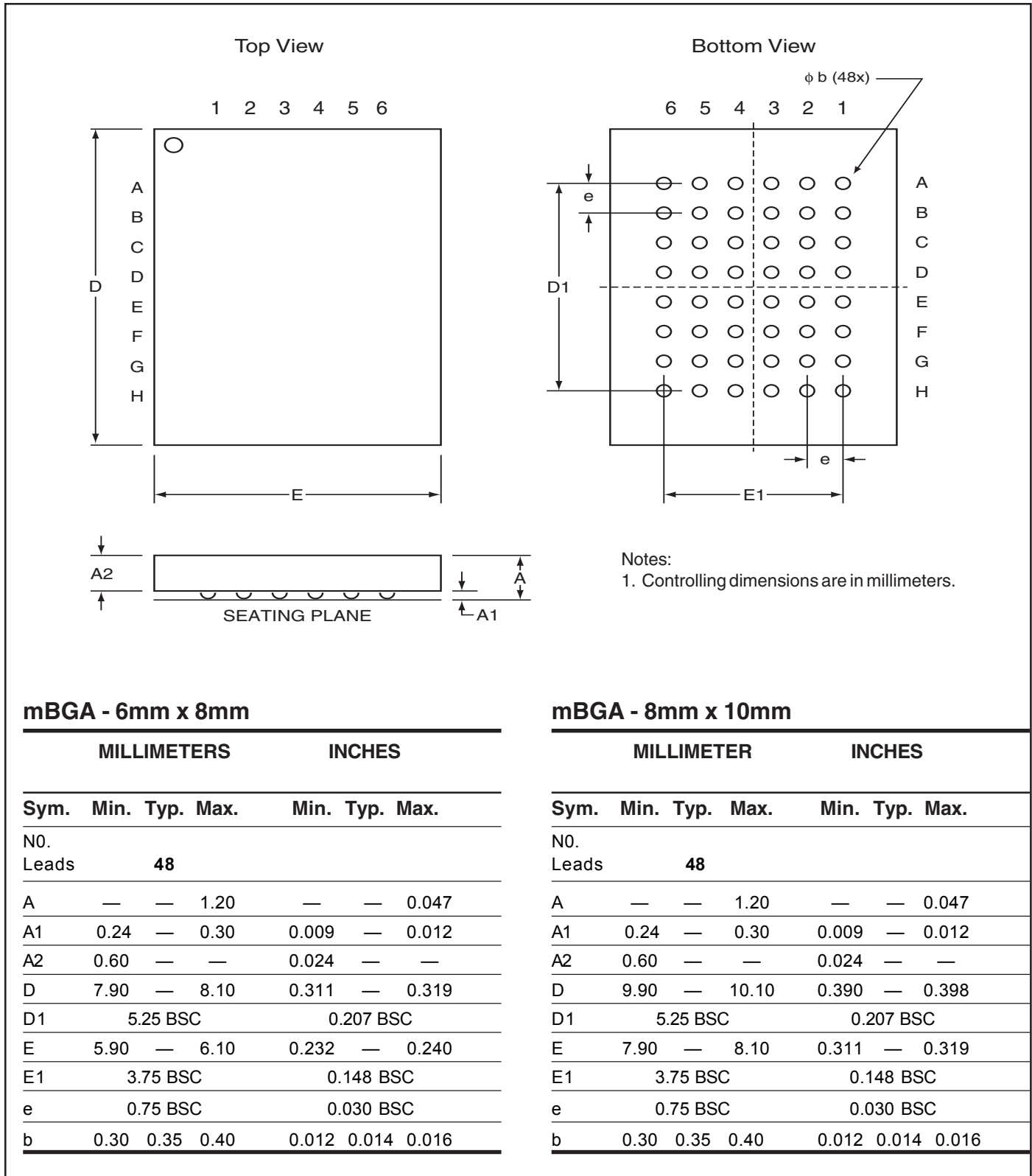
Speed (ns)	Order Part No.	Package
55	IS65WV12816BLL-55TA2	TSOP
	IS65WV12816BLL-55BA2	mini BGA (6mm x 8mm)
	IS65WV12816BLL-55B2A2	mini BGA (6mm x 8mm), 2 CS Option
70	IS65WV12816BLL-70TA2	TSOP
	IS65WV12816BLL-70BA2	mini BGA (6mm x 8mm)
	IS65WV12816BLL-70B2A2	mini BGA (6mm x 8mm), 2 CS Option

## Temperature Range (A3): -40°C to +125°C

Speed (ns)	Order Part No.	Package
55	IS65WV12816BLL-55TA3	TSOP
	IS65WV12816BLL-55TLA3	TSOP, Lead-free
	IS65WV12816BLL-55BA3	mini BGA (6mm x 8mm)
	IS65WV12816BLL-55BLA3	mini BGA (6mm x 8mm), Lead-free
	IS65WV12816BLL-55B2A3	mini BGA (6mm x 8mm), 2 CS Option
70	IS65WV12816BLL-70TA3	TSOP
	IS65WV12816BLL-70BA3	mini BGA (6mm x 8mm)
	IS65WV12816BLL-70B2A3	mini BGA (6mm x 8mm), 2 CS Option

# PACKAGING INFORMATION

## Mini Ball Grid Array Package Code: B (48-pin)



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Rev. D  
01/15/03

# PACKAGING INFORMATION

Plastic TSOP  
 Package Code: T (Type II)



**Notes:**

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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Rev. F  
 06/18/03

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