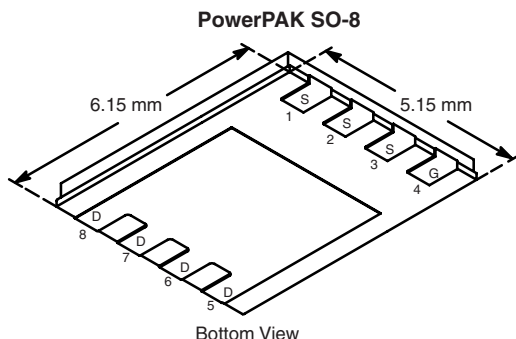




P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.0019 at $V_{GS} = -10$ V	- 60 ^d	128 nC
	0.0030 at $V_{GS} = -4.5$ V	- 60 ^d	



FEATURES

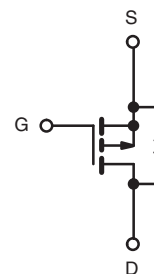
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Adaptor Switch
- Battery Switch
- Load Switch



Ordering Information: Si7141DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	- 60 ^d	A
	$T_C = 70$ °C	- 60 ^d	
	$T_A = 25$ °C	- 42.7 ^b	
	$T_A = 70$ °C	- 34 ^b	
Pulsed Drain Current	I_{DM}	- 100	A
Continuous Source-Drain Diode Current	$T_C = 25$ °C	- 60 ^d	
	$T_A = 25$ °C	- 5.6 ^{a, b}	
Avalanche Current	I_{AS}	- 40	mJ
Single-Pulse Avalanche Energy	E_{AS}	80	
Maximum Power Dissipation	$T_C = 25$ °C	104	W
	$T_C = 70$ °C	66.6	
	$T_A = 25$ °C	6.25 ^{a, b}	
	$T_A = 70$ °C	4.0 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R_{thJA}	15	20	°C/W
Maximum Junction-to-Case	R_{thJC}	0.9	1.2	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. $t = 10$ s.

c. Maximum under Steady State conditions is 54 °C/W.

d. Package limited.

e. See Solder Profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

f. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

Si7141DP

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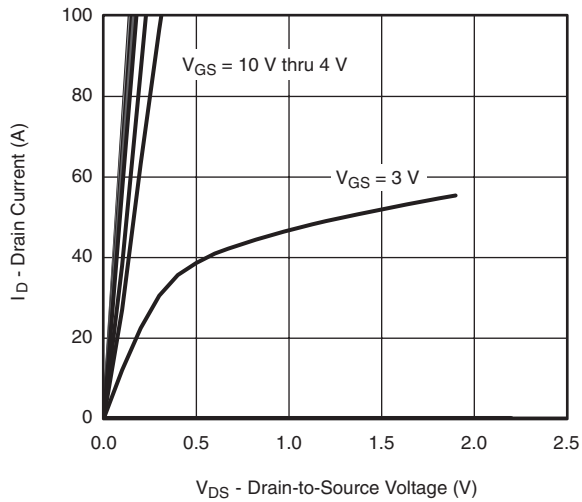
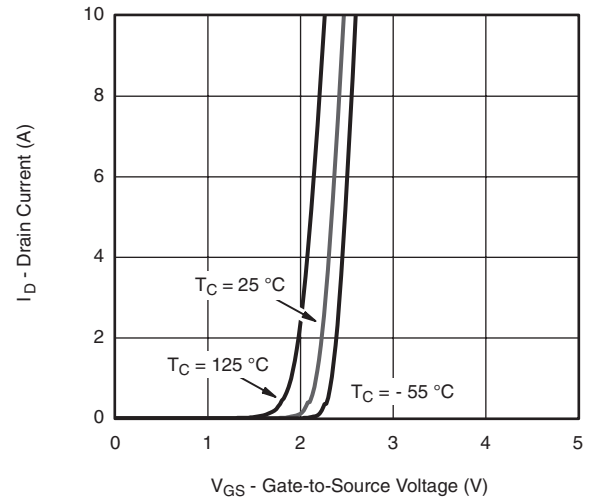
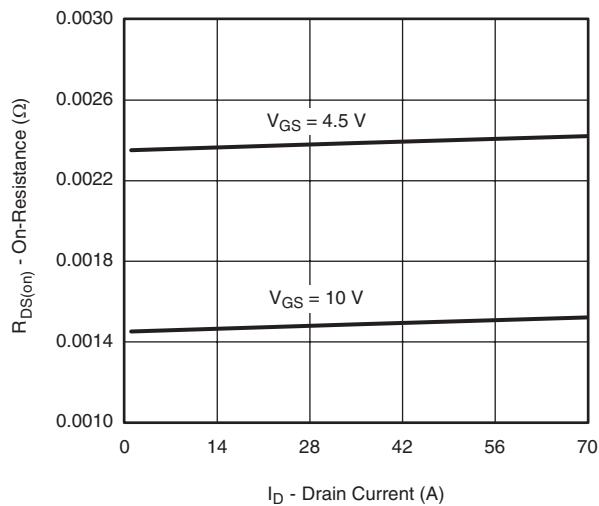
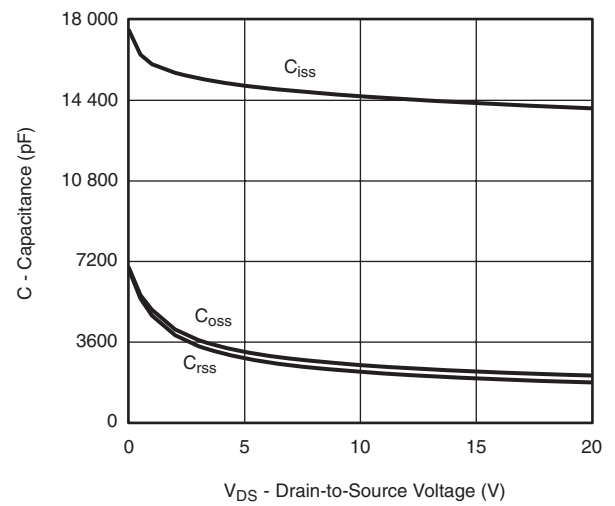
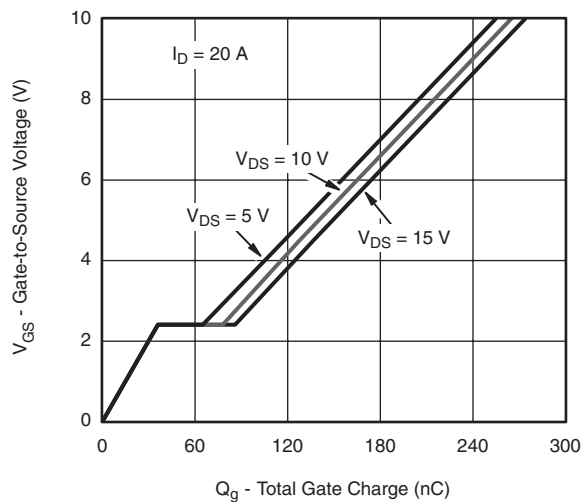
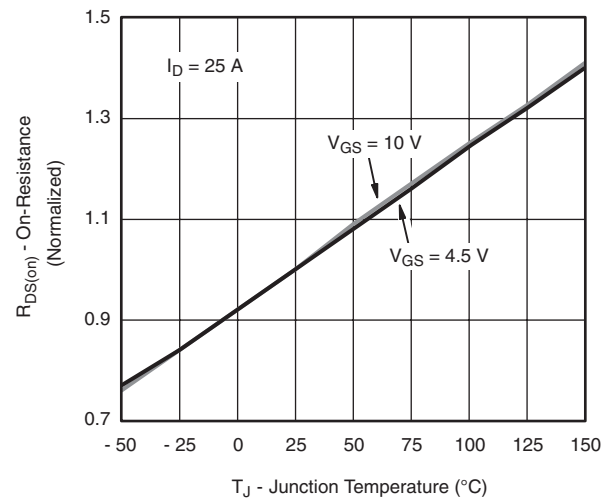


SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 16		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			5.7		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1.0		- 2.3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C			- 5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 10 V, V _{GS} = - 10 V	- 40			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 25 A		0.0015	0.0019	Ω
		V _{GS} = - 4.5 V, I _D = - 20 A		0.0024	0.0030	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 25 A		103		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		14 300		pF
Output Capacitance	C _{oss}			2300		
Reverse Transfer Capacitance	C _{rss}			2600		
Total Gate Charge	Q _g	V _{DS} = - 10 V, V _{GS} = - 10 V, I _D = - 20 A		265	400	nC
		V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 20 A		128	194	
Gate-Source Charge	Q _{gs}			36		
Gate-Drain Charge	Q _{gd}			42		
Gate Resistance	R _g	f = 1 MHz	0.4	1.7	3.4	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 1 Ω I _D ≡ - 10 A, V _{GEN} = - 10 V, R _g = 1 Ω		25	50	ns
Rise Time	t _r			16	30	
Turn-Off DelayTime	t _{d(off)}			130	220	
Fall Time	t _f			38	70	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 1 Ω I _D ≡ - 10 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		130	220	
Rise Time	t _r			120	200	
Turn-Off DelayTime	t _{d(off)}			100	180	
Fall Time	t _f			55	100	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 60	A
Pulse Diode Forward Current	I _{SM}				- 100	
Body Diode Voltage	V _{SD}	I _S = - 5 A, V _{GS} = 0 V		- 0.71	- 1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 10 A, dI/dt = 100 A/μs, T _J = 25 °C		42	80	ns
Body Diode Reverse Recovery Charge	Q _{rr}			36	72	nC
Reverse Recovery Fall Time	t _a			18		ns
Reverse Recovery Rise Time	t _b			24		

Notes:

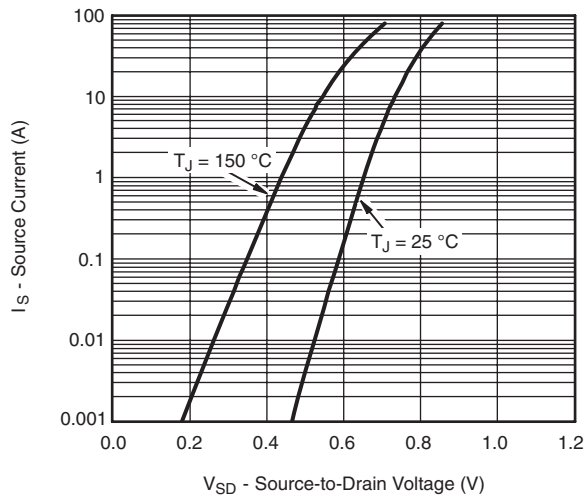
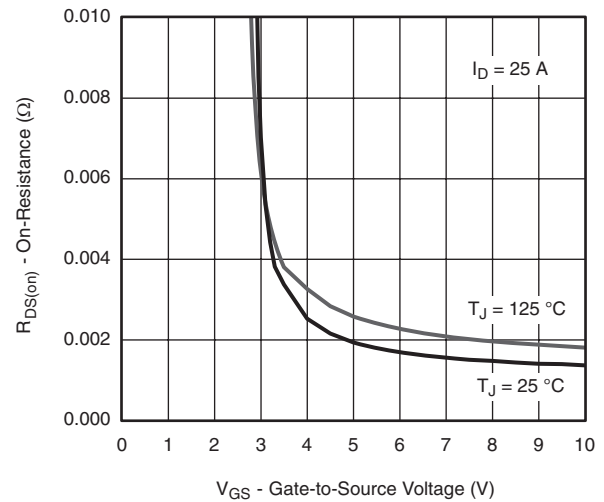
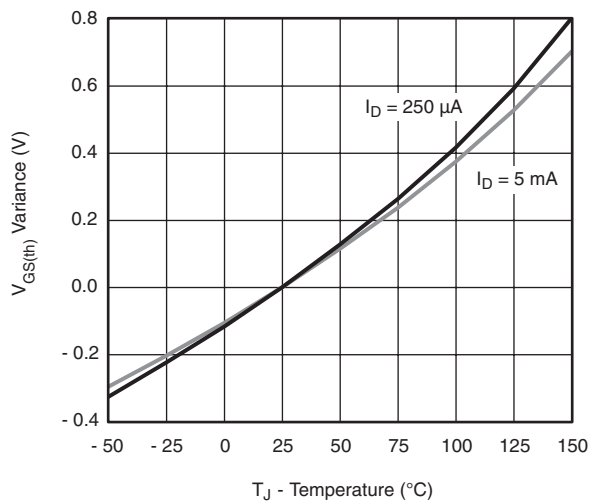
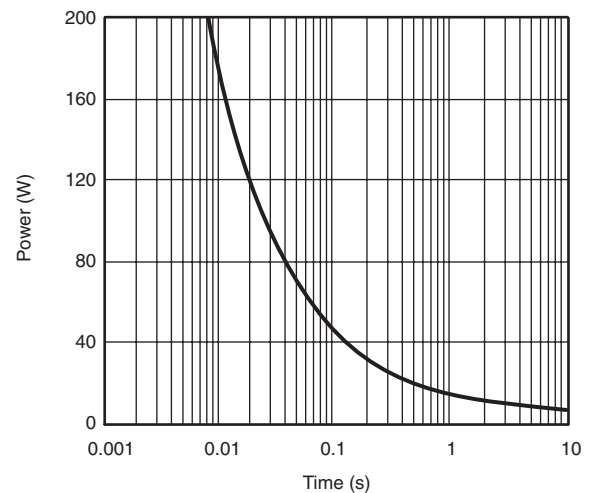
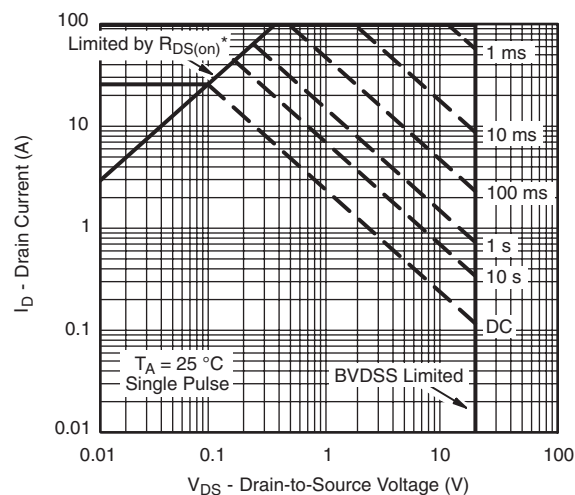
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

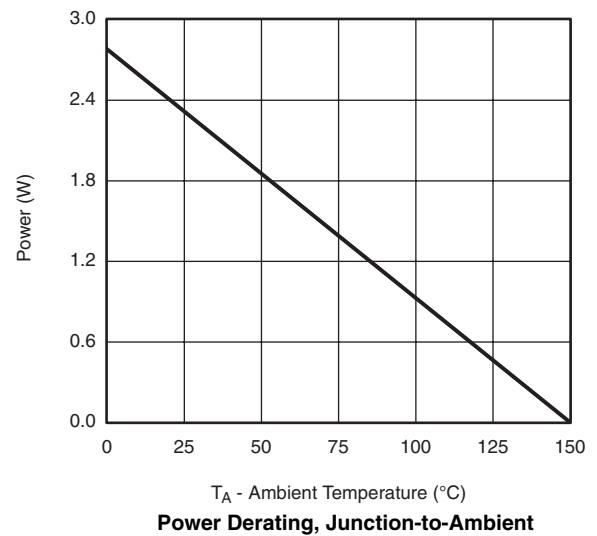
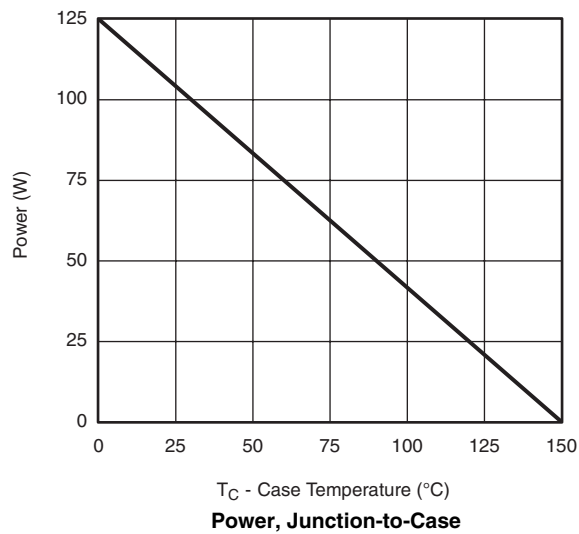
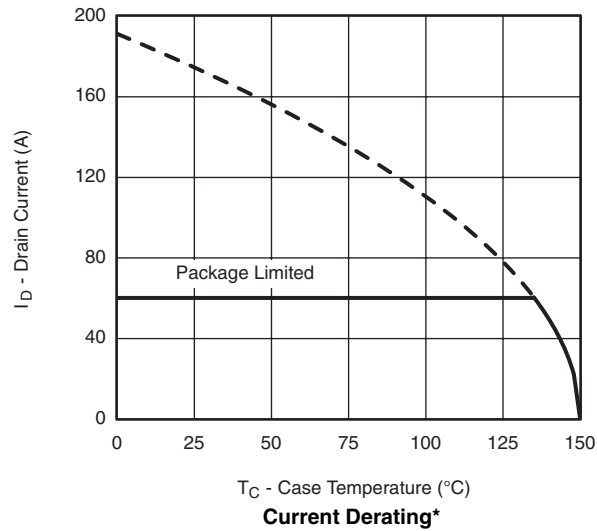
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

Si7141DP

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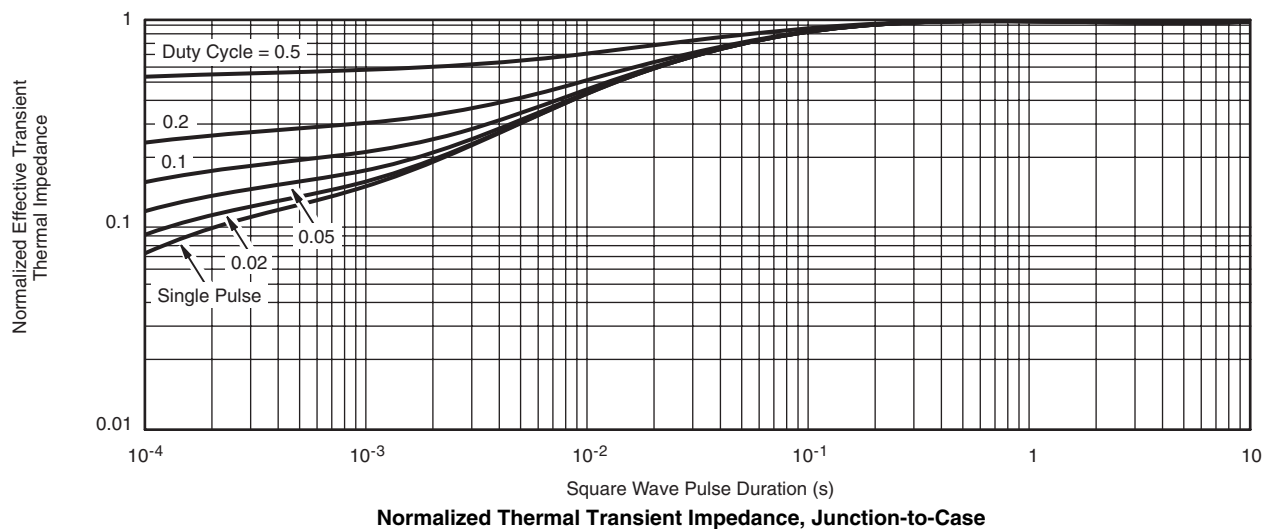
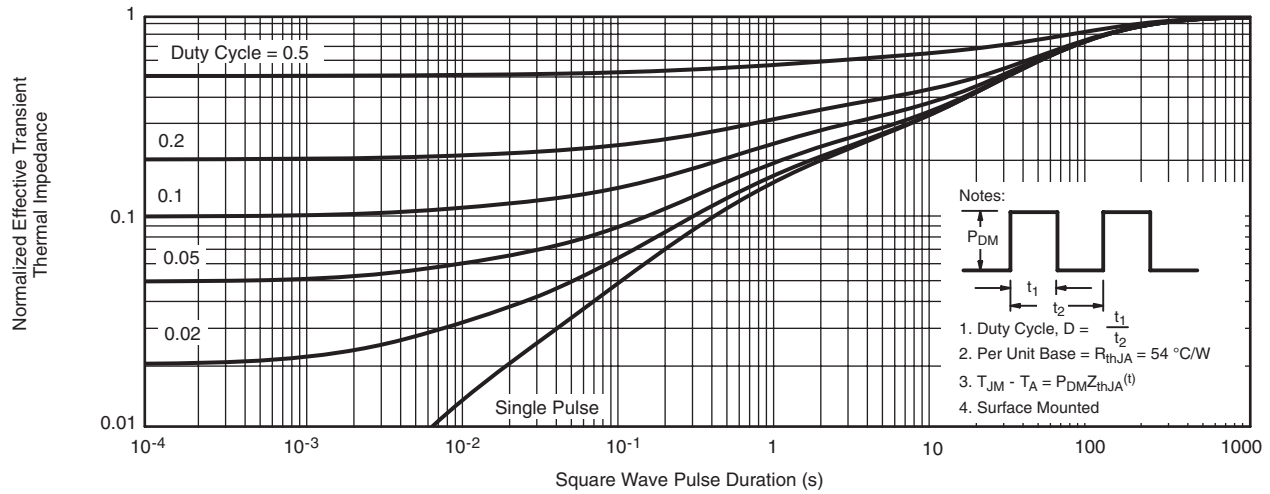
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area**


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si7141DP

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**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9