

FEATURES

2M x 8 MRAM Memory

- +3.3 Volt power supply
- Fast 35 ns read/write cycle
- SRAM compatible timing
- Unlimited read & write endurance
- Data always non-volatile for >20-years at temperature
- RoHS-compliant small footprint BGA and TSOP2 packages
- All products meet MSL-3 moisture sensitivity level



BENEFITS

- One memory replaces FLASH, SRAM, EEPROM and BBSRAM in systems for simpler, more efficient designs
- Improves reliability by replacing battery-backed SRAM



INTRODUCTION

The **MR4A08B** is a 16,777,216-bit magnetoresistive random access memory (MRAM) device organized as 2,097,152 words of 8 bits. The MR4A08B offers SRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The MR4A08B is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.



The **MR4A08B** is available in small footprint 400-mil, 44-lead plastic small-outline TSOP type-II package or 10 mm x 10 mm, 48-pin ball grid array (BGA) package with 0.75 mm ball centers. These packages are compatible with similar low-power SRAM products and other non-volatile RAM products.

The **MR4A08B** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial (0 to +70 °C) and industrial (-40 to +85 °C) operating temperature range options.

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1. DEVICE PIN ASSIGNMENT

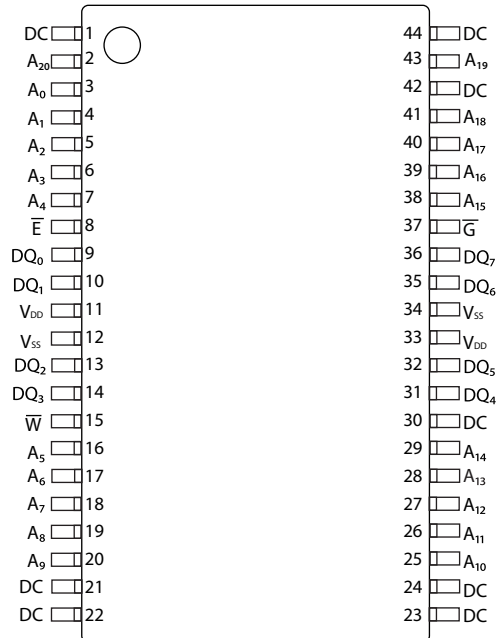
Figure 1.1 Block Diagram



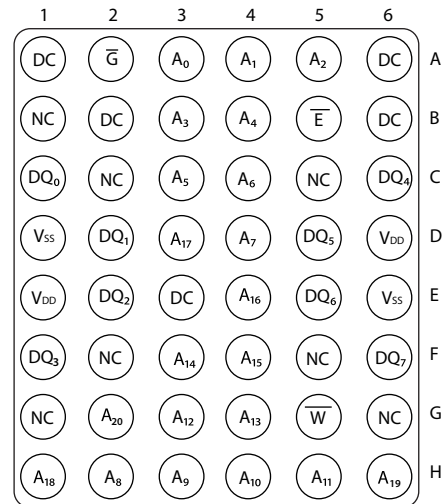
Table 1.1 Pin Functions

| Signal Name | Function |
|-------------|----------------|
| A | Address Input |
| \bar{E} | Chip Enable |
| \bar{W} | Write Enable |
| \bar{G} | Output Enable |
| DQ | Data I/O |
| V_{DD} | Power Supply |
| V_{SS} | Ground |
| DC | Do Not Connect |
| NC | No Connection |

Figure 1.2 Pin Diagrams for Available Packages (Top View)



44 Pin TSOP2



48 Pin FBGA

Table 1.2 Operating Modes

| \bar{E} ¹ | \bar{G} ¹ | \bar{W} ¹ | Mode | V _{DD} Current | DQ[7:0] ² |
|------------------------|------------------------|------------------------|-----------------|-------------------------------------|----------------------|
| H | X | X | Not selected | I _{SB1} , I _{SB2} | Hi-Z |
| L | H | H | Output disabled | I _{DDR} | Hi-Z |
| L | L | H | Byte Read | I _{DDR} | D _{Out} |
| L | X | L | Byte Write | I _{DDW} | D _{in} |

¹ H = high, L = low, X = don't care

² Hi-Z = high impedance

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2.1 Absolute Maximum Ratings¹

| Parameter | Symbol | Value | Unit |
|---|------------------|------------------------|------|
| Supply voltage ² | V_{DD} | -0.5 to 4.0 | V |
| Voltage on any pin ² | V_{IN} | -0.5 to $V_{DD} + 0.5$ | V |
| Output current per pin | I_{OUT} | ± 20 | mA |
| Package power dissipation ³ | P_D | 0.600 | W |
| Temperature under bias | | | |
| MR4A08B (Commercial) | T_{BIAS} | -10 to 85 | °C |
| MR4A08BC (Industrial) | | -45 to 95 | |
| Storage Temperature | T_{stg} | -55 to 150 | °C |
| Lead temperature during solder (3 minute max) | T_{Lead} | 260 | °C |
| Maximum magnetic field during write | | | |
| MR4A08B (All Temperatures) | H_{max_write} | 8000 | A/m |
| Maximum magnetic field during read or standby | H_{max_read} | 8000 | A/m |

¹ Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

² All voltages are referenced to V_{SS} .

³ Power dissipation capability depends on package characteristics and use environment.

Table 2.2 Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|----------|-------------------|---------|-----------------------------|------|
| Power supply voltage | V_{DD} | 3.0 ¹ | 3.3 | 3.6 | V |
| Write inhibit voltage | V_{WI} | 2.5 | 2.7 | 3.0 ¹ | V |
| Input high voltage | V_{IH} | 2.2 | - | $V_{DD} + 0.3$ ² | V |
| Input low voltage | V_{IL} | -0.5 ³ | - | 0.8 | V |
| Temperature under bias MR4A08B (Commercial) MR4A08BC (Industrial) | T_A | 0 -40 | | 70 85 | °C |

1. There is a 2 ms startup time once V_{DD} exceeds $V_{DD}(\min)$. See **Power Up and Power Down Sequencing** below.
2. $V_{IH}(\max) = V_{DD} + 0.3 V_{DC}$; $V_{IH}(\max) = V_{DD} + 2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.
3. $V_{IL}(\min) = -0.5 V_{DC}$; $V_{IL}(\min) = -2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

Power Up and Power Down Sequencing

MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds $V_{DD}(\min)$, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The \bar{E} and \bar{W} control signals should track V_{DD} on power up to $V_{DD} - 0.2$ V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives \bar{E} and \bar{W} should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above $V_{DD}(\min)$.

Figure 2.1 Power and Power Down Diagram



Table 2.3 DC Characteristics

| Parameter | Symbol | Min | Typical | Max | Unit |
|--|--------------|-----------------------|---------|-----------------------|---------|
| Input leakage current | $I_{lkg(I)}$ | - | - | ± 1 | μA |
| Output leakage current | $I_{lkg(O)}$ | - | - | ± 1 | μA |
| Output low voltage ($I_{OL} = +4 \text{ mA}$) ($I_{OL} = +100 \mu A$) | V_{OL} | - | - | 0.4 $V_{SS} + 0.2$ | V |
| Output high voltage ($I_{OH} = -4 \text{ mA}$) ($I_{OH} = -100 \mu A$) | V_{OH} | 2.4 $V_{DD} - 0.2$ | - | - | V |

Table 2.4 Power Supply Characteristics

| Parameter | Symbol | Typical | Max | Unit |
|--|-----------|---------|-----|------|
| AC active supply current - read modes ¹ ($I_{OUT} = 0 \text{ mA}$, $V_{DD} = \text{max}$) | I_{DDR} | 60 | 68 | mA |
| AC active supply current - write modes ¹ ($V_{DD} = \text{max}$) | I_{DDW} | 152 | 180 | mA |
| AC standby current ($V_{DD} = \text{max}$, $\bar{E} = V_{IH}$) <i>no other restrictions on other inputs</i> | I_{SB1} | 9 | 14 | mA |
| CMOS standby current ($\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$) ($V_{DD} = \text{max}$, $f = 0 \text{ MHz}$) | I_{SB2} | 5 | 9 | mA |

¹ All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. TIMING SPECIFICATIONS

Table 3.1 Capacitance¹

| Parameter | Symbol | Typical | Max | Unit |
|---------------------------|-----------|---------|-----|------|
| Address input capacitance | C_{In} | - | 6 | pF |
| Control input capacitance | C_{In} | - | 6 | pF |
| Input/Output capacitance | $C_{I/O}$ | - | 8 | pF |

¹ $f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25 \text{ }^\circ\text{C}$, periodically sampled rather than 100% tested.

Table 3.2 AC Measurement Conditions

| Parameter | Value | Unit |
|---|----------------|------|
| Logic input timing measurement reference level | 1.5 | V |
| Logic output timing measurement reference level | 1.5 | V |
| Logic input pulse levels | 0 or 3.0 | V |
| Input rise/fall time | 2 | ns |
| Output load for low and high impedance parameters | See Figure 3.1 | |
| Output load for all other timing parameters | See Figure 3.2 | |

Figure 3.1 Output Load Test Low and High



Figure 3.2 Output Load Test All Others



Read Mode

Table 3.3 Read Cycle Timing¹

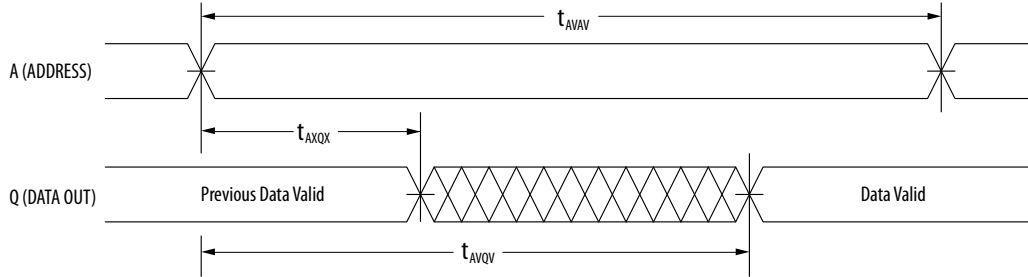
| Parameter | Symbol | Min | Max | Unit |
|---|------------|-----|-----|------|
| Read cycle time | t_{AVAV} | 35 | - | ns |
| Address access time | t_{AVQV} | - | 35 | ns |
| Enable access time ² | t_{ELQV} | - | 35 | ns |
| Output enable access time | t_{GLQV} | - | 15 | ns |
| Output hold from address change | t_{AXQX} | 3 | - | ns |
| Enable low to output active ³ | t_{ELQX} | 3 | - | ns |
| Output enable low to output active ³ | t_{GLQX} | 0 | - | ns |
| Enable high to output Hi-Z ³ | t_{EHQZ} | 0 | 15 | ns |
| Output enable high to output Hi-Z ³ | t_{GHQZ} | 0 | 10 | ns |

¹ \bar{W} is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

² Addresses valid before or at the same time \bar{E} goes low.

³ This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage.

Figure 3.3A Read Cycle 1



Note: Device is continuously selected ($\bar{E} \leq V_{IL}$, $\bar{G} \leq V_{IL}$).

Figure 3.3B Read Cycle 2

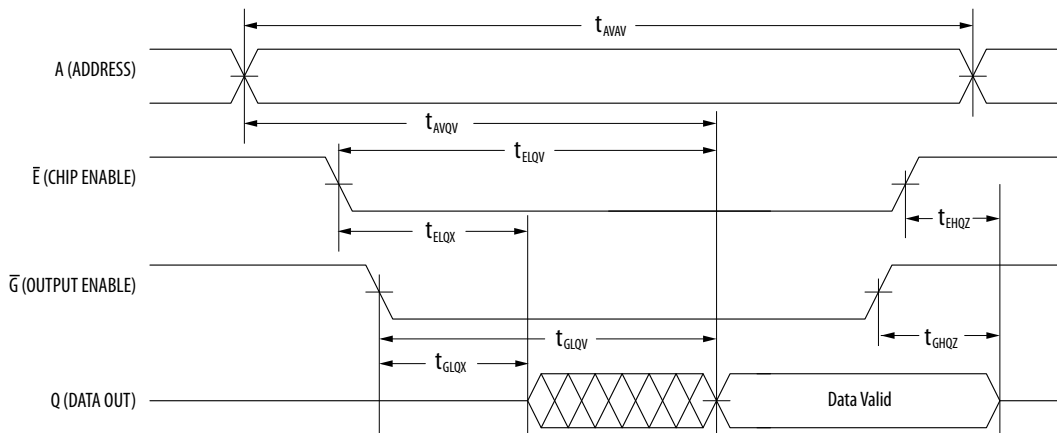


Table 3.4 Write Cycle Timing 1 (\overline{W} Controlled)¹

| Parameter | Symbol | Min | Max | Unit |
|--|--------------------------|-----|-----|------|
| Write cycle time ² | t_{AVAV} | 35 | - | ns |
| Address set-up time | t_{AVWL} | 0 | - | ns |
| Address valid to end of write (\overline{G} high) | t_{AVWH} | 18 | - | ns |
| Address valid to end of write (\overline{G} low) | t_{AVWH} | 20 | - | ns |
| Write pulse width (\overline{G} high) | t_{WLWH} t_{WLEH} | 15 | - | ns |
| Write pulse width (\overline{G} low) | t_{WLWH} t_{WLEH} | 15 | - | ns |
| Data valid to end of write | t_{DVWH} | 10 | - | ns |
| Data hold time | t_{WHDX} | 0 | - | ns |
| Write low to data Hi-Z ³ | t_{WLQZ} | 0 | 12 | ns |
| Write high to output active ³ | t_{WHQX} | 3 | - | ns |
| Write recovery time | t_{WHAX} | 12 | - | ns |

¹ All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} , \overline{E} or $\overline{UB/LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

² All write cycle timings are referenced from the last valid address to the first transition address.

³ This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage. At any given voltage or temperature, $t_{WLQZ}(\text{max}) < t_{WHQX}(\text{min})$

Figure 3.4 Write Cycle Timing 1 (\overline{W} Controlled)

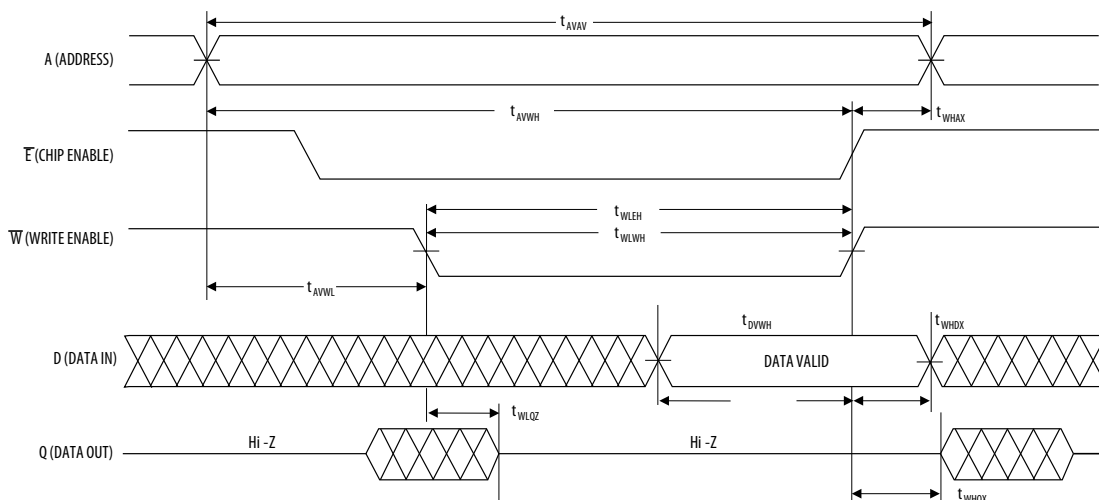


Table 3.5 Write Cycle Timing 2 (\bar{E} Controlled)¹

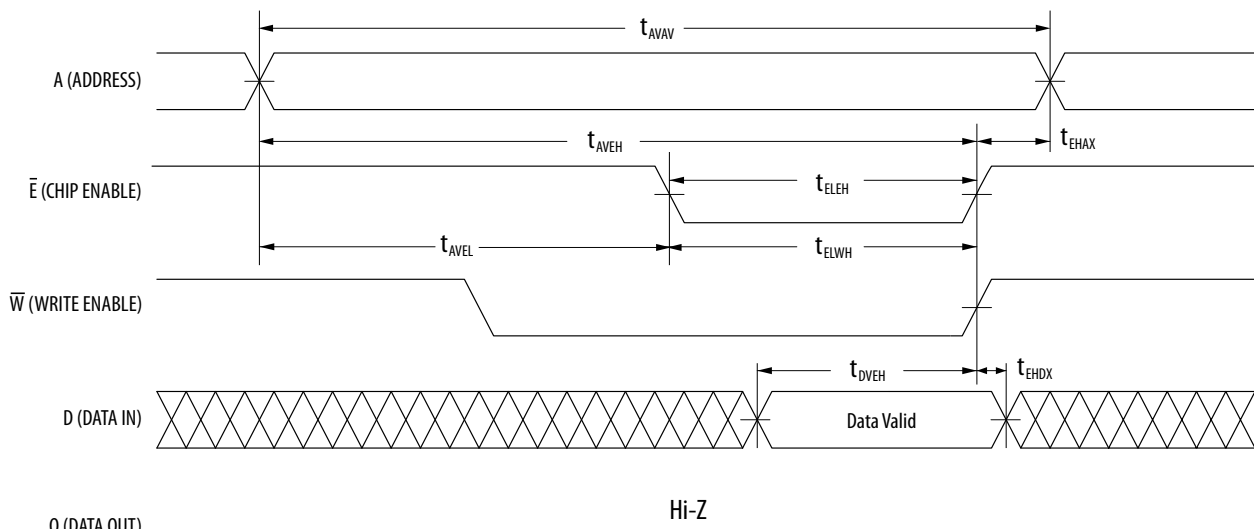
| Parameter | Symbol | Min | Max | Unit |
|--|--------------------------|-----|-----|------|
| Write cycle time ² | t_{AVAV} | 35 | - | ns |
| Address set-up time | t_{AVEL} | 0 | - | ns |
| Address valid to end of write (\bar{G} high) | t_{AVEH} | 18 | - | ns |
| Address valid to end of write (\bar{G} low) | t_{AVEH} | 20 | - | ns |
| Enable to end of write (\bar{G} high) | t_{ELEH} t_{ELWH} | 15 | - | ns |
| Enable to end of write (\bar{G} low) ³ | t_{ELEH} t_{ELWH} | 15 | - | ns |
| Data valid to end of write | t_{DVEH} | 10 | - | ns |
| Data hold time | t_{EHDX} | 0 | - | ns |
| Write recovery time | t_{EHAX} | 12 | - | ns |

¹ All write occurs during the overlap of \bar{E} low and \bar{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \bar{G} goes low at the same time or after \bar{W} goes low, the output will remain in a high impedance state. After \bar{W} , \bar{E} or \bar{UB}/\bar{LB} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \bar{E} being asserted low in one cycle to \bar{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

² All write cycle timings are referenced from the last valid address to the first transition address.

³ If \bar{E} goes low at the same time or after \bar{W} goes low, the output will remain in a high-impedance state. If \bar{E} goes high at the same time or before \bar{W} goes high, the output will remain in a high-impedance state.

Figure 3.5 Write Cycle Timing 2 (\bar{E} Controlled)



4. ORDERING INFORMATION

Figure 4.1 Part Numbering System

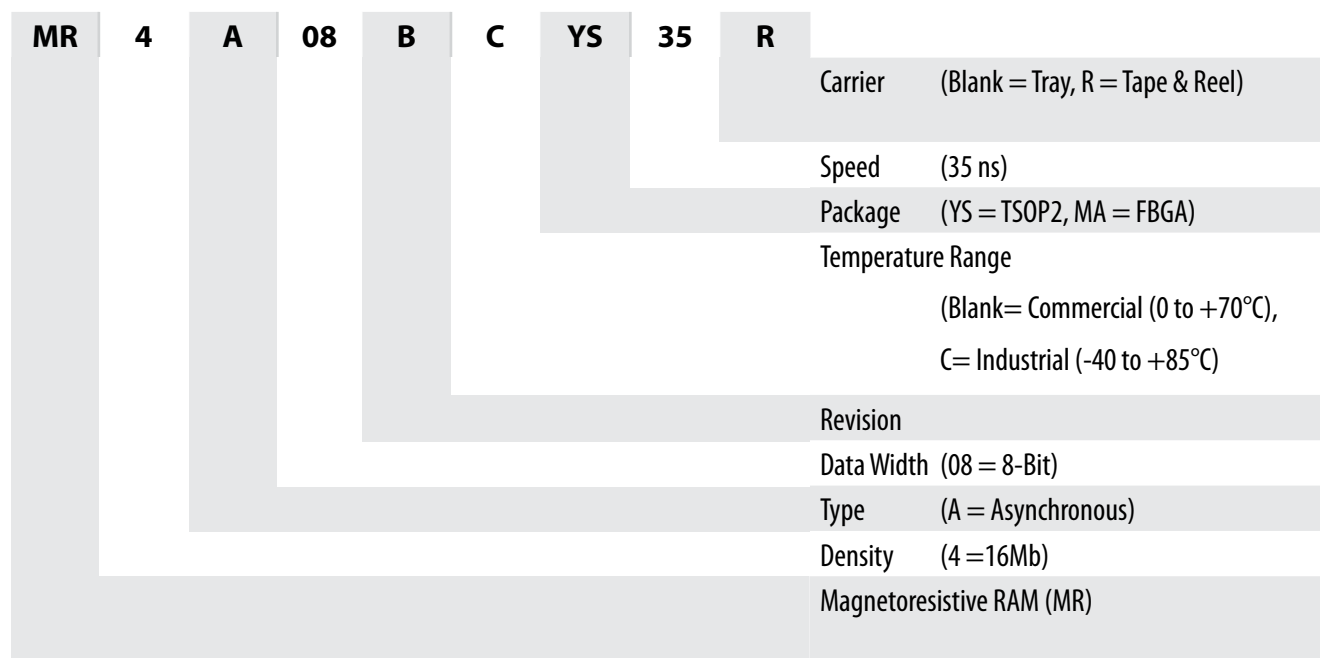


Table 4.1 Available Parts

| Grade | Temp Range | Package | Shipping Container | Part Number |
|------------|--------------|----------|--------------------|---------------|
| Commercial | 0 to +70°C | 44-TSOP2 | Tray | MR4A08BYS35 |
| | | | Tape and Reel | MR4A08BYS35R |
| | | 48-BGA | Tray | MR4A08BMA35 |
| | | | Tape and Reel | MR4A08BMA35R |
| Industrial | -40 to +85°C | 44-TSOP2 | Tray | MR4A08BCYS35 |
| | | | Tape and Reel | MR4A08BCYS35R |
| | | 48-BGA | Tray | MR4A08BCMA35 |
| | | | Tape and Reel | MR4A08BCMA35R |

Figure 5.2 FBGA



| Ref | Min | Nominal | Max |
|-----|-----------|---------|------|
| A | 1.19 | 1.27 | 1.35 |
| A1 | 0.22 | 0.27 | 0.32 |
| b | 0.31 | 0.36 | 0.41 |
| D | 10.00 BSC | | |
| E | 10.00 BSC | | |
| D1 | 5.25 BSC | | |
| E1 | 3.75 BSC | | |
| DE | 0.375 BSC | | |
| SE | 0.375 BSC | | |
| e | 0.75 BSC | | |

| Ref | Tolerance of, from and position |
|-----|---------------------------------|
| aaa | 0.10 |
| bbb | 0.10 |
| ddd | 0.10 |
| eee | 0.15 |
| fff | 0.08 |

Not To Scale

- Dimensions in Millimeters.
- The 'e' represents the basic solder ball grid pitch.
- 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
- Dimension 'ddd' is measured parallel to primary datum C.
- Primary datum C (seating plane) is defined by the crowns of the solder balls.
- Package dimensions refer to JEDEC MO-205 Rev. G.

6. REVISION HISTORY

| Revision | Date | Description of Change |
|----------|--------------------|---|
| 1 | May 29, 2009 | Establish Speed and Power Specifications |
| 2 | July 27, 2009 | Increase BGA Package to 11 mm x 11 mm |
| 3 | May 5, 2010 | Changed speed marking and timing specs to 35 ns part. Changed BGA package to 10 mm x 10mm |
| 4 | Aug 10, 2011 | Max. magnetic field during write ($H_{\text{max write}}$) increased to 8000 A/m. |
| 5 | March 1, 2012 | Added preliminary information on AEC-Q100 Grade 1. |
| 6 | September 20, 2013 | Replaced missing V_{OH} specification line in Table 2.3. |
| 7 | April 25, 2014 | AEC-Q100 removed until qualified product is available. |
| 8 | September 17, 2014 | 48-BGA package options moisture sensitivity level upgraded to MSL-5. |
| 8.1 | May 19, 2015 | Revised Everspin contact information. |
| 8.2 | June 11, 2015 | Corrected Japan Sales Office telephone number. |
| 8.3 | July 29, 2015 | Minor correction to the 'ddd' tolerance value for the BGA Package (Note 4.) |
| 8.4 | March 11, 2016 | The BGA package moisture sensitivity level rating is changed to MSL-6 in Table 4.1. |
| 8.5 | November 22, 2016 | The BGA package moisture sensitivity level rating is changed to MSL-5 in Table 4.1. |
| 8.6 | May 9, 2017 | The BGA package moisture sensitivity level is upgraded to MSL-3 |
| 8.7 | March 23, 2018 | Updated the Contact Us table |

7. HOW TO CONTACT US

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