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December 2014

FCP104N60F

N-Channel SuperFET[®] II FRFET[®] MOSFET 600 V, 37 A, 104 m Ω

Features

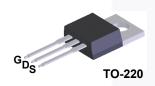
- 650 V @ T_J = 150°C
- Typ. R_{DS(on)} = 91 mΩ
- Ultra Low Gate Charge (Typ. $Q_g = 110 \text{ nC}$)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 313 pF)
- 100% Avalanche Tested

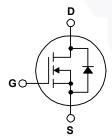
Applications

- · Lighting
- · Solar Inverter
- AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET® II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCP104N60F	Unit	
V _{DSS}	Drain to Source Voltage			600	V	
	Cata ta Cauraa Valtaga	- DC		±20	V	
$V_{ m GSS}$	Gate to Source Voltage	- AC	(f > 1Hz)	±30	V	
	Drain Current	- Continuous (T _C = 25°C)	- Continuous (T _C = 25°C) - Continuous (T _C = 100°C)		Α	
D	Drain Current	- Continuous (T _C = 100°C)				
DM	Drain Current	- Pulsed	(Note 1)	114	Α	
AS	Single Pulsed Avalanche En	ergy	(Note 2)	809	mJ	
AR	Avalanche Current		(Note 1)	6.8	Α	
- AR	Repetitive Avalanche Energy	у	(Note 1)	3.57	mJ	
dv./dt	Peak Diode Recovery dv/dt (Note 3)		(Note 3)	50	1//	
AS AR AR	MOSFET dv/dt			100	V/ns	
.	Dower Dissination	(T _C = 25°C)		357	W	
P_{D}	Power Dissipation - Derate Above 25°C			2.85	W/°C	
Γ _J , T _{STG}	Operating and Storage Temp	perature Range		-55 to +150	°C	
T _L	Maximum Lead Temperature 1/8" from Case for 5 Second	o .		300	°C	

Thermal Characteristics

Symbol	Parameter	FCP104N60F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ,Max.	62.5	· C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP104N60F	FCP104N60F	TO220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted. Parameter

Symbol	Parameter		Test Conditions	Min.	Тур.	Max.	Unit		
Off Characteristics									
D\/	Drain to Source Breakdown Voltage		$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	600	-	-	V		
BV _{DSS}	Drain to Source Breakdown Voltage		$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	650	-	-	V		
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient		I _D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C		
BV _{DS}	Drain-Source Avlanche Breakdown age	Volt-	V _{GS} = 0 V, I _D = 18.5 A	-	700	-	٧		
	Zero Gate Voltage Drain Current		V _{DS} = 600V, V _{GS} = 0 V	-	-	10	^		
IDSS			V _{DS} = 480 V, T _C = 125°C	-	16	-	μΑ		
I _{GSS}	Gate to Body Leakage Current		V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±100	nA		

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3	-	5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 18.5 \text{ A}$	-	91	104	mΩ
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 18.5 \text{ A}$	-	33	-	S

Dynamic Characteristics

_ ,						
C _{iss}	Input Capacitance	V 05.V.V 0.V	- \	4610	6130	pF
C _{oss}	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}$ f = 1 MHz	-	3255	4330	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12	-	155	235	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	-	74	-	pF
Coss eff.	Effective Output Capacitance	$V_{DS} = 0 \text{ V to } 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	313	-	pF
Q _{g(tot)}	Total Gate Charge at 10V		-	110	145	nC
Q _{gs}	Gate to Source Gate Charge	V _{DS} = 380 V, I _D = 18.5 A	-	24	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	V _{GS} = 10 V (Note 4)	-	44	-	nC
ESR	Equivalent Series Resistance	Drain open	1	0.9		Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-/-	34	78	ns
t _r		$V_{DD} = 380 \text{ V}, I_{D} = 18.5 \text{ A}$	/ -	20	50	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_{GEN} = 4.7 Ω	-	102	214	ns
t _f	Turn-Off Fall Time	(Note 4)	-	5.7	21.4	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Dio	Maximum Continuous Drain to Source Diode Forward Current		-	37	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-		114	Α
V_{SD}	Drain to Source Diode Forward Voltage V _{GS} = 0 V, I _{SD} = 18.5 A		- ,	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 18.5 A	-	144	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	0.91	-	μС

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature
- 2. I_{AS} = 6.8 A, V_{DD} = 50 V, R_{G} = 25 Ω , Starting T_{J} = 25°C
- 3. I $_{SD}$ \leq 18.5 A, di/dt \leq 200 A/ μ s, V $_{DD}$ \leq BV $_{DSS}$, Starting T $_{J}$ = 25°C
- 4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Figure 1. On-Region Characteristics

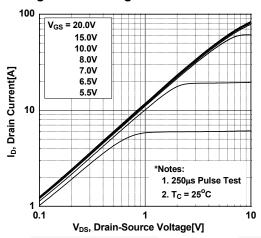


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

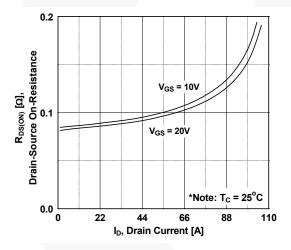


Figure 5. Capacitance Characteristics

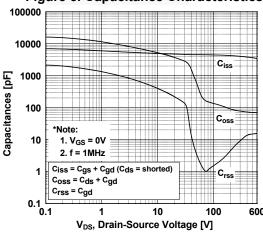


Figure 2. Transfer Characteristics

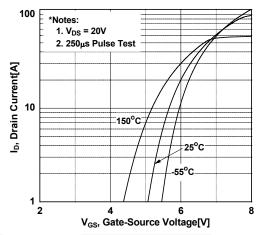


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

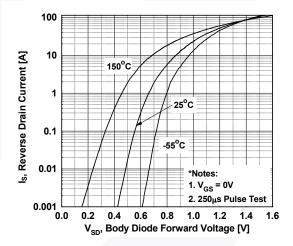
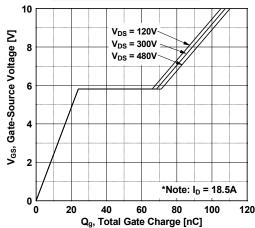


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

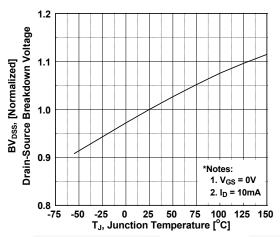


Figure 9. Maximum Safe Operating Area

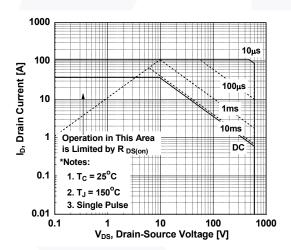


Figure 8. On-Resistance Variation vs. Temperature

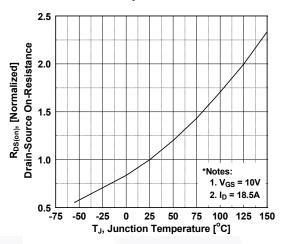


Figure 10. Maximum Drain Current vs. Case Temperature

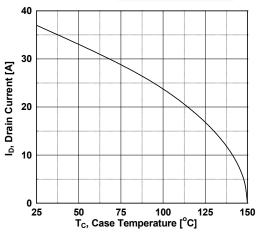


Figure 11. Transient Thermal Response Curve

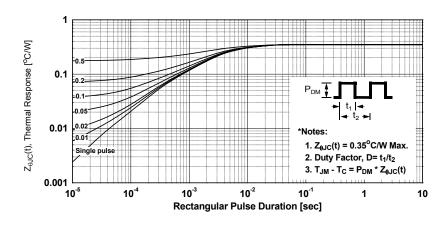


Figure 12. Gate Charge Test Circuit & Waveform

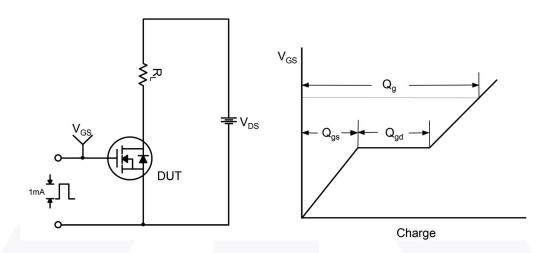


Figure 13. Resistive Switching Test Circuit & Waveforms

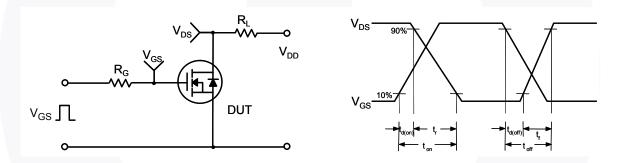
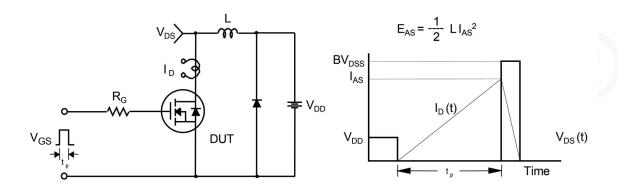


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



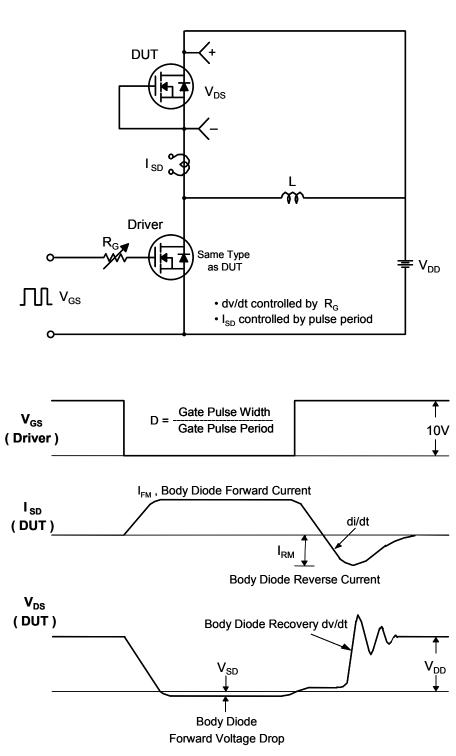
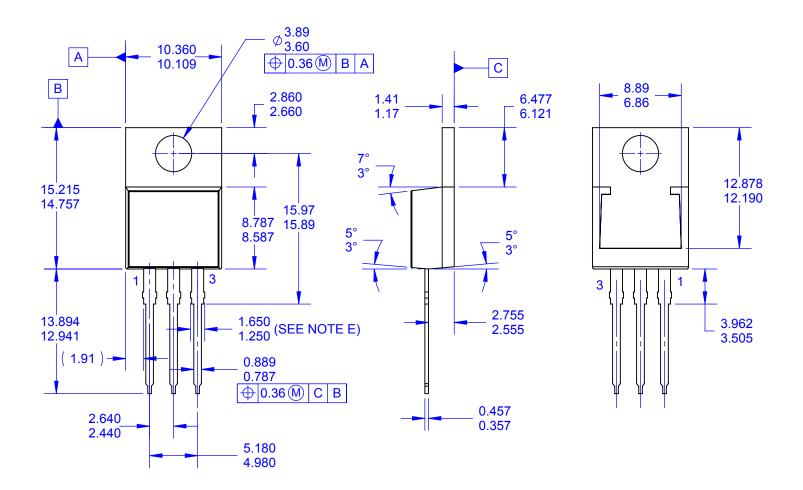
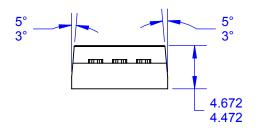


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 **VARIATION AB**
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. MAX WIDTH FOR F102 DEVICE = 1.35mm. F. DRAWING FILE NAME: TO220T03REV4.
- G. FAIRCHILD SEMICONDUCTOR.

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