

512K x36 and 1024K x18 18Mb, SYNCHRONOUS FLOW-THROUGH SRAM

MAY 2015

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- JEDEC 100-pin QFP, 165-ball BGA and 119-ball BGA packages
- Power supply:
 LF: V_{DD} 3.3V (± 5%), V_{DDQ} 3.3V/2.5V (± 5%)
 VF: V_{DD} 2.5V (± 5%), V_{DDQ} 2.5V (± 5%)
 VVF: V_{DD} 1.8V (± 5%), V_{DDQ} 1.8V (± 5%)
- JTAG Boundary Scan for BGA packages
- Commercial, Industrial and Automotive temperature support
- Lead-free available
- For leaded options, please contact ISSI

FAST ACCESS TIME

| Symbol | Parameter | -6.5 | -7.5 | Units |
|--------|-------------------|------|------|-------|
| tKQ | Clock Access Time | 6.5 | 7.5 | ns |
| tKC | Cycle time | 7.5 | 8.5 | ns |
| | Frequency | 133 | 117 | MHz |

DESCRIPTION

The 18Mb product family features high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61(64)LF/VF/VVF51236(32)B organized as 524,288 words by 36(32)bits. The IS61(64)LF/VF/VVF102418B are organized as 1,048,576 words by 18 bits. Fabricated with ISSI's advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable (/BWE) input combined with one or more individual byte write signals (/BWx). In addition, Global Write (/GW) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either /ADSP (Address Status Processor) or /ADSC (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the /ADV (burst address advance) input pin.

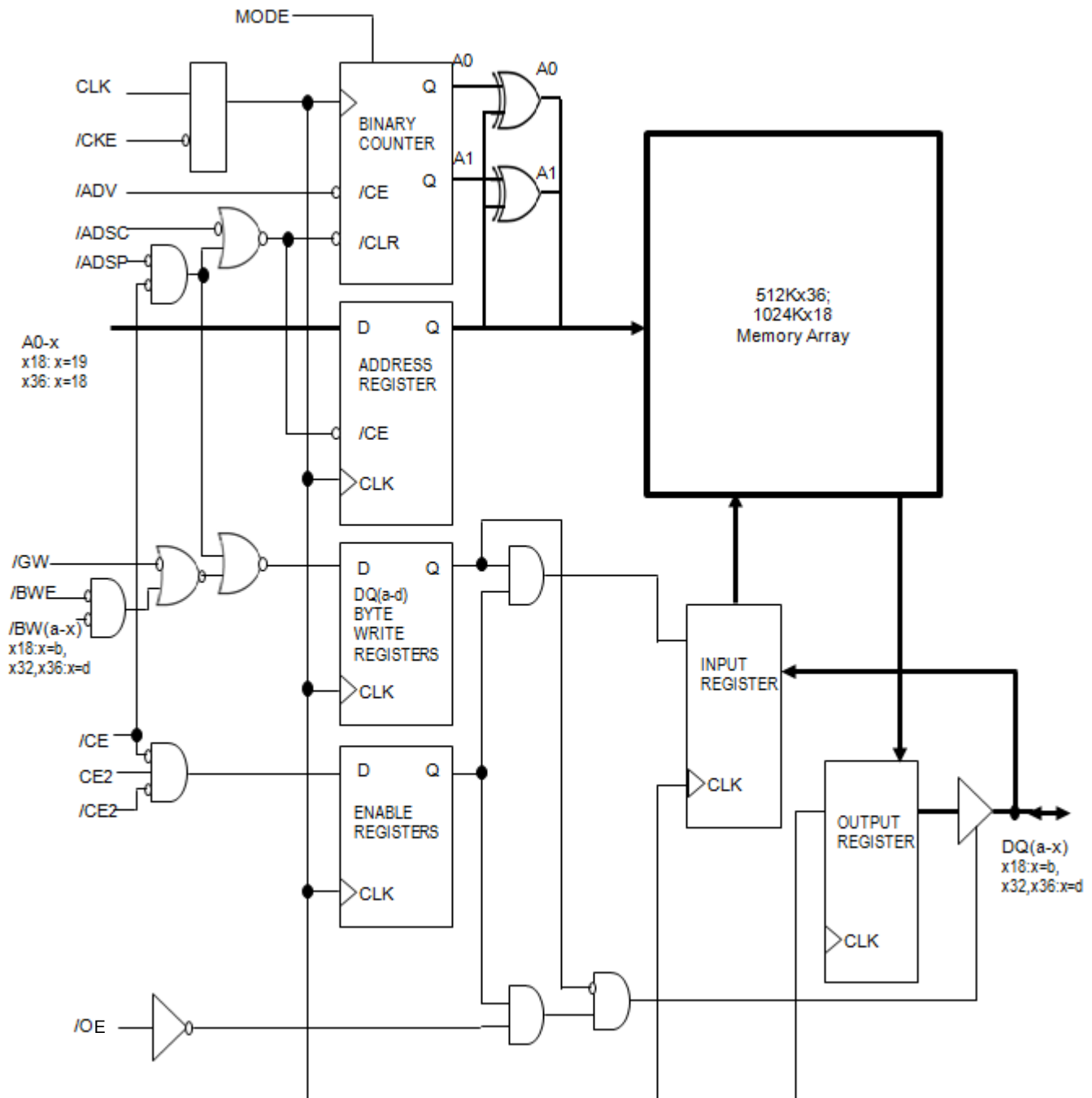
The mode pin is used to select the burst sequence order. Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating

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- a.) the risk of injury or damage has been minimized;
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BLOCK DIAGRAM

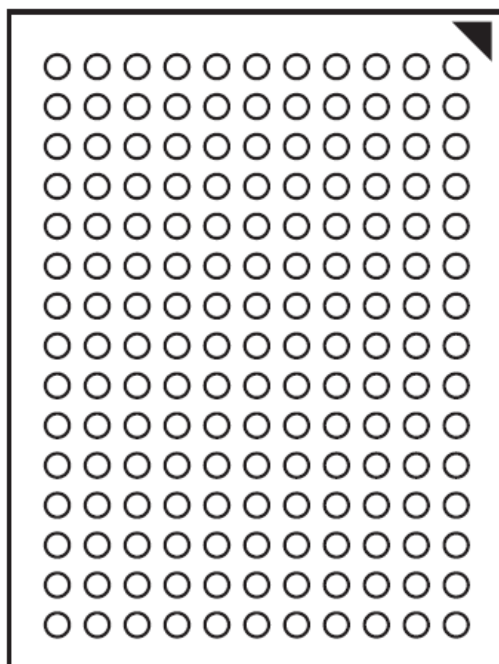


PIN CONFIGURATION

512K x 36, 165-Ball BGA (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|------|-----------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|-----|------|
| A | NC | A | /CE | /BWc | /BWb | /CE2 | /BWE | /ADSC | /ADV | A | NC |
| B | NC | A | CE2 | /BWd | /BWa | CLK | /GW | /OE | /ADSP | A | NC |
| C | DQPc | NC | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | DQPb |
| D | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| E | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| F | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| G | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| H | NC | V _{SS} | NC | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | NC | NC | ZZ |
| J | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| K | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| L | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| M | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| N | DQPd | NC | V _{DDQ} | V _{SS} | NC | A | NC | V _{SS} | V _{DDQ} | NC | DQPa |
| P | NC | NC | A | A | TDI | A1* | TDO | A | A | A | A |
| R | MODE | NC | A | A | TMS | A0* | TCK | A | A | A | A |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
 165-Ball, 13 mm x 15mm BGA

PIN DESCRIPTIONS

| Symbol | Pin Name |
|---------------------|-----------------------------------|
| CLK | Synchronous Clock |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| /ADV | Synchronous Burst Address Advance |
| /ADSP | Address Status Processor |
| /ADSC | Address Status Controller |
| MODE | Burst Sequence Selection |
| /CE,CE2,/CE2 | Synchronous Chip Enable |
| /BWE | Byte Write Enable |
| /BWx (x=a-d) | Synchronous Byte Write Inputs |
| /GW | Global Write Enable |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| DQPx | Parity Data I/O |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| V _{DD} | Power Supply |
| V _{DDQ} | I/O Power Supply |
| V _{SS} | Ground |

512K x 32, 165-Ball BGA (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|------|-----------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|-----|-----|
| A | NC | A | /CE | /BWc | /BWb | /CE2 | /BWE | /ADSC | /ADV | A | NC |
| B | NC | A | CE2 | /BWd | /BWa | CLK | /GW | /OE | /ADSP | A | NC |
| C | NC | NC | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | NC |
| D | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| E | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| F | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| G | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| H | NC | V _{SS} | NC | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | NC | NC | ZZ |
| J | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| K | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| L | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| M | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| N | NC | NC | V _{DDQ} | V _{SS} | NC | A | NC | V _{SS} | V _{DDQ} | NC | NC |
| P | NC | NC | A | A | TDI | A1* | TDO | A | A | A | A |
| R | MODE | NC | A | A | TMS | A0* | TCK | A | A | A | A |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
 165-Ball, 13 mm x 15mm BGA

PIN DESCRIPTIONS

| Symbol | Pin Name |
|---------------------|-----------------------------------|
| CLK | Synchronous Clock |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| /ADV | Synchronous Burst Address Advance |
| /ADSP | Address Status Processor |
| /ADSC | Address Status Controller |
| MODE | Burst Sequence Selection |
| /CE,CE2,/CE2 | Synchronous Chip Enable |
| /BWE | Byte Write Enable |
| /BWx (x=a-d) | Synchronous Byte Write Inputs |
| /GW | Global Write Enable |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| DQPx | Parity Data I/O |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| V _{DD} | Power Supply |
| V _{DDQ} | I/O Power Supply |
| V _{SS} | Ground |

1024K x 18, 165-Ball BGA (Top View)

| | | | | | | | | | | | |
|---|------------------|-----------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|-----------------|------------------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| A | NC | A | /CE | /BWb | NC | /CE2 | /BWE | /ADSC | /ADV | A | A |
| B | NC | A | CE2 | NC | /BWa | CLK | /GW | /OE | /ADSP | A | NC |
| C | NC | NC | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | DQP _a |
| D | NC | DQb | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | NC | DQ _a |
| E | NC | DQb | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | NC | DQ _a |
| F | NC | DQb | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | NC | DQ _a |
| G | NC | DQb | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | NC | DQ _a |
| H | NC | V _{SS} | NC | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | NC | NC | ZZ |
| J | DQb | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | NC |
| K | DQb | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | NC |
| L | DQb | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | NC |
| M | DQb | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | NC |
| N | DQP _b | NC | V _{DDQ} | V _{SS} | NC | A | NC | V _{SS} | V _{DDQ} | NC | NC |
| P | NC | NC | A | A | TDI | A1* | TDO | A | A | A | A |
| R | MODE | NC | A | A | TMS | A0* | TCK | A | A | A | A |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
 165-Ball, 13 mm x 15mm BGA

PIN DESCRIPTIONS

| Symbol | Pin Name |
|--------------------------|-----------------------------------|
| CLK | Synchronous Clock |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| /ADV | Synchronous Burst Address Advance |
| /ADSP | Address Status Processor |
| /ADSC | Address Status Controller |
| MODE | Burst Sequence Selection |
| /CE,CE2,/CE2 | Synchronous Chip Enable |
| /BWE | Byte Write Enable |
| /BW _x (x=a-b) | Synchronous Byte Write Inputs |
| /GW | Global Write Enable |
| /OE | Output Enable |
| DQ _x | Data Inputs/Outputs |
| DQP _x | Parity Data I/O |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| V _{DD} | Power Supply |
| V _{DDQ} | I/O Power Supply |
| V _{SS} | Ground |

512K x 36, 119-Ball BGA (Top View)

| | | | | | | | |
|---|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| A | V _{DDQ} | A | A | /ADSP | A | A | V _{DDQ} |
| B | NC | A | A | /ADSC | A | A | NC |
| C | NC | A | A | V _{DD} | A | A | NC |
| D | DQc | DQPc | V _{SS} | NC | V _{SS} | DQPb | DQb |
| E | DQc | DQc | V _{SS} | /CE | V _{SS} | DQb | DQb |
| F | V _{DDQ} | DQc | V _{SS} | /OE | V _{SS} | DQb | V _{DDQ} |
| G | DQc | DQc | /BWc | /ADV | /BWb | DQb | DQb |
| H | DQc | DQc | V _{SS} | /GW | V _{SS} | DQb | DQb |
| J | V _{DDQ} | V _{DD} | NC | V _{DD} | NC | V _{DD} | V _{DDQ} |
| K | DQd | DQd | V _{SS} | CLK | V _{SS} | DQa | DQa |
| L | DQd | DQd | /BWd | NC | /BWA | DQa | DQa |
| M | V _{DDQ} | DQd | V _{SS} | /BWE | V _{SS} | DQa | V _{DDQ} |
| N | DQd | DQd | V _{SS} | A1* | V _{SS} | DQa | DQa |
| P | DQd | DQPd | V _{SS} | A0* | V _{SS} | DQPa | DQa |
| R | NC | A | MODE | V _{DD} | NC | A | NC |
| T | NC | NC | A | A | A | NC | ZZ |
| U | V _{DDQ} | TMS | TDI | TCK | TDO | NC | V _{DDQ} |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
 119-Ball, 14 mm x 22 mm BGA

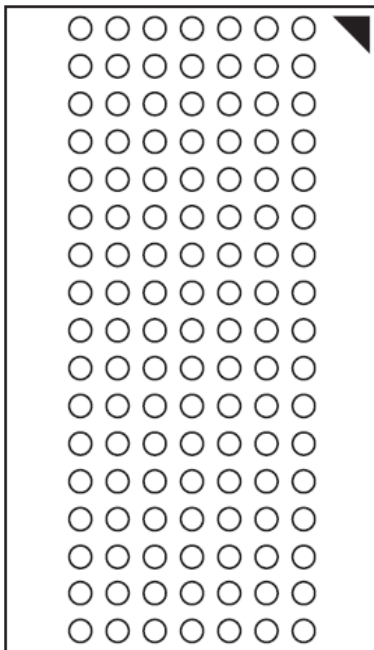
PIN DESCRIPTIONS

| Symbol | Pin Name |
|------------------|-----------------------------------|
| CLK | Synchronous Clock |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| /ADV | Synchronous Burst Address Advance |
| /ADSP | Address Status Processor |
| /ADSC | Address Status Controller |
| MODE | Burst Sequence Selection |
| /CE | Synchronous Chip Enable |
| /BWE | Byte Write Enable |
| /BWx (x=a-d) | Synchronous Byte Write Inputs |
| /GW | Global Write Enable |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| DQPx | Parity Data I/O |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| V _{DD} | Power Supply |
| V _{DDQ} | I/O Power Supply |
| V _{SS} | Ground |

512K x 32, 119-Ball BGA (Top View)

| | | | | | | | |
|---|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| A | V _{DDQ} | A | A | /ADSP | A | A | V _{DDQ} |
| B | NC | A | A | /ADSC | A | A | NC |
| C | NC | A | A | V _{DD} | A | A | NC |
| D | DQc | NC | V _{SS} | NC | V _{SS} | NC | DQb |
| E | DQc | DQc | V _{SS} | /CE | V _{SS} | DQb | DQb |
| F | V _{DDQ} | DQc | V _{SS} | /OE | V _{SS} | DQb | V _{DDQ} |
| G | DQc | DQc | /BWc | /ADV | /BWb | DQb | DQb |
| H | DQc | DQc | V _{SS} | /GW | V _{SS} | DQb | DQb |
| J | V _{DDQ} | V _{DD} | NC | V _{DD} | NC | V _{DD} | V _{DDQ} |
| K | DQd | DQd | V _{SS} | CLK | V _{SS} | DQa | DQa |
| L | DQd | DQd | /BWd | NC | /BWa | DQa | DQa |
| M | V _{DDQ} | DQd | V _{SS} | /BWE | V _{SS} | DQa | V _{DDQ} |
| N | DQd | DQd | V _{SS} | A1* | V _{SS} | DQa | DQa |
| P | DQd | NC | V _{SS} | A0* | V _{SS} | NC | DQa |
| R | NC | A | MODE | V _{DD} | NC | A | NC |
| T | NC | NC | A | A | A | NC | ZZ |
| U | V _{DDQ} | TMS | TDI | TCK | TDO | NC | V _{DDQ} |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
 119-Ball, 14 mm x 22 mm BGA

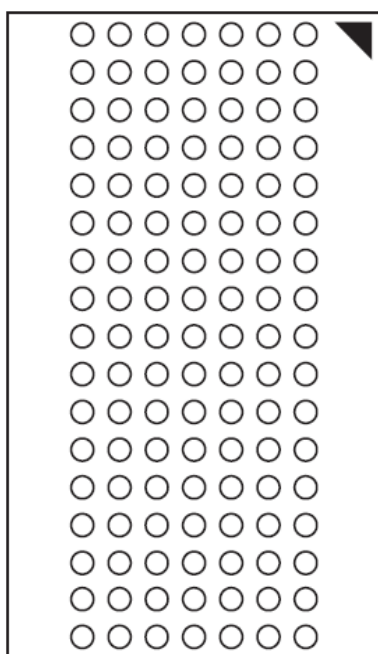
PIN DESCRIPTIONS

| Symbol | Pin Name |
|------------------|-----------------------------------|
| CLK | Synchronous Clock |
| A0,A1 | Synchronous Burst Address Inputs |
| A | Address Inputs |
| /ADV | Synchronous Burst Address Advance |
| /ADSP | Address Status Processor |
| /ADSC | Address Status Controller |
| MODE | Burst Sequence Selection |
| /CE | Synchronous Chip Enable |
| /BWE | Byte Write Enable |
| /BWx (x=a-d) | Synchronous Byte Write Inputs |
| /GW | Global Write Enable |
| /OE | Output Enable |
| DQx | Data Inputs/Outputs |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| V _{DD} | Power Supply |
| V _{DDQ} | I/O Power Supply |
| V _{SS} | Ground |

1024K x 18, 119-Ball BGA (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|------------------|------------------|------------------|-----------------|------------------|------------------|------------------|
| A | V _{DDQ} | A | A | /ADSP | A | A | V _{DDQ} |
| B | NC | A | A | /ADSC | A | A | NC |
| C | NC | A | A | V _{DD} | A | A | NC |
| D | DQb | NC | V _{SS} | NC | V _{SS} | DQP _a | NC |
| E | NC | DQb | V _{SS} | /CE | V _{SS} | NC | DQ _a |
| F | V _{DDQ} | NC | V _{SS} | /OE | V _{SS} | DQ _a | V _{DDQ} |
| G | NC | DQb | /BW _b | /ADV | V _{SS} | NC | DQ _a |
| H | DQb | NC | V _{SS} | /GW | V _{SS} | DQ _a | NC |
| J | V _{DDQ} | V _{DD} | NC | V _{DD} | NC | V _{DD} | V _{DDQ} |
| K | NC | DQb | V _{SS} | CLK | V _{SS} | NC | DQ _a |
| L | DQb | NC | V _{SS} | NC | /BW _a | DQ _a | NC |
| M | V _{DDQ} | DQb | V _{SS} | /BWE | V _{SS} | NC | V _{DDQ} |
| N | DQb | NC | V _{SS} | A1* | V _{SS} | DQ _a | NC |
| P | NC | DQP _b | V _{SS} | A0* | V _{SS} | NC | DQ _a |
| R | NC | A | MODE | V _{DD} | NC | A | NC |
| T | NC | A | A | NC | A | A | ZZ |
| U | V _{DDQ} | TMS | TDI | TCK | TDO | NC | V _{DDQ} |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
 119-Ball, 14 mm x 22 mm BGA

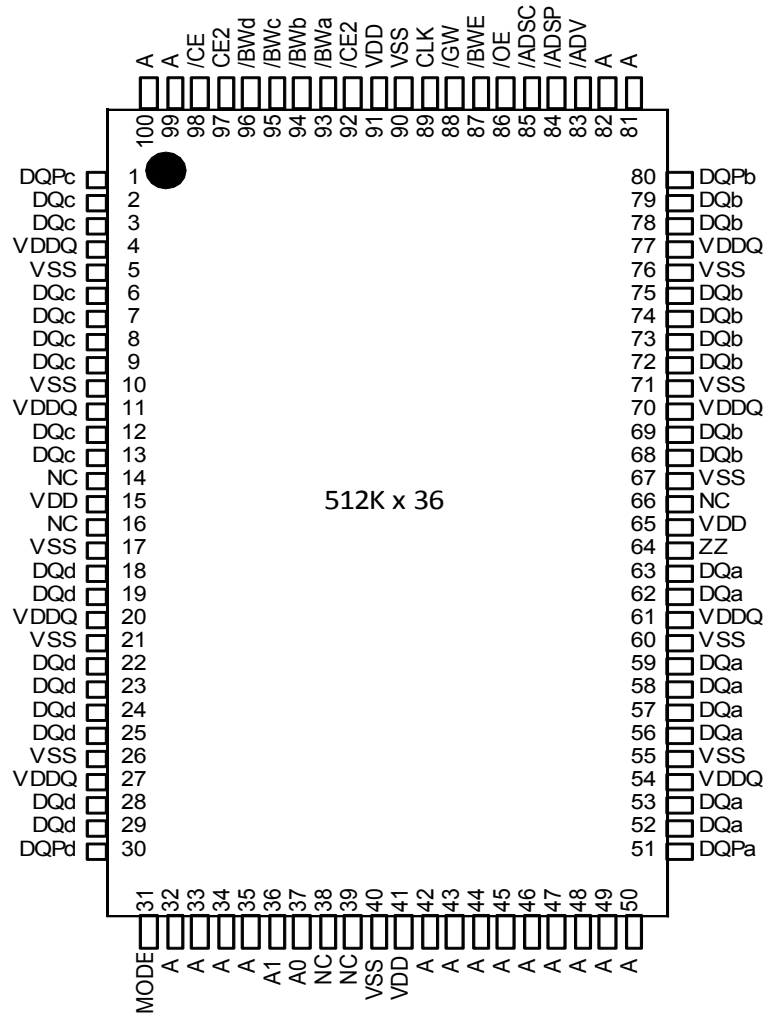
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| /BWE | Byte Write Enable |
| /BW _x (x=a-b) | Synchronous Byte Write Inputs |
| /GW | Global Write Enable |
| /OE | Output Enable |
| DQ _x | Data Inputs/Outputs |
| DQP _x | Parity Data I/O |
| TCK,TDI, TDO,TMS | JTAG Pins |
| ZZ | Power Sleep Mode |
| NC | No Connect |
| V _{DD} | Power Supply |
| V _{DDQ} | I/O Power Supply |
| V _{SS} | Ground |

IS61LF51236(32)B/IS61VF51236(32)B/IS61VVF51236(32)B
 IS61LF102418B/IS61VF102436B/IS61VVF102418B



512K x 36, 100PIN QFP (Top View)

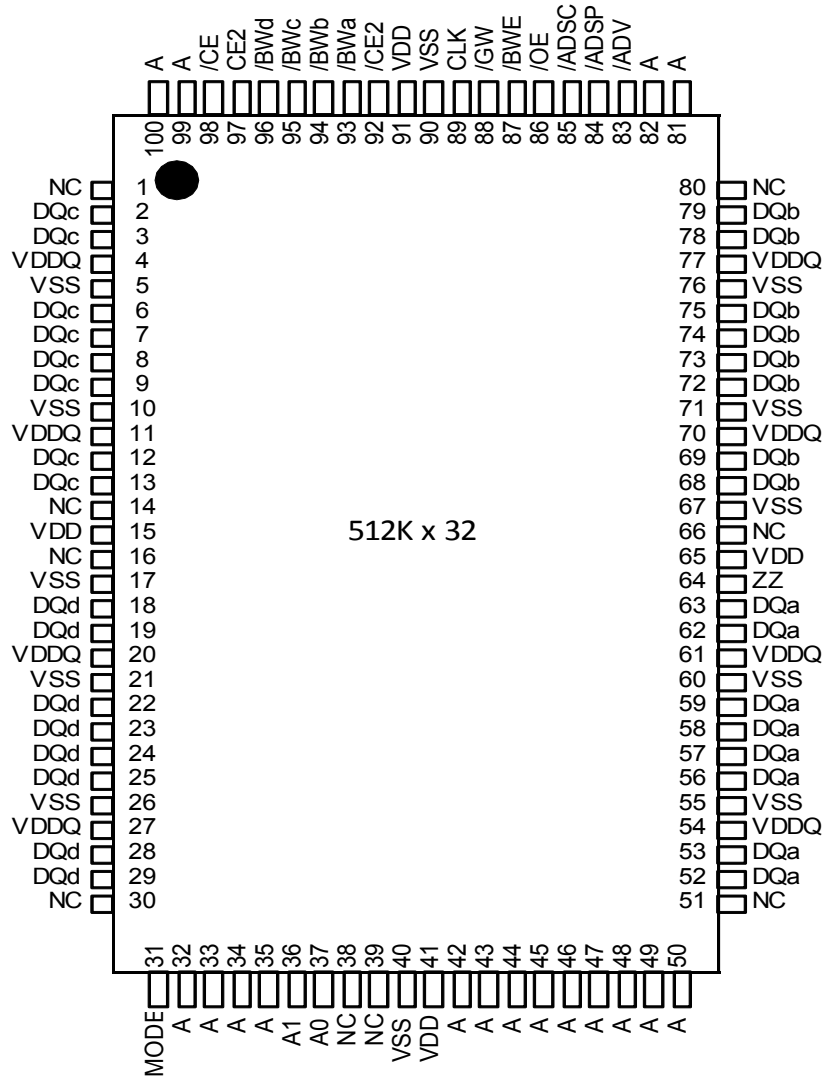


Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name | Symbol | Pin Name |
|--------------|-----------------------------------|------------------|---------------------|
| CLK | Synchronous Clock | /GW | Global Write Enable |
| A0,A1 | Synchronous Burst Address Inputs | /OE | Output Enable |
| A | Address Inputs | DQx | Data Inputs/Outputs |
| /ADV | Synchronous Burst Address Advance | DQPx | Parity Data I/O |
| /ADSP | Address Status Processor | ZZ | Power Sleep Mode |
| /ADSC | Address Status Controller | NC | No Connect |
| MODE | Burst Sequence Selection | V _{DD} | Power Supply |
| /CE,CE2,/CE2 | Synchronous Chip Enable | V _{DDQ} | I/O Power Supply |
| /BWE | Byte Write Enable | V _{SS} | Ground |
| /BWx (x=a-d) | Synchronous Byte Write Inputs | | |

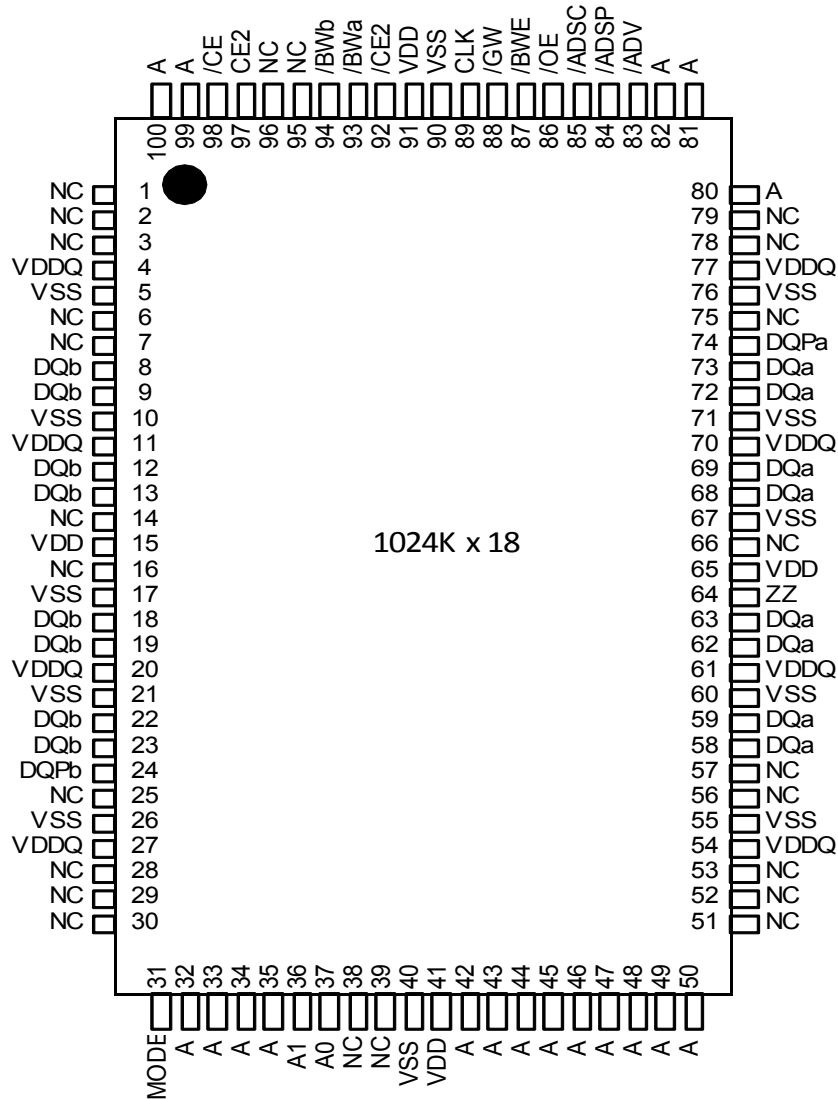
512K x 32, 100PIN QFP (Top View)



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

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| Symbol | Pin Name | Symbol | Pin Name |
|--------------|-----------------------------------|------------------|---------------------|
| CLK | Synchronous Clock | /GW | Global Write Enable |
| A0,A1 | Synchronous Burst Address Inputs | /OE | Output Enable |
| A | Address Inputs | DQx | Data Inputs/Outputs |
| /ADV | Synchronous Burst Address Advance | ZZ | Power Sleep Mode |
| /ADSP | Address Status Processor | NC | No Connect |
| /ADSC | Address Status Controller | V _{DD} | Power Supply |
| MODE | Burst Sequence Selection | V _{DDQ} | I/O Power Supply |
| /CE,CE2,/CE2 | Synchronous Chip Enable | V _{SS} | Ground |
| /BWE | Byte Write Enable | | |
| /BWx (x=a-d) | Synchronous Byte Write Inputs | | |



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name | Symbol | Pin Name |
|--------------|-----------------------------------|------------------|---------------------|
| CLK | Synchronous Clock | /GW | Global Write Enable |
| A0,A1 | Synchronous Burst Address Inputs | /OE | Output Enable |
| A | Address Inputs | DQx | Data Inputs/Outputs |
| /ADV | Synchronous Burst Address Advance | DQPx | Parity Data I/O |
| /ADSP | Address Status Processor | ZZ | Power Sleep Mode |
| /ADSC | Address Status Controller | NC | No Connect |
| MODE | Burst Sequence Selection | V _{DD} | Power Supply |
| /CE,CE2,/CE2 | Synchronous Chip Enable | V _{DDQ} | I/O Power Supply |
| /BWE | Byte Write Enable | V _{SS} | Ground |
| /BWx (x=a-b) | Synchronous Byte Write Inputs | | |

TRUTH TABLE

SYNCHRONOUS TRUTH TABLE

| OPERATION | ADDRESS | /CE | /CE2 | CE2 | ZZ | /ADSP | /ADSC | /ADV | /WRITE | /OE | CLK | DQ |
|-----------------------------|----------|-----|------|-----|----|-------|-------|------|--------|-----|-----|--------|
| Deselect Cycle, Power-Down | None | H | X | X | L | X | L | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | X | L | L | L | X | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | H | X | L | L | X | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | X | L | L | H | L | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | H | X | L | H | L | X | X | X | L-H | High-Z |
| Snooze Mode, Power-Down | None | X | X | X | H | X | X | X | X | X | X | High-Z |
| Read Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | H | L-H | High-Z |
| Write Cycle, Begin Burst | External | L | L | H | L | H | L | X | L | X | L-H | D |
| Read Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | H | L-H | High-Z |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | H | L-H | High-Z |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | H | L-H | High-Z |
| Write Cycle, Continue Burst | Next | X | X | X | L | H | H | L | L | X | L-H | D |
| Write Cycle, Continue Burst | Next | H | X | X | L | X | H | L | L | X | L-H | D |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | H | L-H | High-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | H | L-H | High-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | L | X | L-H | D |
| Write Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | L | X | L-H | D |

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For WRITE, L means one or more byte write enable signals (/BWA-d) and /BWE are LOW or /GW is LOW. /WRITE = H for all /BWx, /BWE, /GW HIGH.
3. /BWA enables WRITES to DQa's and DQPa. /BWb enables WRITES to DQb's and DQPb. /BWC enables WRITES to DQc's and DQPC. /BWD enables WRITES to DQd's and DQPD. DQPa and DQPb are available on the x18 version. DQPa-DQPD are available on the x36 version.
4. All inputs except /OE and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, /OE must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. /ADSP LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and /BWE LOW or /GW LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE

| Operation | /GW | /BWE | /BWa | /BWb | /BWc | /BWd |
|-----------------|-----|------|------|------|------|------|
| READ | H | H | X | X | X | X |
| READ | H | L | H | H | H | H |
| WRITE BYTE a | H | L | L | H | H | H |
| WRITE BYTE b | H | L | H | L | H | H |
| WRITE BYTE c | H | L | H | H | L | H |
| WRITE BYTE d | H | L | H | H | H | L |
| WRITE ALL BYTES | H | L | L | L | L | L |
| WRITE ALL BYTES | L | X | X | X | X | X |

Notes:

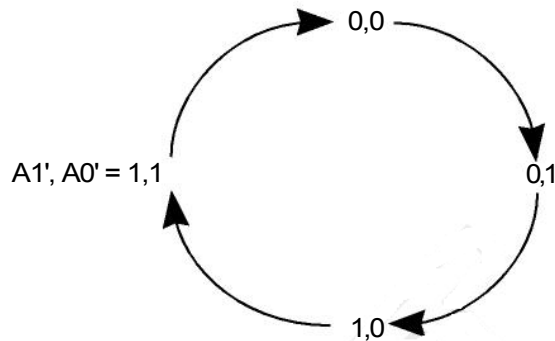
1. X means "Don't Care".
2. All inputs in this table must be set up and hold time around the rising edge of CLK.

ADDRESS SEQUENCE IN BURST MODE

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or NC)

| External Address | 1st Burst Address | 2nd Burst Address | 3rd Burst Address |
|------------------|-------------------|-------------------|-------------------|
| A1 A0 | A1 A0 | A1 A0 | A1 A0 |
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})



Power Up Sequence

V_{DDQ} → V_{DD}¹ → I/O Pins²

Notes:

1. V_{DD} can be applied at the same time as V_{DDQ}.
2. Applying I/O inputs is recommended after V_{DDQ} is stable. The inputs of the I/O pins can be applied at the same time as V_{DDQ} as long as V_{Ih} (level of I/O pins) is lower than V_{DDQ}.

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | LF Value | VF/VVF Value | Unit |
|-----------|--|-------------------------------|--------------------------------|------|
| Tstg | Storage Temperature | -65 to +150 | -65 to +150 | °C |
| Pd | Power Dissipation | 1.6 | 1.6 | W |
| Iout | Output Current (per I/O) | 20 | 20 | mA |
| Vin, Vout | Voltage Relative to Vss for I/O Pins | -0.5 to V _{DDQ} +0.3 | -0.5 to V _{DDQ} + 0.3 | V |
| Vin | Voltage Relative to Vss for Address and Control Inputs | -0.3 to V _{DD} +0.5 | -0.3 to V _{DD} + 0.3 | V |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61LFx)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Automotive | -40°C to +125°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |

OPERATING RANGE (IS61VFx)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|----------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 2.5V ± 5% | 2.5V ± 5% |
| Industrial | -40°C to +85°C | 2.5V ± 5% | 2.5V ± 5% |
| Automotive | *Please contact ISSI | | |

OPERATING RANGE (IS61VVFx)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|----------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 1.8V ± 5% | 1.8V ± 5% |
| Industrial | -40°C to +85°C | 1.8V ± 5% | 1.8V ± 5% |
| Automotive | *Please contact ISSI | | |

CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (Over operating temperature range)

| Symbol | Parameter | Test Conditions | 3.3V | | 2.5V | | 1.8V | | Unit |
|--------|------------------------|---|------|----------------------|------|----------------------|----------------------|----------------------|------|
| | | | Min. | Max. | Min | Max. | Min. | Max. | |
| Voh | Output HIGH Voltage | Ioh=-4.0 mA(3.3V) | 2.4 | — | 2.0 | — | V _{DDQ} | -0.4 | V |
| | | Ioh=-1.0 mA(2.5V,1.8V) | | | | | | | |
| Vol | Output LOW Voltage | Iol=8.0 mA(3.3V) | — | 0.4 | — | 0.4 | — | 0.4 | V |
| | | Iol=1.0 mA(2.5V,1.8V) | | | | | | | |
| Vih | Input HIGH Voltage | | 2.0 | V _{DD} +0.3 | 1.7 | V _{DD} +0.3 | 0.7* V _{DD} | V _{DD} +0.3 | V |
| Vil | Input LOW Voltage | | -0.3 | 0.8 | -0.3 | 0.7 | -0.3 | 0.3* V _{DD} | V |
| Ili | Input Leakage Current | V _{SS} ≤Vin≤ V _{DD} | -1 | 1 | -1 | 1 | -1 | 1 | μA |
| Ilo | Output Leakage Current | V _{SS} ≤Vout≤ V _{DD} ,/OE=Vih | -1 | 1 | -1 | 1 | -1 | 1 | μA |

Notes:

- All voltages referenced to ground.
- Overshoot:
 3.3V and 2.5V: V_{ih} (AC) ≤ V_{DD} + 1.5V (Pulse width less than t_{kc} /2)
 1.8V: V_{ih} (AC) ≤ V_{DD} + 0.5V (Pulse width less than t_{kc} /2)
- Undershoot:
 3.3V and 2.5V: V_{il} (AC) ≥ -1.5V (Pulse width less than t_{kc} /2)
 1.8V: V_{il} (AC) ≥ -0.5V (Pulse width less than t_{kc} /2)
- MODE pin has an internal pull-up and should be tied to V_{DD} or V_{SS}. It exhibits ±100μA maximum leakage current when tied to ≤V_{SS}+0.2V or ≥ V_{DDQ}-0.2V.
- ZZ pin has an internal pull-down and should be tied to V_{DD} or V_{SS}. It exhibits ±100μA maximum leakage current when tied to ≤V_{SS}+0.2V or ≥ V_{DD}-0.2V.

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Temp. range | -6.5 | | -7.5 | | Unit |
|------------------|------------------------------|---|-------------|------|-----|------|-----|------|
| | | | | Max | | Max | | |
| | | | | x18 | x36 | x18 | x36 | |
| I _{CC} | AC Operating, Supply Current | Device Selected, OE = V _{ih} , ZZ ≤ V _{il} , All Inputs ≤ 0.2V or ≥ V _{DD} - 0.2V, Cycle Time ≥ t _{kc} min. | Com. | 240 | 240 | 190 | 190 | mA |
| | | | Ind. | 260 | 260 | 210 | 210 | |
| I _{sb} | Standby Current TTL Input | Device Deselected, V _{DD} = Max., All Inputs ≤ V _{il} or ≥ V _{ih} , ZZ ≤ V _{il} , f = Max. | Com. | 80 | 80 | 70 | 70 | mA |
| | | | Ind. | 90 | 90 | 80 | 80 | |
| I _{sb1} | Standby Current CMOS Input | Device Deselected, V _{DD} = Max., Vin ≤ V _{SS} + 0.2V or ≥ V _{DD} - 0.2V, f = 0 | Com. | 60 | 60 | 60 | 60 | mA |
| | | | Ind. | 70 | 70 | 70 | 70 | |

Note:

- Power-up assumes a linear ramp from 0V to V_{DD} (min) within 200ms. During this time V_{ih} < V_{DD} and V_{DDQ} < V_{DD}

CAPACITANCE

| Symbol | Parameter | Conditions | Max. | Unit |
|--------|--------------------------|------------|------|------|
| Cin | Input Capacitance | Vin = 0V | 6 | pF |
| Cout | Input/Output Capacitance | Vout = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: Ta = 25°C, f = 1 MHz, VDD = 3.3V.

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | -6.5 | | -7.5 | | Unit |
|------------------------|---------------------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| fmax | Clock Frequency | — | 133 | — | 117 | MHz |
| tkc | Cycle Time | 7.5 | — | 8.5 | — | ns |
| tkh | Clock High Time | 2.2 | — | 2.5 | — | ns |
| tkl | Clock Low Time | 2.2 | — | 2.5 | — | ns |
| tkq | Clock Access Time | — | 6.5 | — | 7.5 | ns |
| tkqx ⁽²⁾ | Clock High to Output Invalid | 2.5 | — | 2.5 | — | ns |
| tkqlz ^(2,3) | Clock High to Output Low-Z | 2.5 | — | 2.5 | — | ns |
| tkqhz ^(2,3) | Clock High to Output High-Z | — | 3.8 | — | 4.0 | ns |
| toeq | Output Enable to Output Valid | — | 3.2 | — | 3.4 | ns |
| toelz ^(2,3) | Output Enable to Output Low-Z | 0 | — | 0 | — | ns |
| toehz ^(2,3) | Output Disable to Output High-Z | — | 3.5 | — | 3.5 | ns |
| tas | Address Setup Time | 1.5 | — | 1.5 | — | ns |
| tws | Read/Write Setup Time | 1.5 | — | 1.5 | — | ns |
| tces | Chip Enable Setup Time | 1.5 | — | 1.5 | — | ns |
| tse | Clock Enable Setup Time | 1.5 | — | 1.5 | — | ns |
| tadv | Address Advance Setup Time | 1.5 | — | 1.5 | — | ns |
| tds | Data Setup Time | 1.5 | — | 1.5 | — | ns |
| tah | Address Hold Time | 0.5 | — | 0.5 | — | ns |
| the | Clock Enable Hold Time | 0.5 | — | 0.5 | — | ns |
| twh | Write Hold Time | 0.5 | — | 0.5 | — | ns |
| tceh | Chip Enable Hold Time | 0.5 | — | 0.5 | — | ns |
| tadvh | Address Advance Hold Time | 0.5 | — | 0.5 | — | ns |
| tdh | Data Hold Time | 0.5 | — | 0.5 | — | ns |

Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

3.3V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|-----------------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| V_{TT} | 1.5V |
| V_{LOAD} | 3.3V |
| R1, R2 | 317 Ω , 351 Ω |
| Output Load | See Figures 1 and 2 |

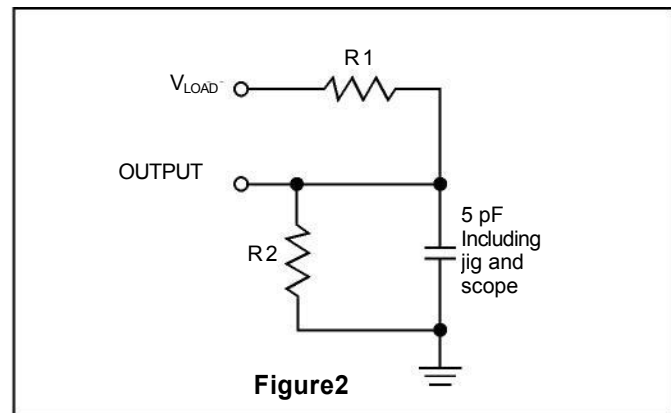
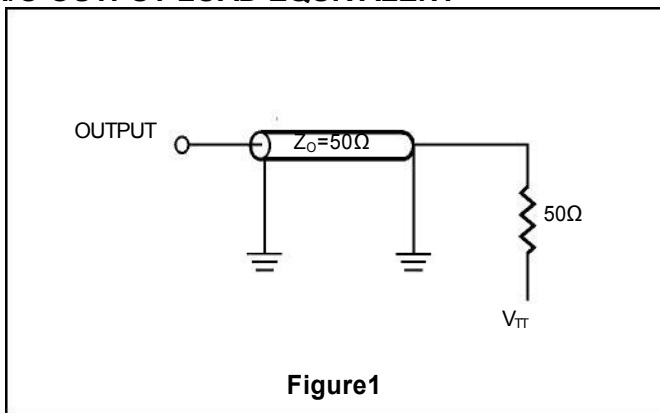
2.5V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|-------------------------------|
| Input Pulse Level | 0V to 2.5V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.25V |
| V_{TT} | 1.25V |
| V_{LOAD} | 2.5V |
| R1, R2 | 1667 Ω , 1538 Ω |
| Output Load | See Figures 1 and 2 |

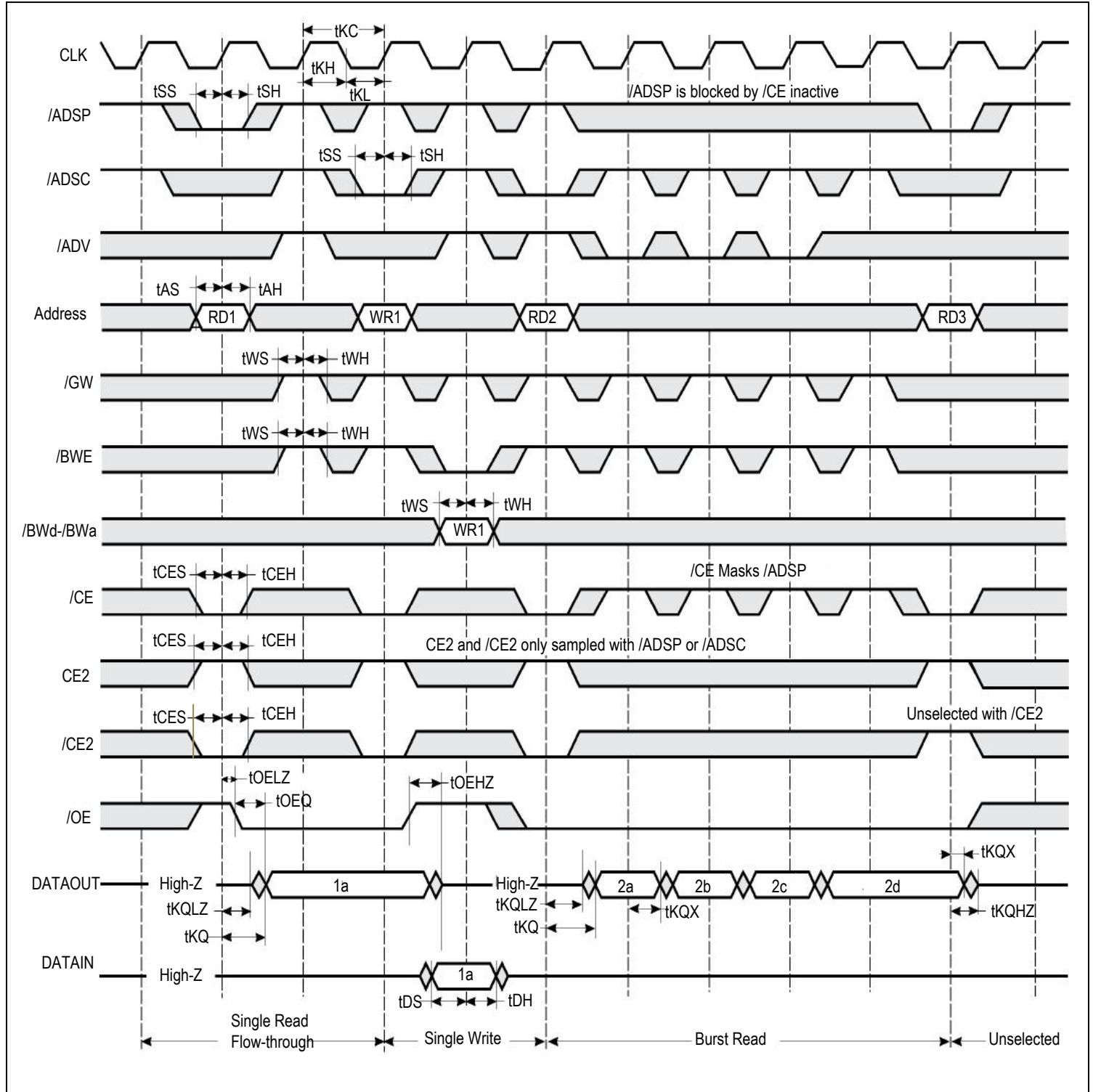
1.8V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------------|
| Input Pulse Level | 0V to 1.8V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 0.9V |
| V_{TT} | 0.9V |
| V_{LOAD} | 1.8V |
| R1, R2 | 1K Ω , 1K Ω |
| Output Load | See Figures 1 and 2 |

I/O OUTPUT LOAD EQUIVALENT



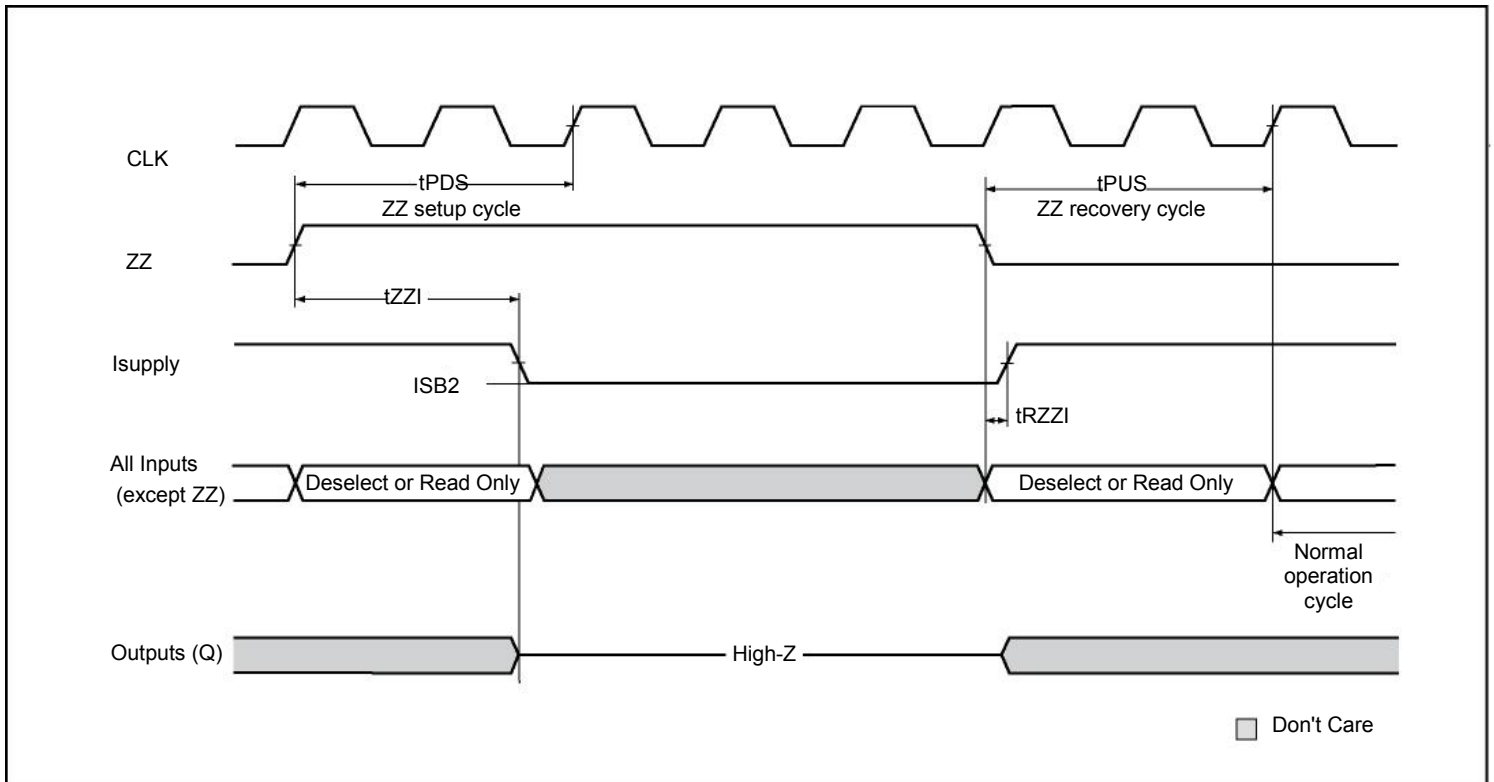
READ/WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Temperature Range | Min. | Max. | Unit |
|--------|------------------------------------|------------------|-------------------|------|------|-------|
| ISB2 | Current during SNOOZE MODE | $ZZ \geq V_{ih}$ | Com. | — | 40 | mA |
| | | | Ind. | — | 50 | |
| | | | Auto. | — | TBD | |
| tPDS | ZZ active to input ignored | | — | — | 2 | cycle |
| tPUS | ZZ inactive to input sampled | | — | 2 | — | cycle |
| tZZI | ZZ active to SNOOZE current | | — | — | 2 | cycle |
| tRZZI | ZZ inactive to exit SNOOZE current | | — | 0 | — | ns |

SLEEP MODE TIMING



IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required

Disabling the JTAG feature

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be left disconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left disconnected. On power-up, the device will come up in a reset state, which will not interfere with device operation.

Test Access Port Signal List:

1. Test Clock (TCK)

This signal uses V_{DD} as a power supply. The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

2. Test Mode Select (TMS)

This signal uses V_{DD} as a power supply. The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK.

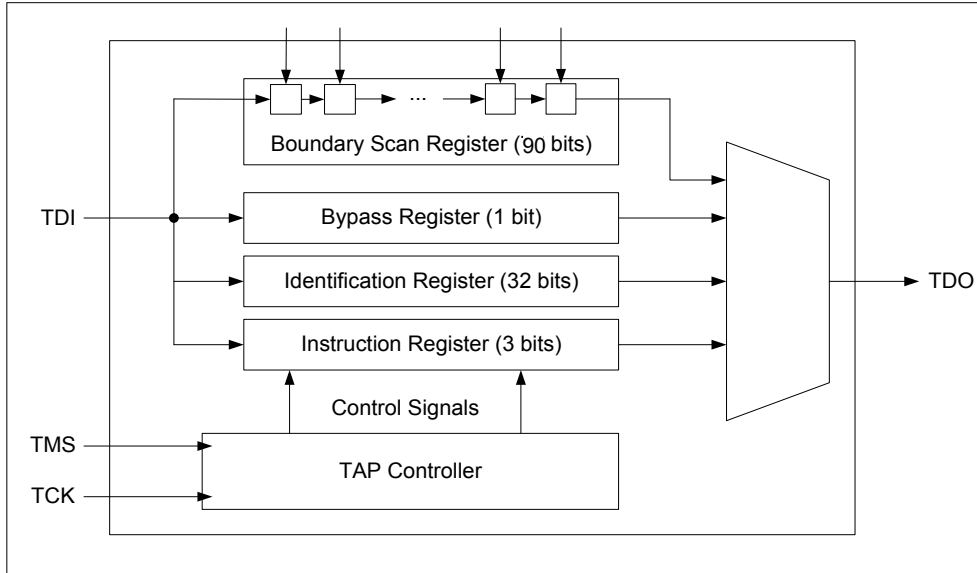
3. Test Data-In (TDI)

This signal uses V_{DD} as a power supply. The TDI input is used to serially input test instructions and information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is connected to the most significant bit (MSB) of any register. For more information regarding instruction register loading, please see the TAP Controller State Diagram.

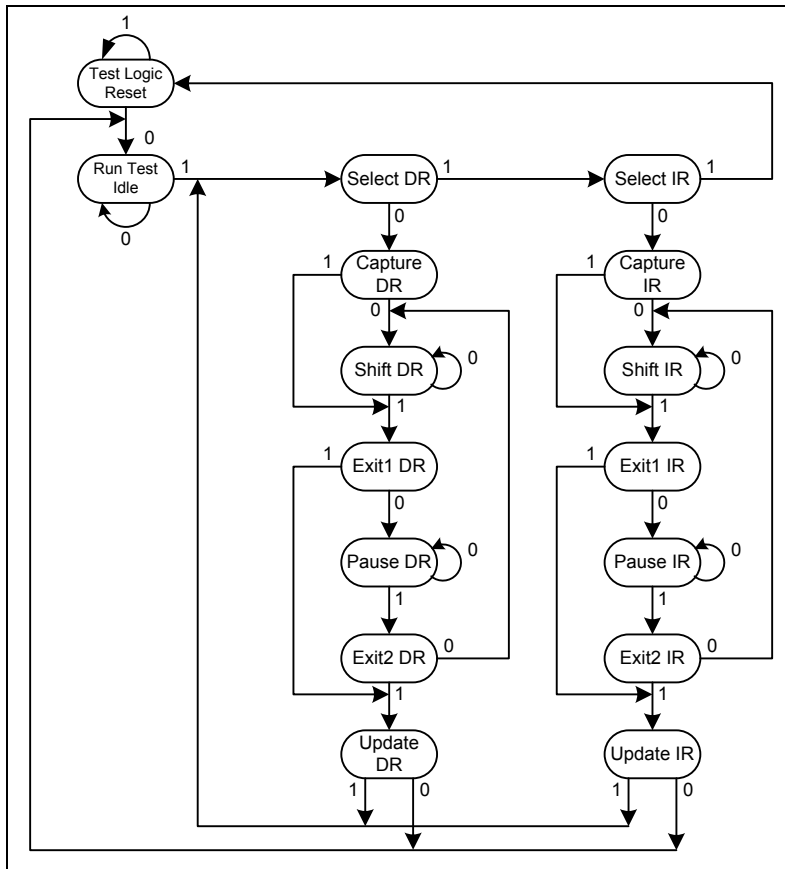
4. Test Data-Out (TDO)

This signal uses V_{DDQ} as a power supply. The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. For more information, please see the TAP Controller State Diagram.

TAP Controller State and Block Diagram



TAP Controller State Machine



Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

1. Instruction Register

This register is loaded during the update-IR state of the TAP controller. At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section. When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

2. Bypass Register

The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

3. Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several balls are also included in the scan register to reserved balls. The boundary scan register is loaded with the contents of the SRAM Input and Output ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

4. Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the shift-DR state.

Scan Register Sizes

| Register Name | Bit Size |
|---------------|----------|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 90 |

TAP Instruction Set

Many instructions are possible with an eight-bit instruction register and all valid combinations are listed in the TAP Instruction Code Table. All other instruction codes that are not listed on this table are reserved and should not be used. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

1. EXTEST

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls.

2. IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

3. SAMPLE Z

If the SAMPLE-Z instruction is loaded in the instruction register, all SRAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the SRAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

4. SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register. The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible. To ensure that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time. The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/ PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register. Once the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary scan register between the TDI and TDO balls.

6. BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

7. PRIVATE

Do not use these instructions. They are reserved for future use and engineering mode.

JTAG DC Operating Characteristics

(Over the Operating Temperature Range, 2.5V and 3.3V Option)

| Parameter | Symbol | Min | Max | Units | Notes |
|-----------------------------|--------------|------|--------------|---------|------------------------------|
| JTAG Input High Voltage | V_{IH1} | 2.0 | $V_{DD}+0.3$ | V | |
| JTAG Input Low Voltage | V_{IL1} | -0.3 | 0.7 | V | |
| JTAG Output High Voltage | V_{OH1} | 1.7 | - | V | $ I_{OH1} =2mA$ |
| JTAG Output Low Voltage | V_{OL1} | - | 0.7 | V | $I_{OL1}=2mA$ |
| JTAG Output High Voltage | V_{OH2} | 2.1 | - | V | $ I_{OH2} =100\mu A$ |
| JTAG Output Low Voltage | V_{OL2} | - | 0.2 | V | $I_{OL2}=100\mu A$ |
| JTAG Input Leakage Current | I_{L1JTAG} | -10 | +10 | μA | $0 \leq V_{in} \leq V_{DD}$ |
| JTAG Output Leakage Current | I_{LOJTAG} | -10 | +10 | μA | $0 \leq V_{out} \leq V_{DD}$ |

Notes:

- All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTTL-compatible.

JTAG DC Operating Characteristics

(Over the Operating Temperature Range, 1.8V Option)

| Parameter | Symbol | Min | Max | Units | Notes |
|-----------------------------|--------------|-----|-----|---------|-------|
| JTAG Input High Voltage | V_{IH1} | TBD | TBD | V | |
| JTAG Input Low Voltage | V_{IL1} | TBD | TBD | V | |
| JTAG Output High Voltage | V_{OH1} | TBD | TBD | V | |
| JTAG Output Low Voltage | V_{OL1} | TBD | TBD | V | |
| JTAG Input Leakage Current | I_{L1JTAG} | TBD | TBD | μA | |
| JTAG Output Leakage Current | I_{LOJTAG} | TBD | TBD | μA | |

Notes:

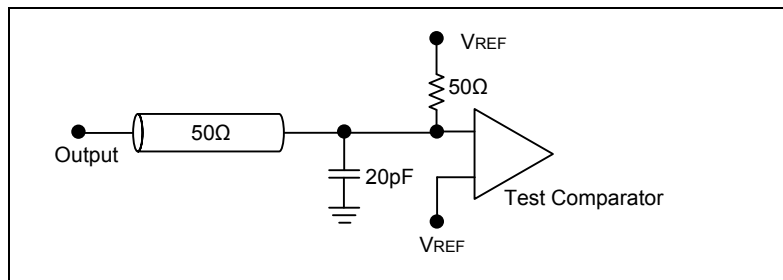
- All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTTL-compatible.

JTAG AC Test Conditions

(Over the Operating Temperature Range)

| Parameter | Symbol | 1.8V Option | 2.5V Option | 3.3V Option | Units |
|---|-----------|-------------|-------------|-------------|-------|
| Input Pulse High Level | V_{IH1} | TBD | 2.5 | 3.0 | V |
| Input Pulse Low Level | V_{IL1} | TBD | 0 | 0 | V |
| Input rise and fall time | T_{R1} | TBD | 1.5 | 1.5 | ns |
| Test load termination supply voltage | V_{REF} | TBD | 1.25 | 1.5 | V |
| Input and Output Timing Reference Level | V_{REF} | TBD | 1.25 | 1.5 | V |

TAP Output Load Equivalent

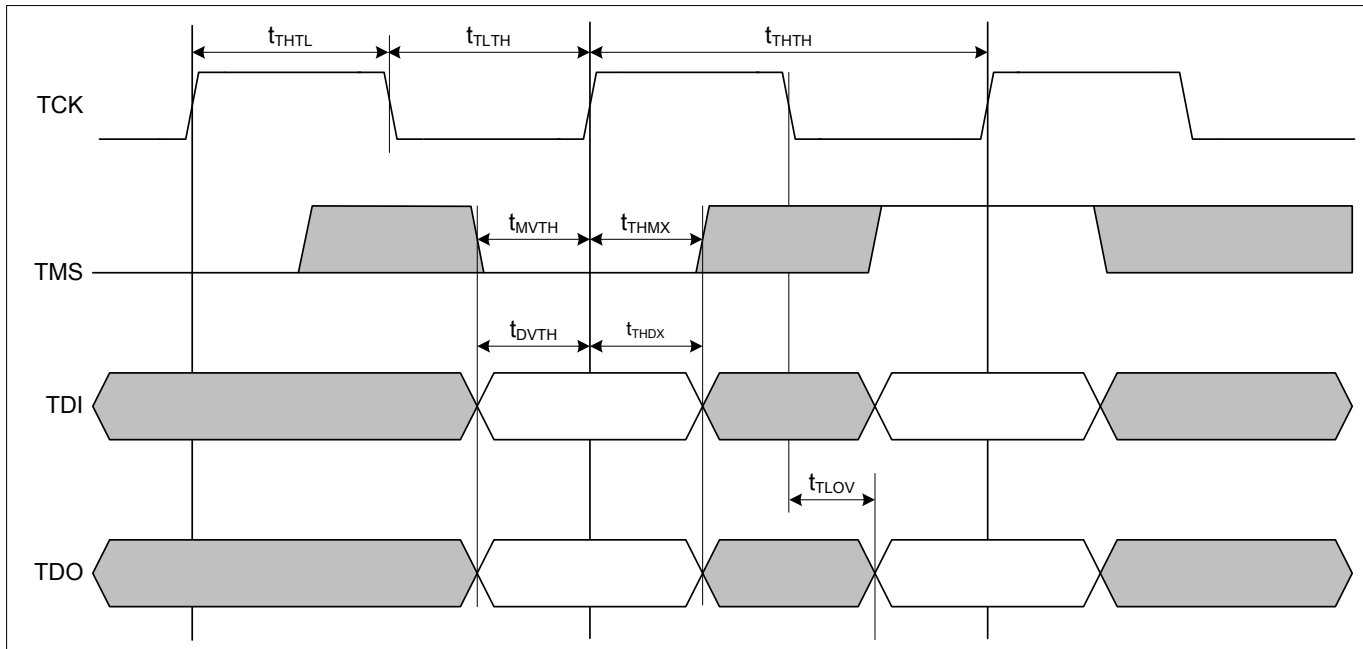


JTAG AC Characteristics

(Over the Operating Temperature Range)

| Parameter | Symbol | Min | Max | Units |
|-----------------------|------------|-----|-----|-------|
| TCK cycle time | t_{THTH} | 100 | – | ns |
| TCK high pulse width | t_{THTL} | 40 | – | ns |
| TCK low pulse width | t_{TLTH} | 40 | – | ns |
| TMS Setup | t_{MVTH} | 10 | – | ns |
| TMS Hold | t_{THMX} | 10 | – | ns |
| TDI Setup | t_{DVTH} | 10 | – | ns |
| TDI Hold | t_{THDX} | 10 | – | ns |
| TCK Low to Valid Data | t_{TLOV} | – | 20 | ns |

JTAG Timing Diagram



Instruction Set

| Code | Instruction | TDO Output | Notes |
|------|------------------|--------------------------------|-------|
| 000 | EXTEST | Boundary Scan Register | 2, 6 |
| 001 | IDCODE | 32-bit Identification Register | |
| 010 | SAMPLE-Z | Boundary Scan Register | 1, 2 |
| 011 | PRIVATE | Do Not Use | 5 |
| 100 | SAMPLE(/PRELOAD) | Boundary Scan Register | 4 |
| 101 | PRIVATE | Do Not Use | 5 |
| 110 | PRIVATE | Do Not Use | 5 |
| 111 | BYPASS | Bypass Register | 3 |

Notes:

1. Places DQs in high-Z in order to sample all input data, regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the shift-DR state.
4. SAMPLE instruction does not place DQs in high-Z.
5. This instruction is reserved. Invoking this instruction will cause improper SRAM functionality.
6. This EXTEST is not IEEE 1149.1-compliant. By default, it places DQ in high-Z. If the internal register on the scan chain is set high, DQ will be updated with information loaded via a previous SAMPLE instruction. The actual transfer occurs during the update IR state after EXTEST is loaded. The value of the internal register can be changed during SAMPLE and EXTEST only.

ID Register Definition

| Instruction Field | Description | 512K x 36 | 1024K x 18 |
|--------------------------|--|-------------|-------------|
| Revision Number (31:28) | Reserved for version number. | xxxx | xxxx |
| Device Depth (27:23) | Defines depth of SRAM. 512K or 1024K | 00111 | 01000 |
| Device Width (22:18) | Defines Width of the SRAM. x36 or x18 | 00100 | 00011 |
| ISSI Device ID (17:12) | Reserved for future use. | xxxxxx | xxxxxx |
| ISSI JEDEC ID (11:1) | Allows unique identification of SRAM vendor. | 00001010101 | 00001010101 |
| ID Register Presence (0) | Indicate the presence of an ID register. | 1 | 1 |

Boundary Scan Order

(TBA – 119 BGA)

| 165 BGA | | | | |
|---------|---------|--------|---------|--------|
| Bit # | X36 | | X18 | |
| | Bump ID | Signal | Bump ID | Signal |
| 1 | N6 | A9 | N6 | A9 |
| 2 | N7 | NC | N7 | NC |
| 3 | N10 | NC | N10 | NC |
| 4 | P11 | A8 | P11 | A8 |
| 5 | P8 | A18 | P8 | A18 |
| 6 | R8 | A17 | R8 | A17 |
| 7 | R9 | A16 | R9 | A16 |
| 8 | P9 | A15 | P9 | A15 |
| 9 | P10 | A14 | P10 | A14 |
| 10 | R10 | A13 | R10 | A13 |
| 11 | R11 | A12 | R11 | A12 |
| 12 | H11 | ZZ | H11 | ZZ |
| 13 | N11 | DQa0 | N11 | NC |
| 14 | M11 | DQa1 | M11 | NC |
| 15 | L11 | DQa2 | L11 | NC |
| 16 | M10 | DQa3 | M10 | DQa8 |
| 17 | L10 | DQa4 | L10 | DQa7 |
| 18 | K11 | DQa5 | K11 | NC |
| 19 | J11 | DQa6 | J11 | NC |
| 20 | K10 | DQa7 | K10 | DQa6 |
| 21 | J10 | DQa8 | J10 | DQa5 |
| 22 | H9 | NC | H9 | NC |
| 23 | H10 | NC | H10 | NC |
| 24 | G11 | DQb8 | G11 | DQa4 |
| 25 | F11 | DQb7 | F11 | DQa3 |
| 26 | G10 | DQb6 | G10 | NC |
| 27 | E11 | DQb5 | E11 | DQa2 |
| 28 | D11 | DQb4 | D11 | DQa1 |
| 29 | F10 | DQb3 | C11 | DQa0 |
| 30 | E10 | DQb2 | E10 | NC |
| 31 | D10 | DQb1 | D10 | NC |
| 32 | C11 | DQb0 | F10 | NC |
| 33 | A11 | NC | A11 | A19 |
| 34 | B11 | NC | B11 | NC |
| 35 | A10 | A11 | A10 | A11 |
| 36 | B10 | A10 | B10 | A10 |
| 37 | A9 | /ADV | A9 | /ADV |
| 38 | B9 | /ADSP | B9 | /ADSP |
| 39 | C10 | NC | C10 | NC |
| 40 | A8 | /ADSC | A8 | /ADSC |

Continued on next page

| 165 BGA | | | | |
|---------|---------|--------|---------|--------|
| | X36 | | X18 | |
| Bit # | Bump ID | Signal | Bump ID | Signal |
| 41 | B8 | /OE | B8 | /OE |
| 42 | A7 | /BWE | A7 | /BWE |
| 43 | B7 | /GW | B7 | /GW |
| 44 | B6 | CLK | B6 | CLK |
| 45 | A6 | /CE2 | A6 | /CE2 |
| 46 | B5 | /Bwa | B5 | /Bwa |
| 47 | A5 | /Bwb | A5 | NC |
| 48 | A4 | /Bwc | A4 | /Bwb |
| 49 | B4 | /Bwd | B4 | NC |
| 50 | B3 | CE2 | B3 | CE2 |
| 51 | A3 | /CE1 | A3 | /CE1 |
| 52 | A2 | A7 | A2 | A7 |
| 53 | B2 | A6 | B2 | A6 |
| 54 | C2 | NC | C2 | NC |
| 55 | B1 | NC | B1 | NC |
| 56 | A1 | NC | A1 | NC |
| 57 | C1 | DQc0 | C1 | NC |
| 58 | D1 | DQc1 | D1 | NC |
| 59 | E1 | DQc2 | E1 | NC |
| 60 | D2 | DQc3 | D2 | DQb8 |
| 61 | E2 | DQc4 | E2 | DQb7 |
| 62 | F1 | DQc5 | F1 | NC |
| 63 | G1 | DQc6 | G1 | NC |
| 64 | F2 | DQc7 | F2 | DQb6 |
| 65 | G2 | DQc8 | G2 | DQb5 |
| 66 | H1 | NC | H1 | NC |
| 67 | H2 | NC | H2 | NC |
| 68 | H3 | NC | H3 | NC |
| 69 | J1 | DQd8 | J1 | DQb4 |
| 70 | K1 | DQd7 | K1 | DQb3 |
| 71 | J2 | DQd6 | J2 | NC |
| 72 | L1 | DQd5 | L1 | DQb2 |
| 73 | M1 | DQd4 | M1 | DQb1 |
| 74 | K2 | DQd3 | N1 | DQb0 |
| 75 | L2 | DQd2 | L2 | NC |
| 76 | M2 | DQd1 | M2 | NC |
| 77 | N1 | DQd0 | K2 | NC |
| 78 | N2 | NC | N2 | NC |
| 79 | P1 | NC | P1 | NC |
| 80 | R1 | MODE | R1 | MODE |

Continue on next page

| 165 BGA | | | | |
|---------|---------|--------|---------|--------|
| | X36 | | X18 | |
| Bit # | Bump ID | Signal | Bump ID | Signal |
| 81 | R2 | NC | R2 | NC |
| 82 | P3 | A5 | P3 | A5 |
| 83 | R3 | A4 | R3 | A4 |
| 84 | P2 | NC | P2 | NC |
| 85 | P4 | A2 | P4 | A2 |
| 86 | R4 | A3 | R4 | A3 |
| 87 | N5 | NC | N5 | NC |
| 88 | P6 | A1 | P6 | A1 |
| 89 | R6 | A0 | R6 | A0 |
| 90 | * | Int | * | Int |

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

| V _{DD} | Speed | X36 | X18 | Package |
|--|-------|---------------------------------------|----------------------|--------------------|
| V _{DD} =3.3V, V _{DDQ} =2.5V/3.3V | 6.5ns | IS61LF51236B-6.5TQ | IS61LF102418B-6.5TQ | 100 QFP |
| | | IS61LF51236B-6.5B3 | IS61LF102418B-6.5B3 | 165 BGA |
| | | IS61LF51236B-6.5B2 | IS61LF102418B-6.5B2 | 119 BGA |
| | | IS61LF51236B-6.5TQL | IS61LF102418B-6.5TQL | 100 QFP, Lead-free |
| | | IS61LF51236B-6.5B3L | IS61LF102418B-6.5B3L | 165 BGA, Lead-free |
| | | IS61LF51236B-6.5B2L | IS61LF102418B-6.5B2L | 119 BGA, Lead-free |
| | 7.5ns | IS61LF51236B-7.5TQ | IS61LF102418B-7.5TQ | 100 QFP |
| | | IS61LF51236B-7.5B3 | IS61LF102418B-7.5B3 | 165 BGA |
| | | IS61LF51236B-7.5B2 | IS61LF102418B-7.5B2 | 119 BGA |
| | | IS61LF51236B-7.5TQL | IS61LF102418B-7.5TQL | 100 QFP, Lead-free |
| | | IS61LF51236B-7.5B3L | IS61LF102418B-7.5B3L | 165 BGA, Lead-free |
| | | IS61LF51236B-7.5B2L | IS61LF102418B-7.5B2L | 119 BGA, Lead-free |
| V _{DD} =2.5V, V _{DDQ} =2.5V | 6.5ns | <i>*Please contact ISSI Marketing</i> | | |
| | 7.5ns | <i>*Please contact ISSI Marketing</i> | | |
| V _{DD} =1.8V, V _{DDQ} =1.8V | 6.5ns | <i>*Please contact ISSI Marketing</i> | | |
| | 7.5ns | <i>*Please contact ISSI Marketing</i> | | |

ORDERING INFORMATION

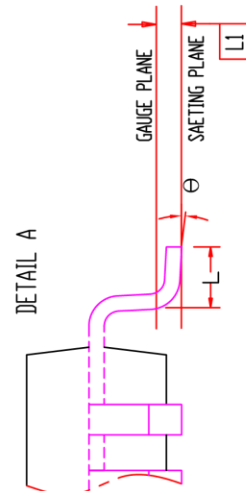
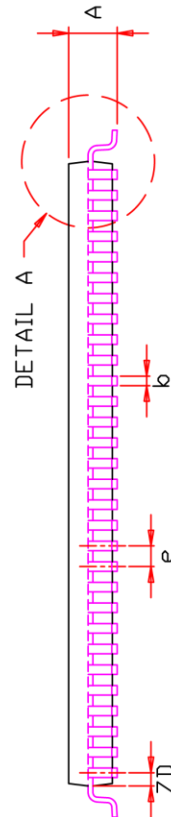
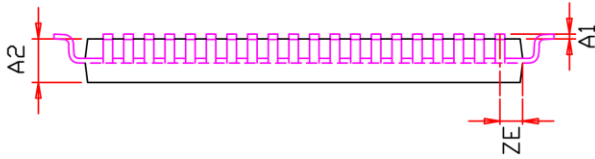
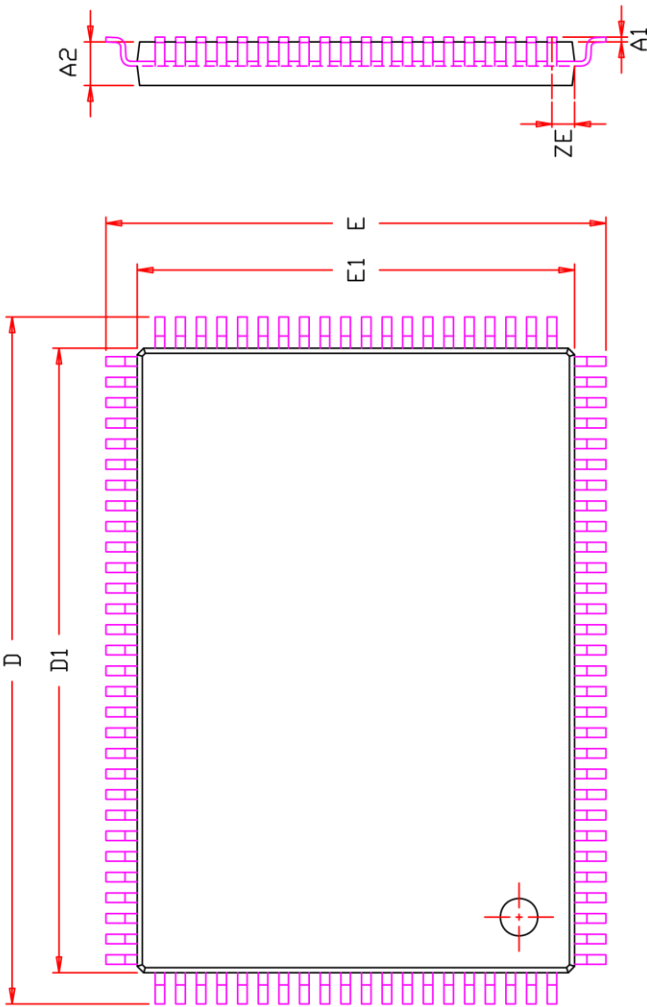
Industrial Range: -40°C to +85°C

| V _{DD} | Speed | X36 | X18 | Package |
|---|-------|---------------------------------------|-----------------------|--------------------|
| V _{DDQ} =3.3V, V _{DDQ} =2.5V/3.3V | 6.5ns | IS61LF51236B-6.5TQI | IS61LF102418B-6.5TQI | 100 QFP |
| | | IS61LF51236B-6.5B3I | IS61LF102418B-6.5B3I | 165 BGA |
| | | IS61LF51236B-6.5B2I | IS61LF102418B-6.5B2I | 119 BGA |
| | | IS61LF51236B-6.5TQLI | IS61LF102418B-6.5TQLI | 100 QFP, Lead-free |
| | | IS61LF51236B-6.5B3LI | IS61LF102418B-6.5B3LI | 165 BGA, Lead-free |
| | | IS61LF51236B-6.5B2LI | IS61LF102418B-6.5B2LI | 119 BGA, Lead-free |
| | 7.5ns | IS61LF51236B-7.5TQI | IS61LF102418B-7.5TQI | 100 QFP |
| | | IS61LF51236B-7.5B3I | IS61LF102418B-7.5B3I | 165 BGA |
| | | IS61LF51236B-7.5B2I | IS61LF102418B-7.5B2I | 119 BGA |
| | | IS61LF51236B-7.5TQLI | IS61LF102418B-7.5TQLI | 100 QFP, Lead-free |
| | | IS61LF51236B-7.5B3LI | IS61LF102418B-7.5B3LI | 165 BGA, Lead-free |
| | | IS61LF51236B-7.5B2LI | IS61LF102418B-7.5B2LI | 119 BGA, Lead-free |
| V _{DD} =2.5V, V _{DDQ} =2.5V | 6.5ns | <i>*Please contact ISSI Marketing</i> | | |
| | 7.5ns | <i>*Please contact ISSI Marketing</i> | | |
| V _{DD} =1.8V, V _{DDQ} =1.8V | 6.5ns | <i>*Please contact ISSI Marketing</i> | | |
| | 7.5ns | <i>*Please contact ISSI Marketing</i> | | |

Automotive Range: -40°C to +125°C

| V _{DD} | Speed | X36 | Package |
|--|-------|-----------------------|--------------------|
| V _{DD} =3.3V, V _{DDQ} =2.5V/3.3V | 6.5ns | IS64LF51236B-6.5TQLA3 | 100 QFP, Lead-free |
| | | IS64LF51236B-6.5B3LA3 | 165 BGA, Lead-free |
| | | IS64LF51236B-6.5B2LA3 | 119 BGA, Lead-free |
| | 7.5ns | IS64LF51236B-7.5TQLA3 | 100 QFP, Lead-free |
| | | IS64LF51236B-7.5B3LA3 | 165 BGA, Lead-free |
| | | IS64LF51236B-7.5B2LA3 | 119 BGA, Lead-free |

**For all other voltages and options in automotive grade, please contact ISSI.*



| SYMBOL | DIMENSION IN MM | | DIMENSION IN INCH | |
|--------|-----------------|-----------|-------------------|-----------|
| | MIN. | NOM. MAX. | MIN. | NOM. MAX. |
| A | 1.40 | 1.60 | 0.055 | 0.063 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 1.35 | 1.45 | 0.053 | 0.057 |
| b | 0.22 | 0.38 | 0.009 | 0.015 |
| D | 21.90 | 22.00 | 0.862 | 0.866 |
| D1 | 19.90 | 20.00 | 0.783 | 0.791 |
| E | 15.90 | 16.00 | 0.626 | 0.630 |
| E1 | 13.90 | 14.00 | 0.547 | 0.555 |
| e | 0.65 BSC. | | 0.026 BSC. | |
| L | 0.45 | 0.60 | 0.018 | 0.024 |
| L1 | 0.25 BSC. | | 0.010 BSC. | |
| ZD | 0.575 REF. | | 0.023 REF. | |
| ZE | 0.825 REF. | | 0.032 REF. | |
| theta | 0 | 3.5° | 0 | 3.5° |

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



TITLE

100L 14x20x1.4mm LQFP
 (Footprint : 2.0 mm)
 Package Outline

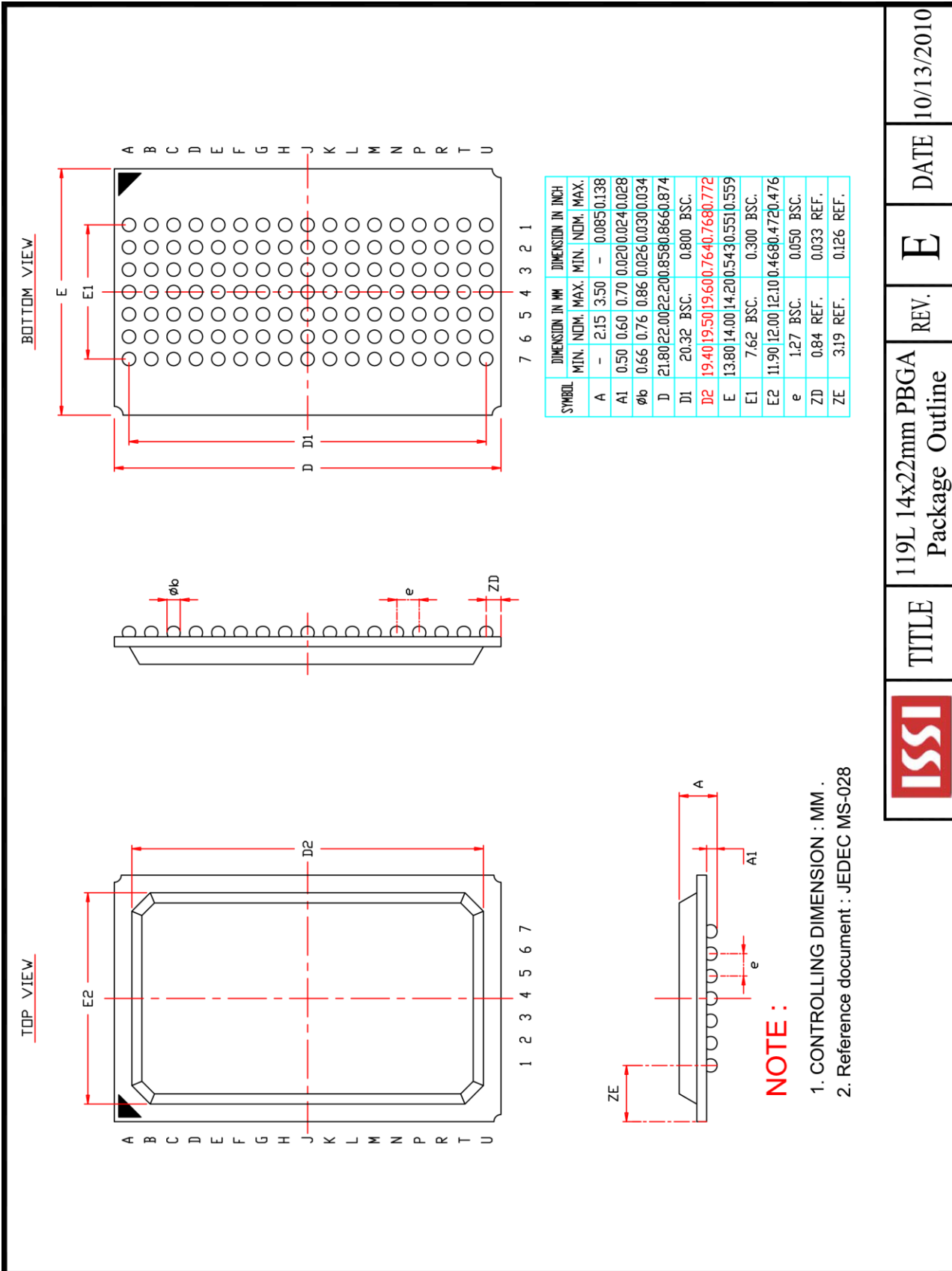
REV.

F

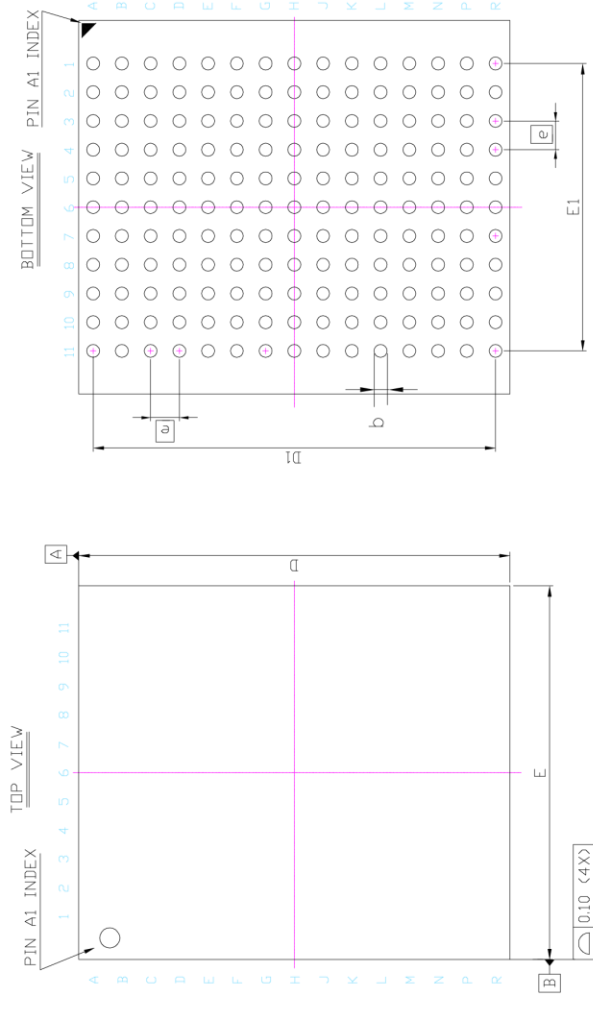
DATE

09/01/2009

280-600-011 REV. A



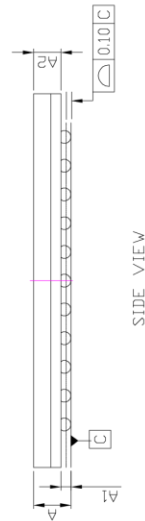
| | | | | | | |
|--|-------|--------------------------------------|------|---|------|------------|
| | TITLE | 119L 14x22mm PBGA Package Outline | REV. | E | DATE | 10/13/2010 |
|--|-------|--------------------------------------|------|---|------|------------|



| SYM. | DIMENSION (mm) | | | DIMENSION (inch) | | |
|------|----------------|-------|-------|------------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.25 | 0.35 | 0.40 | 0.010 | 0.014 | 0.016 |
| A2 | — | 0.79 | — | — | 0.031 | — |
| b | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| D | 14.90 | 15.00 | 15.10 | 0.587 | 0.591 | 0.594 |
| D1 | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| E | 12.90 | 13.00 | 13.10 | 0.508 | 0.512 | 0.516 |
| E1 | 9.90 | 10.00 | 10.10 | 0.390 | 0.394 | 0.398 |
| E1 | 1.00 BSC | | | 0.039 BSC | | |

NOTE :

1. CONTROLLING DIMENSION : MM .



| | | | | | | |
|--|-------|-------------------------------------|------|---|------|------------|
| | TITLE | 165L 13x15mm TF-BGA Package Outline | REV. | B | DATE | 08/28/2008 |
|--|-------|-------------------------------------|------|---|------|------------|

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

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moschip.ru_9