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March 2015

FCD3400N80Z / FCU3400N80Z N-Channel SuperFET® II MOSFET

900 V 2 A 2 A O

800 V, 2 A, 3.4 Ω

Features

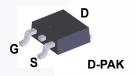
- $R_{DS(on)} = 2.75 \Omega (Typ.)$
- Ultra Low Gate Charge (Typ. $Q_g = 7.4 \text{ nC}$)
- Low E_{oss} (Typ. 0.9 uJ @ 400V)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 41 pF)
- · 100% Avalanche Tested
- · RoHS Compliant
- · ESD Improved Capability

Applications

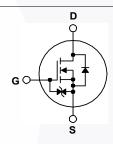
- · AC DC Power Supply
- · LED Lighting

Description

SuperFET[®] II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as Audio, Laptop adapter, Lighting, ATX power and industrial power applications.







Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		FCD3400N80Z FCU3400N80Z	Unit			
V _{DSS}	Drain to Source Voltage			800	V	
V_{GSS}	Cata to Source Voltage	- DC		±20	V	
	Gate to Source Voltage	- AC	(f > 1 Hz)	±30	_ v	
I _D	Drain Current	- Continuous (T _C = 25°C)		2.0	^	
	Drain Current	- Continuous (T _C = 100°C)		1.2	A	
I _{DM}	Drain Current	- Pulsed	(Note 1)	4.0	Α	
E _{AS}	Single Pulsed Avalanche Energ	gy	(Note 2)	12.8	mJ	
I _{AR}	Avalanche Current		(Note 1)	0.4	Α	
E _{AR}	Repetitive Avalanche Energy		(Note 1)	0.32	mJ	
dv/dt	MOSFET dv/dt Peak Diode Recovery dv/dt (Note 3)		100	1//20		
dv/dt			20	V/ns		
n	Dawer Dissipation	(T _C = 25°C)		32	W	
P_{D}	Power Dissipation - Derate Above 25°C			0.26	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150	οС	
TL	Maximum Lead Temperature for	or Soldering, 1/8" from Case for 5 So	econds	300	οС	

Thermal Characteristics

Symbol	Parameter	FCD3400N80Z FCU3400N80Z	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case, Max.	3.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	· C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD3400N80Z	FCD340080Z	DPAK	Tape and Reel	330 mm	16 mm	2500 units
FCU3400N80Z	FCU340080Z	IPAK	Tube	N/A	N/A	75 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 25^{\circ}\text{C}$	800	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	-	0.9	-	V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V	-	-	25	
I _{DSS}		$V_{DS} = 640 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	250	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±10	μΑ

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 0.2 \text{ mA}$	2.5	-	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 1 \text{ A}$	-	2.75	3.4	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 1 \text{ A}$	-	2	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 400 V V 0 V	- \	299	400	pF
C _{oss}	Output Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	-	12.7	15	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12	-	0.36	-	pF
C _{oss}	Output Capacitance	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	6.2	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	-	41	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 640 V, I _D = 2 A,	-	7.4	9.6	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	1.6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	3.1	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	3.2	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	10	30	ns
t _r	Turn-On Rise Time	$V_{DD} = 400 \text{ V}, I_D = 2 \text{ A},$	- /	6.4	23	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_g = 4.7 \Omega$	-	22.7	55	ns
t _f	Turn-Off Fall Time	(Note 4)	_	14	38	ns

Drain-Source Diode Characteristics

Is	Maximum Continuous Drain to Source Dio	Maximum Continuous Drain to Source Diode Forward Current		-	1.6	Α
I_{SM}	Maximum Pulsed Drain to Source Diode F	Maximum Pulsed Drain to Source Diode Forward Current		-	3.8	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 2 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 2 A,	-	119	-//	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	868	-	nC

Notes:

- 1. Repetitive rating: pulse width limited by maximum junction temperature.
- 2. I_{AS} = 0.4 A, R_G = 25 Ω , starting T_J = 25°C
- 3. I $_{SD} \le 2$ A, di/dt ≤ 200 A/ μ s, V $_{DD} \le BV_{DSS}$, starting T $_{J}$ = 25°C
- 4. Essentially independent of operating temperature typical characteristic.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

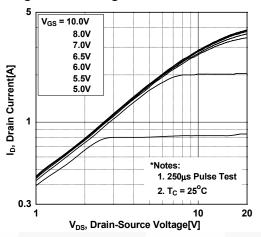


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

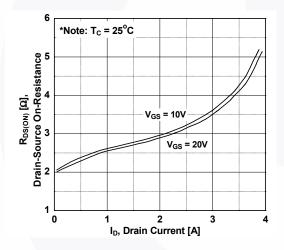


Figure 5. Capacitance Characteristics

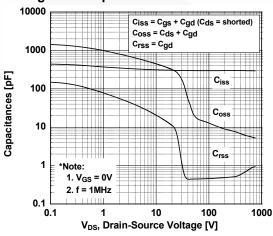


Figure 2. Transfer Characteristics

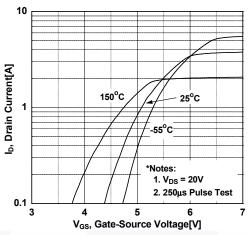


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

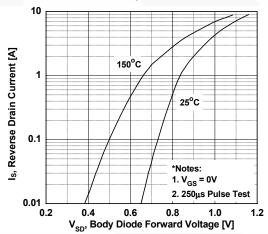
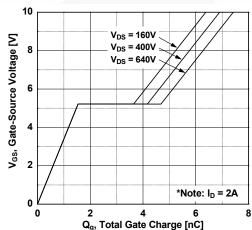


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

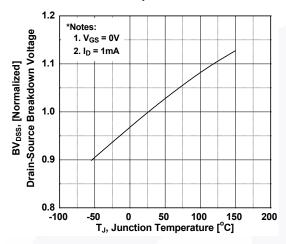


Figure 9. Maximum Safe Operating Area

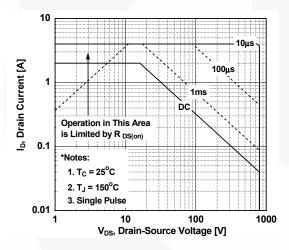


Figure 11. Eoss vs. Drain to Source Voltage

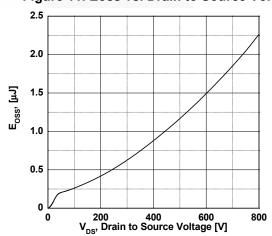


Figure 8. On-Resistance Variation vs. Temperature

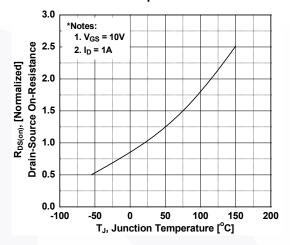
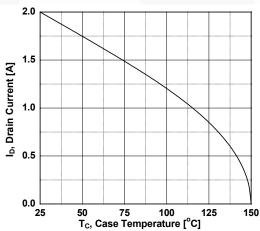
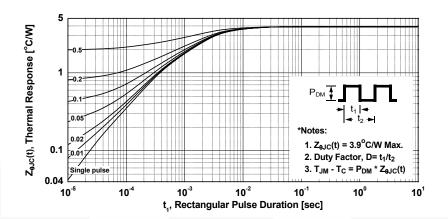


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



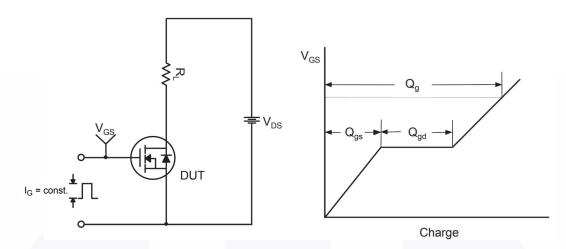


Fig 13. Gate Charge Test Circuit & Waveform

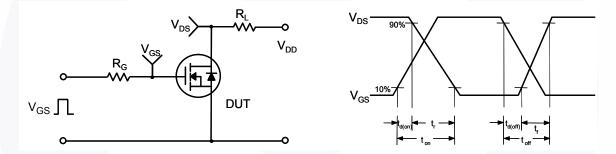


Fig 14. Resistive Switching Test Circuit & Waveforms

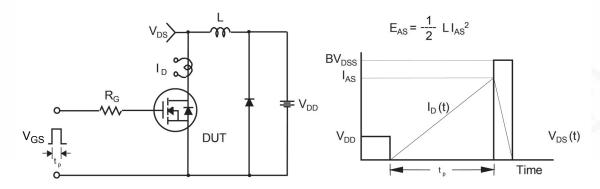


Fig 15. Unclamped Inductive Switching Test Circuit & Waveforms

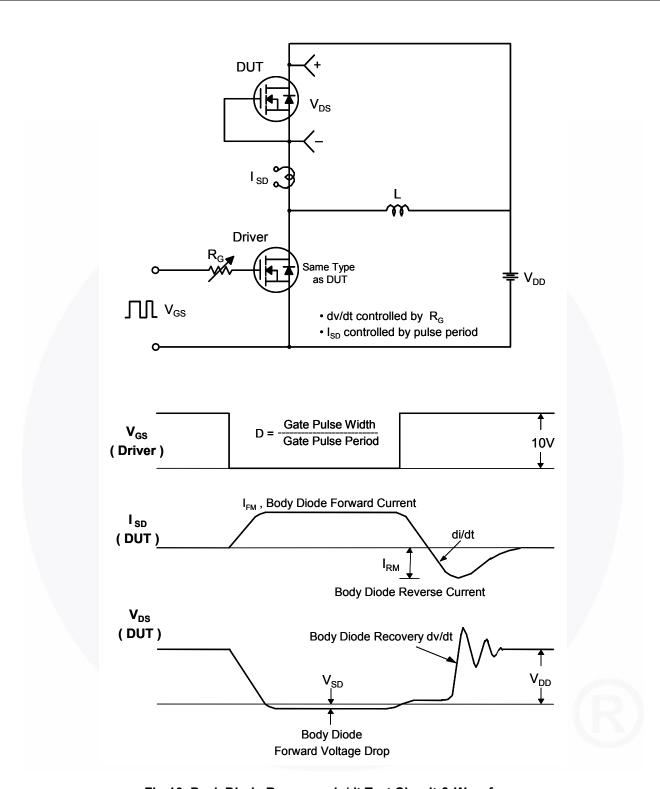
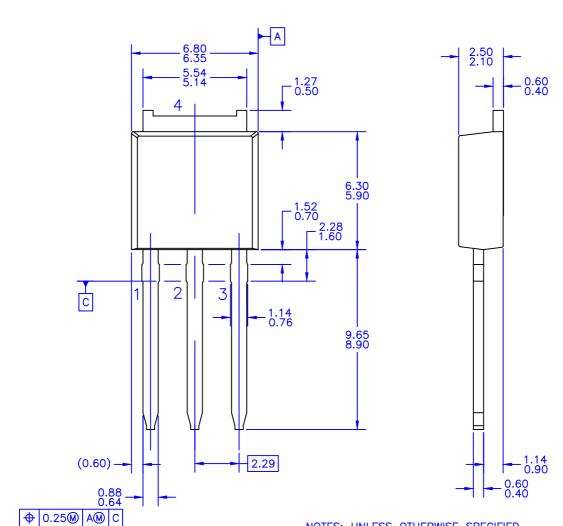
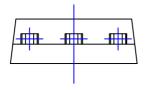


Fig 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



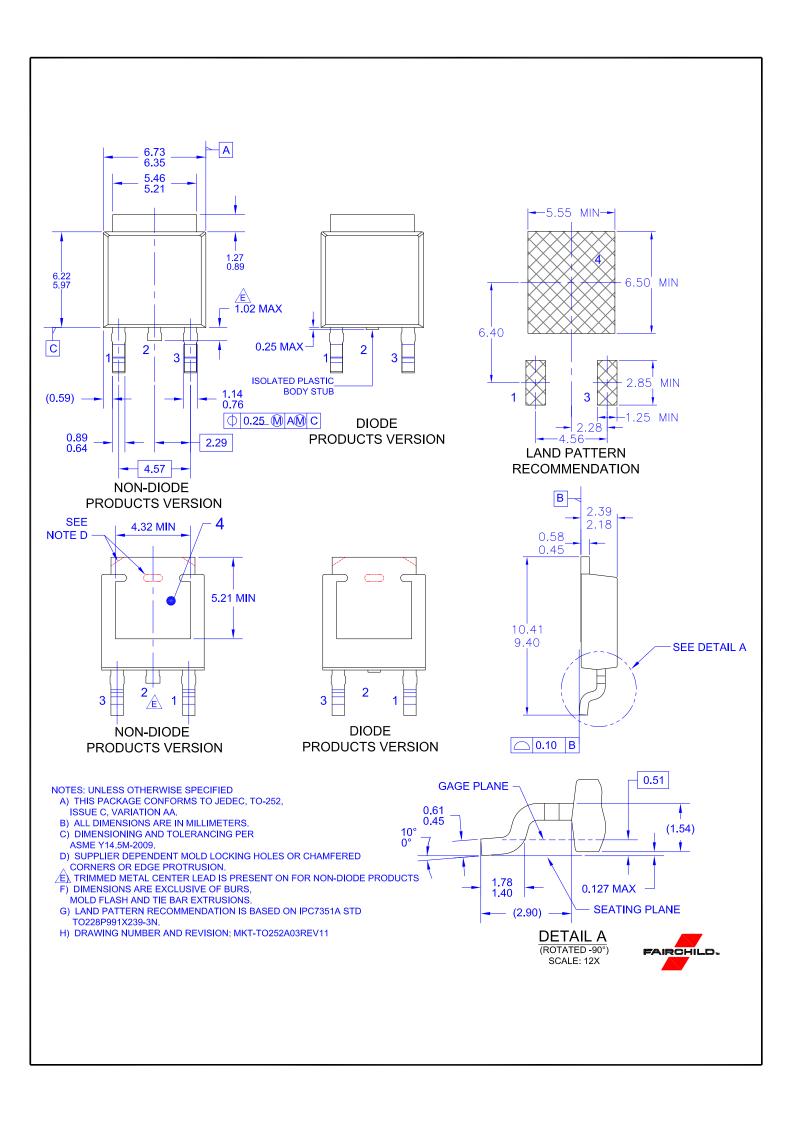


3 PLCS

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