NCV7383

FlexRay™ Bus Driver

NCV7383 is a single−channel FlexRay bus driver compliant with the FlexRay Electrical Physical Layer Specification Rev. 3.0.1, capable of communicating at speeds of up to 10 Mbit/s. It provides differential transmit and receive capability between a wired FlexRay communication medium on one side and a protocol controller and a host on the other side.

NCV7383 mode control functionality is optimized for nodes without the need of extended power management provided by transceivers with permanent connection to the car battery as is on NCV7381. NCV7383 is primarily intended for nodes switched off by ignition.

It offers excellent Electromagnetic compatibility (EMC) and Electrostatic discharge (ESD) performance.

KEY FEATURES

General

- Compliant with FlexRay Electrical Physical Layer Specification Rev 3.0.1
- FlexRay Transmitter and Receiver in Normal−Power Modes for Communication up to 10 Mbit/s
- Support of 60 ns Bit Time
- FlexRay Low−Power Mode Receiver for Remote Wakeup Detection
- Excellent Electromagnetic Susceptibility (EMS) Level Over Full Frequency Range. Very Low Electromagnetic Emissions (EME)
- Bus Pins Protected Against >10 kV System ESD Pulses
- Safe Behavior Under Missing Supply or No Supply Conditions
- Interface Pins for a Protocol Controller and a Host (TxD, RxD, TxEN, STBN, BGE, ERRN, CSN, SCK, SDO)
- Supply Pins V_{CC}, V_{IO} with Independent Voltage Ramp Up:
  - V_{CC} Supply Parametrical Range from 4.75 V to 5.25 V
  - V_{IO} Supply Parametrical Range from 2.3 V to 5.25 V
- TxEN Timeout and BGE Feedback
- Two Error Indication Modes
  - Track mode − Error Signaling on ERRN Pin
  - Latched mode − Status Register accessible via SPI
- Compatible with 14 V and 28 V Systems
- Operating Ambient Temperature −40°C to +125°C (T_{AMB_Class1})
- Junction Temperature Monitoring
- TSSOP−14 Package
- These are Pb−Free Devices

FlexRay Functional Classes

- Bus Driver − Bus Guardian Interface
- Bus Driver Logic Level Adaptation
- Bus Driver Remote Wakeup

Quality

- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

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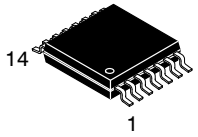
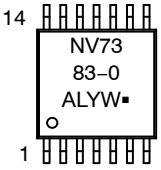


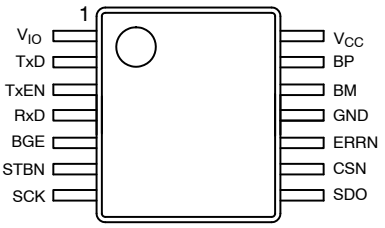
TSSOP−14
CASE 948G

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

BLOCK DIAGRAM

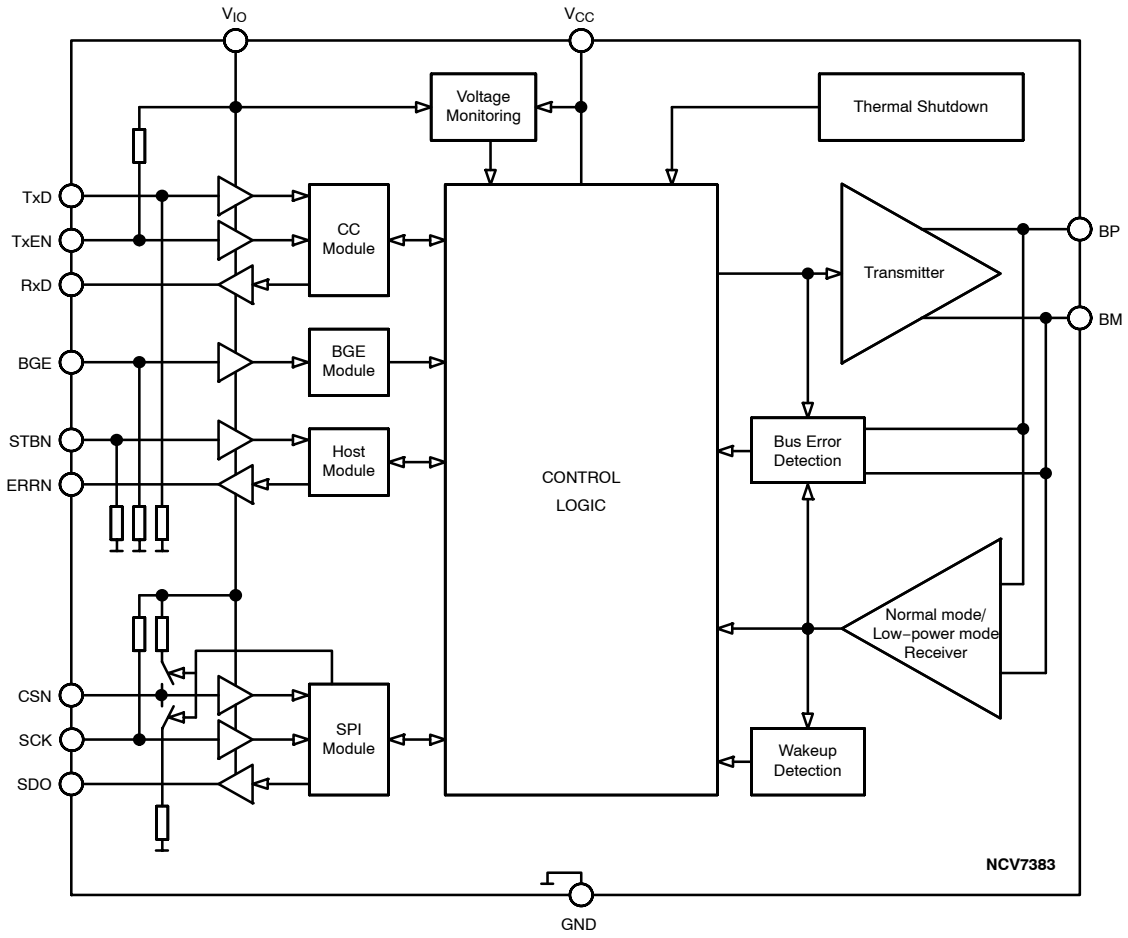


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Pin Type	Pin Function
1	V_{IO}	supply	Supply voltage for digital pins level adaptation
2	TxD	digital input, internal PD	Data to be transmitted
3	TxEN	digital input, internal PU	Transmitter enable input; when High, transmitter disabled
4	RxD	digital output	Receive data output
5	BGE	digital input, internal PD	Bus guardian enable input; when Low, transmitter disabled
6	STBN	digital input, internal PD	Mode control input
7	SCK	digital input, internal PU	SPI clock input
8	SDO	digital output	SPI data output
9	CSN	digital input, internal PU or PD	Chip select input, active Low
10	ERRN	digital output	Bus Driver error condition indication
11	GND	ground	Ground connection
12	BM	high−voltage analog input/output	Bus line minus
13	BP	high−voltage analog input/output	Bus line plus
14	V_{CC}	supply	Bus driver core supply voltage; 5V nominal

Notes: PU means Pull−up
PD means Pull−down

APPLICATION INFORMATION

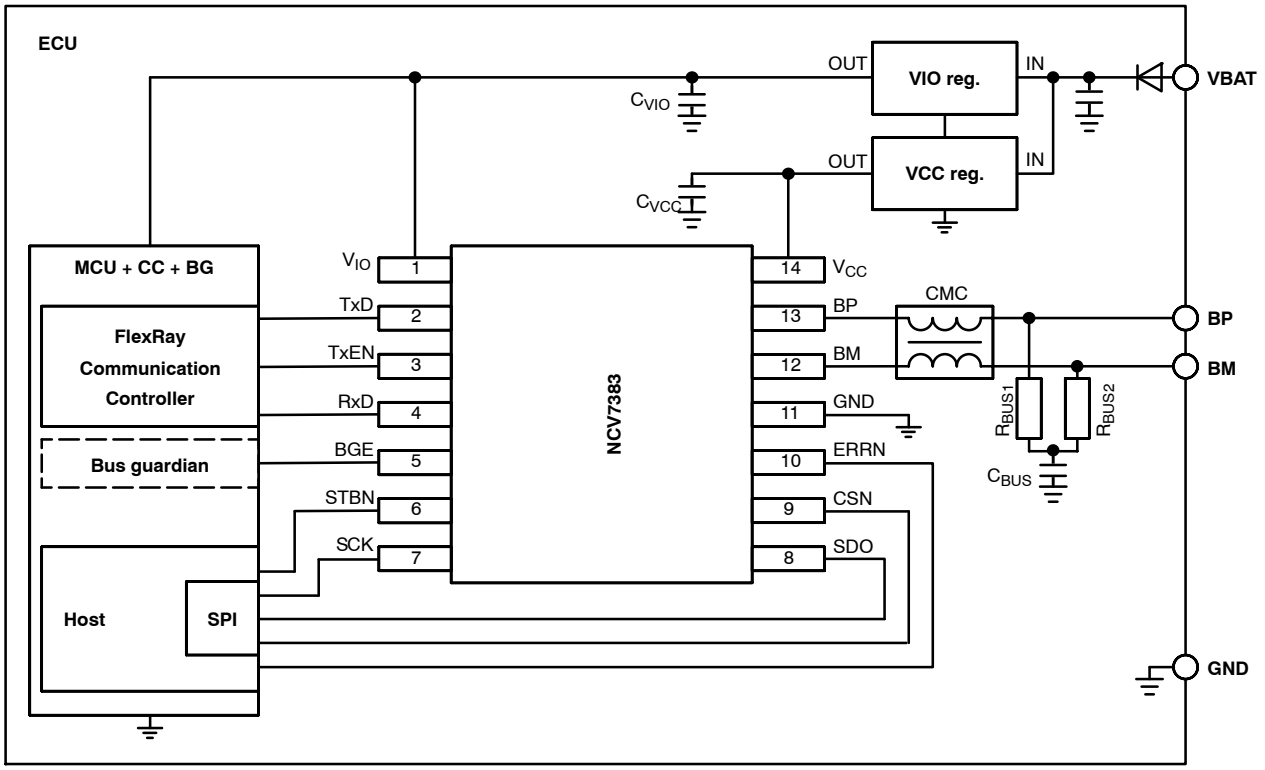


Figure 2. Application Diagram

Table 2. RECOMMENDED EXTERNAL COMPONENTS FOR THE APPLICATION DIAGRAM

Component	Function	Min	Typ	Max	Unit	Note
C_{VCC}	Decoupling capacitor on V_{CC} supply line, ceramic		100		nF	
C_{VIO}	Decoupling capacitor on V_{IO} supply line, ceramic		100		nF	
R_{BUS1}	Bus termination resistor		47.5		Ω	(Note 1)
R_{BUS2}	Bus termination resistor		47.5		Ω	(Note 1)
C_{BUS}	Common−mode stabilizing capacitor, ceramic		4.7		nF	(Note 2)
CMC	Common−mode choke		100		μH	

1. Tolerance ±1%, type 0805. The value R_{BUS1}+R_{BUS2} should match the nominal cable impedance.
2. Tolerance ±20%, type 0805

FUNCTIONAL DESCRIPTION

Operating Modes

NCV7383 can switch between two operating modes depicted in Figure 3. In Normal mode, the chip interconnects a FlexRay communication controller with the bus medium for full−speed communication. This mode is also referred to as normal−power mode.

In Standby mode, the communication is suspended and the power consumption is substantially reduced. A wakeup on the bus can be detected and signaled to the host. The Standby mode is referred to as low−power mode.

The operating mode selected is a function of the host signal STBN, the state of the supply voltages and the wakeup detection. As long as both supplies (V_{CC} and V_{IO}) remain above their respective under−voltage detection levels, the logical control by STBN pin shown in Figure 3 applies. Influence of the power−supplies and of the wakeup detection on the operating modes is described in subsequent paragraphs.

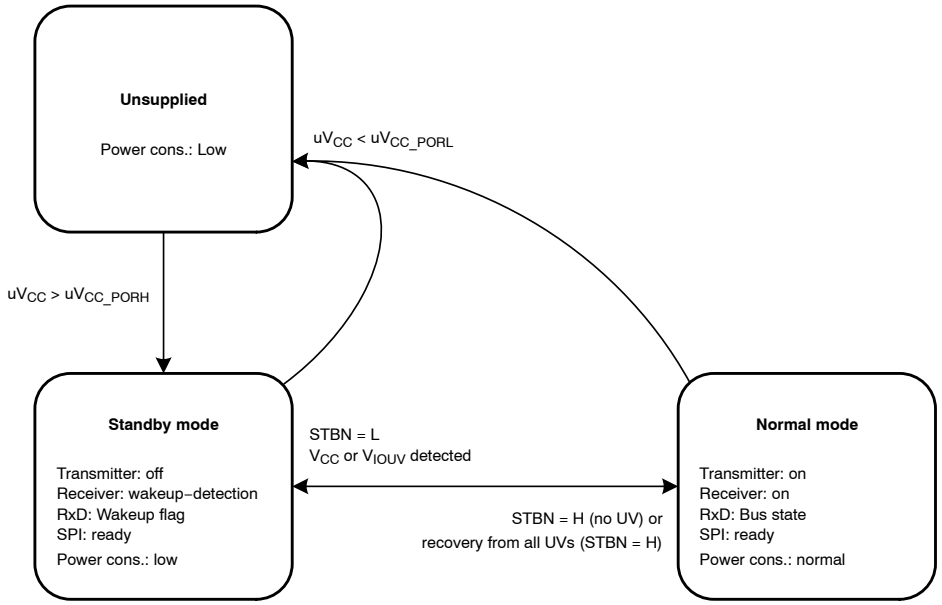


Figure 3. State Diagram

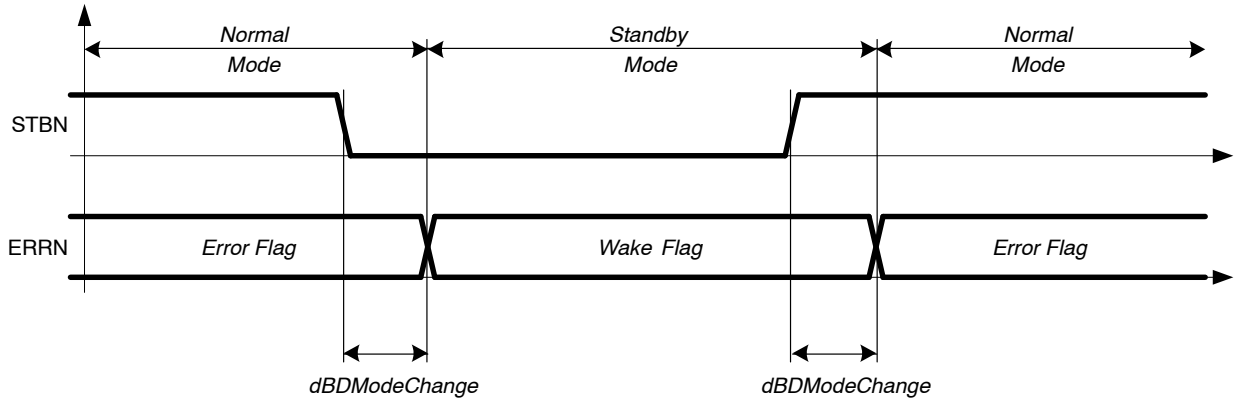


Figure 4. Timing Diagram of Operating Modes Control by the STBN Pin

Power Supplies and Power Supply Monitoring

NCV7383 is supplied by two pins. V_{CC} is the main 5 V supply powering NCV7383 and the FlexRay bus driver core. V_{IO} supply serves to adapt the logical levels of NCV7383 to the host and/or the FlexRay communication controller digital signal levels. Both supplies should be properly decoupled by filtering capacitors − see Figure 2 and Table 2.

V_{IO} supply voltage can be applied prior to V_{CC} during Power−up event, however the NCV7383 is not considered

supplied until V_{CC} supply voltage is above uV_{CC_PORH} threshold ($V_{CC} > uV_{CC\_PORH}$) − See Table 3.

Both supplies are monitored by under−voltage detectors with individual thresholds and filtering times both for under−voltage detection and recovery − see Table 15.

Junction Temperature Monitoring

In order to protect the NCV7383 from being damaged in case of thermal event, a junction temperature monitoring is implemented. High ambient temperature together with the device high power dissipation can lead to junction temperature reaching a critical temperature. Under certain failure conditions (e.g. bus pin shorted to the supply voltage during the transmitter active state), the device power dissipation can be rapidly increased even though the absolute short current is limited. If the junction temperature is higher than T_{JSD} (typically 165°C) in Normal mode, Thermal Shutdown flag is set and the transmitter is disabled. This will reduce the power dissipation and decrease the junction temperature.

The transmitter is enabled as soon as the Thermal Shutdown flag is cleared. This requires the junction temperature falling below the Thermal Shutdown level and TxEN pin being set to High in Normal mode.

Logic Level Adaptation

Level shift input V_{IO} is used to apply a reference voltage $uV_{DIG} = uV_{IO}$ to all digital inputs and outputs in order to adapt the logical levels of NCV7383 to the host and/or the FlexRay communication controller digital signal levels.

Internal Flags

The NCV7383 control logic uses a number of internal flags (i.e. one−bit memories) reflecting important conditions or events. Table 3 summarizes the individual flags and the conditions that lead to a set or reset of the flags.

Table 3. INTERNAL FLAGS

Flag	Set Condition	Reset Condition	Comment
Remote Wakeup	V_{CC} Under−voltage flag is not set and Remote Wakeup is detected in Standby mode	Normal mode is entered	RxD and ERRN are set Low if Remote Wakeup flag is set and STBN is Low
Mode	Normal mode is entered	Normal mode is left	
Transmitter Ready	All of the following terms are valid: The bus driver is in Normal mode TxEN Timeout flag is not set BGE is High Thermal Shutdown flag is not set	Any of the following terms is valid: The bus driver is not in Normal mode TxEN Timeout flag is set BGE is Low Thermal Shutdown flag is set	
Power−on	V_{CC} power supply level becomes sufficient for the operation of the control logic	Normal mode is entered	
Bus Error	Transmitter is enabled and Data on bus are different from TxD signal (sampled after each TXD edge)	(Transmitter is enabled and Data on bus are identical to TxD signal) or TxEN is set High or Normal mode is left	The bus error flag has no influence on the bus driver function
Thermal Shutdown	Junction temperature is higher than *Tjsd* (typ. 165°C) in a Normal mode	Junction temperature is below *Tjsd* in a Normal mode and TxEN is High or Normal mode is left	The transmitter is disabled as long as the thermal shutdown flag is set
TxEN Time-out	TxEN is Low for longer than dBDTxActiveMax (typ. 1.5 ms) in a Normal mode	TxEN is High or Normal mode is left	The transmitter is disabled as long as the timeout flag is set
V_{CC} Under−voltage	V_{CC} is below the under−voltage threshold for longer than $dBDUVV_{CC}$	V_{CC} is above the under−voltage threshold for longer than $dBDRV_{CC}$	Standby mode is forced as long as the V_{CC} UV flag is set
V_{IO} Under−voltage	V_{IO} is below the under−voltage threshold for longer than dUV_{IO}	V_{IO} is above the under−voltage threshold for longer than $dBDRV_{IO}$ or Remote Wakeup flag becomes set	Standby mode is forced as long as the V_{IO} UV flag is set

Table 3. INTERNAL FLAGS

Flag	Set Condition	Reset Condition	Comment
SPI Error	SPI error is detected: Number of SCK falling edges while CSN is Low is different from 16 or SCK is not Low at CSN falling or rising edge	CSN falling edge is detected or Track mode is entered	The status bits update is discarded if SPI Error is detected
Error	Any of the following flags is set: • Bus error • Thermal Shutdown • TxEN Timeout • V_{CC} Under−voltage • V_{IO} Under−voltage • SPI Error	All of the following Flags (Track mode) or Status bits (Latched mode) are reset: • Bus error • Thermal Shutdown • TxEN Timeout • V_{CC} Under−voltage • V_{IO} Under−voltage • SPI Error	ERRN is set Low if Error flag is set and STBN is High

Internal Error Flag

There are two Error Signaling modes:

- Track mode − the common Error flag is reset when all of the Error related flags are reset − Error flag is directly visible on ERRN pin if STBN pin is High. Minimum ERRN pin indication time is $dBDERRN_{STABLE}$.
- Latched mode − the common Error flag is reset when all of the related Status Bits are reset (requires successful status Register read−out while all these flags are reset). The common Error flag is visible on ERRN pin if STBN pin is High and the particular flags are accessible via SPI interface.

After Power−up the Error signaling is switched to the Latched mode by default (internal Pull−Up on CSN pin).

When V_{IO} is not in under−voltage Error indication Track mode can be selected by host request (setting CSN pin Low for longer than *dERRNModeChange* while SCK is set High − see Figure 5), or simply by leaving CSN pin permanently connected to GND and SCK pin permanently connected to V_{IO}. As soon as Error Indication Track mode is selected, CSN pin internal Pull−Up is switched to Pull−Down providing the CSN pin input current is reduced.

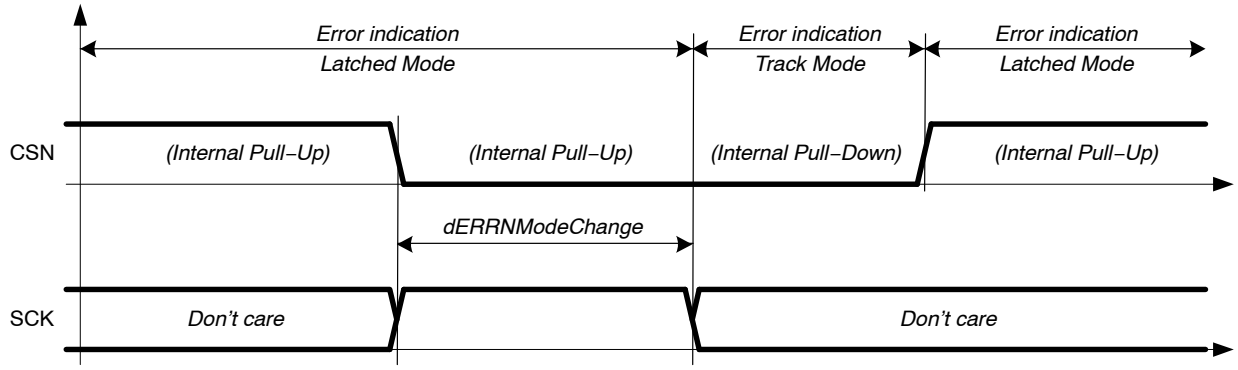


Figure 5. Timing Diagram of Error Indication Mode Control.

ERRN Pin signaling

Provided V_{IO} supply is present together with V_{CC}, the digital output ERRN indicates the state of the internal "Error" flag when the Normal mode is commanded by STBN and the state of the internal "Wake" flag when the Standby mode is commanded by STBN.

The polarity of the indication is reversed − ERRN pin is pulled Low when the "Error" flag or "Wake" flag (depends on STBN pin state) is set. The signaling on pin ERRN is functional in both operating modes.

Table 4. SIGNALING ON ERRN PIN

STBN	Description	Error Flag	Wake Flag	ERRN
High	Detected error signaling	not set	x	High
		set	x	Low
Low	Detected Wakeup event signaling	x	not set	High
		x	set	Low

Failure Conditions Handling

Safe behavior of the NCV7383 is guaranteed in order not to disturb the rest of the FlexRay network in case the NCV7383 is under following fault conditions:

- Undervoltage on V_{IO} and/or V_{CC} − Standby mode is entered and transmitter is disabled
- BP or BM is shorted to GND or to Supply voltage − The absolute bus pins output current is limited
- BP and BM are shorted together − The absolute bus pins output current is limited
- GND pin is unconnected while all digital inputs are High − Absolute BP and BM leakage current and input current of the digital input pins are limited.
- TxEN is Low for longer than *dBDTxActiveMax* (typ. 1.5 ms) when the NCV7383 is in a Normal mode −the transmitter is disabled
- Junction temperature exceeds the Thermal Shutdown Temperature (T_{JSD}, typ. 165°C) when the NCV7383 is in a Normal mode − the transmitter is disabled

SPI Interface and Status Register

A full set of internal bits referred to as status register can be read through the Serial Peripheral Interface (SPI). The status register content is described in Table 5 while an example of the read−out waveform is shown in Figure 6.

As long as the CSN chip select is High, the SCK clock input is not relevant and the SDO output is kept in High−Impedance state. The signal on the SCK input is taken into account only when CSN chip select input is set to Low.

The individual status bits are channeled to SDO pin at the rising edge on SCK pin. The NCV7383 SPI supports baud rates from 10 kbit/s to 2 Mbit/s. The status register consist of 16 main bits and 16 additional bits providing information about the analog and digital part version. The read−out always starts with bit S0.

One SPI frame consists of exactly sixteen bits transferred from the NCV7383 to the host through output pin SDO. The number of SCK falling edges is checked on every SPI frame. If the number is different from 16, the SPI frame is considered as incorrect, SPI frame error flag is set and the status register bits S4−S10 are not reset when the read−out is finished. As soon as the CSN is set to High and no violation was detected in the SPI frame, the read−out is considered as finished. At the same time, the status register bits S4 to S10 are reset provided the corresponding flags are reset − see Table 5.

Additionally, the total number of bits shifted to SDO during the read−out can be extended to 32, considering the SPI frame incorrect. This provides ability to obtain the additional status register bits identifying the production masks version. Such SPI frame sets the SPI frame error flag and the status register bits S4−S10 are not reset when the read−out is finished.

SPI interface is fully functional only if Latched Error Indication mode is selected and V_{IO} supply is not in undervoltage.

SPI interface is disabled in Power−Off mode (V_{CC} < uV_{CC_PORL}) even if V_{IO} supply voltage is not in undervoltage.

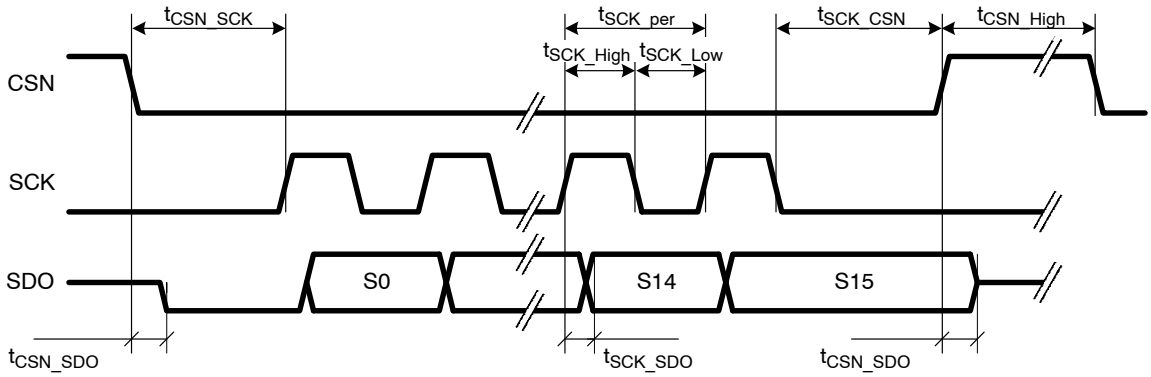


Figure 6. Definition of SPI Timing Parameters

Table 5. STATUS REGISTER

Bit Number	Status Bit Content	Note	Reset After Finished Read−out
S0	Remote wakeup flag	reflects directly the corresponding flag	no
S1	Mode flag		
S2	Transmitter ready flag		
S3	BGE Feedback	Normal mode: BGE pin logical state (Note 3) Other modes: Low	−
S4	Power−on status	the status bit is set if the corresponding flag was set previously (the respective High level of the flag is latched in its status counter−part)	yes, if the corresponding flag is reset and the SPI frame was correct (no SPI error)
S5	Bus error status		
S6	Thermal shutdown status		
S7	TxEN Timeout status		
S8	V_{CC} Under−voltage status		
S9	V_{IO} Under−voltage status		
S10	SPI Error status		
S11	not used; always Low	−	−
S12	not used; always High	−	−
S13	not used; always Low	−	−
S14	not used; always High	−	−
S15	Parity	Exclusive−OR of Status bits S0−S14	−
S16−S23	Version of the NCV7383 analog part	Fixed values identifying the production masks version. Cannot be read out without detection of an SPI Error	−
S24−S31	Version of the NCV7383 digital part		

3. The BGE pin state is latched during Status bit S2 read−out, at the SCK pin falling edge.

Mode Changes Caused by Internal Flags

Changes of some internal flags described in Table 3 can force an operating mode transition complementing or overruling the operating mode control by the digital input STBN which is shown in Figure 3:

- Setting the V_{IO} or V_{CC} under−voltage flag causes a transition to the Standby mode
- Reset of the Under−voltage flag (i.e. recovery from under−voltage) re−enables the control of the chip by digital input STBN.
- Setting of the Wake flag causes the reset of all under−voltage flags. The NCV7383 stays in the Standby mode.

FlexRay Bus Driver

NCV7383 contains a fully−featured FlexRay bus driver compliant with Electrical Physical Layer Specification Rev. 3.0.1. The transmitter part translates logical signals on digital inputs TxEN, BGE and TxD into appropriate bus levels on pins BP and BM. A transmission cannot be started with Data_1. In case the TxEN is set Low for longer than *dBDTxActiveMax* in Normal mode, the TxEN Timeout flag is set and the transmitter is disabled. The receiver part monitors bus pins BP and BM and signals the detected levels on digital output RxD. The different bus levels are defined in Figure 7. The function of the bus driver and the related digital pins in different operating modes is detailed in Tables 6 and 7.

- The transmitter can only be enabled if the activation of the transmitter is initiated in Normal mode.
- The Normal mode receiver function is enabled by entering the Normal mode.
- The Low power receiver function is enabled by entering the Standby mode.

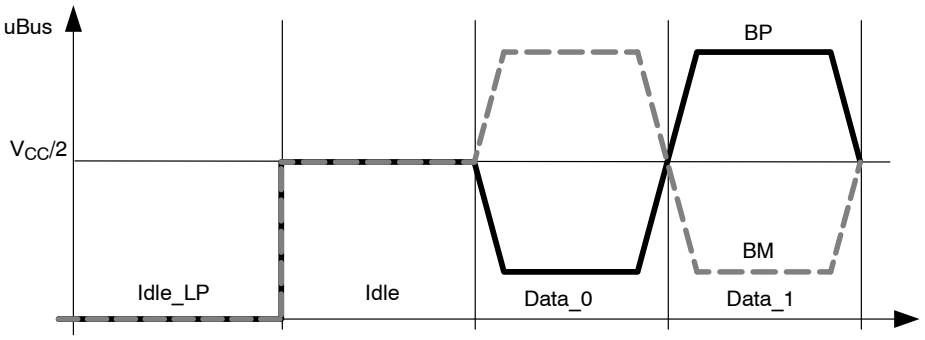


Figure 7. FlexRay Bus Signals

Table 6. TRANSMITTER FUNCTION AND TRANSMITTER−RELATED PINS

Operating Mode	BGE	TxEN	TxD	Transmitted Bus Signal
Standby	x	x	x	Idle_LP
Normal	0	x	x	Idle
	1	1	x	Idle
	1	0	0	Data_0
	1	0	1	Data_1

Table 7. RECEIVER FUNCTION AND RECEIVER−RELATED PINS

Operating Mode	Signal on Bus	Wake flag	RxD
Standby	x	not set	High
	x	set	Low
Normal	Idle	x	High
	Data_0	x	Low
	Data_1	x	High

Bus Guardian Interface

The interface consists of the BGE digital input signal allowing a Bus Guardian unit to disable the transmitter.

Bus Driver Remote Wakeup Detection

During the Standby mode and under the presence of V_{CC} voltage, a low−power receiver constantly monitors the

activity on bus pins BP and BM. A valid remote wake−up is detected when either a wakeup pattern or a dedicated wakeup frame is received.

A wakeup pattern is composed of two Data_0 symbols separated by Data_1 or Idle symbols. The basic wakeup pattern composed of Data_0 and Idle symbols is shown in Figure 8; the wakeup pattern composed of Data_0 and Data_1 symbols − referred to as “alternative wakeup pattern” − is depicted in Figure 9.

A remote wake−up is detected even if a transition from Normal mode to Standby mode takes place while a valid wakeup pattern is being received (if the wakeup pattern starts in Normal mode and ends in Standby mode).

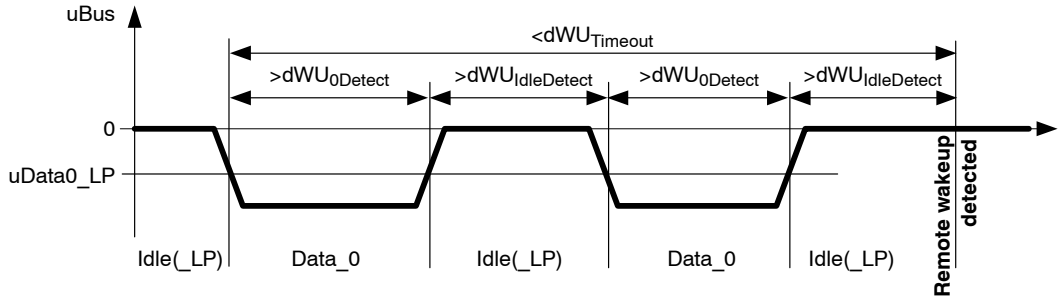


Figure 8. Valid Remote Wakeup Pattern

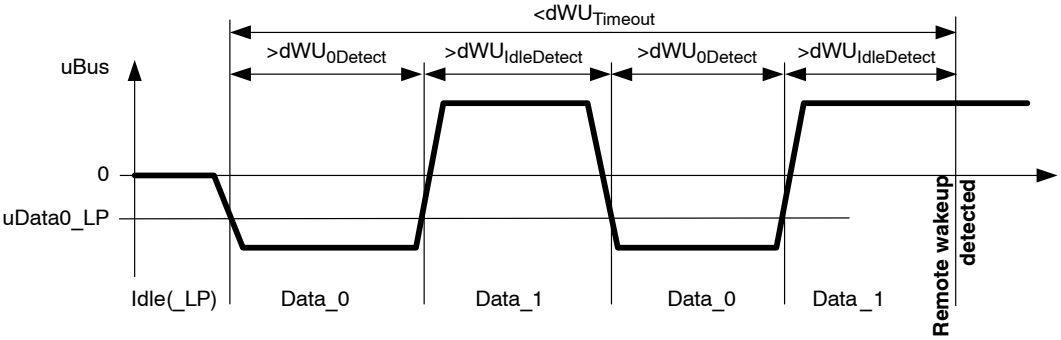


Figure 9. Valid Alternative Remote Wakeup Pattern

A remote wakeup will be also detected if NCV7383 receives a full FlexRay frame at 10 Mbit/s with the following payload data:
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF
The wakeup pattern, the alternative wakeup pattern and the wakeup frame lead to identical wakeup treatment and signaling.

ABSOLUTE MAXIMUM RATINGS

Table 8. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
uV_{CC-MAX}	5V Supply voltage		−0.3	5.5	V
uV_{IO-MAX}	Supply voltage for V_{IO} voltage level adaptation		−0.3	5.5	V
$uDigIn_{MAX}$	DC voltage at digital inputs (STBN, TxD, TxEN, BGE, SCSN, SCLK)		−0.3	5.5	V
$uDigOut_{MAX}$	DC voltage at digital Outputs (RxD, ERRN, SDO)		−0.3	V_{IO}+0.3	V
$iDigOut_{IN-MAX}$	Digital output pins input current (V_{IO} = 0 V)		−10	10	mA
uBM_{MAX}	DC voltage at pin BM		−50	50	V
uBP_{MAX}	DC voltage at pin BP		−50	50	V
T_{J_MAX}	Junction temperature		−40	175	°C
T_{STG}	Storage Temperature Range		−55	150	°C
$uESD_{IEC}$	System HBM on pins BP and BM (as per IEC 61000−4−2; 150 pF/330 Ω)		−10	+10	kV
$uESD_{EXT}$	Component HBM on pins BP, BM (as per EIA−JESD22−A114−B; 100 pF/1500 Ω)		−8	+8	kV
$uESD_{INT}$	Component HBM on all other pins (as per EIA−JESD22−A114−B; 100 pF/1500 Ω)		−4	+4	kV
uV_{TRAN}	Voltage transients, pins BP and BM According to ISO7637−2, Class C (Note 4)	test pulses 1	−100	−	V
		test pulses 2a	−	+75	V
		test pulses 3a	−150	−	V
		test pulses 3b	−	+100	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. Test is carried out according to setup in *FlexRay Physical Layer EMC Measurement Specification, Version 3.0*. This specification is referring to ISO7637. Test for higher voltages is planned.

OPERATING RANGES

Table 9. NCV7383: OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
uV_{CC-OP}	Supply voltage 5 V	4.75	5.25	V
uV_{IO-OP}	Supply voltage for V_{IO} voltage level adaptation	2.3	5.25	V
$uDigIO_{OP}$	DC voltage at digital pins (TxD, TxEN, RxD, BGE, STBN, ERRN, SCSN, SCLK, SDO)	0	V_{IO}	V
uBM_{OP}	DC voltage at pin BM	−50	50	V
uBP_{OP}	DC voltage at pin BP	−50	50	V
T_{AMB}	Ambient temperature (Note 5)	−40	125	°C
T_{J_OP}	Junction temperature	−40	150	°C

5. The specified range corresponds to T_{AMB_Class1}

THERMAL CHARACTERISTICS

Table 10. PACKAGE THERMAL RESISTANCE

Symbol	Rating	Value	Unit
$R_{\theta JA\_1}$	Thermal Resistance Junction−to−Air, JEDEC 1S0P PCB	153	K/W
$R_{\theta JA\_2}$	Thermal Resistance Junction−to−Air, JEDEC 2S2P PCB	104	K/W

ELECTRICAL CHARACTERISTICS

The characteristics defined in this section are guaranteed within the operating ranges listed in Table 9, unless stated otherwise. Positive currents flow into the respective pin.

Table 11. CURRENT CONSUMPTION

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$iV_{CC-NORM-IDLE}$	Current consumption from V_{CC}	Normal mode − bus signals Idle			15	mA
$iV_{CC-NORM-ACTIVE}$		Normal mode − bus signals Data_0/1 R_{BUS} = No load			37	mA
		Normal mode − bus signals Data_0/1 R_{BUS} = 40−55 Ω			72	mA
iV_{CC-LP}		Standby mode, $T_J \le 85°C$ (Note 6)			30	μA
$iV_{IO-NORM}$	Current consumption from V_{IO}	Normal mode			1	mA
iV_{IO-LP}		Standby mode, $T_J \le 85°C$ (Note 6)			6	μA
$iTot_{-LP}$	Total current consumption − Sum from all supply pins	Standby mode			53	μA
		Standby mode, $T_J < 85°C$ (Note 6)			37	μA
		Standby mode, $T_J < 25°C$ (Note 6)			24	μA

6. Values based on design and characterization, not tested in production

Table 12. TRANSMISSION PARAMETERS

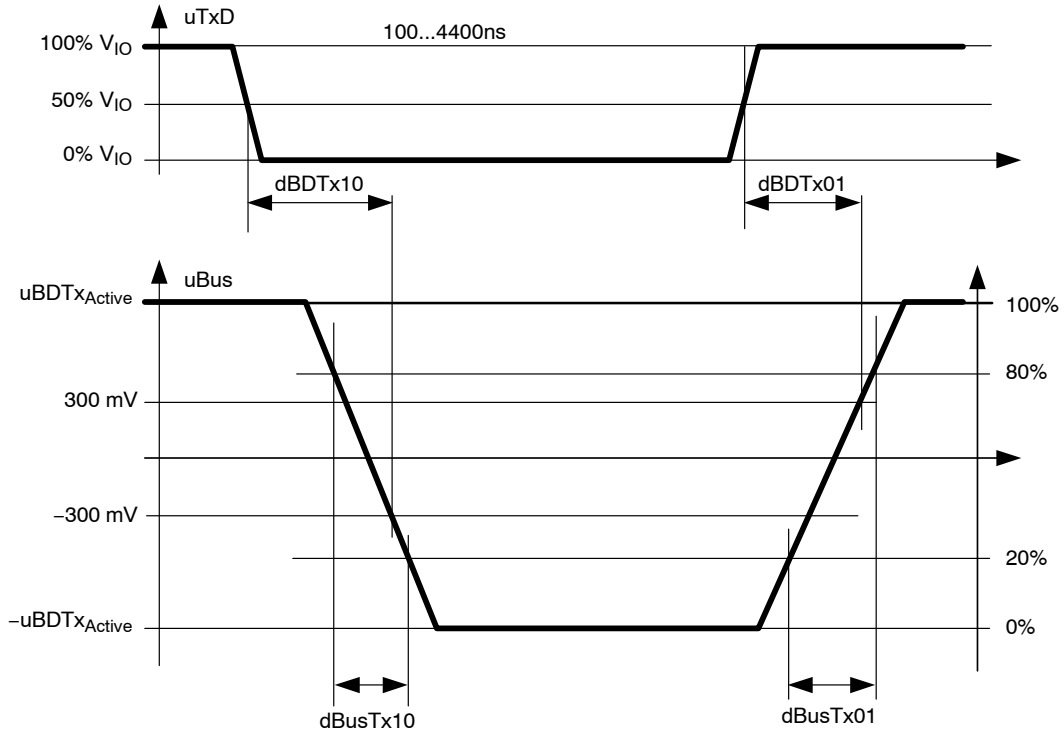
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$uBDTx_{active}$	Differential voltage |uBP−uBM| when sending symbol "Data_0" or "Data_1" (Functional class Bus driver increased voltage amplitude transmitter)	R_{BUS} = 40−55 Ω; C_{BUS} = 100 pF Parameters defined in Figure 10.	600		2000	mV
$uBDTx_{Idle}$	Differential voltage |uBP−uBM| when driving signal "Idle"		0		25	mV
dBDTx10	Transmitter delay, negative edge	Test setup as per Figure 14 with R_{BUS} = 40 Ω; C_{BUS} =100 pF Sum of TxD signal rise and fall time (20%−80% V_{IO}) of up to 9 ns Parameters defined in Figure 10.			60	ns
dBDTx01	Transmitter delay, positive edge				60	ns
dBDTxAsym	Transmitter delay mismatch, |dBDTx10−dBDTx01| (Note 8)				4	ns
dBusTx10	Fall time of the differential bus voltage from 80% to 20%		6		18.75	ns
dBusTx01	Rise time of the differential bus voltage from 20% to 80%		6		18.75	ns
dBusTxDif	Differential bus voltage fall and rise time mismatch |dBusTx10−dBusTx01|				3	ns

7. Values based on design and characterization, not tested in production
8. Guaranteed for ±300mV and ±150 mV level of uBus
9. Not tested in production. Limits based on bus driver simulations. For more information see *FlexRay Communication System − Electrical Physical Layer Specification, Version 3.0.1*.

Table 12. TRANSMISSION PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$dTxEN_{LOW}$	Time span of bus activity	Test setup as per Figure 14 with R_{BUS} = 40 Ω; C_{BUS} = 100 pF Parameters defined in Figure 11.	550		650	ns
dBDTxia	Transmitter delay idle –> active				75	ns
dBDTxai	Transmitter delay active –> idle				75	ns
dBDTxDM	Idle−active transmitter delay mismatch | dBDTxia − dBDTxai |				50	ns
dBusTxia	Transition time idle >active				30	ns
dBusTxai	Transition time active > idle				30	ns
dBDBGEia	BGE delay idle –> active (Note 7)	R_{BUS} = 40 Ω; C_{BUS} = 100 pF			75	ns
dBDBGEai	BGE delay active > idle (Note 7)				75	ns
dBDTxActiveMax	Maximum length of transmitter activation		650		2600	μs
$iBP_{BMShortMax}$ $iBM_{BPShortMax}$	Absolute maximum output current when BP shorted to BM − no time limit	$R_{ShortCircuit} \le 1\ \Omega$			60	mA
$iBP_{GNDShortMax}$ $iBM_{GNDShortMax}$	Absolute maximum output current when shorted to GND − no time limit	$R_{ShortCircuit} \le 1\ \Omega$			60	mA
$iBP_{-5VShortMax}$ $iBM_{-5VShortMax}$	Absolute maximum output current when shorted to −5 V − no time limit	$R_{ShortCircuit} \le 1\ \Omega$			60	mA
$iBP_{BAT27ShortMax}$ $iBM_{BAT27ShortMax}$	Absolute maximum output current when shorted to 27 V − no time limit	$R_{ShortCircuit} \le 1\ \Omega$			60	mA
$iBP_{BAT48ShortMax}$ $iBM_{BAT48ShortMax}$	Absolute maximum output current when shorted to 48 V − no time limit	$R_{ShortCircuit} \le 1\ \Omega$			72	mA
$R_{BDTransmitter}$	Bus interface equivalent output impedance Bus driver simulation model parameter (Note 9)		31	105	500	Ω

7. Values based on design and characterization, not tested in production
8. Guaranteed for ±300mV and ±150 mV level of uBus
9. Not tested in production. Limits based on bus driver simulations. For more information see *FlexRay Communication System − Electrical Physical Layer Specification, Version 3.0.1*.



TxD signal is constant for 100..4400 ns before the first edge.
All parameters values are valid even if the test is performed with opposite polarity.

Figure 10. Transmission Parameters (TxEN is Low and BGE is High)

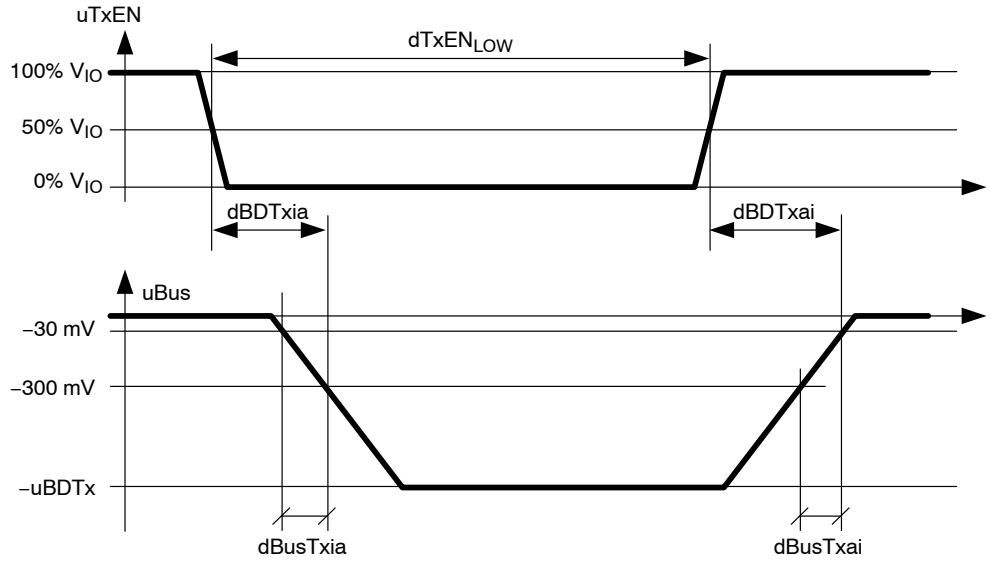


Figure 11. Transmission Parameters for Transitions between Idle and Active (TxD is Low)

Table 13. RECEPTION PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
uData0	Receiver threshold for detecting Data_0	Activity detected previously. |uBP−uBM| ≤ 3 V	−300		−150	mV
uData1	Receiver threshold for detecting Data_1		150		300	mV
|uData1|−|uData0|	Mismatch of receiver thresholds	(uBP+uBM)/2 = 2.5 V	−30		30	mV
uData0_LP	Low power receiver threshold for detecting Data_0	uV_{CC} = 5 V.	−400		−100	mV
uCM	Common mode voltage range (with respect to GND) that does not disturb the receiver function and reception level parameters	uBP = (uBP+uBM)/2 (Note10)	−10		15	V
uBias	Bus bias voltage during bus state Idle in Normal mode	R_{BUS}= 40 − 55 Ω; C_{BUS}= 100 pF (Note 11)	1800	2500	3150	mV
	Bus bias voltage during bus state Idle in Standby mode		−100	0	100	mV
R_{CM1}, R_{CM2}	Receiver common mode resistance	(Note 11)	10		40	kΩ
C_BP, C_BM	Input capacitance on BP and BM pin (Note 13)	f = 5 MHz			20	pF
C_Bus_{DIF}	Bus differential input capacitance (Note 13)	f = 5 MHz			5	pF
iBP_{LEAK} iBM_{LEAK}	Absolute leakage current when driver is off	uBP = uBM = 5 V All other pins = 0 V			5	μA
$iBP_{LEAKGND}$ $iBM_{LEAKGND}$	Absolute leakage current, in case of loss of GND	uBP = uBM = 0 V All other pins = 16 V			1600	μA
$uBusRx_{Data}$	Test signal parameters for reception of Data_0 and Data_1 symbols	Test signal and parameters defined in Figures 12 and 13. RxD pin loaded with 25 pF capacitor.	400		3000	mV
$dBusRx0_{BD}$			60		4330	ns
$dBusRx1_{BD}$			60		4330	ns
dBusRx10					22.5	ns
dBusRx01					22.5	ns
dBDRx10	Receiver delay, negative edge (Note 12)				75	ns
dBDRx01	Receiver delay, positive edge (Note 12)				75	ns
dBDRxAsym	Receiver delay mismatch |dBDRx10− dBDRx01| (Note 12)				5	ns
uBusRx	Test signal parameters for bus activity detection		400		3000	mV
dBusActive			590		610	ns
dBusIdle			590		610	ns
dBusRxia			18		22	ns
dBusRxai			18		22	ns
dBDIdleDetection	Bus driver filter−time for idle detection		50		200	ns
dBDActivityDetection	Bus driver filter−time for activity detection		100		250	ns
dBDRxai	Bus driver idle reaction time		100		275	ns
dBDRxia	Bus driver activity reaction time		100		325	ns
dBDTxRxai	Idle−Loop delay				300	ns

10. Tested on a receiving bus driver. Sending bus driver has a ground offset voltage in the range of [−12.5 V to +12.5 V] and sends a 50/50 pattern.
11. Bus driver is connected to GND and uV_{CC} = 5 V.
12. Guaranteed for ±300 mV and ±150 mV level of *uBus*
13. Values based on design and characterization, not tested in production

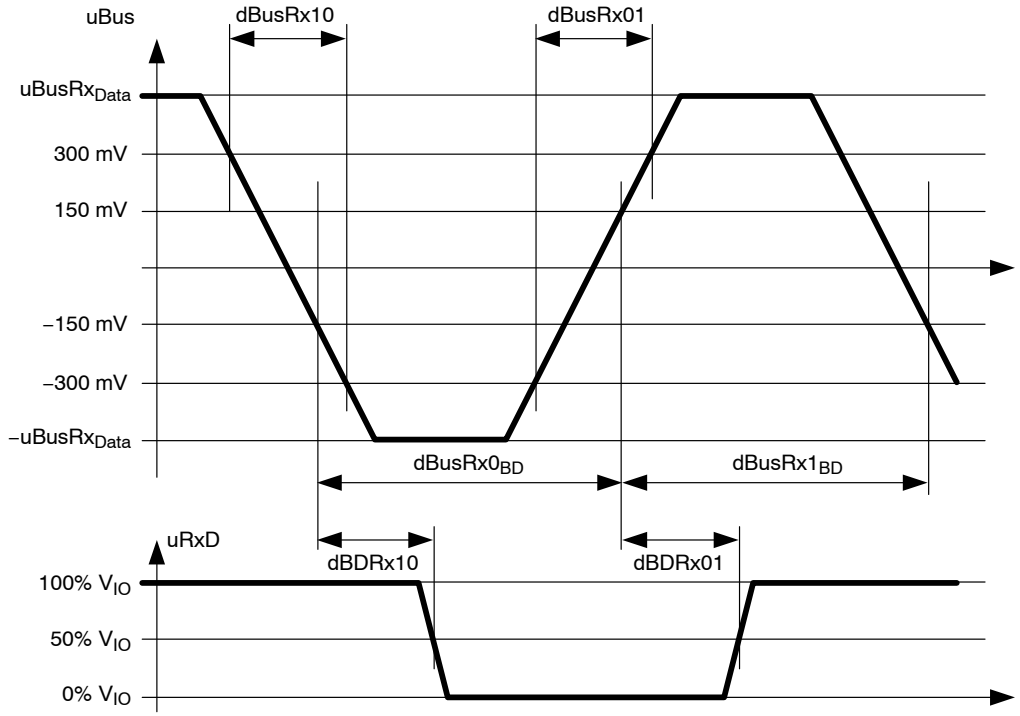


Figure 12. Reception Parameters

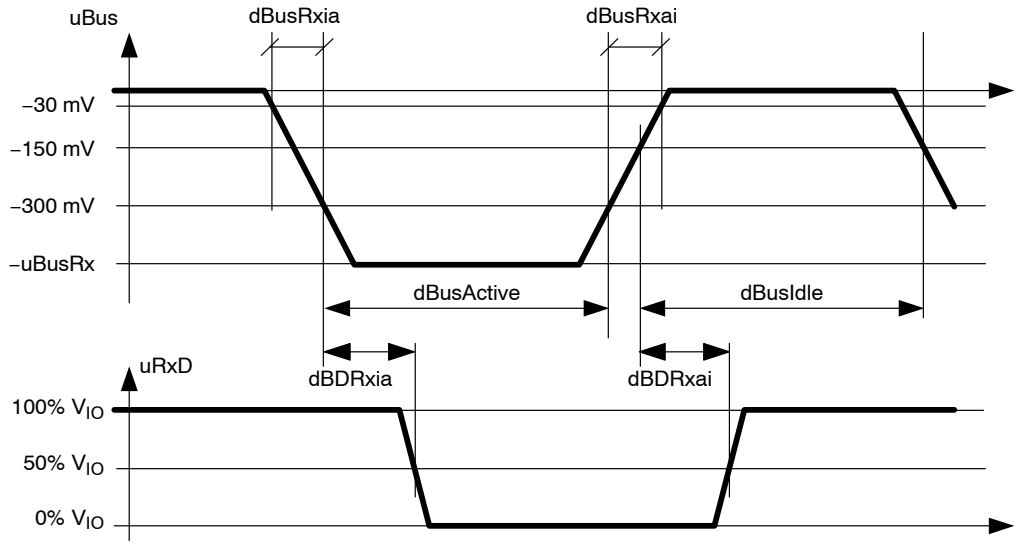


Figure 13. Parameters of Bus Activity Detection

Table 14. REMOTE WAKE−UP DETECTION PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$dWU_{0Detect}$	Wake−up detection time for Data_0 symbol		1		4	μs
$dWU_{IdleDetect}$	Wake−up detection time for Idle/Data_1		1		4	μs
$dWU_{Timeout}$	Total Wake−up detection time (Note 15)		50		140	μs
$dWU_{Interrupt}$	Acceptance timeout for interruptions	(Note 14)	0.13		1	μs
dBDWakeup $Reaction_{remote}$	Reaction time after remote wakeup event (Note 15)				50	μs

14. The minimum value is only guaranteed, when the phase that is interrupted was continuously present for at least 870ns.
15. Values based on design and characterization, not tested in production

Table 15. POWER SUPPLY MONITORING PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$uBDUVV_{CC}$	V_{CC} under−voltage threshold		4		4.5	V
uUV_{IO}	V_{IO} under−voltage threshold		2		2.3	V
uUV_HYST	Hysteresis of the under−voltage detectors		20	100	200	mV
$dBDUVV_{CC}$	V_{CC} Undervoltage detection time (Note 16)		35	60	100	μs
$dBDUVV_{IO}$	V_{IO} Undervoltage detection time (Note 16)		35	60	100	μs
$dBDRV_{CC}$	V_{CC} Undervoltage recovery time (Note 16)		35	60	100	μs
$dBDRV_{IO}$	V_{IO} Undervoltage recovery time (Note 16)		14	30	48	μs
uV_{CC_PORH}	V_{CC} threshold for power on event		3.0		3.9	V
uV_{CC_PORL}	V_{CC} threshold for power off event		2.95		3.85	V

16. Values based on design and characterization, not tested in production

Table 16. TEMPERATURE MONITORING PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{JSD}	Thermal shut−down level		150	165	185	°C

Table 17. HOST INTERFACE TIMING PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dBDModeChange	STBN level filtering time for operating mode transition (Note 17)		14		50	μs
$dReactionTime_{ERRN}$	Reaction time on ERRN pin				50	μs
$dBDERRN_{STABLE}$	Error signaling time	Track mode	1		10	μs
dERRNModeChange	Error signaling mode change request detection time	Latched mode V_{IO} UV flag not set	95		330	μs

17. Values based on design and characterization, not tested in production

Table 18. SPI INTERFACE TIMING CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dCSN_SCK	First SPI clock edge after CSN active		250			ns
dSCK_CSN	Last SPI clock edge before CSN inactive		250			ns
dCSN_SDO	SDO output stable after CSN active				150	ns
	SDO output High−Z after CSN inactive				150	ns
dSCK_per	SPI clock period		0.5		100	μs
dSCK_High	Duration of SPI clock High level		250			ns
dSCK_Low	Duration of SPI clock Low level		250			ns
dSCK_SDO	SDO output stable after an SPI clock rising edge				150	ns
dCSN_High	SPI Inter−frame space (CSN inactive)		250			ns

DIGITAL INPUT SIGNALS

Table 19. DIGITAL INPUT SIGNALS VOLTAGE THRESHOLDS (Pins STBN, BGE, TxEN, CSN, SCK)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$uV_{DIG-IN-LOW}$	Low level input voltage	$uV_{DIG} = uV_{IO}$	−0.3		$0.3*V_{IO}$	V
$uV_{DIG-IN-HIGH}$	High level input voltage		$0.7*V_{IO}$		5.5	V

Table 20. TxD PIN PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
uBDLogic_0	Low level input voltage		−0.3		$0.4*V_{IO}$	V
uBDLogic_1	High level input voltage		$0.6*V_{IO}$		5.5	V
R_{PD}_TxD	Pull−down resistance		5	11	20	kΩ
$iTxD_{IL}$	Low level input current	uTXD = 0 V	−1	0	1	uA
C_BDTxD	Input capacitance on TxD pin	uTXD = 100 mV, f = 5 MHz (Note 18)			10	pF

18. Values based on design and characterization, not tested in production

Table 21. TxEN PIN PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}_TxEN	Pull−up resistance		50	110	200	kΩ
$iTxEN_{IH}$	High level input current	$uTXEN = V_{IO}$	−1	0	1	μA
$iTxEN_{LEAK}$	Input leakage current	uTxEN = 5.25V, V_{IO} = 0 V	−1	0	1	μA

Table 22. STBN PIN PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PD}_STBN	Pull−down resistance		50	110	200	kΩ
$iSTBN_{IL}$	Low level input current	uSTBN = 0 V	−1	0	1	μA

Table 23. BGE PIN PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PD}_BGE	Pull−down resistance		150		500	kΩ
$iBGE_{IL}$	Low level input current	uBGE = 0 V	−1	0	1	μA

Table 24. CSN PIN PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}_CSN	Pull−up resistance	Latched mode	50	110	200	kΩ
$iCSN_{IH}$	High level input current	Latched mode, $uCSN = V_{IO}$	−1	0	1	μA
R_{PD}_CSN	Pull−down resistance	Track mode	50	110	200	kΩ
$iCSN_{IL}$	Low level input current	Track mode, uCSN = 0V	−1	0	1	μA
$iCSN_{LEAK}$	Input leakage current	uCSN = 5.25V, V_{IO} = 0V	−1	0	1	μA

Table 25. SCK PIN PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}_SCK	Pull−up resistance		50	110	200	kΩ
$iSCK_{IH}$	High level input current,	$uSCK = V_{IO}$	−1	0	1	μA
$iSCK_{LEAK}$	Input leakage current	uSCK = 5.25V, V_{IO} = 0 V	−1	0	1	μA

DIGITAL OUTPUT SIGNALS

Table 26. DIGITAL OUTPUT SIGNALS VOLTAGE LIMITS (Pins RxD, ERRN and SDO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$uV_{DIG-OUT-LOW}$	Low level output voltage	$iRxD_{OL}$ = 3 mA, $iERRN_{OL}$ = 0.7 mA, $iSDO_{OL}$ = 1 mA (Note 19)	0		0.2*V_{IO}	V
$uV_{DIG-OUT-HIGH}$	High level output voltage	$iRxD_{OH}$ = −3 mA, $iERRN_{OH}$ = −0.7 mA, $iSDO_{OH}$ = −1 mA (Note 19)	0.8*V_{IO}		V_{IO}	V
$uV_{DIG-OUT-UV}$	Output voltage on a digital output when V_{IO} in undervoltage (Note 20)	R_{LOAD} = 100 kΩ to GND, V_{CC} supplied			500	mV
$uV_{DIG-OUT-OFF}$	Output voltage on a digital output when unsupplied	R_{LOAD} = 100 kΩ to GND			500	mV

19. uV_{DIG} = uV_{IO}. No undervoltage on V_{IO} and V_{CC} supplied.
20. RxD and ERRN outputs forced Low, SDO output switched to High Impedance state

Table 27. RxD PIN PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$dBDRxD_{R15}$	RxD signal rise time (20%−80% V_{IO})	RxD pin loaded with 15 pF capacitor (Note 21)			6.5	ns
$dBDRxD_{F15}$	RxD signal fall time (20%−80% V_{IO})				6.5	ns
$dBDRxD_{R15}$ + $dBDRxD_{F15}$	Sum of rise and fall time (20%−80% V_{IO})				13	ns
$\lvert dBDRxD_{R15} - dBDRxD_{F15}\rvert$	Difference of rise and fall time				5	ns
$dBDRxD_{R25}$	RxD signal rise time (20%−80% V_{IO})	RxD pin loaded with 25 pF capacitor			8.5	ns
$dBDRxD_{F25}$	RxD signal fall time (20%−80% V_{IO})				8.5	ns
$dBDRxD_{R25}$ + $dBDRxD_{F25}$	Sum of rise and fall time (20%−80% V_{IO})				16.5	ns
$\lvert dBDRxD_{R25} - dBDRxD_{F25}\rvert$	Difference of rise and fall time				5	ns
$dBDRxD_{R10\_MS}$ + $dBDRxD_{F10\_MS}$	RXD signal sum of rise and fall time at TP4_CC (20%−80% V_{IO})	RxD pin loaded with 10 pF at the end of a 50 Ω, 1 ns microstripline (Note 22)			16.5	ns
$\lvert dBDRxD_{R10\_MS} - dBDRxD_{F10\_MS}\rvert$	RxD signal difference of rise and fall time at TP4_CC (20%−80% V_{IO})				5	ns

21. Values based on design and characterization, not tested in production
22. Simulation result. Simulation performed within T_{J_OP} range, according to *FlexRay Electrical Physical Layer Specification, Version 3.0.1*

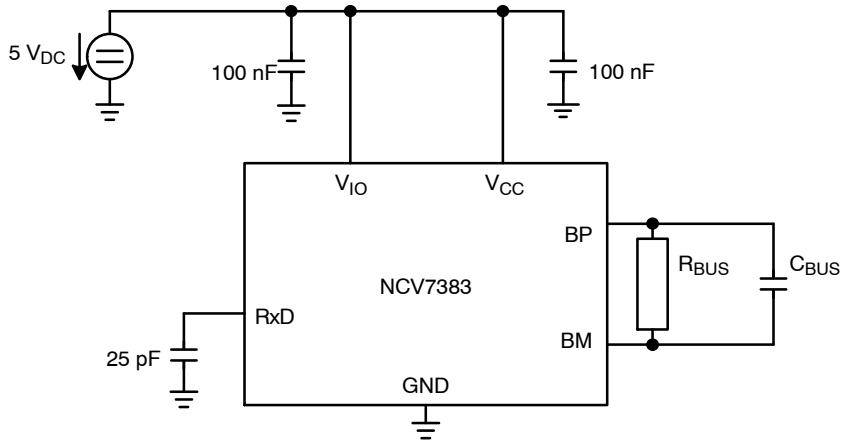


Figure 14. Test Setup for Dynamic Characteristics

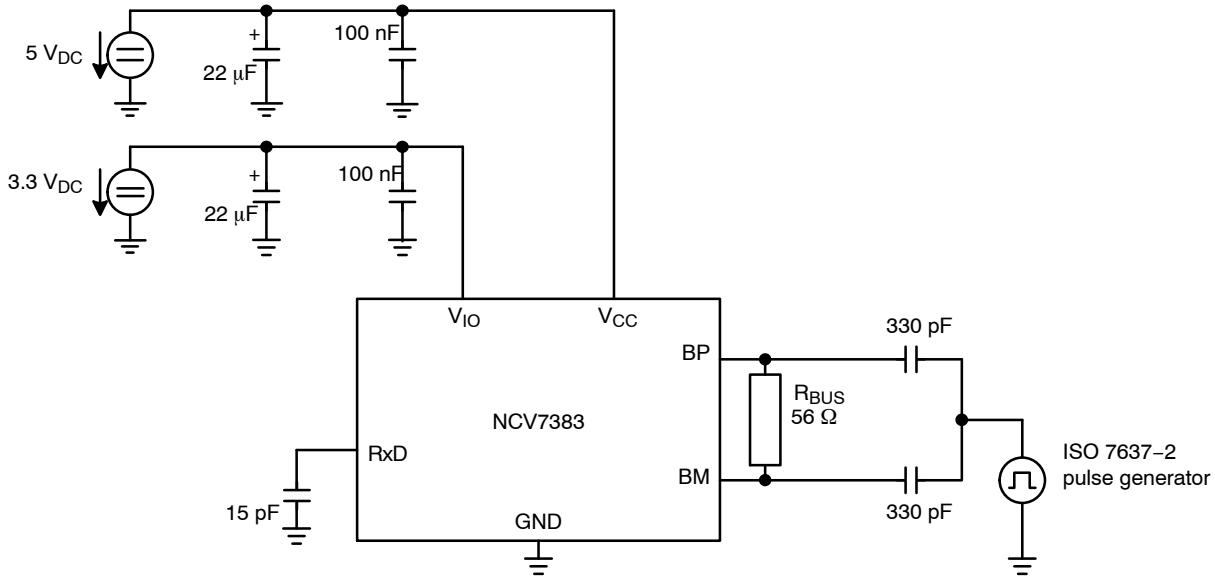


Figure 15. Test Setup for Transients Test Pulses

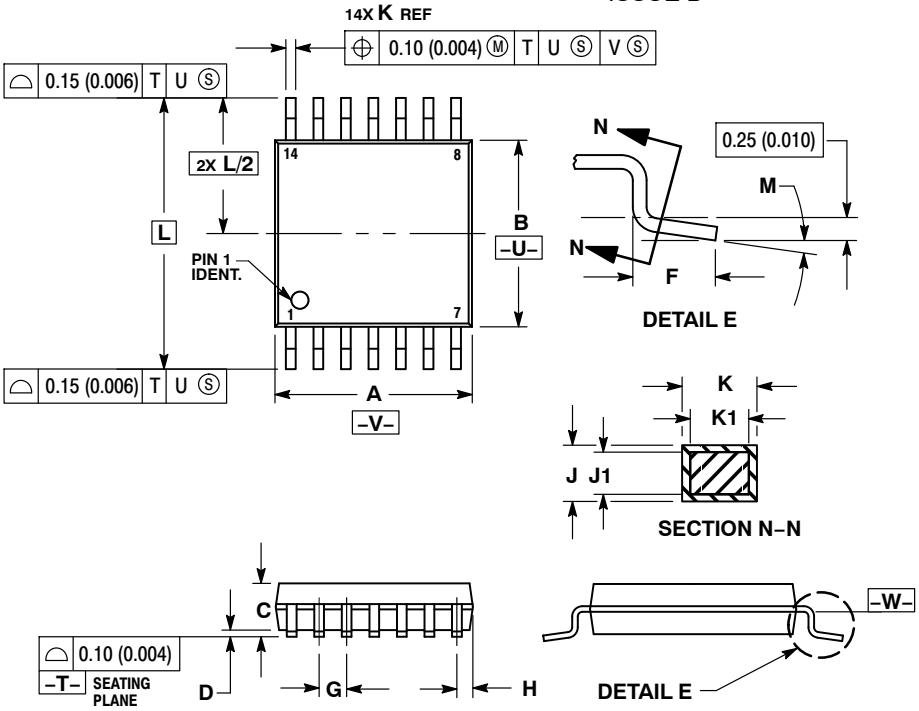
ORDERING INFORMATION

Device	Description	Temperature Range	Package	Shipping†
NCV7383DB0R2G	Clamp 15 FlexRay Transceiver	−40°C to +125°C	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

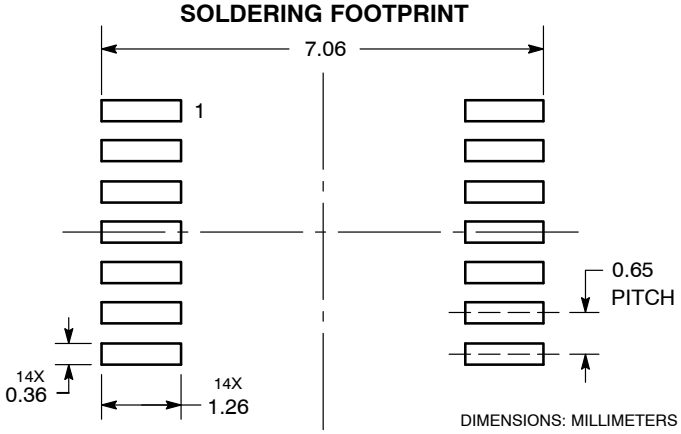
TSSOP−14
CASE 948G
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



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