

### **FEATURES**

- Single input voltage range from 5V to 21V
- Wide input voltage range from 1.0V to 21V with external V<sub>CC</sub> bias voltage
- Integrated MOSFET drivers, Control FET, Synchronous FET with Schottky diode, bootstrap diode and the internal LDO
- Enable input with voltage monitoring capability
- · Logic Level Tri-state PWM input
- Thermally compensated Over Current Indicator
- Open-drain over temperature and over current fault indication
- Under-voltage Lockout of VCC/LDO\_Out
- Operating temp: -40°C < T<sub>i</sub> < 125°C</li>
- Package size: 5mm x 6mm PQFN
- RoHS6 Compliant, lead-free and halogen-free

### DESCRIPTION

The IR3742 integrated PowIRstage<sup>®</sup> is a synchronous buck gate driver IC with co-packed control and synchronous MOSFETs and Schottky diode. It is optimized internally for PCB layout, heat transfer and driver/MOSFET timing. Custom designed gate driver and MOSFET combination enables higher efficiency at lower output voltages required by cutting edge ASIC, FPGA and advanced controller.

Up to 1.5MHz switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency. The IR3742's superior efficiency enables smallest size and lower solution cost.

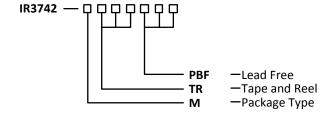
The IR3742 includes an over current indicator and over temperature indicator in the event of a fault condition.

### **APPLICATIONS**

- · Computing Applications
- Set Top Box Applications
- Storage Applications
- Data Center Applications
- Distributed Point of Load Power Architectures

### ORDERING INFORMATION

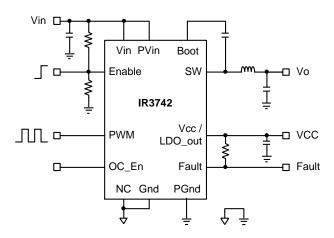
Base Part Number	Bookaga Typa	Standar	d Pack	Orderable Part Number	
base Part Number	Package Type	Form	Quantity	Orderable Part Number	
IR3742	PQFN 5 mm x 6 mm	Tape and Reel	4000	IR3742MTRPBF	



www.irf.com © 2014 International Rectifier Submit Datasheet Feedback March 12, 2014



## **BASIC APPLICATION**





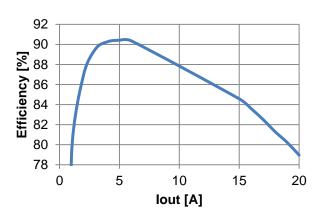


Figure 2: IR3742 Efficiency -PVin=Vin=12V, Vout=1.2V, Fs=300kHz, L=470nH [DCR=0.165mOhm]

## **PINOUT DIAGRAM**

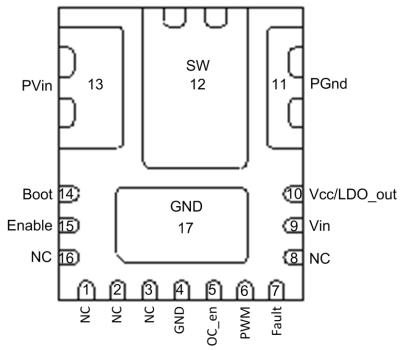


Figure 3: 5mm x 6mm PQFN (Top View)



## **BLOCK DIAGRAM**

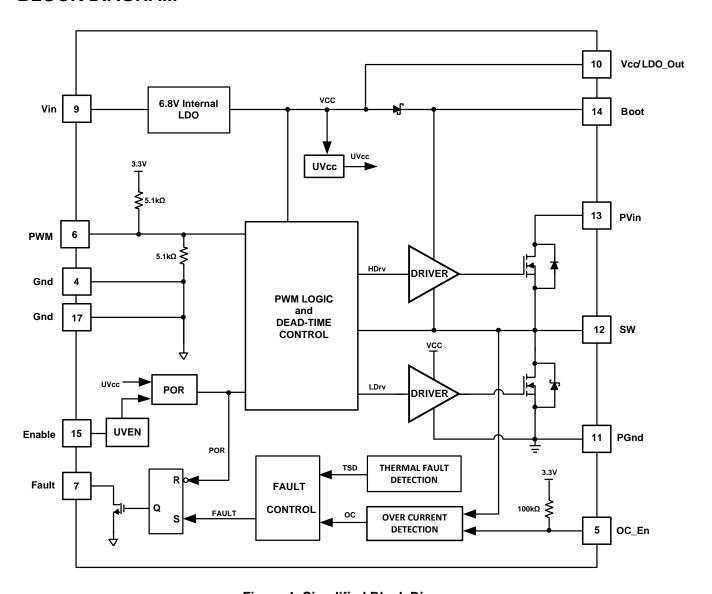


Figure 4: Simplified Block Diagram



## **PIN DESCRIPTIONS**

PIN#	PIN NAME	PIN DESCRIPTION
1, 2, 3, 8, 16	NC	Must be connected to signal ground on the PCB layout.
4, 17	Gnd	Signal ground for internal reference and control circuitry.
5	OC_En	Over current detection enable pin. Floating this pin enables the over current detection. Shorting this pin to GND disables the over current detection.
6	PWM	Logic level tri-state PWM input. "High" turns the control MOSFET on, and "Low" turns the synchronous MOSFET on. "Tri-state" turns both MOSFETs off.
7	Fault	Open-drain fault indication. Connect a pull-up resistor from this pin to Vcc. Fault pin stays high when VCC/LDO_Out or Enable voltage is below their thresholds. In normal operation, Fault pin stays high. When over temperature or over current occurs, Fault pin is latched low. Recycle Vcc or Enable to reset.
9	$V_{in}$	Input for internal LDO. A 1.0µF capacitor should be connected between this pin and PGnd. If an external supply is connected to Vcc/LDO_out pin, this pin should be shorted to Vcc/LDO_out pin.
10	Vcc/LDO_Out	Output of the internal LDO and optional input of an external biased supply voltage. A minimum 2.2µF ceramic capacitor is recommended between this pin and PGnd.
11	PGnd	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
12	sw	Switch node. Connect this pin to the output inductor.
13	$PV_in$	Input voltage for power stage.
14	Boot	Supply voltage for high side driver, a 100nF capacitor should be connected between this pin and SW pin.
15	Enable	Enable pin to turn on and off the device. Input voltage monitoring (input UVLO) can also be implemented by connecting this pin to PVin pin through a resistor divider.



## **ABSOLUTE MAXIMUM RATINGS**

Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin, Vin to PGnd (Note 4)	-0.3V to 25V		
Vcc/LDO_Out to PGnd (Note 4)	-0.3V to 8V (Note 1)		
Boot to PGnd (Note 4)	-0.3V to 33V		
SW to PGnd (Note 4)	-0.3V to 25V (DC), -V <sub>CC</sub> for 20ns (AC)		
Boot to SW	-0.3V to V <sub>CC</sub> + 0.3V (Note 2)		
Fault to Gnd (Note 4)	-0.3V to V <sub>CC</sub> + 0.3V (Note 2)		
PWM, to Gnd	-0.3V to 5V		
Enable, OC_En to Gnd (Note 4)	-0.3V to +3.9V		
PGnd to Gnd	-0.3V to +0.3V		
THERMAL INFORMATION			
Junction to Ambient Thermal Resistance $\Theta_{jA}$	30 °C/W (Note 3)		
Junction to PCB Thermal Resistance $\Theta_{j\text{-PCB}}$	2 °C/W		
Storage Temperature Range	-55°C to 150°C		
Junction Temperature Range	-40°C to 150°C		

Note 1: Vcc must not exceed 7.5V for Junction Temperature between -10°C and -40°C.

Note 2: Must not exceed 8V.

Note 3: Based on a 4-layer PCB board (2.23"x2") using 2 oz. copper on each layer.

Note 4: PGnd pin and Gnd pin are connected together.

www.irf.com © 2014 International Rectifier Submit Datasheet Feedback March 12, 2014



## **ELECTRICAL SPECIFICATIONS**

#### RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	MAX	UNITS
Input Voltage Range with External Vcc Note 5, Note 7	$PV_{in}$	1.0	21	
Input Voltage Range with Internal LDO Note 6, Note 7	$V_{in}$ , $PV_{in}$	5.5	21	V
Supply Voltage Range (Note 6)	V <sub>CC</sub>	4.5	7.5	
Supply Voltage Range (Note 6)	Boot to SW	4.5	7.5	
Output Current Range	I <sub>0</sub>	0	20	А
Switching Frequency	Fs	300	1500	kHz
Operating Junction Temperature	TJ	-40	125	°C

Note 5:  $V_{in}$  is connected to  $V_{cc}$  to bypass the internal LDO.

**Note 6:**  $V_{in}$  is connected to  $PV_{in}$ . For single-rail applications with  $PV_{in} = V_{in} < 7.4V$ , the internal LDO may operate in dropout mode. Please refer to the application information of the Internal LDO and the Over Current Protection.

Note 7: Maximum SW node voltage should not exceed 25V.

### **ELECTRICAL CHARACTERISTICS**

Unless otherwise specified, these specifications apply over,  $7.4V < V_{in} = PV_{in} < 21V$ ,  $0^{\circ}C < T_{J} < 125^{\circ}C$ . Typical values are specified at  $T_{a} = 25^{\circ}C$ .

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Power Stage							
Power Losses	P <sub>LOSS</sub>	$PV_{in} = V_{in} = 12V, \ V_o = 1.2V, \\ I_o = 20A, \ F_s = 600kHz, \ L = \\ 0.3uH, \ Note \ 8$		4.98		W	
Top Switch R <sub>DS(ON)</sub>	R <sub>DS(on)-T</sub>	$V_{BOOT}$ –Vsw = 6.8V, $I_0$ = 20A, $T_j$ = 25°C		8	10.4	mΩ	
Bottom Switch R <sub>DS(ON)</sub>	R <sub>DS(on)-B</sub>	$V_{cc} = 6.8V, I_o = 20A,$ $T_j = 25^{\circ}C$		4	5.2		
Bootstrap Diode Forward Voltage	$V_{\text{FWD}}$	I(Boot) = 15mA	200	370	550	mV	
SW Leakage Current	I <sub>SW</sub>	V <sub>SW</sub> = 0V, Enable = 0V			1	μA	
Dead Band Time	$T_D$	Note 8		10		ns	
PWM Comparator							
PWM Input High Threshold	V <sub>PWM-HIGH</sub>	PWM Tri-State to High	2.5			V	
PWM Input Low Threshold	$V_{PWM\text{-}LOW}$	PWM Tri-State to Low			0.8	V	
PWM Tri-State Float Voltage	$V_{PWM-TRI}$	PWM Floating	1.35	1.65	1.8	V	
Hysteresis	V <sub>PWM-HYS</sub>	Active to Tri-state or Tri-state to Active, Note 8	0.1	0.2	0.3	V	

6 <u>www.irf.com</u> © 2014 International Rectifier <u>Submit Datasheet Feedback</u> March 12, 2014



## **ELECTRICAL CHARACTERISTICS (CONTINUED)**

Unless otherwise specified, these specifications apply over,  $7.4V < V_{in} = PV_{in} < 21V$ ,  $0^{\circ}C < T_{J} < 125^{\circ}C$ . Typical values are specified at  $T_{a} = 25^{\circ}C$ .

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tri-State Propagation Delay	T <sub>PWM-DELAY</sub>	PWM Tri-state to low transition of SW node, Note 8		19.8		ns
TH-State FTopagation Delay	I PWM-DELAY	PWM Tri-state to high transition of SW node, Note 8		36.4		ns
PWM Sink Impedance	R <sub>PWM-SINK</sub>	PWM = 3.3V	3.57	4.8	6.63	kΩ
PWM Source Impedance	R <sub>PWM</sub> -SOURCE	PWM = GND	3.57	4.8	6.63	kΩ
Internal Pull Up Voltage	V <sub>PWM-PULLUP</sub>	Vcc > UVLO		3.3		V
Minimum Pulse Width	T <sub>PWM-MIN</sub>	Note 8		41	58	ns
		Supply Current				
Vin Supply Current (standby)	l <sub>in(Standby)</sub>	EN = Low, No Switching			125	μΑ
		$EN = High, F_s = 600kHz,$ $V_{in} = PV_{in} = 21V$		20	23	mA
		V <sub>CC</sub> /LDO_Out				
Output Voltage	V <sub>cc</sub>	$V_{in(min)}$ = 7.4V, $I_o$ = 0-50mA, Cload = 2.2uF; EN = High	6.5	6.8	7.0	V
LDO Dropout Voltage	V <sub>cc_drop</sub>	V <sub>in</sub> =6.5V,I <sub>o</sub> =50mA, Cload=2.2uF			0.88	V
Short Circuit Current	I <sub>short</sub>	EN = High		70		mA
		Under-Voltage Lockout				
V <sub>cc</sub> -Start Threshold	V <sub>CC</sub> UVLO Start	V <sub>cc</sub> rising trip Level	3.9	4.15	4.4	V
V <sub>cc</sub> -Stop Threshold	V <sub>CC</sub> UVLO Stop	Vcc falling trip Level	3.5	3.86	4.1	V
Enable-Start-Threshold	Enable UVLO Start	ramping up	1.13	1.19	1.27	V
Enable-Stop-Threshold	Enable UVLO Stop	ramping down 0.85 0.93 1.1		1.1	V	
Enable Leakage Current	I <sub>EN_LK</sub>	Enable = 3.3V			1	μΑ

www.irf.com © 2014 International Rectifier Submit Datasheet Feedback March 12, 2014



## **ELECTRICAL CHARACTERISTICS (CONTINUED)**

Unless otherwise specified, these specifications apply over,  $7.4V < V_{in} = PV_{in} < 21V$ ,  $0^{\circ}C < T_{J} < 125^{\circ}C$ . Typical values are specified at  $T_{a} = 25^{\circ}C$ .

Fault							
Over Current Limit	I <sub>LIMIT</sub>	T <sub>j</sub> = 25°C	29	35	41	Α	
Over Temperature Threshold	T <sub>TSD</sub>	Note 8		145		°C	
Fault Voltage Low	$V_{FAULT}$	I <sub>FAULT</sub> = -5mA			0.5	V	
OC_EN Fault Disable Threshold	OC <sub>DISABLE</sub>	Note 8			0.8	V	

**Note 8:** Guaranteed by design, but not tested in production.

8 <u>www.irf.com</u> © 2014 International Rectifier <u>Submit Datasheet Feedback</u> March 12, 2014



Test Conditions: PVin=Vin=12V, VCC=6.8V, Vout = 1.2V, L=470nH, Switching Frequency = 300kHz,  $T_A=25^{\circ}C$  and natural convention cooling unless otherwise noted.

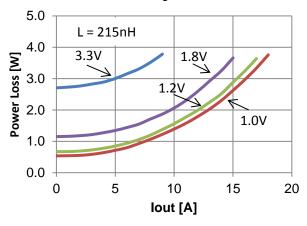


Figure 5: Power Loss vs. Output Current

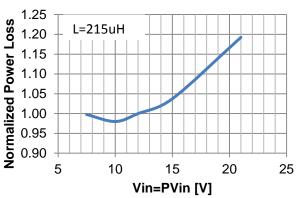


Figure 7: Power Loss vs. Input Voltage

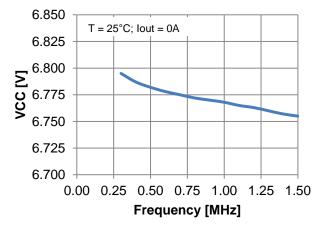


Figure 9: VCC vs. Frequency

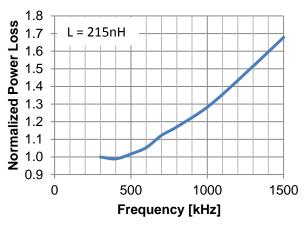


Figure 6: Power Loss vs. Switching Frequency

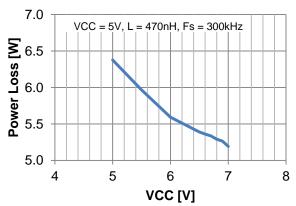


Figure 8: Power Loss vs. Driver Supply Voltage

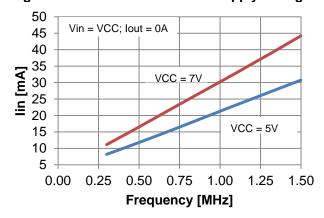
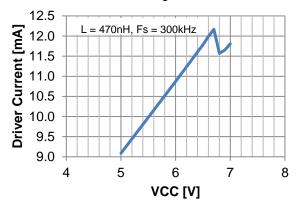


Figure 10: Driver Supply Current vs. Switching Frequency

www.irf.com © 2014 International Rectifier Submit Datasheet Feedback March 12, 2014



Test Conditions: PVin=Vin=12V, VCC=6.8V, Vout = 1.2V, L=470nH, Switching Frequency = 300kHz,  $T_A=25^{\circ}C$  and natural convention cooling unless otherwise noted.



1.05 L = 470nH 1.00 Fs = 1MHz 0.95 0.90 0 5 10 15 20 lout [A]

Figure 11: Driver Supply Current vs. Driver Supply Voltage

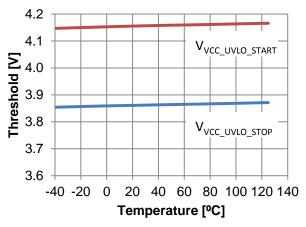


Figure 12: Normalized Driver Supply Current vs.
Output Current

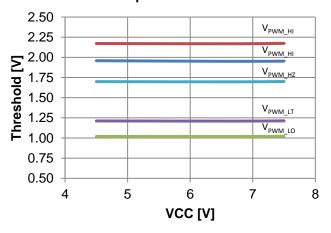


Figure 13: UVLO Threshold vs. Temperature

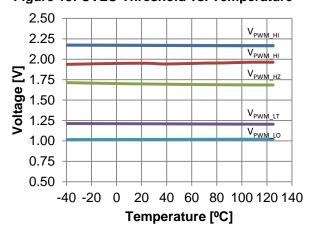


Figure 14: PWM Threshold vs. Driver Supply Voltage

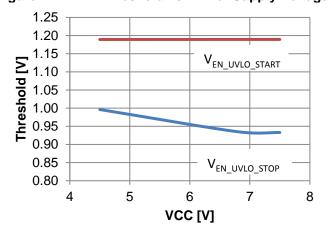


Figure 15: PWM Threshold vs. Temperature

Figure 16: EN Threshold vs. VCC Voltage



Test Conditions: PVin=Vin=12V, VCC=6.8V, Vout = 1.2V, L=470nH, Switching Frequency = 300kHz,  $T_A=25^{\circ}C$  and natural convention cooling unless otherwise noted.

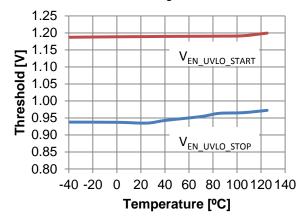


Figure 17: EN Threshold vs. Temperature

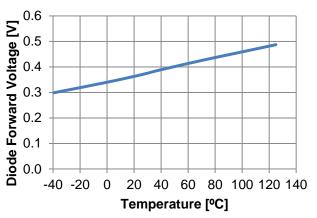
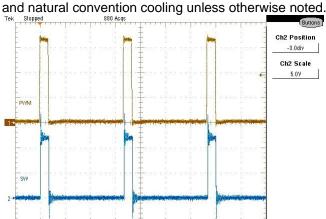


Figure 18: Boot Diode Forward Voltage vs. Temperature



Test Conditions: PVin=Vin=12V, VCC=6.8V, Vout = 1.2V, L=470nH, Switching Frequency = 300kHz,  $T_A=25^{\circ}C$ 



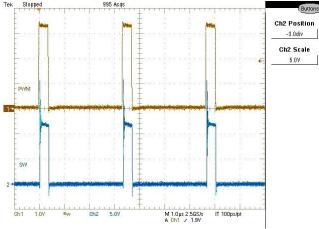
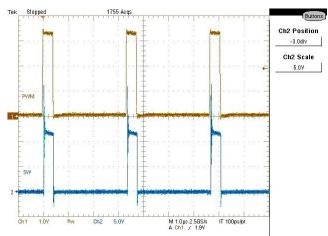


Figure 19: Switching Waveform, lout = 0A

Figure 20: Switching Waveform, lout = 10A



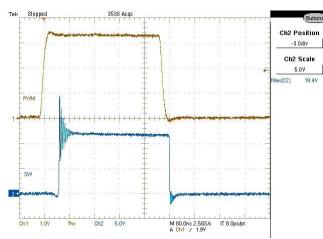
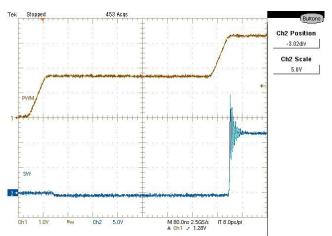


Figure 21: Switching Waveform, lout = 20A

Figure 22: PWM to SW Delay, lout = 10A



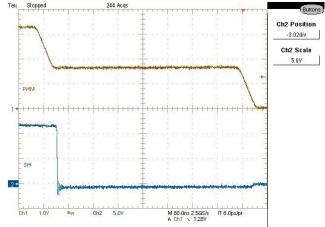


Figure 23: PWM Tri-state Delay, lout = 10A

Figure 24: PWM Tri-state Delay, lout = 10A

www.irf.com © 2014 International Rectifier



### THEORY OF OPERATION

#### **DESCRIPTION**

The IR3742 PowIRStage<sup>®</sup> is a synchronous buck driver with co-packed MOSFETs with integrated Schottky diode, which provices system designers with ease of use and flexibility required in medium current low-profile applications.

The IR3742 is designed to work with a PWM controller. The IR3742 PWM input is compatible with 3.3V logic signal and 7V tolerant. It accepts 3-level PWM input signals with tri-state.

The IR3742 provides a fault indicator that monitors over current events and over temperature events.

#### UNDER-VOLTAGE LOCKOUT AND POR

The Power On Ready (POR) circuit monitors the voltage of  $V_{\rm CC}/L{\rm DO}\_{\rm Output}$  pin and the Enable pin. It assures that the MOSFET driver outputs remain off whenever either of these two signals is below the set thresholds. The POR signal is generated when all these signals reach the valid logic level (see system block diagram). Normal operation resumes once both  $V_{\rm CC}/L{\rm DO}\_{\rm Output}$  and Enable voltages rise above their thresholds.

### **ENABLE/EXTERNAL PVIN MONITOR**

The IR3742 has an Enable function providing another level of flexibility for start-up. The Enable pin has a precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. If the voltage at Enable pin is below its UVLO threshold, both high-side and low-side FETs are off. When Enable pin is below its UVLO, and Fault stays low.

The Enable pin should not be left floating. A pull-down resistor in the range of several kilo-ohms is recommended to between the Enable Pin and ground.

In addition to being a logical input, the Enable pin can help form a precise input voltage UVLO. As shown in Figure 25, the input of the Enable pin is derived from the PV<sub>in</sub> voltage by a resistive divider, R1 and R2. By selecting different divider ratios, users can program the UVLO threshold voltage for

the bus voltage UVLO. It prevents the IR3742 from regulating at PV<sub>in</sub> lower than the desired voltage level. Figure 26 shows the start-up waveform with the input UVLO voltage set at 10V.

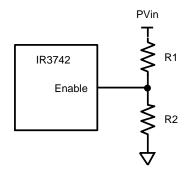


Figure 25: Implementation of Input Under-Voltage Lockout (UVLO) using Enable Pin

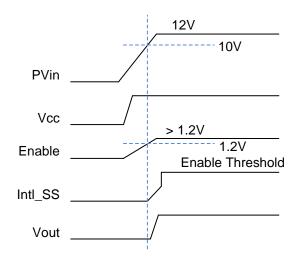


Figure 26: Illustration of start-up with PVin UVLO threshold voltage of 10V. The internal soft-start is used in this case.

#### **INTERNAL LDO**

The IR3742 has an internal Low Dropout Regulator (LDO), offering 6.8V. 6.8  $V_{\rm CC}$  voltage results in higher full load efficiency due to less conduction loss.

The internal LDO is beneficial for single rail (supply) applications, where no external bias supplies will be



needed. For these applications,  $V_{in}$  pin should be connected to  $PV_{in}$  and  $V_{CC}/LDO\_Out$  pin is left floating as shown in Figure 27.  $1.0\mu F$  and  $2.2\mu F$  ceramic bypass capacitors should be placed close to  $V_{in}$  pin and  $V_{CC}/LDO\_Out$  pin respectively.

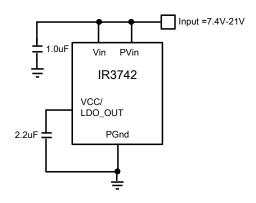


Figure 27: Internally Biased Single-Rail Configuration

V<sub>CC</sub>/LDO\_Out pin can be directly connected to the PV<sub>in</sub> pin to bypass the internal LDO and therefore to avoid the voltage drop on the internal LDO. This configuration is illustrated in Figure 28.

Figure 29 shows the configuration using an external  $V_{\text{CC}}$  voltage. With this configuration, the input voltage range can be extended down to 1.0V.

It should be noted as the  $V_{\rm CC}$  voltage decreases, the efficiency and the over current limit will decrease due to the increase of  $R_{\rm DS(ON)}$ . Please refer to the section of the over current protection for more information.

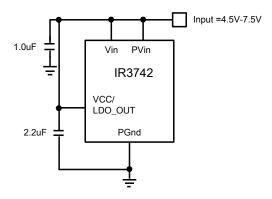


Figure 28: Single-Rail Configuration for 4.5V-7V inputs

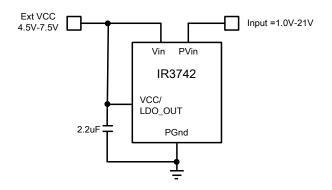


Figure 29: Use External Bias Voltage

#### **PWM TRI-STATE INPUT**

The IR3742 PWM accepts 3-level input signals. When PWM input is high, the synchronous MOSFET is turned off and the control MOSFET is turned on. When the PWM input is low, control MOSFET is turned off and synchronous MOSFET is turned on. Figure 19 - Figure 24 show the PWM input and the corresponding SW output of the IR3742. If PWM pin is floated, the built-in resistors pull the PWM pin into a tri-state region centered about 1.65V.

#### OVER CURRENT INDICATOR AND OC EN

The over current indication monitors the current through the Synchronous MOSFET using  $R_{DS(on)}$  sensing. This method enhances the converter's efficiency and reduces cost by eliminating a current sense resistor and any layout related noise issues. The current limit is pre-set internally and is compensated according to the IC temperature. So at different ambient temperature, the over-current threshold remains almost constant.

Over current is measured at the valley of the inductor current. Over current events are flagged after PWM goes high and the internal LDrv signal goes low. The drivers follow the PWM signal even when an over current event is detected and/or the Fault indicator is set.

OC\_en signal enables the over current fault indicator functionality. IR3742 pulls Fault low when an over current event is detected, if OC\_en is set high. If a fault is set, toggling OC\_en does not reset the Fault signal.

4 <u>www.irf.com</u> © 2014 International Rectifier <u>Submit Datasheet Feedback</u> March 12, 2014



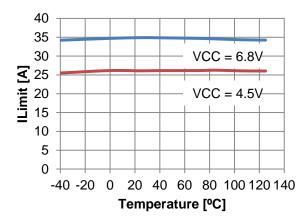


Figure 30: OC Indicator Threshold over temperature

#### THERMAL FAULT INDICATOR

Temperature sensing is provided inside IR3742. The trip threshold is typically set to 145°C. When trip threshold is exceeded, the open drain fault pin pulls low. The driver will continue switching if a PWM signal is applied and the part is enabled. The fault pin remains low until Enable is pulled low or VCC UVLO STOP is triggered.

#### **FAULT OUTPUT**

The Fault signal is an open drain signal that requires an external pull up resistor. High state indicates no over current event occurred and no over temperature events were detected. The Fault signal is an indicator that does not prevent the driver from following the PWM signal when set.

Clearing or resetting the Fault signal requires the toggling of the Enable signal or toggling the VCC UVLO. Fault remains low after setting until it is reset with Enable or VCC.

## MINIMUM SWITCH PULSE AND PWM PULSE **CONSIDERATIONS**

PWM pulses control the switching of the converter in normal operation. However, the IR3742 blanks PWM pulses that are too short. To avoid blanking PWM pulses, ensure the minimum PWM pulse is greater than 70nS.

The switch node also has a minimum pulse width. The minimum pulse is the shortest amount of time which Ctrl FET may be reliably turned on.

Any design or application using IR3742 must ensure operation with a pulse width that is longer than this minimum on-time and preferably higher than 70ns. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{V_{in} \times F_s}$$

In any application that uses IR3742, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on}$$

$$t_{on(\min)} \leq \frac{V_{out}}{V_{in} \times F_s}$$
 , therefore,  $V_{in} \times F_s \leq \frac{V_{out}}{t_{on(\min)}}$ 

The minimum output voltage is limited by the reference voltage and hence  $V_{out(min)} = 0.6 \text{ V}.$ Therefore,

$$V_{in} \times F_s \le \frac{V_{out(min)}}{t_{on(min)}} = \frac{0.6V}{70ns} = 8.57V / \mu s$$

Therefore, at the maximum recommended input voltage 21V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 408 kHz. Conversely, at the maximum switching frequency (1.5 MHz) and minimum output voltage (0.6V), the input voltage (PV<sub>in</sub>) should not exceed 5.7V, otherwise pulse skipping will happen.

#### **MAXIMUM DUTY RATIO**

The maximum duty ratio for the IR3742 is determined by the Toff time. Each cycle requires the gate to be turned off for a minimum of 250nS. This provides an upper limit on the operating duty ratio. IR3742 is designed to operate from 300 kHz to 1.5 MHz. implying maximum duty cycles of 92.5% and 62.5% respectively.



## **DESIGN EXAMPLE**

The following example is a typical application for IR3742. The application circuit is shown in Figure 1.

$$PV_{in} = V_{in} = 12V (\pm 10\%)$$

$$V_0 = 1.2V$$

$$I_0 = 20A$$

Peak-to-Peak Ripple Voltage = ±1% of V<sub>o</sub>

$$\Delta V_o = \pm 4\%$$
 of  $V_o$  (for 30% Load Transient)

$$F_s = 300 \text{ kHz}$$

### **EXTERNAL PVIN MONITOR (INPUT UVLO)**

As explained in the section of Enable/External  $PV_{in}$  monitor, the input voltage,  $PV_{in}$ , can be monitored by connecting the Enable pin to  $PV_{in}$  through a set of resistor divider. When  $PV_{in}$  exceeds the desired voltage level such that the voltage at the Enable pin exceeds the Enable threshold, 1.2V, the IR3742 is turned on. The implementation of this function is shown in Figure 25.

For a typical Enable threshold of  $V_{EN} = 1.2 \text{ V}$ 

$$PV_{in(min)} \times \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2$$

$$R_2 = R_1 \times \frac{V_{EN}}{PV_{in(min)} - V_{EN}}$$

For the minimum input voltage PV<sub>in (min)</sub> = 9.2V, select R<sub>1</sub>=49.9k $\Omega$ , and R<sub>2</sub>=7.5k $\Omega$ .

#### **BOOTSTRAP CAPACITOR SELECTION**

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor, C1, as shown in Figure 31. The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled low. V<sub>CC</sub> starts to charge C1 through the internal bootstrap

diode. The voltage,  $V_c$ , across the bootstrap capacitor C1 can be calculated as

$$V_C = V_{CC} - V_D$$

where  $V_{\text{D}}$  is the forward voltage drop of the bootstrap diode.

When the control FET turns on in the next cycle, the SW node voltage rises to the bus voltage,  $PV_{in}$ . The voltage at the Boot pin becomes:

$$V_{BOOT} = PV_{in} + V_{CC} - V_{D}$$

A good quality ceramic capacitor of  $0.1\mu F$  with voltage rating of at least 25V is recommended for most applications.

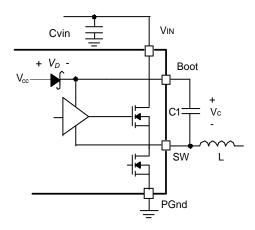


Figure 31: Bootstrap circuit to generate the supply voltage for the high-side driver voltage

#### INPUT CAPACITOR SELECTION

Good quality input capacitors are necessary to minimize the input ripple voltage and to supply the switch current during the on-time. The input capacitors should be selected based on the RMS value of the input ripple current and requirement of the input ripple voltage.

The RMS value of the input ripple current can be calculated as follows:



$$I_{RMS} = I_o \times \sqrt{D \times (1-D)}$$

Where D is the duty cycle and Io is the output current. For I<sub>o</sub>=20A and D=0.1, I<sub>RMS</sub>= 6A

The input voltage ripple is the result of the charging of the input capacitors and the voltage induced by ESR and ESL of the input capacitors.

Ceramic capacitors are recommended due to their high ripple current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency.

For this application, it is suggested to use three 22μF/25V ceramic capacitors, C3216X5R1E226M, from TDK. In addition, although not mandatory, a 1x330uF, 25V SMD capacitor EEE-FK1E331P from Panasonic may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

## HIGH OUTPUT VOLTAGE DESIGN CONSIDERATION

When using IR3742 for higher voltage levels, the design should consider maximum duty cycle, power loss and current sensing. Power loss and thermals need to be accounted for when running high loads.

The maximum output voltage is limited by the required off time. When selecting the switching frequency and output voltage, each cycle should never have less than 250nS off time. IR3742 can reach higher output voltages at lower switching frequencies since the required off time is a smaller percentage at slower frequencies.

IR3742 can provide high output voltages, but may require an external cooling. When running high output voltage or higher current rails, care should be taken to ensure the part is adequate cooled.

Inductor current sensing range needs to be addressed. Depending on the controller and current sense methodology, the input range of the current sense circuit maybe a limiting factor on the maximum output voltage.

#### INDUCTOR SELECTION

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor ( $\Delta i$ ). The optimum point is usually found between 20% and 40% ripple of the output current.

The saturation current of the inductor is desired to be higher than the over current limit plus the inductor ripple current. An inductor with soft-saturation characteristic is recommended.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$PV_{in\, ext{max}} - V_o = L \times \frac{\Delta i_{L\, ext{max}}}{\Delta t}; \ \Delta t = \frac{D}{F_o}$$

$$L = (PV_{in \max} - V_o) \times \frac{V_o}{V_{in} \times \Delta i_{L\max} \times F_s}$$

Where:

PV<sub>inmax</sub> = Maximum input voltage

= Output Voltage

= Maximum Inductor Peak-to-Peak  $\Delta i_{Lmax}$ 

Ripple Current

 $F_s$ = Switching Frequency

Δt = On time D = Duty Cycle

Select  $\Delta i_{Lmax} \approx 35\% \times I_o$ , then the output inductor is calculated to be 0.51 µH. Select L=0.47 µH, 744309047, from Wurth Electronics which provides an inductor suitable for this application.

### **OUTPUT CAPACITOR SELECTION**

Output capacitors are usually selected to meet two specific requirements: (1) Output ripple voltage and (2) load transient response. The load transient response is also greatly affected by the control bandwidth. So it is common practice to select the output capacitors to meet the requirements of the



output ripple voltage first, and then design the control bandwidth to meet the transient load response. For some cases, even with the highest allowable control bandwidth, the resulting load transient response still cannot meet the requirement. The number of output capacitors then need to be increased.

The voltage ripple is attributed by the ripple current charging the output capacitors, and the voltage drop due to the Equivalent Series Resistance (ESR) and the Equivalent Series Inductance (ESL). Following lists the respective peak-to-peak ripple voltages:

$$\Delta V_{o(C)} = \frac{\Delta i_{L \max}}{8 \times C_o \times F_s}$$

$$\Delta V_{o(ESR)} = \Delta i_{L \max} \times ESR$$

$$\Delta V_{o(ESL)} = (\frac{PV_{in} - V_o}{L}) \times ESL$$

Where  $\Delta i_{Lmax}$  is maximum inductor peak-to-peak ripple current.

Good quality ceramic capacitors are recommended due to their low ESR, ESL and the small package size. It should be noted that the capacitance of ceramic capacitors are usually de-rated with the DC and AC biased voltage. It is important to use the derated capacitance value for the calculation of output ripple voltage as well as the voltage loop compensation design. The de-rated capacitance value may be obtained from the manufacturer's datasheets.

In this case, three 22uF ceramic capacitors, C2012X5R0J226M, from TDK are used to achieve ±12mV peak-to-peak ripple voltage requirement. The de-rated capacitance value with 1.2VDC bias and 10mVAC voltage is around 18uF each.



### LAYOUT RECOMMENDATIONS

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with worse than expected results.

Make the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The inductor, output capacitors and the IR3742 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the  $PV_{in}$  pin of IR3742.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for  $V_{in}$  and  $V_{CC}$  should be close to their respective pins. In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane in top layer.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using via holes. Figure 32 - Figure 35 illustrates the implementation of the layout guidelines outlined above, on the IRDC3742 4-layer demo board.

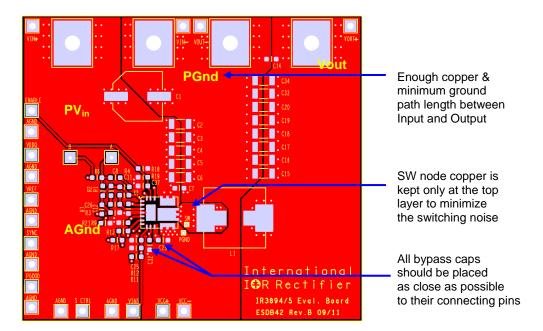


Figure 32: IRDC3742 Demo Board - Top Layer

19 <u>www.irf.com</u> © 2014 International Rectifier <u>Submit Datasheet Feedback</u> March 12, 2014



Single point connection between AGND & PGND, should be close to the

noise sources

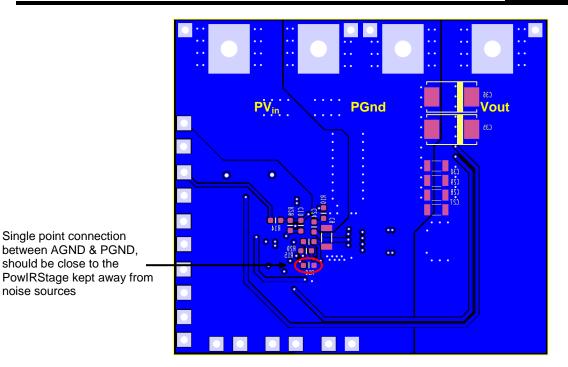


Figure 33: IRDC3742 Demo Board - Bottom Layer

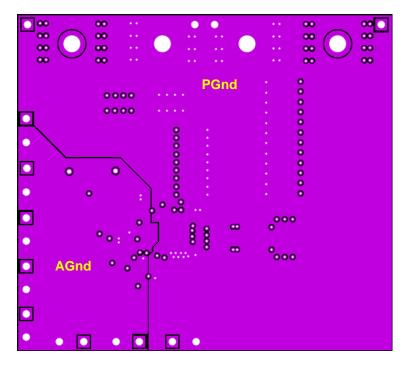


Figure 34: IRDC3742 Demo Board - Middle Layer 1

20 www.irf.com



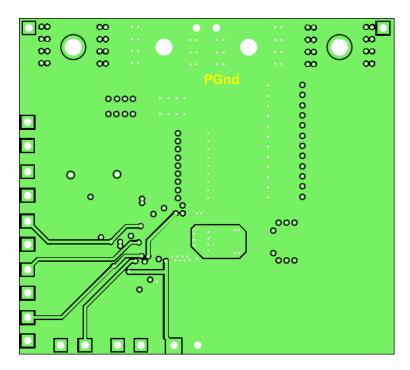


Figure 35: IRDC3742 Demo Board - Middle Layer 2

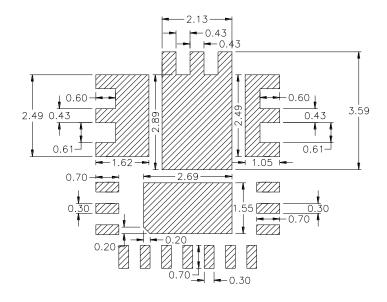


### PCB METAL AND COMPONENT PLACEMENT

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout as shown in following figures. PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and

experiments should be run to confirm the limits of self-centering on specific processes.

For further information, please refer to "SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note." (AN1132)



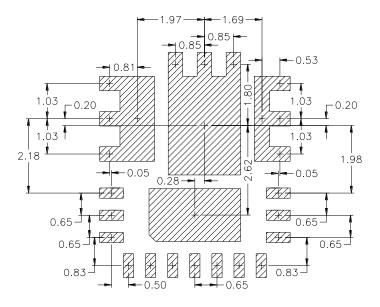


Figure 36: PCB Metal Pad Spacing (all dimensions in mm)

22

<sup>\*</sup> Contact International Rectifier to receive an electronic PCB Library file in your preferred format



### SOLDER RESIST

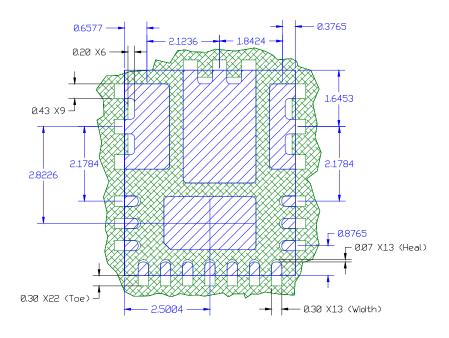
IR recommends that the larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying Copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability.

When using SMD pads, the underlying copper traces should be at least 0.05mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1mm in X & Y.)

However, for the smaller Signal type leads around the edge of the device, IR recommends that these are Non Solder Mask Defined (NSMD) or Copper Defined.

When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025mm on each edge, (i.e. 0.05mm in X&Y,) in order to accommodate any layer to layer misalignment.

Ensure that the solder resist in-between the smaller signal lead areas are at least 0.15mm wide, due to the high x/y aspect ratio of the solder mask strip.



All Dimensions In mm All Pads are Solder Mask Defined Pad Center to Center dimensions

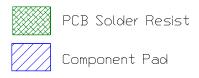


Figure 37: Solder Resist

23 <u>www.irf.com</u> © 2014 International Rectifier <u>Submit Datasheet Feedback</u> March 12, 2014



### STENCIL DESIGN

Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.

Evaluations have shown that the best overall performance is achieved using the stencil design shown in following figure. This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

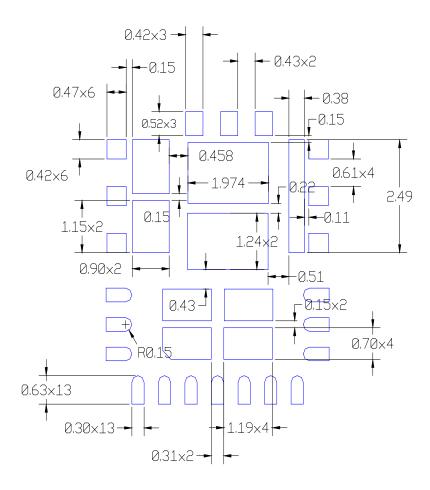
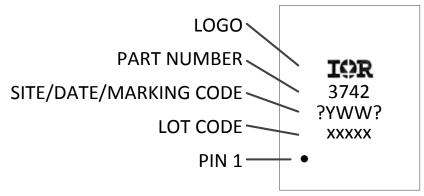


Figure 38: Stencil Pad Spacing (all dimensions in mm)

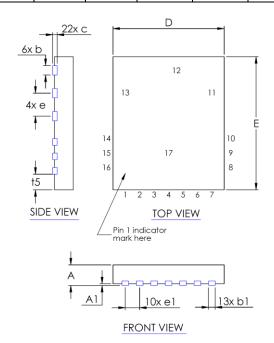


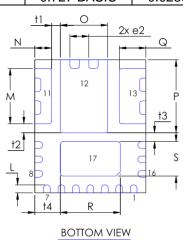
## **MARKING INFORMATION**



## **PACKAGE INFORMATION**

DIM	MILIM	ITERS	INC	HES	DIM	MILIM	ITERS	INC	HES
DIIVI	MIN	MAX	MIN	MAX	ואווט	MIN	MAX	MIN	MAX
Α	0.800	1.000	0.0315	0.0394	L	0.350	0.450	0.0138	0.0177
A1	0.000	0.050	0.0000	0.0020	М	2.441	2.541	0.0961	0.1000
b	0.375	0.475	0.1477	0.1871	N	0.703	0.803	0.0277	0.0316
b1	0.250	0.350	0.0098	0.1379	0	2.079	2.179	0.0819	0.0858
С	0.203	REF.	0.008	REF.	Р	3.242	3.342	0.1276	0.1316
D	5.000	BASIC	1.969	BASIC	Q	1.265	1.365	0.0498	0.0537
Е	6.000	BASIC	2.362	BASIC	R	2.644	2.744	0.1041	0.1080
е	1.033	BASIC	0.0407	BASIC	S	1.500	1.600	0.0591	0.0630
e1	0.650	BASIC	0.0256	BASIC	t1, t2, t3	0.401	BASIC	0.016	BACIS
e2	0.852	BASIC	0.0335	BASIC	t4	1.153	BASIC	0.045	BASIC
					t5	0.727	BASIC	0.0286	BASIC







## **ENVIRONMENTAL QUALIFICATIONS**

Qualification Level		Industrial			
Moisture Sensitivity Level		5mm x 6mm PQFN JEDEC Level 2 @ 260°C			
	Machine Model	Class B			
	(JESD22-A115A)	≥200V to <400V			
ESD	Human Body Model	Class 2			
E9D	(JESD22-A114F)	≥2000V to <4000V			
	Charged Device Model	Class II			
(JESD22-C101D)		≥200V to <500V			
RoHS6 Compliant		Yes			

<sup>†</sup> Qualification standards can be found at International Rectifier web site: http://www.irf.com

Data and specifications subject to change without notice. Qualification Standards can be found on IR's Web site.



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105 TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information. www.irf.com

www.irf.com © 2014 International Rectifier Submit Datasheet Feedback March 12, 2014

## **ПОСТАВКА** ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

# Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

### http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru\_6 moschip.ru\_4 moschip.ru\_9