

50 A, VRPower® Integrated Power Stage

DESCRIPTION

The SiC783A is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency and high power density performance. Packaged in Vishay's proprietary MLP 6 mm x 6 mm package, SiC783A enables voltage regulator designs to deliver currents up to 50 A per phase.

The internal power MOSFETs utilize Vishay's state-of-the-art trench MOSFET technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC783A incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and a thermal warning (THWn) that alerts the system of excessive junction temperature. This driver is compatible with wide range of PWM controllers and supports tri-state PWM logic (3.3 V) as well as zero current detect to improve light load efficiency.

FEATURES

- Thermally enhanced PowerPAK® MLP66-40L package
- Industry benchmark MOSFET with integrated Schottky diode
- Delivers up to 50 A continuous current
- High frequency operation up to 1 MHz
- Optimized for 12 V input rail applications
- 3.3 V PWM logic with tri-state threshold
- Zero current detect control for light load efficiency improvement.
- Short PWM propagation delay (< 20 ns)
- Thermal monitor flag
- Faster disable
- V_{CIN} under voltage lock out (UVLO)

APPLICATIONS

- Synchronous buck converters
- Multi-phase VRDs for CPU, GPU and memory
- DC/DC POL modules

TYPICAL APPLICATION DIAGRAM

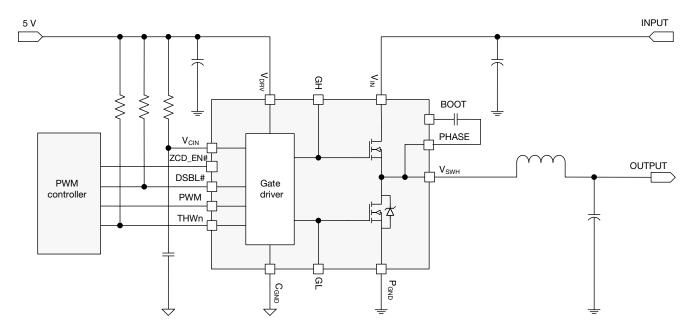


Fig. 1 - SiC783A Typical Application Diagram

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PINOUT CONFIGURATION

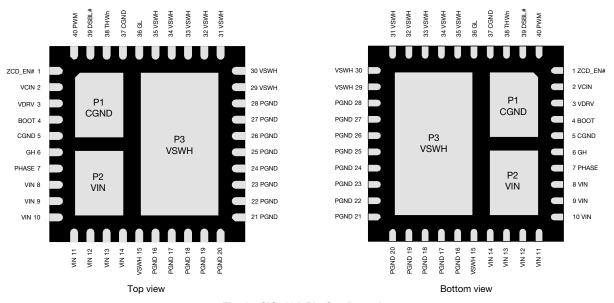


Fig. 2 - SiC783A Pin Configuration

PIN DESCRIPTIO	PIN DESCRIPTION						
PIN NUMBER	NAME	FUNCTION					
1	ZCD_EN#	ZCD control. Active low					
2	V _{CIN}	Supply voltage for internal logic circuitry					
3	V _{DRV}	Supply voltage for internal gate driver					
4	BOOT	High-side driver bootstrap voltage					
5, 37, P1	C _{GND}	Analog ground for the driver IC					
6	GH	High-side gate signal					
7	PHASE	Return path of high-side gate driver					
8 to 14, P2	V _{IN}	Power stage input voltage. Drain of high-side MOSFET					
15, 29 to 35, P3	V _{SWH}	Switch node of the power stage					
16 to 28	P _{GND}	Power ground					
36	GL	Low-side gate signal					
38	THWn	Thermal warning open drain output					
39	DSBL#	Disable pin. Active low					
40	PWM	PWM control input					

ORDERING INFORMATION						
PART NUMBER	PACKAGE	MARKING CODE				
SiC783ACD-T1-GE3	PowerPAK MLP66-40L	SiC783A				
SiC783ADB	Reference Board					



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ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	SYMBOL	LIMITS	UNIT
Input Voltage	V _{IN}	-0.3 to +20	
Control Logic Supply Voltage	V _{CIN}	-0.3 to +7	
Drive Supply Voltage	V_{DRV}	-0.3 to +7	
Switch Node (DC voltage)	V	-0.3 to +20	
Switch Node (AC voltage) (1)	V _{swн}	-7 to +27	
BOOT Voltage (DC voltage)	V	27	V
BOOT Voltage (AC voltage) (2)	V _{BOOT}	34	
BOOT to PHASE (DC voltage)	V	-0.3 to +7	
BOOT to PHASE (AC voltage) (3)	VBOOT_PHASE	-0.3 to +8	
All Logic Inputs and Outputs (PWM, DSBL#, ZCD_EN# and THWn)		-0.3 to V _{CIN} +0.3	
Max. Operating Junction Temperature	TJ	150	
Ambient Temperature	T _A	-40 to +125	°C
Storage Temperature		-65 to +150	
Electrostatic Discharge Protection	Human body model, JESD22-A114	4000	V
Electrostatic Discharge Protection	Charged device model, JESD22-C101	1000	7 v

Notes

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings
 only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the
 specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- $^{(1)}$ The specification values indicate "AC voltage" is V_{SWH} to P_{GND} , -7 V (< 50 ns, 10 μ J), minimum and 27 V (< 50 ns), maximum.
- $^{(2)}$ The specification value indicates "AC voltage" is V_{BOOT} to P_{GND} , 34 V (< 50 ns) maximum.
- (3) The specification value indicates "AC voltage" is V_{BOOT} to V_{PHASE}, 8 V (< 20 ns) maximum.

RECOMMENDED OPERATING RANGE						
ELECTRICAL	MIN.	TYP.	MAX.	UNIT		
Input Voltage (V _{IN})	4.5	-	16			
Drive Supply Voltage (V _{DRV})	4.5	5	5.5			
Control Logic Supply Voltage (V _{CIN})	4.5	5	5.5	V		
Switch Node (V _{SWH} , DC voltage)	-	-	20			
BOOT to PHASE (V _{BOOT_PHASE} , DC voltage)	4	4.5	5.5			
Thermal Resistance						
Thermal Resistance from Junction to Case	-	2.5	-	°C/W		
Thermal Resistance from Junction to PAD	-	1	-	C/VV		



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PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED (DSBL# = ZCD_EN# = 5 V, V _{IN} = 12 V, V _{DRV} = V _{CIN} = 5 V, T _A = 25 °C)	MIN.	TYP. (1)	MAX.	UNIT	
POWER SUPPLIES		VDRV = VCIN = 3 V, 1A = 23 O)					
1 0 11 2 11 2 11 2 11 2 11 2 11 2 11 2		V _{DSBL#} = 0 V, no switching	_	13	_		
Control Logic Supply Current	I _{VCIN}	V _{DSBL#} = 5 V, no switching, V _{PWM} = FLOAT	-	300	-	μΑ	
		$V_{DSBL\#} = 5 \text{ V}, f_s = 300 \text{ kHz}, D = 0.1$	-	325	-	1	
		f _s = 300 kHz, D = 0.1	-	16	25		
		f _s = 1 MHz, D = 0.1	-	55	=	mA	
Drive Supply Current	I _{VDRV}	V _{DSBL#} = 0 V, no switching	-	20	=		
		V _{DSBL#} = 5 V, no switching	=	55	-	μA	
BOOTSTRAP SUPPLY	L						
Bootstrap Switch Forward Voltage	V _F	I _F = 2 mA	-	-	0.4	V	
PWM CONTROL INPUT							
Rising Threshold	V _{TH_PWM_R}		2.1	2.4	2.8		
Falling Threshold	V _{TH_PWM_F}		0.7	0.9	1.2		
Tri-state Rising Threshold	V _{TH_TRI_R}		0.9	1.2	1.5	V	
Tri-state Falling Threshold	V _{TH_TRI_F}		1.9	2.2	2.6		
Tri-state Voltage	V_{TRI}	V _{PWM} = FLOAT	-	1.8	-		
Tri-state Rising Threshold Hysteresis	V _{HYS_TRI_R}		-	250	-	>/	
Tri-state Falling Threshold Hysteresis	V _{HYS_TRI_F}		-	350	-	mV	
DWW O		V _{PWM} = 0 V	-	-	-225		
PWM Current	I _{PWM}	V _{PWM} = 3.3 V	-	-	225	μA	
DRIVER TIMING							
Tri-state to GH/GL Rising Propagation Delay	t _{PD_TRI_R}		-	30	-		
Tri-state Hold-Off Time	t _{TSHO}		-	130	=		
GH - Turn Off Propagation Delay	t _{PD_OFF_GH}		-	20	-		
GH - Turn On Propagation Delay (Dead time rising)	t _{PD_ON_GH}		-	8	-	ns	
GL - Turn Off Propagation Delay	t _{PD_OFF_GL}		-	12	-		
GL - Turn On Propagation Delay (Dead time falling)	t _{PD_ON_GL}		-	8	-		
DSBL# Low to GH/GL Falling Propagation Delay	t _{PD_DSBL_F}	Fig. 5	-	15	-		
DSBL#, ZCD_EN# INPUT							
DCDI # Logic Input Voltage	V _{IH_DSBL} #	Input logic high	2	-	-		
DSBL# Logic Input Voltage	V _{IL_DSBL#}	Input logic low	-	-	0.8	v	
ZCD EN# Logic Input Voltage	V _{IH_ZCD_EN#}	Input logic high	2	-	-	V	
ZCD_EN# Logic Input Voltage	V _{IL_ZCD_EN#}	Input logic low	-	-	0.8		



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ELECTRICAL SPECIFICATIONS							
PARAMETER	SYMBOL	$ \begin{array}{c} \textbf{TEST CONDITIONS} \\ \textbf{UNLESS OTHERWISE SPECIFIED} \\ (\text{DSBL\#} = \text{ZCD_EN\#} = 5 \text{ V}, \text{V}_{\text{IN}} = 12 \text{ V}, \\ \text{V}_{\text{DRV}} = \text{V}_{\text{CIN}} = 5 \text{ V}, \text{T}_{\text{A}} = 25 \text{ °C}) \end{array} $	MIN.	TYP. ⁽¹⁾	MAX.	UNIT	
PROTECTION							
Under Voltage Lockout	V _{UVLO}	V _{CIN} rising, on threshold	-	3.7	4.3	V	
Onder Voltage Lockout	VUVLO	V _{CIN} falling, off threshold	2.7	3.2	-	\ \ \	
Under Voltage Lockout Hysteresis	V _{UVLO_HYST}		1	500	ı	mV	
THWn Flag Set (2)	T _{THWn_SET}		-	160	-		
THWn Flag Clear (2)	T _{THWn_CLEAR}		-	135	-	°C	
THWn Flag Hysteresis (2)	T _{THWn_HYST}		-	25	-		
THWn Output Low	V _{OL_THWn}	I _{THWn} = 2 mA	-	0.02	-	V	

Notes

⁽²⁾ Guaranteed by design.

DEVICE TRUTH TABLE								
DSBL#	ZCD_EN#	PWM	GH	GL				
Open	X	X	L	L				
L	X	Х	L	L				
Н	L	L	L	H, I _L > 0 A L, I _L < 0 A				
Н	L	Н	Н	L				
Н	L	Tri-state	L	L				
Н	Н	L	L	Н				
Н	Н	Н	Н	L				
Н	Н	Tri-state	L	L				

⁽¹⁾ Typical limits are established by characterization and are not production tested.



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DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. PWM input operates as follows for two state logic. When PWM is driven above V_{TH PWM R} the low-side is turned off and the high-side is turned on. When PWM input is driven below V_{TH PWM F} the high-side turns off and the low-side turns on. For tri-state logic, the PWM input operates as above for driving the MOSFETs. However, if the PWM input stays tri-state for the tri-state hold-off period, t_{TSHO}, both high-side and low-side MOSFETs are turned off. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering.

The SiC783A incorporates PWM voltage thresholds that are compatible with 3.3 V logic.

Disable (DSBL#)

In the low-state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFETs. In this state, the standby current is minimized. If DSBL# is left unconnected an internal pull-down resistor will pull the pin down to $C_{\mbox{\footnotesize GND}}$ and shut down the IC.

Diode Emulation Mode (ZCD EN#)

When ZCD_EN# pin is low and PWM signal switches low, GL is forced on (after normal BBM time). During this time, it is under control of the ZCD (zero crossing detect) comparator. If, after the internal blanking delay, the inductor current becomes zero, GL is turned off. This improves light load efficiency by avoiding discharge of output capacitors.

If PWM enters tri-state, then device will go into normal tri-state mode after tri-state Delay. The GL output will be turned off regardless of Inductor current, this is an alternative method of improving light load efficiency by reducing switching losses.

Thermal Warning (THWn)

The THWn pin is an open drain signal that flags the presence of excessive junction temperature. Connect a maximum of 20 k Ω to pull this pin up to V_{CIN}. An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THWn flag is set. When the junction temperature drops below 135 °C the device will clear the THWn signal. The SiC783A does not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The switch node, V_{SWH}, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter.

The PHASE pin is internally connected to the switch node V_{SWH} . This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20 k Ω resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground Connections (C_{GND} and P_{GND})

 P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the printed circuit board should be such that the inductance separating C_{GND} and P_{GND} is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (VDRV, VCIN)

 V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate driver noise into the IC.

Bootstrap Circuit (BOOT)

An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a bootstrap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.



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Shoot-Through Protection and Adaptive Dead Time (AST)

The SiC783A has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFETs are not turned on at the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are monitored to prevent the one turning on from tuning on until the other's gate voltage is sufficiently low (< 1 V). Built in delays also ensure that one power MOS is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC783A also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20 $k\Omega$ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

FUNCTIONAL BLOCK DIAGRAM

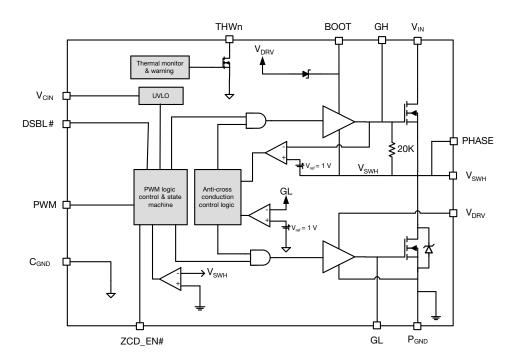


Fig. 3 - SiC783A Functional Block Diagram



PWM TIMING DIAGRAM

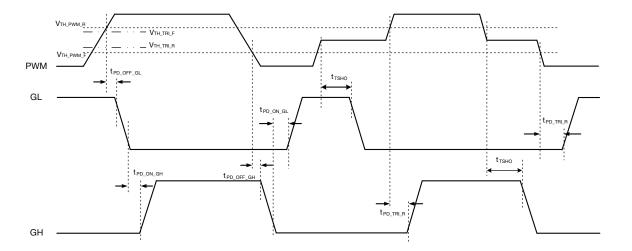


Fig. 4 - Definition of PWM Logic and Tri-State

OPERATION TIMING DIAGRAM: DSBL#

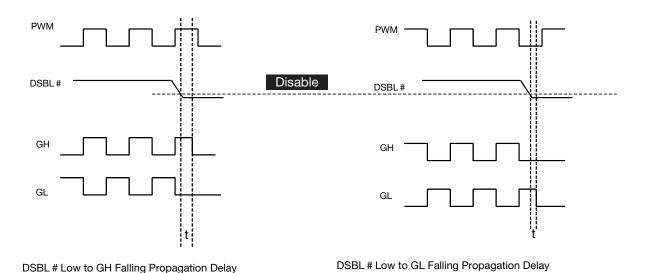


Fig. 5 - DSBL# Propagation Delay



ELECTRICAL CHARACTERISTICS

 $(V_{IN} = 12 \text{ V, F}_{SW} = 500 \text{ kHz}, V_{DRV} = V_{CIN} = 5 \text{ V, L}_{O/P} = 0.33 \text{ } \mu\text{H} \text{ / DCR } 0.83 \text{ } m\Omega \text{ (IHLP-5050FD0R33-01), unless noted otherwise)}$

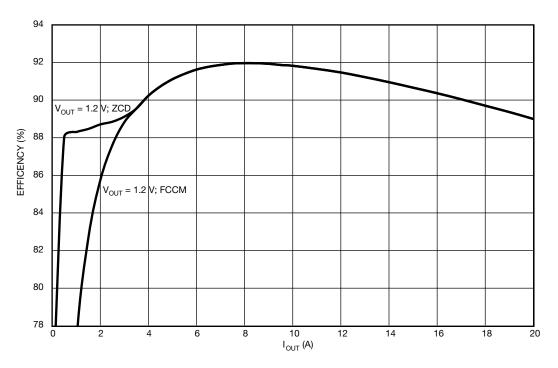


Fig. 6 - Efficiency vs. I_{OUT}

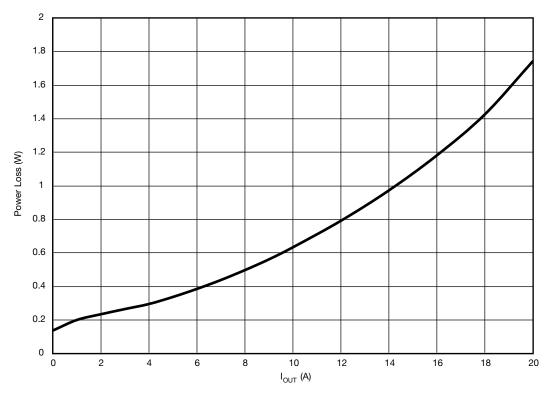


Fig. 7 - Power Stage Power Loss vs. I_{OUT}



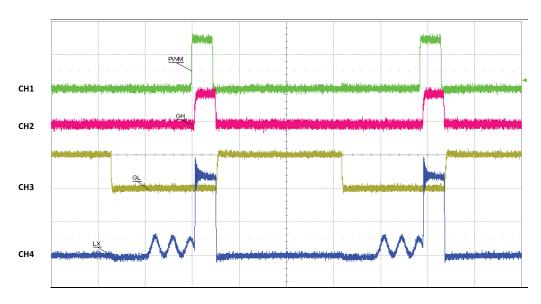
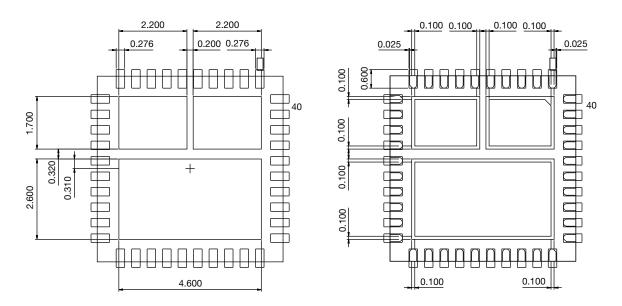


Fig. 8 - Zero Cross Detect Mode Operation (ZCD)
CH1 (green) = PWM (2V/div), CH2 (red) = GH (5V/div), CH3 (yellow) = GL (5V/div), CH4 (blue) = V_{SWH} (5V/div)

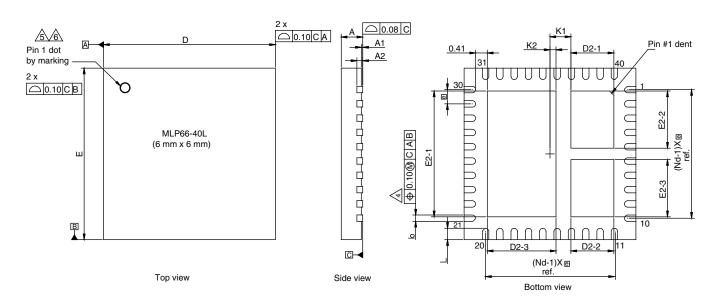
RECOMMENDED LAND PATTERN PowerPAK MLP66-40L



All Dimensions are in milimeters

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PACKAGE OUTLINE DRAWING

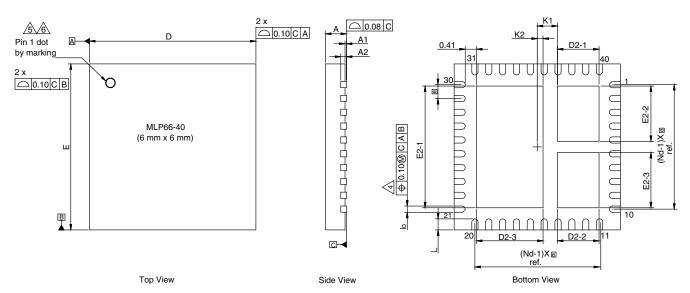


DIM		MILLIMETERS			INCHES		
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	0.70	0.75	0.80	0.027	0.029	0.031	
A1	0.00	-	0.05	0.000	-	0.002	
A2		0.20 ref.			0.008 ref.		
b	0.20	0.25	0.30	0.078	0.098	0.011	
D		6.00 BSC			0.236 BSC		
е		0.50 BSC			0.019 BSC		
E	6.00 BSC				0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017	
N		40			40		
Nd		10			10		
Ne		10			10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061	
D2-2	1.45	1.50	1.55	0.057	0.059	0.061	
D2-3	2.35	2.40	2.45	0.095	0.094	0.096	
E2-1	4.35	4.40	4.45	0.171	0.173	0.175	
E2-2	1.95	2.00	2.05	0.076	0.078	0.080	
E2-3	1.95	2.00	2.05	0.076	0.078	0.080	
K1		0.73 BSC		0.028 BSC			
K2		0.21 BSC	-		0.008 BSC	_	

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?64902.



PowerPAK® MLP66-40 Case Outline



DIM.		MILLIMETERS			INCHES	
DIIVI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A ⁽⁸⁾	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b ⁽⁴⁾	0.20	0.25	0.30	0.078	0.098	0.011
D		6.00 BSC			0.236 BSC	
е		0.50 BSC			0.019 BSC	
Е		6.00 BSC		0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N ⁽³⁾		40 40				
Nd ⁽³⁾		10			10	
Ne ⁽³⁾		10			10	
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1		0.73 BSC	•	0.028 BSC		
K2		0.21 BSC			0.008 BSC	

ECN: T14-0826-Rev. B, 12-Jan-15

DWG: 5986

Notes

- 1. Use millimeters as the primary measurement
- 2. Dimensioning and tolerances conform to ASME Y14.5M. 1994
- 3. N is the number of terminals. Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction

 Δ Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip

The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body Exact shape and size of this feature is optional

7. Package warpage max. 0.08 mm

Applied only for terminals

Revision: 12-Jan-15 1 Document Number: 64846



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Revision: 02-Oct-12 Document Number: 91000

ПОСТАВКА ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

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http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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