1. General description

Dual Standard level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- AEC-Q101 compliant
- · Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with V_{GS(th)} rating of greater than 1 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- · Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Limiting values	Limiting values FET1 and FET2						
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	80	٧
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	23	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	68	W
Static characte	eristics FET1 and FET2				•		
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_{D} = 10 A; T_{j} = 25 °C; Fig. 11		-	11.2	15	mΩ
Dynamic chara	acteristics FET1 and FE	T2			•		_
Q_{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 64 V; V _{GS} = 10 V; T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>		-	11.3	-	nC
Source-drain o	liode FET1 and FET2						
Q _r	recovered charge	I_S = 10 A; dI_S/dt = -100 A/ μ s; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C		-	37.7	-	nC



Dual N-channel 80 V, 15 m Ω standard level MOSFET

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	8 7 6 5	D1 D1 D2 D2
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		S1 G1 S2 G2
6	D2	drain2		mbk725
7	D1	drain1	1 2 3 4	
8	D1	drain1	LFPAK56D (SOT1205)	

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
BUK7K15-80E	LFPAK56D	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205			

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K15-80E	71580E

Dual N-channel 80 V, 15 mΩ standard level MOSFET

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Limiting val	ues FET1 and FET2		'	'	_	
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	80	V
V_{DGR}	drain-gate voltage	R _{GS} = 20 kΩ		-	80	V
V _{GS}	gate-source voltage	DC; T _j ≤ 175 °C		20	-20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	68	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	23	Α
		V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 2</u>		-	16	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$; Fig. 3		-	92	Α
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drai	n diode FET1 and FET2			•		
Is	source current	T _{mb} = 25 °C		-	23	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	92	Α
Avalanche r	ruggedness FET1 and FET2					
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 23 A; $V_{sup} \le 80$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[1] [2]	-	133	mJ

- Single-pulse avalanche rating limited by maximum junction temperature of 175 $^{\circ}\text{C}.$ Refer to application note AN10273 for further information.

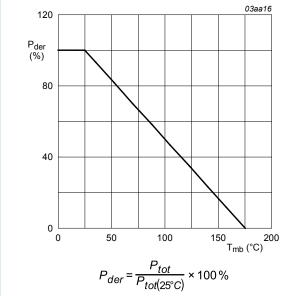


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

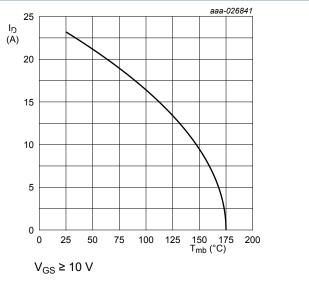


Fig. 2. Continuous drain current as a function of mounting base temperature, FET1 and FET2

BUK7K15-80E

Dual N-channel 80 V, 15 m Ω standard level MOSFET

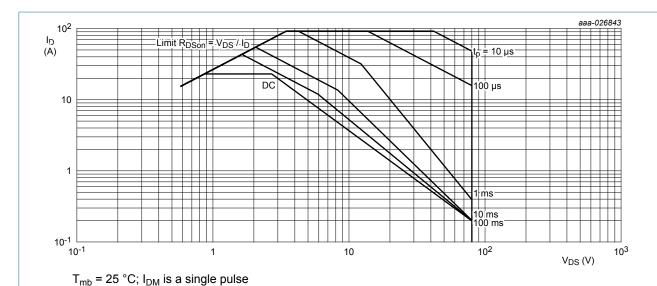


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and

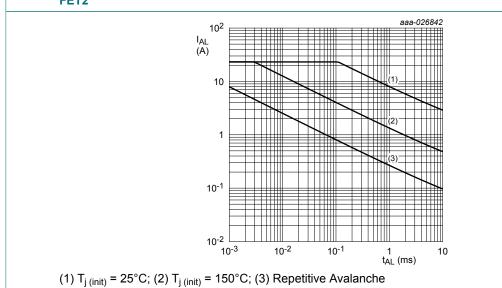


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

Dual N-channel 80 V, 15 m Ω standard level MOSFET

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	2.21	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

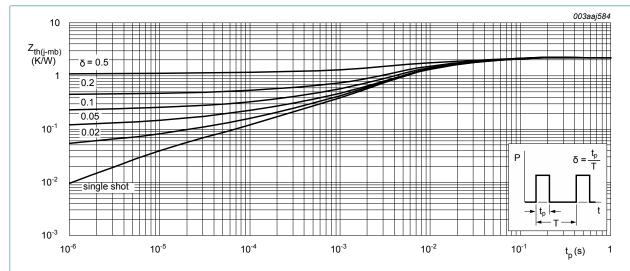


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

Dual N-channel 80 V, 15 m Ω standard level MOSFET

10. Characteristics

Table 7. Characteristics

Parameter	Conditions	Min	Тур	Max	Unit
cteristics FET1 and FET2			'		'
drain-source	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	80	-	-	V
breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	72	-	-	V
gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 9; Fig. 10$	2.4	3	4	V
	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C; Fig. 10	-	-	4.5	V
	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 175 °C; Fig. 10	1	-	-	V
drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _j = 25 °C	-	0.03	1	μΑ
	V _{DS} = 80 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
drain-source on-state resistance	V_{GS} = 10 V; I_{D} = 10 A; T_{j} = 25 °C; Fig. 11	-	11.2	15	mΩ
	V_{GS} = 10 V; I_{D} = 10 A; T_{j} = 175 °C; Fig. 12	-	-	38	mΩ
aracteristics FET1 and FE	T2		'		_
total gate charge	I _D = 10 A; V _{DS} = 64 V; V _{GS} = 10 V;	-	35.1	-	nC
gate-source charge	T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	7.4	-	nC
gate-drain charge		-	11.3	-	nC
input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz;	-	1847	2457	pF
output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	194	233	pF
reverse transfer capacitance		-	115	158	pF
turn-on delay time	$V_{DS} = 60 \text{ V}; R_L = 5 \Omega; V_{GS} = 10 \text{ V};$	-	8.8	-	ns
rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 ^{\circ}C$	-	12.6	-	ns
turn-off delay time		-	25.1	-	ns
fall time		-	15.1	-	ns
n diode FET1 and FET2		'			
source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _j = 25 °C; <u>Fig. 16</u>	-	0.8	1.2	V
reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/ μ s; V_{GS} = 0 V; V_{DS} = 25 V; T_i = 25 °C	-	30.5	-	ns
	drain-source breakdown voltage gate-source threshold voltage drain leakage current drain-source on-state resistance aracteristics FET1 and FET1 total gate charge gate-source charge gate-drain charge input capacitance output capacitance reverse transfer capacitance turn-on delay time rise time turn-off delay time fall time n diode FET1 and FET2 source-drain voltage		$ \begin{array}{ c c c c } \hline \textbf{Conditions} & \textbf{Min} \\ \hline \textbf{Cteristics FET1 and FET2} \\ \hline \\ $		

Dual N-channel 80 V, 15 mΩ standard level MOSFET

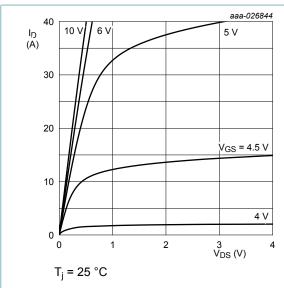


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2

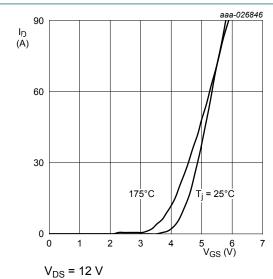


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

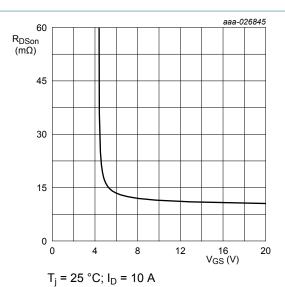


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2

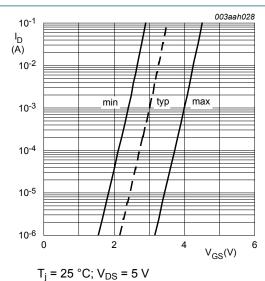


Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

Dual N-channel 80 V, 15 mΩ standard level MOSFET

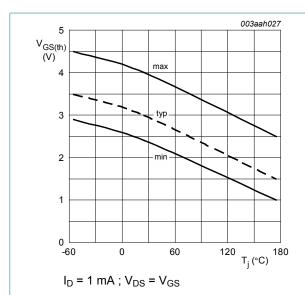


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

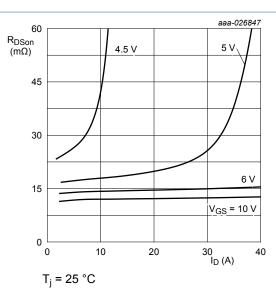


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

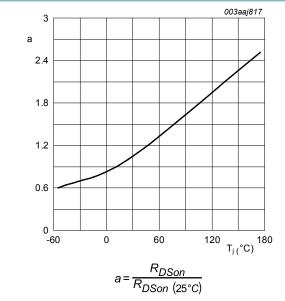


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

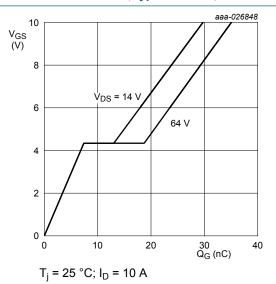


Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

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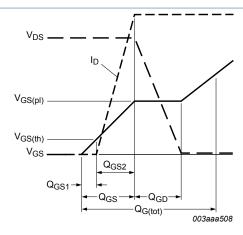
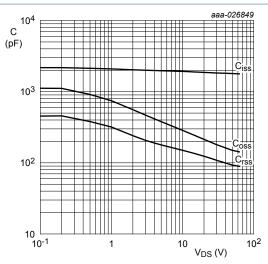
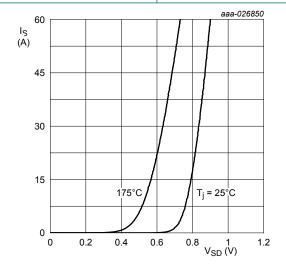


Fig. 14. Gate charge waveform definitions



 $V_{GS} = 0 V$; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

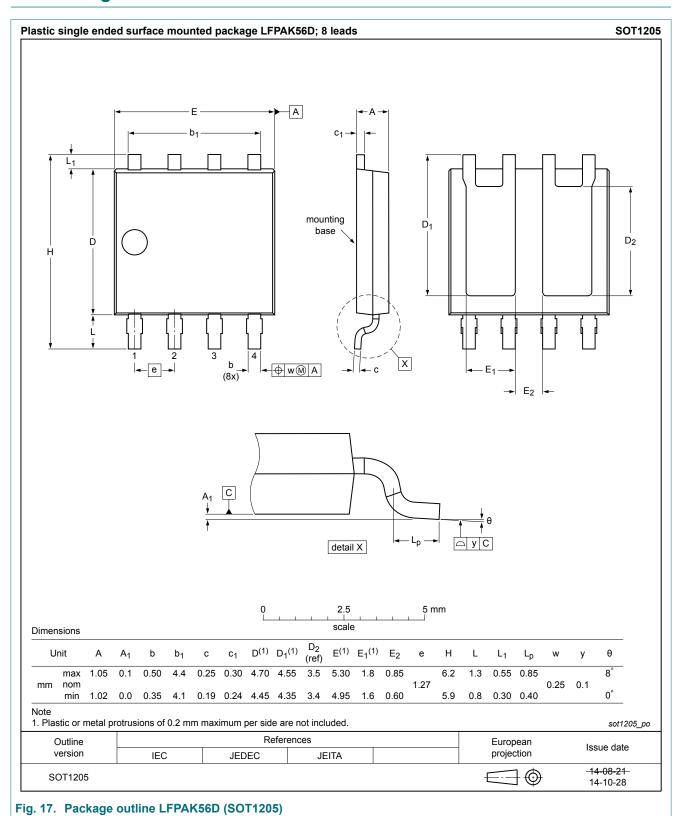


 $V_{GS} = 0 V$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

Dual N-channel 80 V, 15 mΩ standard level MOSFET

11. Package outline



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Dual N-channel 80 V, 15 mΩ standard level MOSFET

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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BUK7K15-80E

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Dual N-channel 80 V, 15 m Ω standard level MOSFET

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