Low Power, Three Electrode Electrocardiogram (ECG) Analog Front End

Data Sheet

ADAS1000-3/ADAS1000-4

FEATURES

Biopotential signals in; digitized signals out
3 acquisition (ECG) channels and one driven lead
Can be ganged for 8 electrode + RLD using master ADAS1000 or ADAS1000-1
AC and DC lead-off detection
Internal pace detection algorithm on 3 leads
Support for user's own pace
Thoracic impedance measurement (internal/external path)
Selectable reference lead
Scalable noise vs. power control, power-down modes
Low power operation from
11 mW (1 lead), 15 mW (3 leads)
Lead or electrode data available
Supports AAMI EC11:1991/(R)2001/(R)2007, AAMI EC38 R2007, EC13:2002/(R)2007, IEC60601-1 ed. 3.0 b:2005, IEC60601-2-25 ed. 2.0 :2011, IEC60601-2-27 ed. 2.0 b:2005, IEC60601-2-51 ed. 1.0 b: 2005
Fast overload recovery
Low or high speed data output rates
Serial interface SPI-/QSPI™-/DSP-compatible
56-lead LFCSP package (9 mm × 9 mm)
64-lead LQFP package (10 mm × 10 mm body size)

APPLICATIONS

ECG: monitor and diagnostic
Bedside patient monitoring, portable telemetry, Holter, AED, cardiac defibrillators, ambulatory monitors, pace maker programmer, patient transport, stress testing

GENERAL DESCRIPTION

The ADAS1000-3/ADAS1000-4 measure electro cardiac (ECG) signals, thoracic impedance, pacing artifacts, and lead-on/off status and output this information in the form of a data frame supplying either lead/vector or electrode data at programmable data rates. Its low power and small size make it suitable for portable, battery-powered applications. The high performance also makes it suitable for higher end diagnostic machines.

The ADAS1000-4 is a full-featured, 3-channel ECG including respiration and pace detection, while the ADAS1000-3 offers only ECG channels with no respiration or pace features.

The ADAS1000-3/ADAS1000-4 are designed to simplify the task of acquiring and ensuring quality ECG signals. They provide a low power, small data acquisition system for biopotential applications. Auxiliary features that aid in better quality ECG signal acquisition include: multichannel averaged driven lead, selectable reference drive, fast overload recovery, flexible respiration circuitry returning magnitude and phase information, internal pace detection algorithm operating on three leads, and the option of ac or dc lead-off detection. Several digital output options ensure flexibility when monitoring and analyzing signals. Value-added cardiac post processing is executed externally on a DSP, microprocessor, or FPGA.

Because ECG systems span different applications, the ADAS1000-3/ADAS1000-4 feature a power/noise scaling architecture where the noise can be reduced at the expense of increasing power consumption. Signal acquisition channels may be shut down to save power. Data rates can be reduced to save power.

To ease manufacturing tests and development as well as offer holistic power-up testing, the ADAS1000-3/ADAS1000-4 offer a suite of features, such as dc and ac test excitation via the calibration DAC and CRC redundancy testing in addition to readback of all relevant register address space.

The input structure is a differential amplifier input thereby allowing users a variety of configuration options to best suit their application.

The ADAS1000-3/ADAS1000-4 are available in two package options: either a 56-lead LFCSP or a 64-lead LQFP package; they are specified over −40°C to +85°C temperature range.

Rev. B
Document Feedback

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11/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

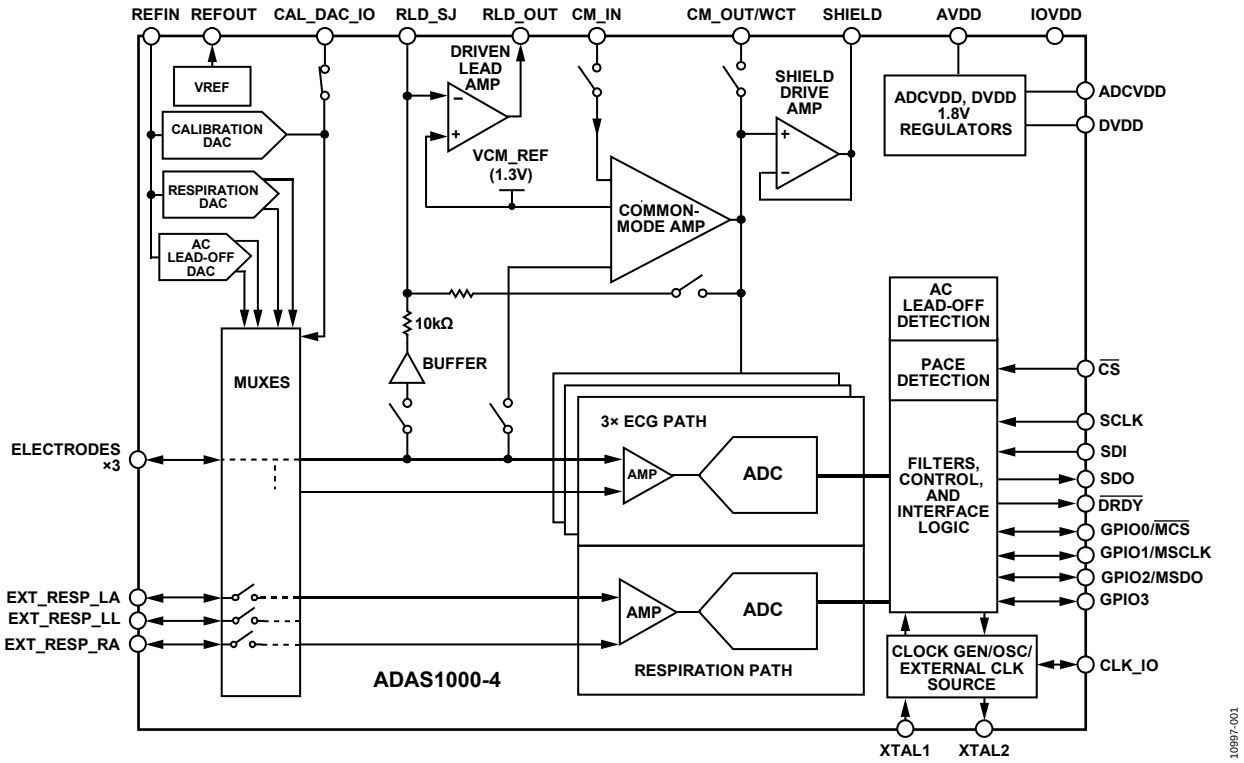


Figure 1. ADAS1000-4 3-Channel Full Featured Model

Table 1. Overview of Features Available from ADAS1000 Generics

Generic	ECG	Operation	Right Leg Drive	Respiration	Pace Detection	Shield Driver	Master Interface[1]	Package Option
ADAS1000	5 ECG channels	Master/slave	Yes	Yes	Yes	Yes	Yes	LFCSP, LQFP
ADAS1000-1	5 ECG channels	Master/slave	Yes			Yes	Yes	LFCSP
ADAS1000-2[2]	5 ECG channels	Slave						LFCSP, LQFP
ADAS1000-3	3 ECG channels	Master/slave	Yes			Yes	Yes	LFCSP, LQFP
ADAS1000-4	3 ECG channels	Master/slave	Yes	Yes	Yes	Yes	Yes	LFCSP, LQFP

[1] Master interface is provided for users wishing to utilize their own digital pace algorithm; see the Secondary Serial Interface section.
[2] This is a companion device for increased channel count purposes. It has a subset of features and is not intended for standalone use. It may be used in conjunction with any master device.

SPECIFICATIONS

AVDD = 3.3 V ± 5%, IOVDD = 1.65 V to 3.6 V, AGND = DGND = 0 V, REFIN tied to REFOUT, externally supplied crystal/clock = 8.192 MHz. Decoupling for reference and supplies as noted in the Power Supply, Grounding, and Decoupling Strategy section. T_A = −40°C to +85°C, unless otherwise noted. Typical specifications are mean values at T_A = 25°C.

For specified performance, internal ADCVDD and DVDD linear regulators have been used. They may be supplied from external regulators. ADCVDD = 1.8 V ± 5%, DVDD = 1.8 V ± 5%.

Front-end gain settings: GAIN 0 = ×1.4, GAIN 1 = ×2.1, GAIN 2 = ×2.8, GAIN 3 = ×4.2.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ECG CHANNEL					These specifications apply to the following pins: ECG1_LA, ECG2_LL, ECG3_RA, CM_IN (CE mode), EXT_RESP_xx pins when used in extend switch mode
Electrode Input Range					Independent of supply
	0.3	1.3	2.3	V	GAIN 0 (gain setting ×1.4)
	0.63	1.3	1.97	V	GAIN 1 (gain setting ×2.1)
	0.8	1.3	1.8	V	GAIN 2 (gain setting ×2.8)
	0.97	1.3	1.63	V	GAIN 3 (gain setting ×4.2)
Input Bias Current	−40	±1	+40	nA	Relates to each electrode input; over operating range; dc and ac lead-off are disabled
	−200		+200	nA	AGND to AVDD
Input Offset		−7		mV	Electrode/vector mode with VCM = VCM_REF GAIN 3
		−7		mV	GAIN 2
		−15		mV	GAIN 1
		−22		mV	GAIN 0
Input Offset Tempco[1]		±2		µV/°C	
Input Amplifier Input Impedance[2]		1‖10		GΩ‖pF	At 10 Hz
CMRR[2]	105	110		dB	51 kΩ imbalance, 60 Hz with ±300 mV differential dc offset; per AAMI/IEC standards; with driven leg loop closed
Crosstalk[1]		80		dB	Between channels
Resolution[2]		19		Bits	Electrode/vector mode, 2 kHz data rate, 24-bit data-word
		18		Bits	Electrode/vector mode, 16 kHz data rate, 24-bit data-word
		16		Bits	Electrode/analog lead mode, 128 kHz data rate, 16-bit data-word
Integral Nonlinearity Error		30		ppm	GAIN 0; all data rates
Differential Nonlinearity Error		5		ppm	GAIN 0
Gain[2]					Referred to input; $(2 \times VREF)/gain/(2^N - 1)$; Applies after factory calibration. User calibration adjusts this number.
GAIN 0 (×1.4)		4.9		µV/LSB	At 19-bit level in 2 kHz data rate
		9.81		µV/LSB	At 18-bit level in 16 kHz data rate
		39.24		µV/LSB	At 16-bit level in 128 kHz data rate
GAIN 1 (×2.1)		3.27		µV/LSB	At 19-bit level in 2 kHz data rate
		6.54		µV/LSB	At 18-bit level in 16 kHz data rate
		26.15		µV/LSB	At 16-bit level in 128 kHz data rate
GAIN 2 (×2.8)		2.45		µV/LSB	At 19-bit level in 2 kHz data rate
		4.9		µV/LSB	At 18-bit level in 16 kHz data rate
		19.62		µV/LSB	At 16-bit level in 128 kHz data rate
GAIN 3 (×4.2)		1.63		µV/LSB	No factory calibration for this gain setting At 19-bit level in 2 kHz data rate
		3.27		µV/LSB	At 18-bit level in 16 kHz data rate
		13.08		µV/LSB	At 16-bit level in 128 kHz data rate

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Gain Error	−1	+0.01	+1	%	GAIN 0 to GAIN 2, factory calibrated; programmable user or factory calibration option enables; factory gain calibration applies only to standard ECG interface
	−2	+0.1	+2	%	GAIN 3 setting, no factory calibration for this gain
Gain Matching	−0.1	+0.02	+0.1	%	GAIN 0 to GAIN 2
	−0.5	+0.1	+0.5	%	GAIN 3
Gain Tempco[1]		25		ppm/°C	
Input Referred Noise[1]					GAIN 2, 2 kHz data rate, see Table 4
Analog Lead Mode		6		µV p-p	0.5 Hz to 40 Hz; high performance mode
		10		µV p-p	0.05 Hz to 150 Hz; high performance mode
		12		µV p-p	0.05 Hz to 150 Hz; low power mode
Electrode Mode		11		µV p-p	0.05 Hz to 150 Hz; high performance mode
		12		µV p-p	0.05 Hz to 150 Hz; low power mode
Digital Lead Mode		14		µV p-p	0.05 Hz to 150 Hz; high performance mode
		16		µV p-p	0.05 Hz to 150 Hz; low power mode
Power Supply Sensitivity[2]		100		dB	At 120 Hz
Analog Channel Bandwidth[1]		65		kHz	
Dynamic Range[1]		104		dB	GAIN 0, 2 kHz data rate, −0.5 dBFS input signal, 10 Hz
Signal-to-Noise Ratio[1]		100		dB	−0.5 dB FS input signal
COMMON-MODE INPUT					CM_IN pin
Input Voltage Range	0.3		2.3	V	
Input Impedance[2]		1||10		GΩ||pF	
Input Bias Current	−40	±1	+40	nA	Over operating range; dc and ac lead-off disabled
	−200		+200	nA	AGND to AVDD
COMMON-MODE OUTPUT					CM_OUT pin
VCM_REF	1.28	1.3	1.32	V	Internal voltage; independent of supply
Output Voltage, VCM	0.3	1.3	2.3	V	No dc load
Output Impedance[1]		0.75		kΩ	Not intended to drive current
Short-Circuit Current[1]		4		mA	
Electrode Summation Weighting Error[2]		1		%	Resistor matching error
RESPIRATION FUNCTION (ADAS1000-4 ONLY)					These specifications apply to the following pins: EXT_RESP_LA, EXT_RESP_LL, EXT_RESP_RA and selected internal respiration paths (Lead I, Lead II, Lead III)
Input Voltage Range	0.3		2.3	V	AC-coupled, independent of supply
Input Voltage Range (Linear Operation)		1.8/gain		V p-p	Programmable gain (10 states)
Input Bias Current	−10	±1	+10	nA	Applies to EXT_RESP_xx pins over AGND to AVDD
Input Referred Noise[1]		0.85		µV rms	
Frequency[2]		46.5 to 64		kHz	Programmable frequency, see Table 30
Excitation Current					Respiration drive current corresponding to differential voltage programmed by the RESPAMP bits in the RESPCTL register; internal respiration mode, cable 5 kΩ/200 pF, 1.2 kΩ chest impedance
		64		µA p-p	Drive Range A
		32		µA p-p	Drive Range B[2]
		16		µA p-p	Drive Range C[2]
		8		µA p-p	Drive Range D[2]
Resolution[2]		24		Bits	Update rate 125 Hz
Measurement Resolution[1]		0.2		Ω	Cable <5 kΩ/200 pF per electrode, body resistance modeled as 1.2 kΩ
		0.02		Ω	No cable impedance, body resistance modeled as 1.2 kΩ
In-Amp Gain[1]		1 to 10			Digitally programmable in steps of 1
Gain Error			1	%	LSB weight for GAIN 0 setting
Gain Tempco[1]		25		ppm/C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RIGHT LEG DRIVE/DRIVEN LEAD					
Output Voltage Range	0.2		AVDD − 0.2	V	
RLD_OUT Short-Circuit Current	−5	±2	+5	mA	External protection resistor required to meet regulatory patient current limits; output shorted to AVDD/AGND
Closed-Loop Gain Range[2]	25			V/V	
Slew Rate[2]		200		mV/ms	
Input Referred Noise[1]		8		μV p-p	0.05 Hz to 150 Hz
Amplifier GBP[2]		1.5		MHz	
DC LEAD-OFF					Internal current source, pulls up open ECG pins; programmable in 10 nA steps: 10 nA to 70 nA
Lead-Off Current Accuracy		±10		%	Of programmed value
High Threshold Level[1]		2.4		V	Inputs are compared to threshold levels; if inputs exceed levels, lead-off flag is raised
Low Threshold Level[1]		0.2		V	
Threshold Accuracy		25		mV	
AC LEAD-OFF					Programmable in 4 steps: 12.5 nA rms, 25 nA rms, 50 nA rms, 100 nA rms
Frequency Range		2.039		kHz	Fixed frequency
Lead-Off Current Accuracy		±10		%	Of programmed value, measured into low impedance
REFIN					
Input Range[2]	1.76	1.8	1.84	V	Channel gain scales directly with REFIN
Input Current		113		μA	Per active ADC
	450	675	950	μA	Three ECG channels and respiration enabled
REFOUT					On-chip reference voltage for ADC; not intended to drive other components reference inputs directly, must be buffered externally
Output Voltage, VREF	1.785	1.8	1.815	V	
Reference Tempco[1]		±10		ppm/°C	
Output Impedance[2]		0.1		Ω	
Short-Circuit Current[1]		4.5		mA	Short circuit to ground
Voltage Noise[1]		33		μV p-p	0.05 Hz to 150 Hz (ECG band)
		17		μV p-p	0.05 Hz to 5 Hz (respiration)
CALIBRATION DAC					Available on CAL_DAC_IO (output for master, input for slave)
DAC Resolution		10		Bits	
Full-Scale Output Voltage	2.64	2.7	2.76	V	No load, nominal FS output is 1.5 × REFOUT
Zero-Scale Output Voltage	0.24	0.3	0.36	V	No load
DNL	−1		+1	LSB	
Output Series Resistance[2]		10		kΩ	Not intended to drive low impedance load, used for slave CAL_DAC_IO configured as an input
Input Current		±5		nA	When used as an input
CALIBRATION DAC TEST TONE					
Output Voltage	0.9	1	1.1	mV p-p	Rides on common-mode voltage, VCM_REF = 1.3 V
Square Wave		1		Hz	
Low Frequency Sine Wave		10		Hz	
High Frequency Sine Wave		150		Hz	
SHIELD DRIVER					
Output Voltage Range	0.3		2.3	V	Rides on common-mode voltage (VCM)
Gain		1		V/V	
Offset Voltage	−20		+20	mV	
Short-Circuit Current		15	25	μA	Output current limited by internal series resistance
Stable Capacitive Load[2]			10	nF	
CRYSTAL OSCILLATOR					Applied to XTAL1 and XTAL2
Frequency[2]		8.192		MHz	
Start-Up Time[2]		15		ms	Internal startup

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK_IO					External clock source supplied to CLK_IO; this pin is configured as an input when the device is programmed as a slave
Operating Frequency[2]		8.192		MHz	
Input Duty Cycle[2]	20		80	%	
Output Duty Cycle[2]		50		%	
DIGITAL INPUTS					Applies to all digital inputs
Input Low Voltage, V_{IL}			0.3 × IOVDD	V	
Input High Voltage, V_{IH}	0.7 × IOVDD			V	
Input Current, I_{IH}, I_{IL}	−1		+1	µA	
	−20		+20	µA	$\overline{\text{RESET}}$ has an internal pull-up resistor
Pin Capacitance[2]		3		pF	
DIGITAL OUTPUTS					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 1 mA
Output High Voltage, V_{OH}	IOVDD − 0.4			V	I_{SOURCE} = −1 mA
Output Rise/Fall Time		4		ns	Capacitive load = 15 pF, 20% to 80%
DVDD REGULATOR					Internal 1.8 V regulator for DVDD
Output Voltage	1.75	1.8	1.85	V	
Available Current[1]		1		mA	Droop < 10 mV; for external device loading purposes
Short-Circuit Current Limit		40		mA	
ADCVDD REGULATOR					Internal 1.8 V regulator for ADCVDD; not recommended as a supply for other circuitry
Output Voltage	1.75	1.8	1.85	V	
Short-Circuit Current Limit		40		mA	
POWER SUPPLY RANGES[2]					
AVDD	3.15	3.3	5.5	V	
IOVDD	1.65		3.6	V	
ADCVDD	1.71	1.8	1.89	V	If applied by external 1.8 V regulator
DVDD	1.71	1.8	1.89	V	If applied by external 1.8 V regulator
POWER SUPPLY CURRENTS					
AVDD Standby Current		785	975	µA	
IOVDD Standby Current		1	60	µA	
EXTERNALLY SUPPLIED ADCVDD AND DVDD					All three channels enabled, RLD enabled, pace enabled
AVDD Current		2.4	4.1	mA	High performance mode
		2.2	4.1	mA	Low performance mode
		3.2		mA	High performance mode, respiration enabled
ADCVDD Current		4.5	6.5	mA	High performance mode
		3.3	5.5	mA	Low performance mode
		5.4		mA	High performance mode, respiration enabled
DVDD Current		2.0	4	mA	High performance mode
		1.1	3	mA	Low performance mode
		2.0		mA	High performance mode, respiration enabled
INTERNALLY SUPPLIED ADCVDD AND DVDD					All three channels enabled, RLD enabled, pace enabled
AVDD Current		9	12.6	mA	High performance mode
		6.6	9.6	mA	Low performance mode
		11	14.6	mA	High performance mode, respiration enabled
POWER DISSIPATION					All 3 channels enabled, RLD enabled, pace enabled
Externally Supplied ADCVDD and DVDD[3]					
Three Input Channels and RLD		19.6		mW	High performance (low noise)
		15.2		mW	Low power mode
Internally Supplied ADCVDD and DVDD					All three channels enabled, RLD enabled, pace enabled
Three Input Channels and RLD		29.7		mW	High performance (low noise)
		21.8		mW	Low power mode

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OTHER FUNCTIONS[4]					
Power Dissipation					
Respiration		7.6		mW	
Shield Driver		150		µW	
EXTERNALLY SUPPLIED ADCVDD AND DVDD					Two electrodes enabled for one lead measurement, RLD enabled, pace enabled
AVDD Current		1.9	3.7	mA	High performance mode
		1.7	3.7	mA	Low performance mode
ADCVDD Current		3.6	5.5	mA	High performance mode
		2.5	4.5	mA	Low performance mode
DVDD Current		1.7	4	mA	High performance mode
		0.9	3	mA	Low performance mode
INTERNALLY SUPPLIED ADCVDD AND DVDD					Two electrodes enabled for one lead measurement, RLD enabled, pace enabled
AVDD Current		7.3	10.7	mA	High performance mode
		5.3	8.2	mA	Low performance mode
POWER DISSIPATION					Two electrodes enabled for one lead measurement, RLD enabled, pace enabled
Externally Supplied ADCVDD and DVDD[3]					
Two Input Channels and RLD		15.8		mW	High performance (low noise)
		11.7		mW	Low power mode
Internally Supplied ADCVDD and DVDD					
Two Input Channels and RLD		24		mW	High performance (low noise)
		17.5		mW	Low power mode

[1] Guaranteed by characterization, not production tested.
[2] Guaranteed by design, not production tested.
[3] ADCVDD and DVDD can be powered from an internal LDO or, alternatively, can be powered from an external 1.8 V rail, which may result in a lower power solution.
[4] Pace is a digital function and incurs no power penalty.

NOISE PERFORMANCE

Table 3. Typical Input Referred Noise over a 0.5 sec Window (μV p-p)[1]

Mode	Data Rate[2]	GAIN 0 (×1.4) ±1 VCM	GAIN 1 (×2.1) ±0.67 VCM	GAIN 2 (×2.8) ±0.5 VCM	GAIN 3 (×4.2) ±0.3 VCM
Analog Lead Mode[3]					
High Performance Mode	2 kHz (0.5 Hz to 40 Hz)	8	6	5	4
	2 kHz (0.05 Hz to 150 Hz)	14	11	9	7.5

[1] Typical values measured at 25°C, not subject to production test.
[2] Data gathered using the 2 kHz packet/frame rate is measured over 0.5 seconds. The ADAS1000-3/ADAS1000-4 internal programmable low-pass filter is configured for either 40 Hz or 150 Hz bandwidth. The data is gathered and post processed using a digital filter of either 0.05 Hz or 0.5 Hz to provide data over noted frequency bands.
[3] Analog lead mode as shown in Figure 56.

Table 4. Typical Input Referred Noise (μV p-p)[1]

Mode	Data Rate[2]	GAIN 0 (×1.4) ±1 VCM	GAIN 1 (×2.1) ±0.67 VCM	GAIN 2 (×2.8) ±0.5 VCM	GAIN 3 (×4.2) ±0.3 VCM
Analog Lead Mode[3]					
High Performance Mode	2 kHz (0.5 Hz to 40 Hz)	12	8.5	6	5
	2 kHz (0.05 Hz to 150 Hz)	20	14.5	10	8.5
	2 kHz (0.05 Hz to 250 Hz)	27	18	14.5	10.5
	2 kHz (0.05 Hz to 450 Hz)	33.5	24	19	13.5
	16 kHz	95	65	50	39
	128 kHz	180	130	105	80
Low Power Mode	2 kHz (0.5 Hz to 40 Hz)	13	9.5	7.5	5.5
	2 kHz (0.05 Hz to 150 Hz)	22	15.5	12	9
	16 kHz	110	75	59	45
	128 kHz	215	145	116	85
Electrode Mode[4]					
High Performance Mode	2 kHz (0.5 Hz to 40 Hz)	13	9.5	8	5.5
	2 kHz (0.05 Hz to 150 Hz)	21	15	11	9
	2 kHz (0.05 Hz to 250 Hz)	26	19	15.5	11.5
	2 kHz (0.05 Hz to 450 Hz)	34.5	25	20.5	14.5
	16 kHz	100	70	57	41
	128 kHz	190	139	110	85
Low Power Mode	2 kHz (0.5 Hz to 40 Hz)	14	9.5	7.5	5.5
	2 kHz (0.05 Hz to 150 Hz)	22	15.5	12	9.5
	16 kHz	110	75	60	45
	128 kHz	218	145	120	88
Digital Lead Mode[5, 6]					
High Performance Mode	2 kHz (0.5 Hz to 40 Hz)	16	11	9	6.5
	2 kHz (0.05 Hz to 150 Hz)	25	19	15	10
	2 kHz (0.05 Hz to 250 Hz)	34	23	18	13
	2 kHz (0.05 Hz to 450 Hz)	46	31	24	17.5
	16 kHz	130	90	70	50
Low Power Mode	2 kHz (0.5 Hz to 40 Hz)	18	12.5	10	7
	2 kHz (0.05 Hz to 150 Hz)	30	21	16	11
	16 kHz	145	100	80	58

[1] Typical values measured at 25°C, not subject to production test.
[2] Data gathered using the 2 kHz packet/frame rate is measured over 20 seconds. The ADAS1000-3/ADAS1000-4 internal programmable low-pass filter is configured for either 40 Hz or 150 Hz bandwidth. The data is gathered and post processed using a digital filter of either 0.05 Hz or 0.5 Hz to provide data over noted frequency bands.
[3] Analog lead mode as shown in Figure 56.
[4] Single-ended input electrode mode as shown in Figure 59. Electrode mode refers to common electrode A, common electrode B, and single-ended input electrode configurations.
[5] Digital lead mode as shown in Figure 57.
[6] Digital lead mode is available in 2 kHz and 16 kHz data rates.

TIMING CHARACTERISTICS

Standard Serial Interface

AVDD = 3.3 V ± 5%, IOVDD = 1.65 V to 3.6 V, AGND = DGND = 0 V, REFIN tied to REFOUT, externally supplied crystal/clock = 8.192 MHz. T_A = −40°C to +85°C, unless otherwise noted. Typical specifications are mean values at T_A = 25°C.

Table 5.

	IOVDD				
Parameter[1]	**3.3 V**	**2.5 V**	**1.8 V**	**Unit**	**Description**
Output Rate[2]	2		128	kHz	Across specified IOVDD supply range; three programmable output data rates available as configured in FRMCTL register (see Table 37) 2 kHz, 16 kHz, 128 kHz; use skip mode for slower rates.
SCLK Cycle Time	25	40	50	ns min	See Table 21 for details on SCLK frequency vs. packet data/frame rates.
t_{CSSA}	8.5	9.5	12	ns min	$\overline{CS}$ valid setup time to rising SCLK.
t_{CSHA}	3	3	3	ns min	$\overline{CS}$ valid hold time to rising SCLK.
t_{CH}	8	8	8	ns min	SCLK high time.
t_{CL}	8	8	8	ns min	SCLK low time.
t_{DO}	8.5	11.5	20	ns typ	SCLK falling edge to SDO valid delay; SDO capacitance of 15 pF.
	11	19	24	ns max	
t_{DS}	2	2	2	ns min	SDI valid setup time from SCLK rising edge.
t_{DH}	2	2	2	ns min	SDI valid hold time from SCLK rising edge.
t_{CSSD}	2	2	2	ns min	$\overline{CS}$ valid setup time from SCLK rising edge.
t_{CSHD}	2	2	2	ns min	$\overline{CS}$ valid hold time from SCLK rising edge.
t_{CSW}	25	40	50	ns min	$\overline{CS}$ high time between writes (if used). Note that $\overline{CS}$ is an optional input, it may be tied permanently low. See a full description in the Serial Interfaces section.
t_{DRDY_CS}[2]	0	0	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ setup time.
t_{CSO}	6	7	9	ns typ	Delay from $\overline{CS}$ assert to SDO active.
$\overline{RESET}$ Low Time[2]	20	20	20	ns min	Minimum pulse width; $\overline{RESET}$ is edge triggered.

[1] Guaranteed by characterization, not production tested.
[2] Guaranteed by design, not production tested.

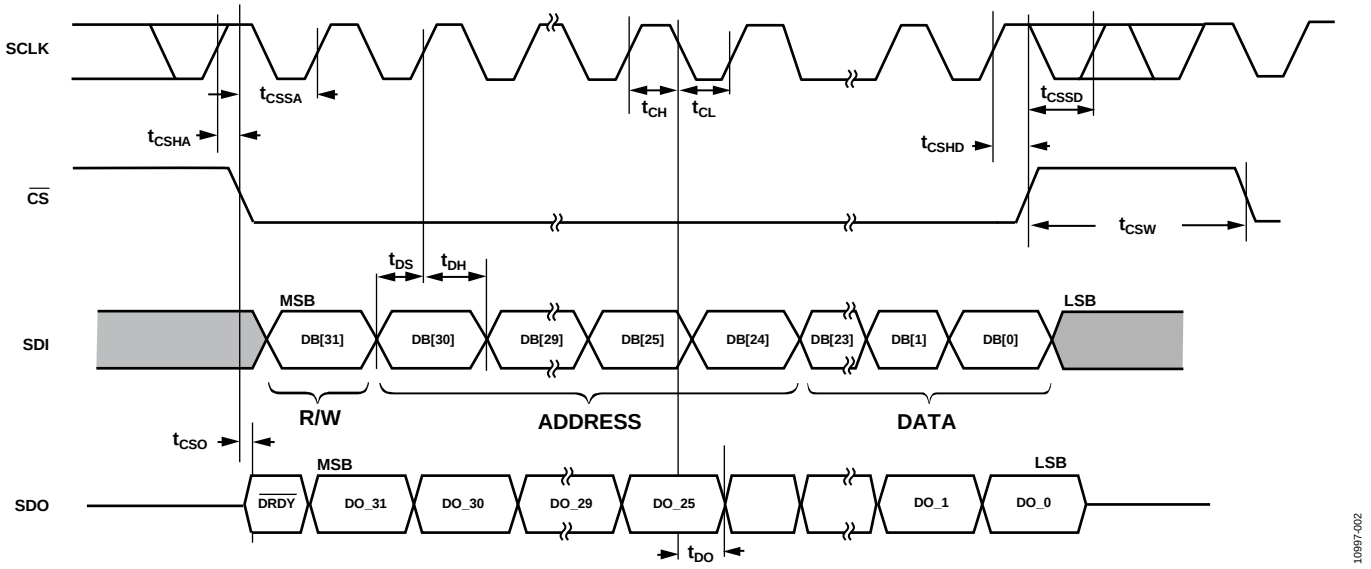


Figure 2. Data Read and Write Timing Diagram (CPHA = 1, CPOL = 1)

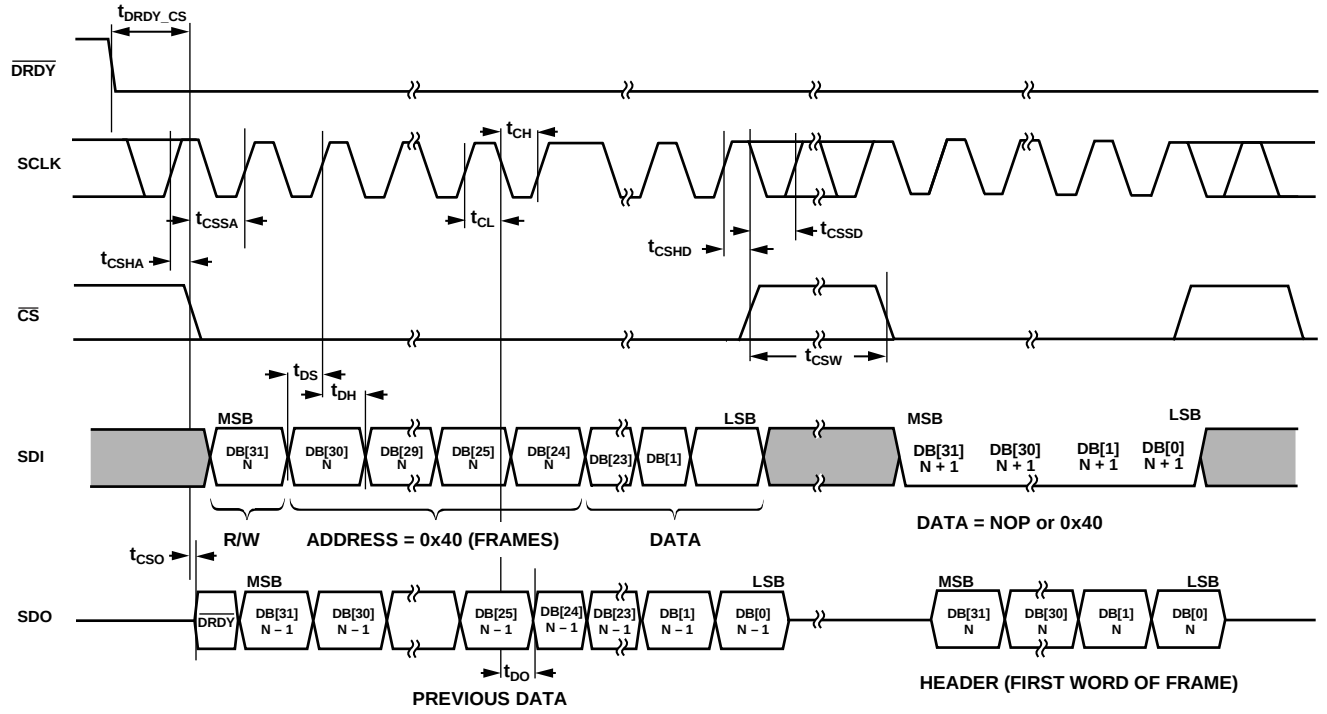


Figure 3. Starting Read Frame Data (CPHA = 1, CPOL = 1)

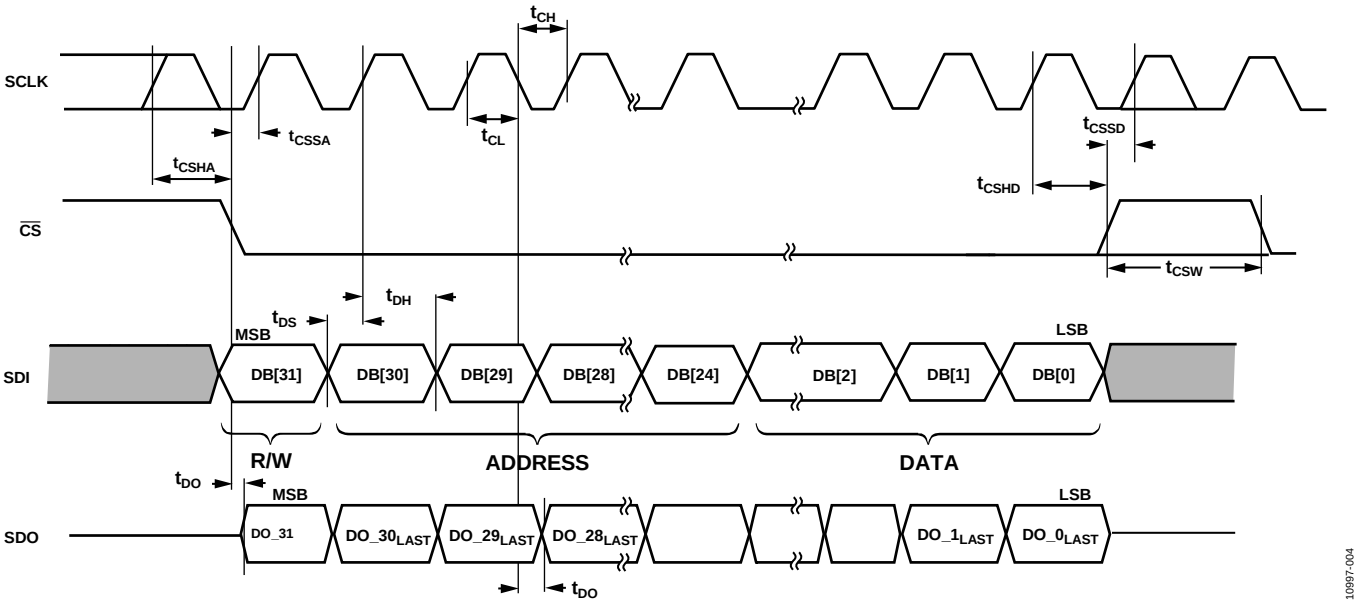


Figure 4. Data Read and Write Timing Diagram (CPHA = 0, CPOL = 0)

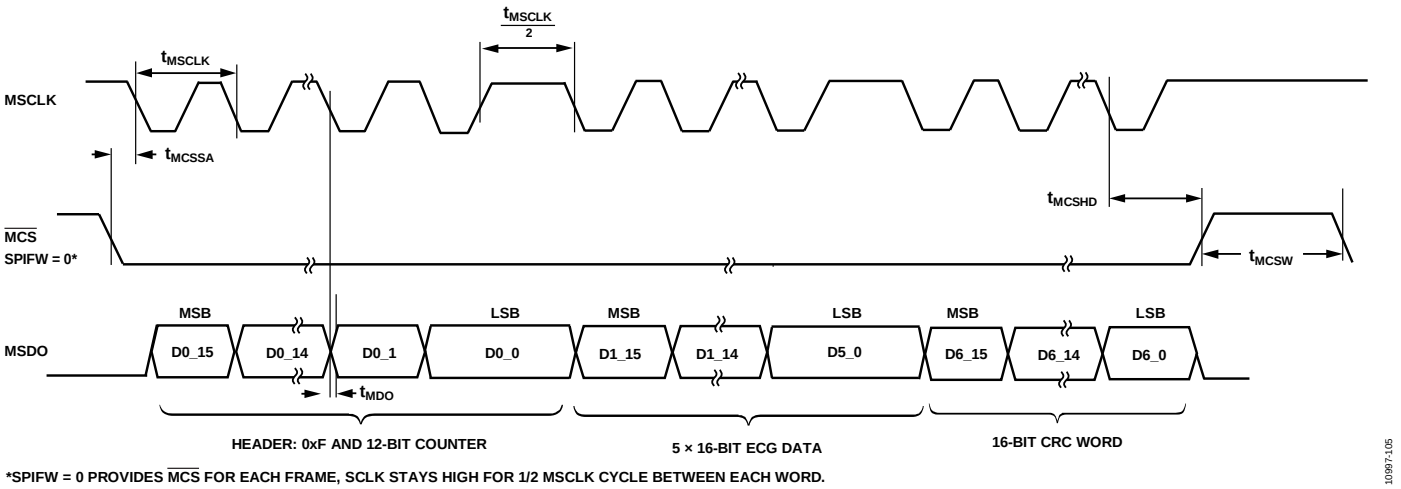
Secondary Serial Interface (Master Interface for Customer-Based Digital Pace Algorithm) ADAS1000-4 Only

AVDD = 3.3 V ± 5%, IOVDD = 1.65 V to 3.6 V, AGND = DGND = 0 V, REFIN tied to REFOUT, externally supplied crystal/clock = 8.192 MHz. T_A = −40°C to +85°C, unless otherwise noted. Typical specifications are mean values at T_A = 25°C. The following timing specifications apply for the master interface when the ECGCTL register is configured for high performance mode (ECGCTL[3] = 1), see Table 28.

Table 6.

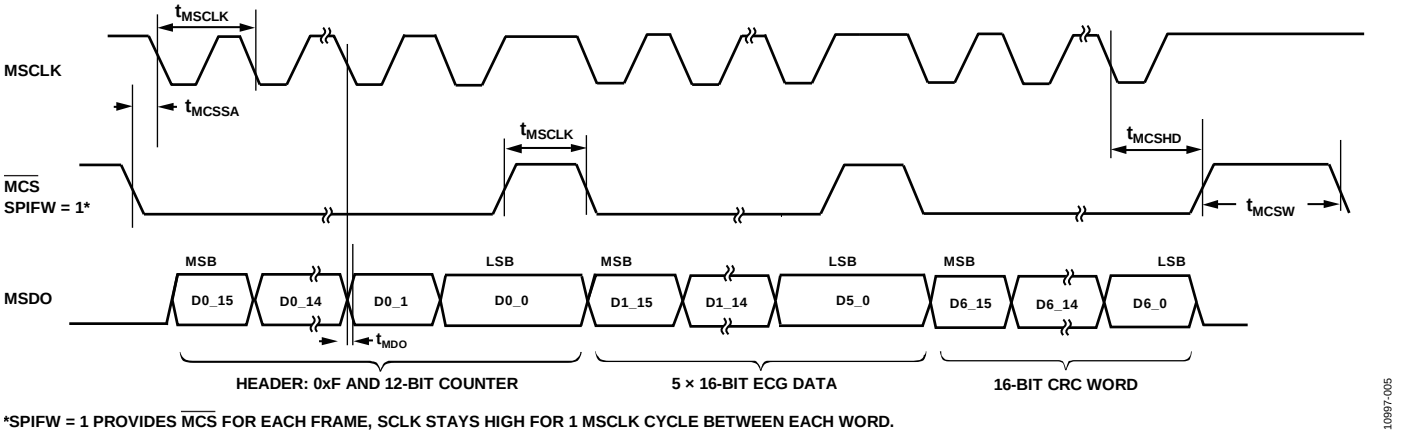
Parameter[1]	Min	Typ	Max	Unit	Description
Output Frame Rate[2]		128		kHz	All five 16-bit ECG data-words are available at frame rate of 128 kHz only
f_{SCLK}[2]		2.5 × crystal frequency		MHz	Crystal frequency = 8.192 MHz
t_{MCSSA}		24.4		ns	$\overline{MCS}$ valid setup time
t_{MDO}		0		ns	MSCLK rising edge to MSDO valid delay
t_{MCSHD}		48.8		ns	$\overline{MCS}$ valid hold time from MSCLK falling edge
t_{MCSW}		2173		ns	$\overline{MCS}$ high time, SPIFW = 0, $\overline{MCS}$ asserted for entire frame as shown in Figure 5, and configured in Table 33
		2026		ns	$\overline{MCS}$ high time, SPIFW = 1, $\overline{MCS}$ asserted for each word in frame as shown in Figure 6 and configured in Table 33

[1] Guaranteed by characterization, not production tested.
[2] Guaranteed by design, not production tested.



*SPIFW = 0 PROVIDES $\overline{MCS}$ FOR EACH FRAME, SCLK STAYS HIGH FOR 1/2 MSCLK CYCLE BETWEEN EACH WORD.

Figure 5. Data Read and Write Timing Diagram for SPIFW = 0, Showing Entire Packet Of Data (Header, 5 ECG Word = [ECG1, ECG2, ECG3 and 2 Words with Zeros], and CRC Word)



*SPIFW = 1 PROVIDES $\overline{MCS}$ FOR EACH FRAME, SCLK STAYS HIGH FOR 1 MSCLK CYCLE BETWEEN EACH WORD.

Figure 6. Data Read and Write Timing Diagram for SPIFW = 1, Showing Entire Packet Of Data (Header, 5 ECG Word = [ECG1, ECG2, ECG3 and 2 Words with Zeros], and CRC Word)

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
AVDD to AGND	−0.3 V to +6 V
IOVDD to DGND	−0.3 V to +6 V
ADCVDD to AGND	−0.3 V to +2.5 V
DVDD to DGND	−0.3 V to +2.5 V
REFIN/REFOUT to REFGND	−0.3 V to +2.1 V
ECG and Analog Inputs to AGND	−0.3 V to AVDD + 0.3 V
Digital Inputs to DGND	−0.3 V to IOVDD + 0.3 V
REFIN to ADCVDD	ADCVDD + 0.3 V
AGND to DGND	−0.3 V to + 0.3 V
REFGND to AGND	−0.3 V to + 0.3 V
ECG Input Continuous Current	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Junction Temperature Range	−40°C to +85°C
Reflow Profile	J-STD-20 (JEDEC)
Junction Temperature	150°C max
ESD	
HBM	2500 V
FICDM	1000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 8. Thermal Resistance[1]

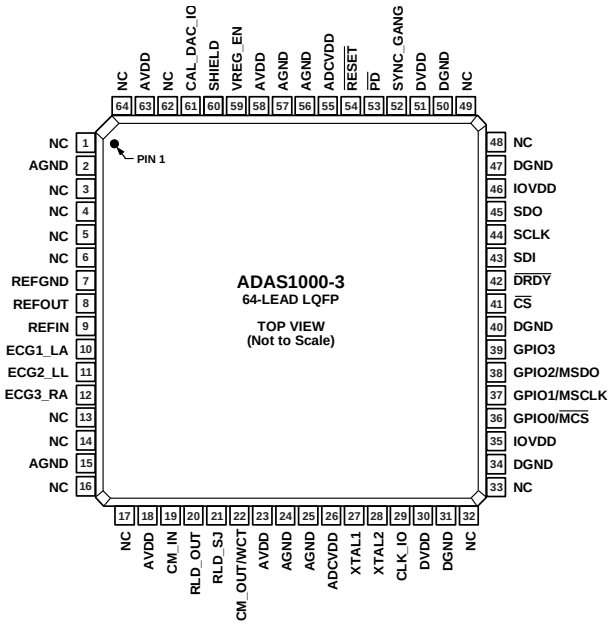
Package Type	θ_{JA}	Unit
56-Lead LFCSP	35	°C/W
64-Lead LQFP	42.5	°C/W

[1] Based on JEDEC standard 4-layer (2S2P) high effective thermal conductivity test board (JESD51-7) and natural convection.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

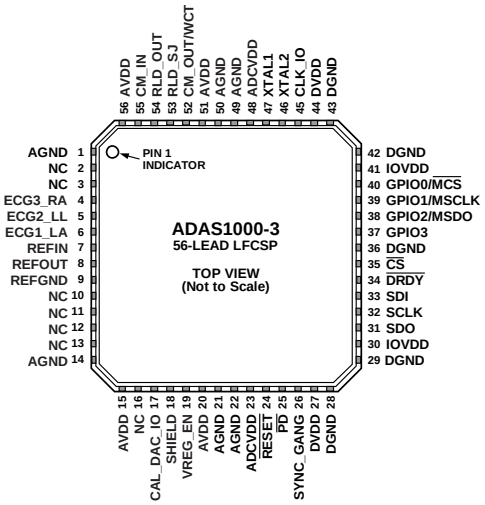
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.

10997-007

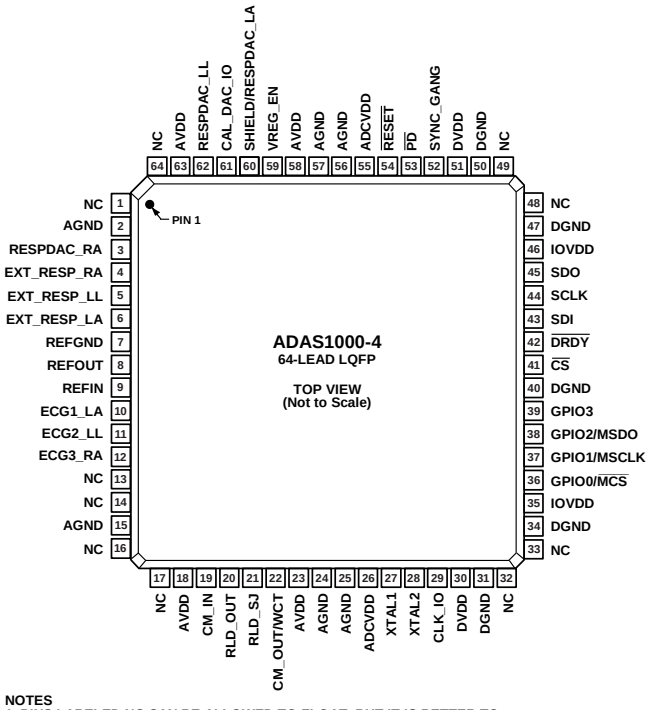
Figure 7. ADAS1000-3, 64-Lead LQFP Pin Configuration



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.
2. THE EXPOSED PAD IS ON THE TOP OF THE PACKAGE; IT IS CONNECTED TO THE MOST NEGATIVE POTENTIAL, AGND.

10997-006

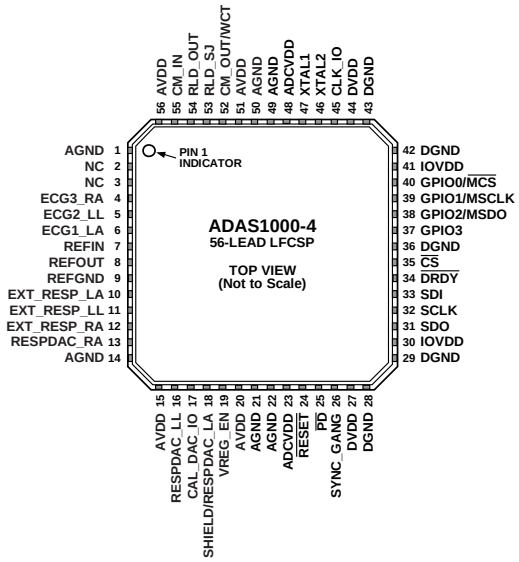
Figure 8. ADAS1000-3, 56-Lead LFCSP Pin Configuration



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.

10997-009

Figure 9. ADAS1000-4, 64-Lead LQFP Pin Configuration



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.
2. THE EXPOSED PAD IS ON THE TOP OF THE PACKAGE; IT IS CONNECTED TO THE MOST NEGATIVE POTENTIAL, AGND.

10997-008

Figure 10. ADAS1000-4, 56-Lead LFCSP Pin Configuration

Table 9. Pin Function Descriptions

ADAS1000-3 Pin No.		ADAS1000-4 Pin No.			
LQFP	**LFCSP**	**LQFP**	**LFCSP**	**Mnemonic**	**Description**
18, 23, 58, 63	15, 20, 51, 56	18, 23, 58, 63	15, 20, 51, 56	AVDD	Analog Supply. See recommendations for bypass capacitors in the Power Supply, Grounding, and Decoupling Strategy section.
35, 46	30, 41	35, 46	30, 41	IOVDD	Digital Supply for Digital Input/Output Voltage Levels. See recommendations for bypass capacitors in the Power Supply, Grounding, and Decoupling Strategy section.
26, 55	23, 48	26, 55	23, 48	ADCVDD	Analog Supply for ADC. There is an on-chip linear regulator providing the supply voltage for the ADCs. These pins are primarily provided for decoupling purposes; however, the pin may also be supplied by an external 1.8 V supply should the user wish to use a more efficient supply to minimize power dissipation. In this case, use the VREG_EN pin tied to ground to disable the ADCVDD and DVDD regulators. The ADCVDD pin should not be used to supply other functions. See recommendations for bypass capacitors in the Power Supply, Grounding, and Decoupling Strategy section.
30, 51	27, 44	30, 51	27, 44	DVDD	Digital Supply. There is an on-chip linear regulator providing the supply voltage for the digital core. These pins are primarily provided for decoupling purposes; however, the pin may also be overdriven supplied by an external 1.8 V supply should the user wish to use a more efficient supply to minimize power dissipation. In this case, use the VREG_EN pin tied to ground to disable the ADCVDD and DVDD regulators. See recommendations for bypass capacitors in the Power Supply, Grounding, and Decoupling Strategy section.
2, 15, 24, 25, 56, 57	1, 14, 21, 22, 49, 50	2, 15, 24, 25, 56, 57	1, 14, 21, 22, 49, 50	AGND	Analog Ground.
31, 34, 40, 47, 50	28, 29, 36, 42, 43	31, 34, 40, 47, 50	28, 29, 36, 42, 43	DGND	Digital Ground.
59	19	59	19	VREG_EN	Enables or disables the internal voltage regulators used for ADCVDD and DVDD. Tie this pin to AVDD to enable or tie this pin to ground to disable the internal voltage regulators.
10	6	10	6	ECG1_LA	Analog Input, Left Arm (LA).
11	5	11	5	ECG2_LL	Analog Input, Left Leg (LL).
12	4	12	4	ECG3_RA	Analog Input, Right Arm (RA).
		4	12	EXT_RESP_RA	Optional External Respiration Input.
		5	11	EXT_RESP_LL	Optional External Respiration Input.
		6	10	EXT_RESP_LA	Optional External Respiration Input.
		62	16	RESPDAC_LL	Optional Path for Higher Performance Respiration Resolution, Respiration DAC Drive, Negative Side 0.
		60	18	SHIELD/ RESPDAC_LA	Shared Pin (User-Configured). Output of Shield Driver (SHIELD). Optional Path for Higher Performance Respiration Resolution, Respiration DAC Drive, Negative Side 1 (RESPDAC_LA).
60	18			SHIELD	Output of Shield Driver.
		3	13	RESPDAC_RA	Optional Path for Higher Performance Respiration Resolution, Respiration DAC Drive, Positive Side.
22	52	22	52	CM_OUT/WCT	Common-Mode Output Voltage (Average of Selected Electrodes). Not intended to drive current.
19	55	19	55	CM_IN	Common-Mode Input.
21	53	21	53	RLD_SJ	Summing Junction for Right Leg Drive Amplifier.
20	54	20	54	RLD_OUT	Output and Feedback Junction for Right Leg Drive Amplifier.
61	17	61	17	CAL_DAC_IO	Calibration DAC Input/Output. Output for a master device, input for a slave. Not intended to drive current.
9	7	9	7	REFIN	Reference Input. For standalone mode, use REFOUT connected to REFIN. External 10 µF capacitors with ESR < 0.2 Ω in parallel with 0.1 µF bypass capacitors to GND are required and should be placed as close to the pin as possible. An external reference can be connected to REFIN.
8	8	8	8	REFOUT	Reference Output.
7	9	7	9	REFGND	Reference Ground. Connect to a clean ground.
27, 28	47, 46	27, 28	47, 46	XTAL1, XTAL2	External crystal connects between these two pins; external clock drive should be applied to CLK_IO. Each XTAL pin requires a 15 pF capacitor to ground.
29	45	29	45	CLK_IO	Buffered Clock Input/Output. Output for a master device; input for a slave. Powers up in high impedance.
41	35	41	35	$\overline{CS}$	Chip Select and Frame Sync, Active Low. $\overline{CS}$ can be used to frame each word or to frame the entire suite of data in framing mode.

ADAS1000-3 Pin No.		ADAS1000-4 Pin No.			
LQFP	**LFCSP**	**LQFP**	**LFCSP**	**Mnemonic**	**Description**
44	32	44	32	SCLK	Clock Input. Data is clocked into the shift register on a rising edge and clocked out on a falling edge.
43	33	43	33	SDI	Serial Data Input.
53	25	53	25	$\overline{PD}$	Power-Down, Active Low.
45	31	45	31	SDO	Serial Data Output. This pin is used for reading back register configuration data and for the data frames.
42	34	42	34	$\overline{DRDY}$	Digital Output. This pin indicates that conversion data is ready to be read back when low, busy when high. When reading packet data, the entire packet must be read to allow $\overline{DRDY}$ to return high.
54	24	54	24	$\overline{RESET}$	Digital Input. This pin has an internal pull-up resistor. This pin resets all internal nodes to their power-on reset values.
52	26	52	26	SYNC_GANG	Digital Input/Output (Output on Master, Input on Slave). Used for synchronization control where multiple devices are connected together. Powers up in high impedance.
36	40	36	40	GPIO0/$\overline{MCS}$	General-Purpose I/O or Master 128 kHz SPI $\overline{CS}$.
37	39	37	39	GPIO1/MSCLK	General-Purpose I/O or Master 128 kHz SPI SCLK.
38	38	38	38	GPIO2/MSDO	General-Purpose I/O or Master 128 kHz SPI SDO.
39	37	39	37	GPIO3	General-Purpose I/O.
1, 3, 4, 5, 6, 13, 14, 16, 17, 32, 33, 48, 49, 62, 64	2, 3, 10, 11, 12, 13, 16	1, 13, 14, 16, 17, 32, 33, 48, 49, 64	2, 3	NC	No connect. Do not connect to these pins (see Figure 7, Figure 8, Figure 9, and Figure 10).
	57		57	EPAD	Exposed Pad. The exposed pad is on the top of the package; it is connected to the most negative potential, AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

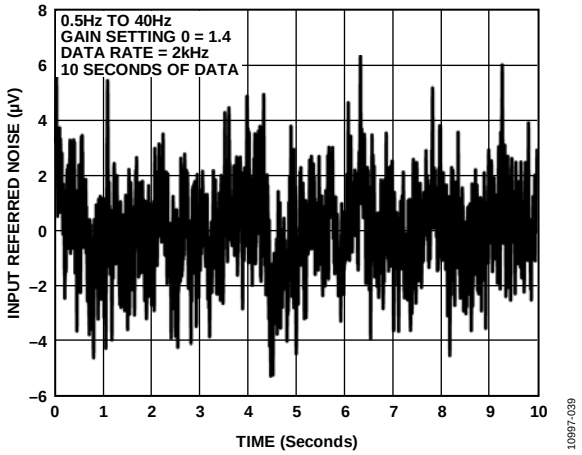


Figure 11. Input Referred Noise for 0.5 Hz to 40 Hz Bandwidth, 2 kHz Data Rate, GAIN 0 (1.4)

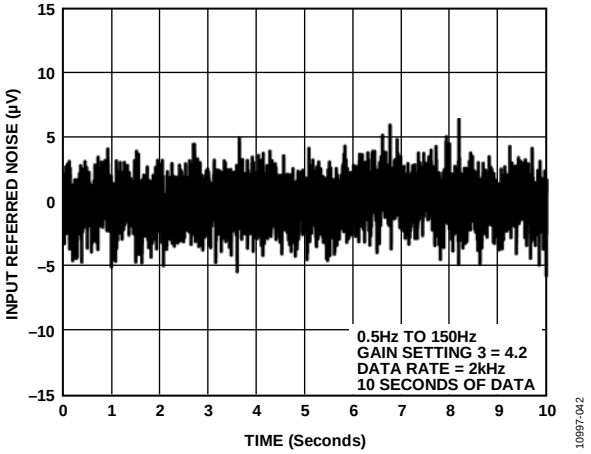


Figure 14. Input Referred Noise for 0.5 Hz to 150 Hz Bandwidth, 2 kHz Data Rate, GAIN 3 (4.2)

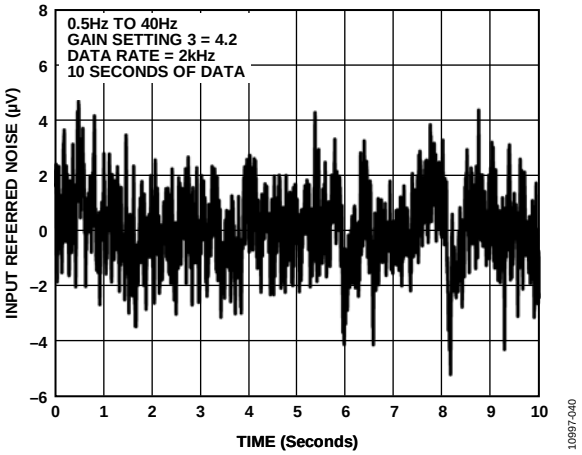


Figure 12. Input Referred Noise for 0.5 Hz to 40 Hz Bandwidth, 2 kHz Data Rate, GAIN 3 (4.2)

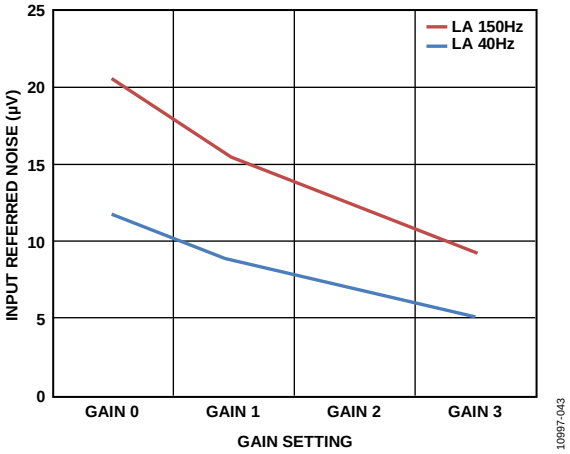


Figure 15. ECG Channel Noise Performance over a 0.5 Hz to 40 Hz or 0.5 Hz to 150 Hz Bandwidth vs. Gain Setting

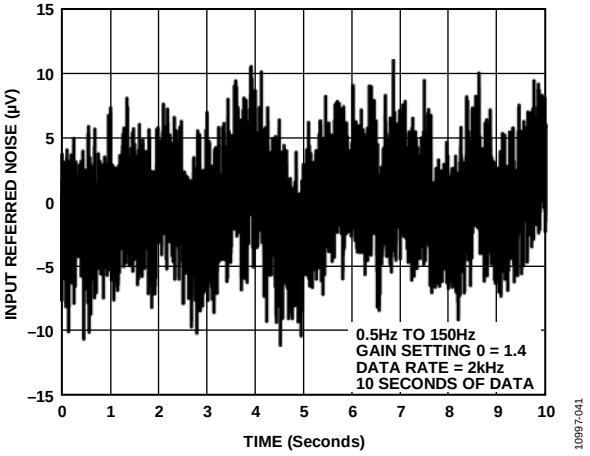


Figure 13. Input Referred Noise for 0.5 Hz to 150 Hz Bandwidth, 2 kHz Data Rate, GAIN 0 (1.4)

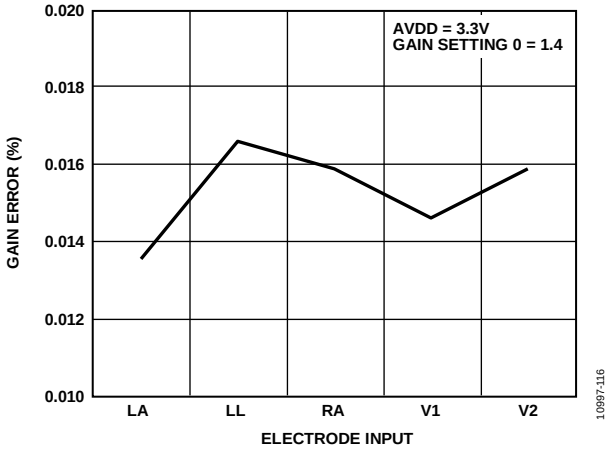


Figure 16. Typical Gain Error Across Channels

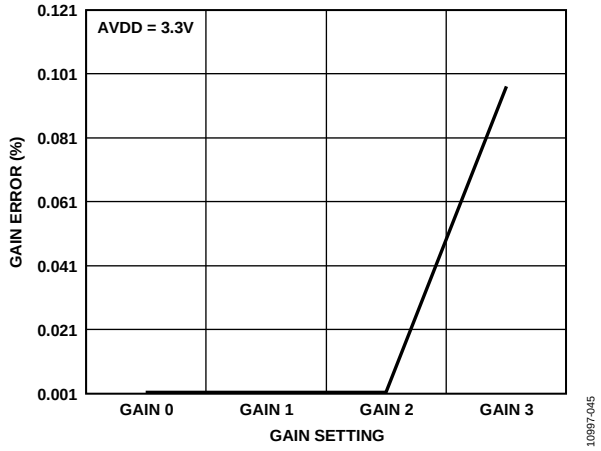


Figure 17. Typical Gain Error vs. Gain

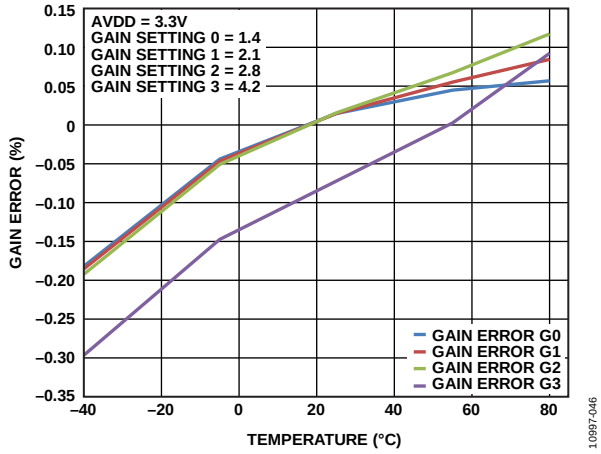


Figure 18. Typical Gain Error for All Gain Settings Across Temperature

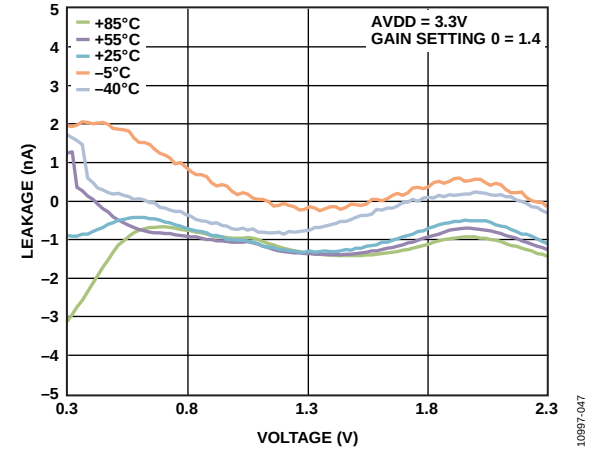


Figure 19. Typical ECG Channel Leakage Current over Input Voltage Range vs. Temperature

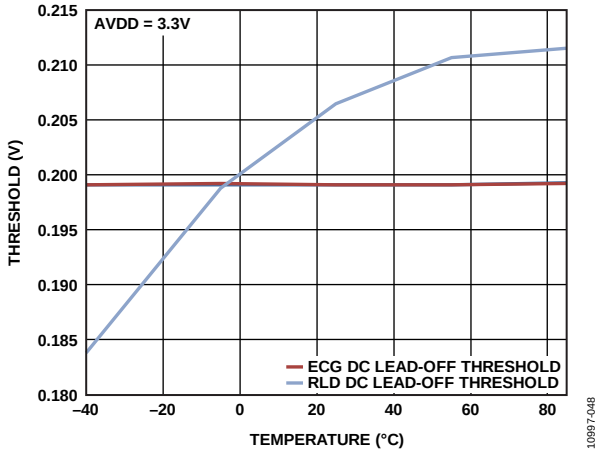


Figure 20. DC Lead-Off Comparator Low Threshold vs. Temperature

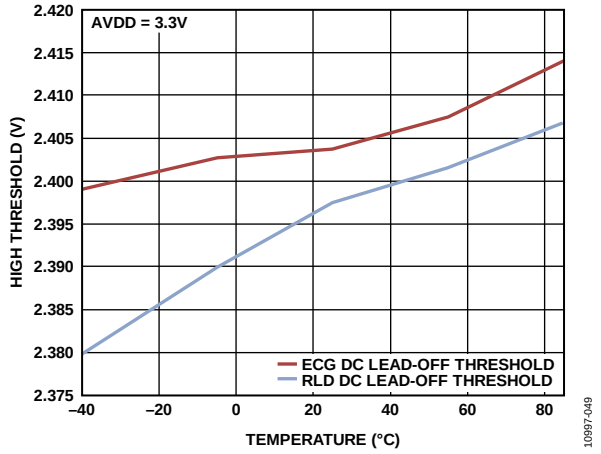


Figure 21. DC Lead-Off Comparator High Threshold vs. Temperature

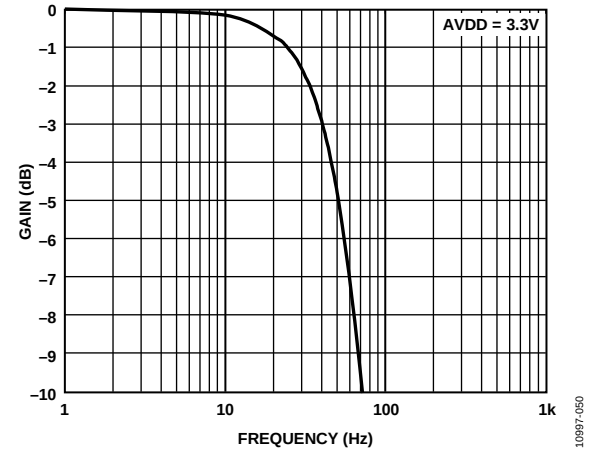


Figure 22. Filter Response with 40 Hz Filter Enabled, 2 kHz Data Rate; See Figure 72 for Digital Filter Overview

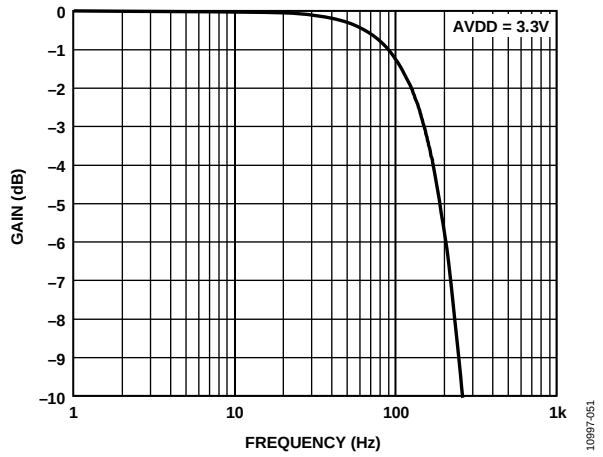


Figure 23. Filter Response with 150 Hz Filter Enabled, 2 kHz Data Rate; See Figure 72 for Digital Filter Overview

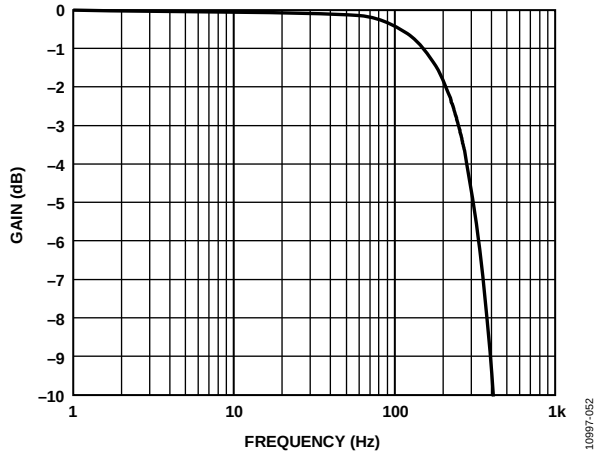


Figure 24. Filter Response with 250 Hz Filter Enabled, 2 kHz Data Rate; See Figure 72 for Digital Filter Overview

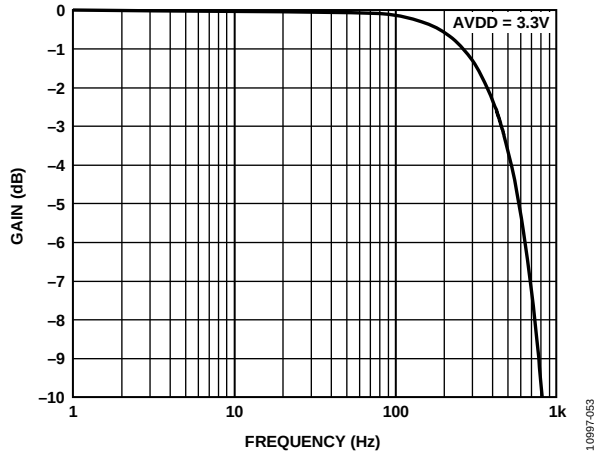


Figure 25. Filter Response with 450 Hz Filter Enabled, 2 kHz Data Rate; See Figure 72 for Digital Filter Overview

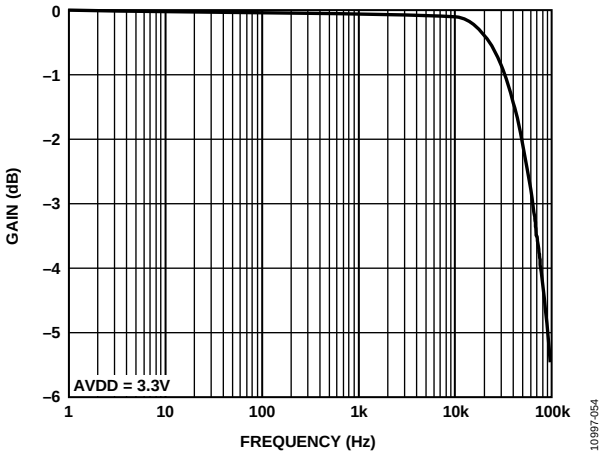


Figure 26. Analog Channel Bandwidth

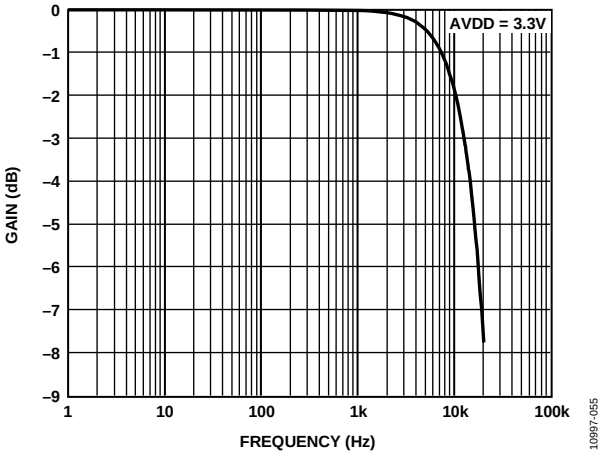


Figure 27. Filter Response Running at 128 kHz Data Rate; See Figure 72 for Digital Filter Overview

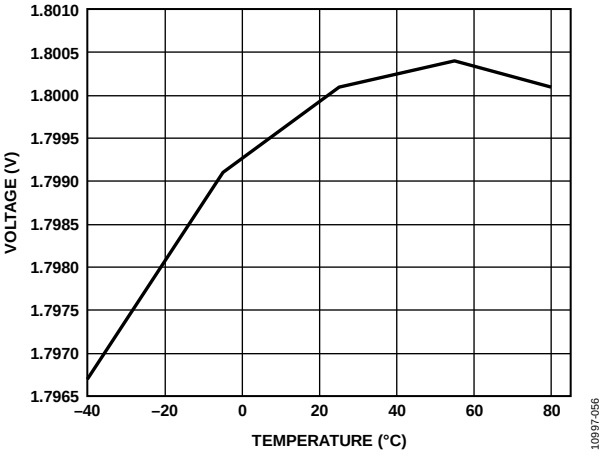


Figure 28. Typical Internal VREF vs. Temperature

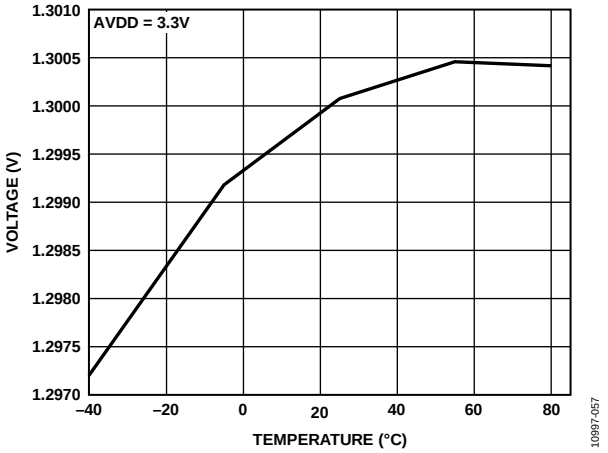


Figure 29. VCM_REF vs. Temperature

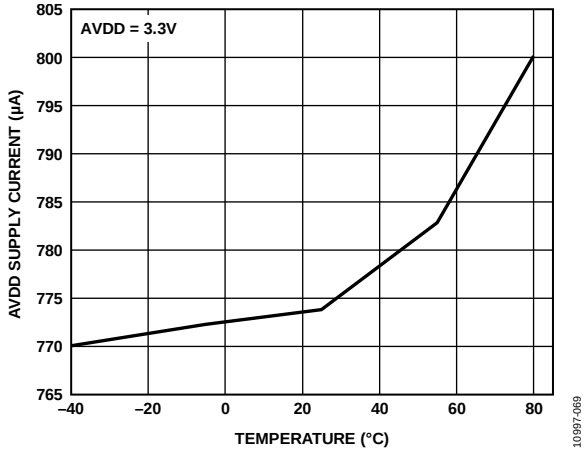


Figure 32. Typical AVDD Supply Current vs. Temperature in Standby Mode

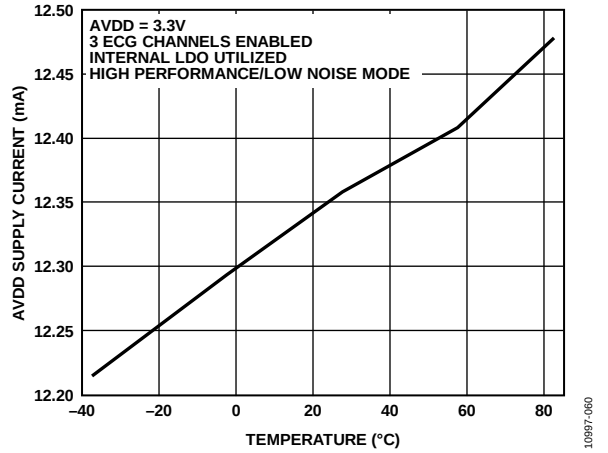


Figure 30. Typical AVDD Supply Current vs. Temperature, Using Internal ADVCDD/DVDD Supplies

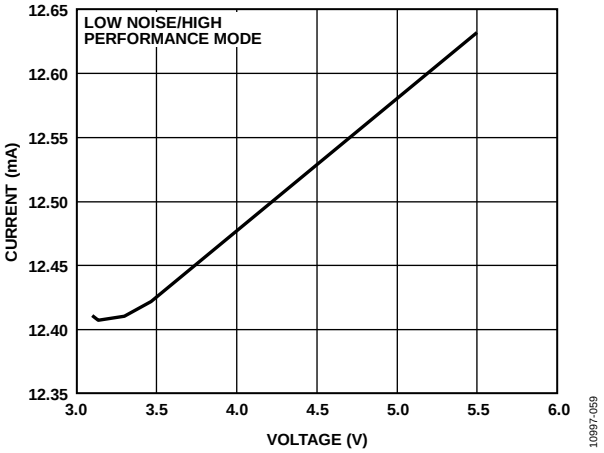


Figure 33. Typical AVDD Supply Current vs. AVDD Supply Voltage

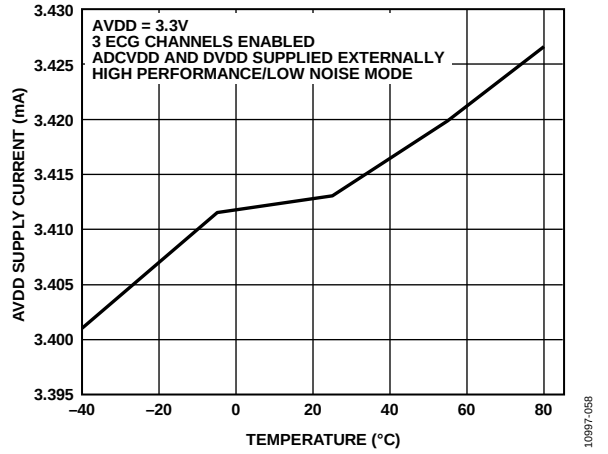


Figure 31. Typical AVDD Supply Current vs. Temperature, Using Externally Supplied ADVCDD/DVDD

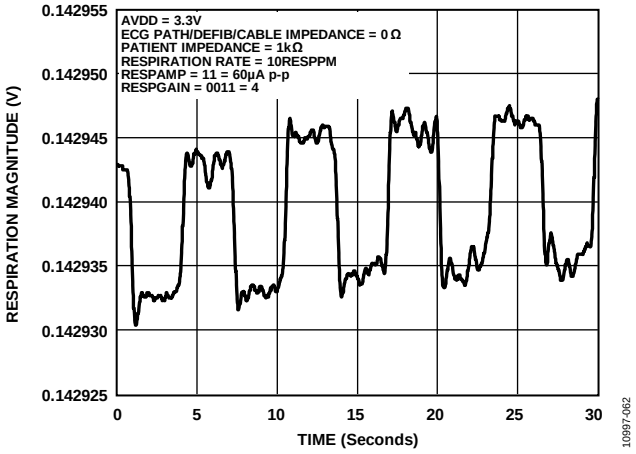


Figure 34. Respiration with 200 mΩ Impedance Variation, Using Internal Respiration Paths and Measured with a 0 Ω Patient Cable

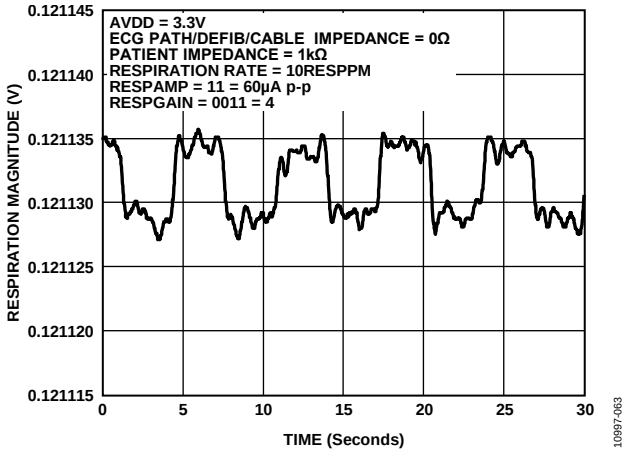


Figure 35. Respiration with 100 mΩ Impedance Variation, Using Internal Respiration Paths and Measured with a 0 Ω Patient Cable

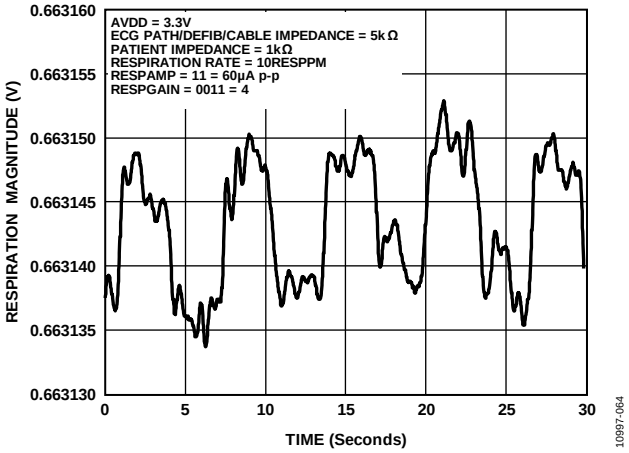


Figure 36. Respiration with 200 mΩ Impedance Variation, Using Internal Respiration Paths and Measured with a 5 kΩ Patient Cable

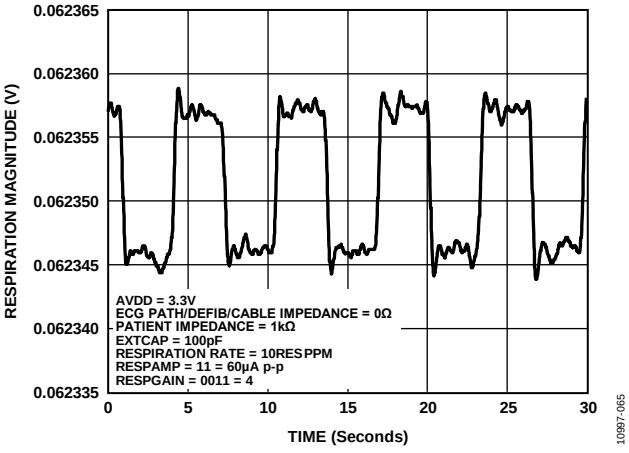


Figure 37. Respiration with 200 mΩ Impedance Variation, Using External Respiration DAC Driving a 100 pF External Capacitor and Measured with a 0 Ω Patient Cable

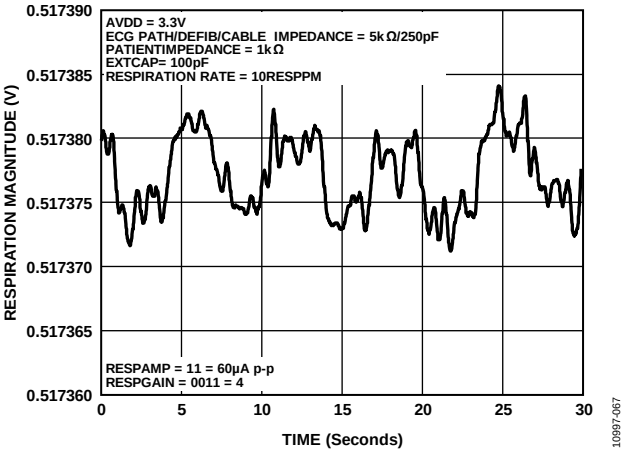


Figure 38. Respiration with 200 mΩ Impedance Variation, Using External Respiration DAC Driving a 100 pF External Capacitor and Measured with a 5 kΩ Patient Cable

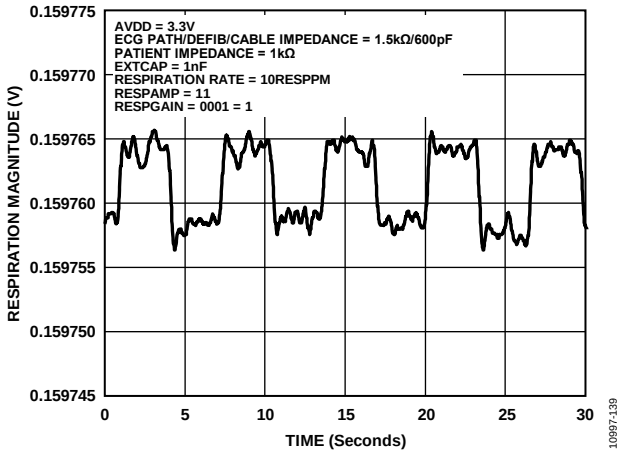


Figure 39. Respiration with 200 mΩ Impedance Variation, Using External Respiration DAC Driving a 1 nF External Capacitor and Measured with a 1.5 kΩ Patient Cable

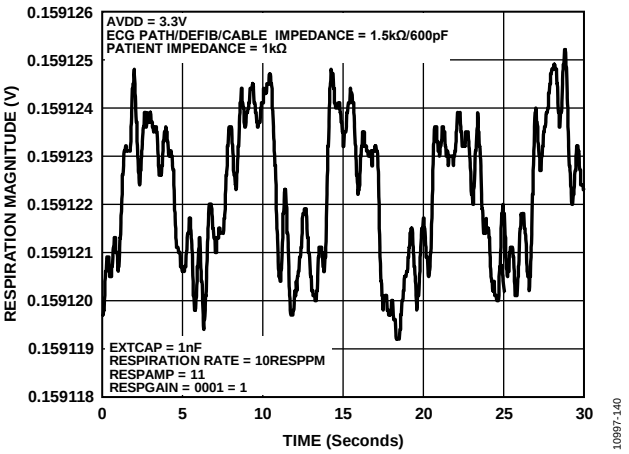


Figure 40. Respiration with 100 mΩ Impedance Variation, Using an External Respiration DAC Driving a 1 nF External Capacitor and Measured with a 1.5 kΩ Patient Cable

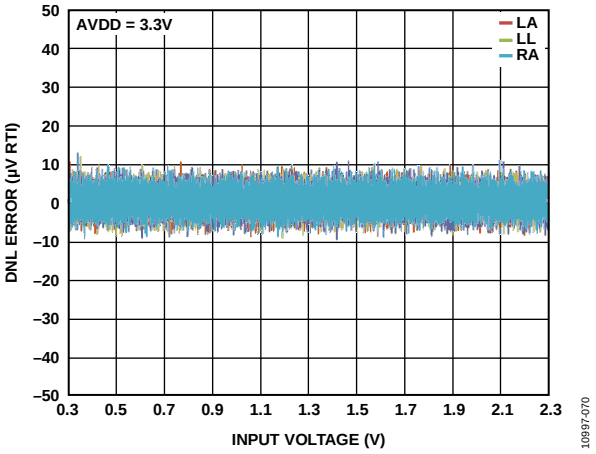


Figure 41. DNL Error vs. Input Voltage Range Across Electrodes at 25°C

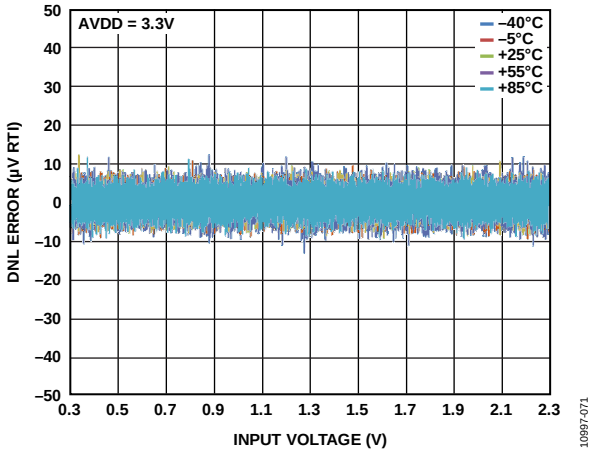


Figure 42. DNL Error vs. Input Voltage Range Across Temperature

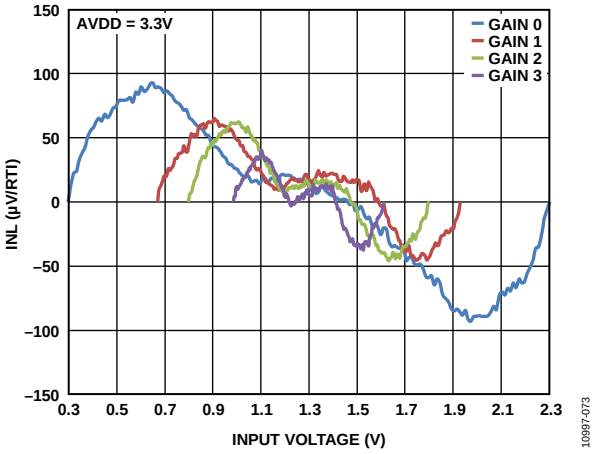


Figure 43. INL vs. Input Voltage Across Gain Setting for 2 kHz Data Rate

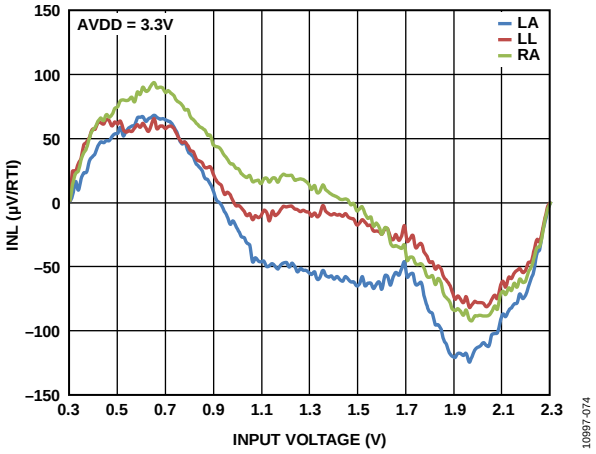


Figure 44. INL vs. Input Voltage Across Electrode Channel for 2 kHz Data Rate

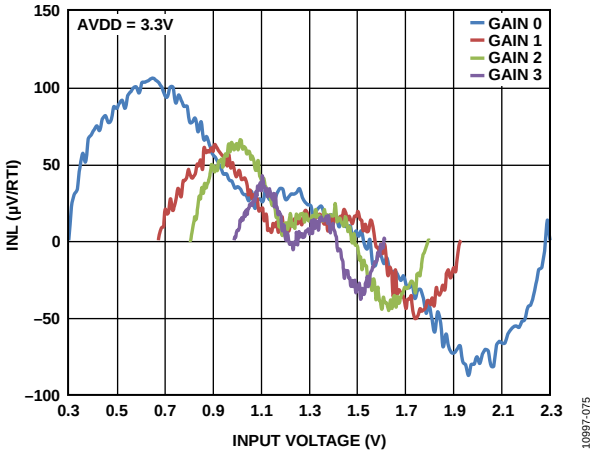


Figure 45. INL vs. Input Voltage Across Gain Setting for 16 kHz Data Rate

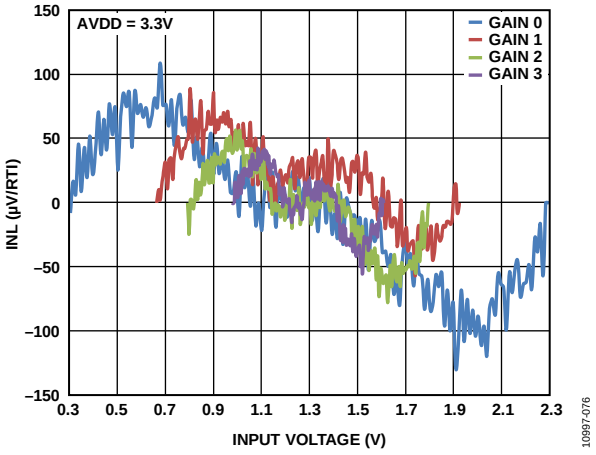


Figure 46. INL vs. Input Voltage Across Gain Setting for 128 kHz Data Rate

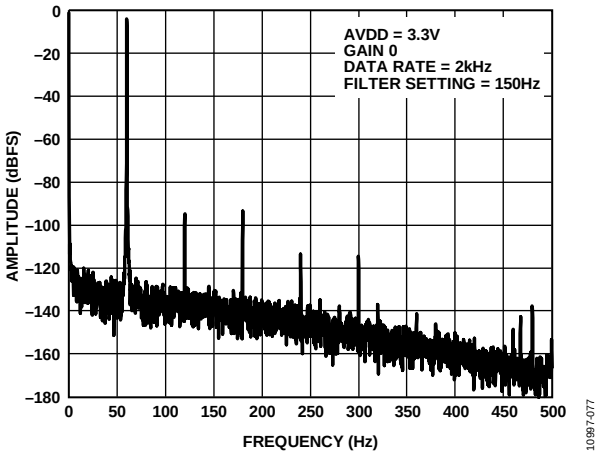


Figure 47. FFT with 60 Hz Input Signal

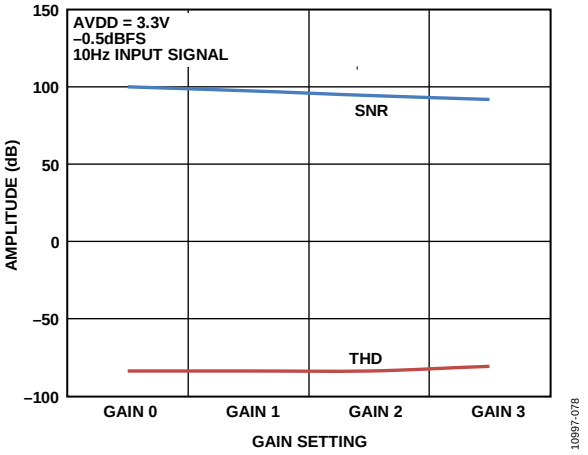


Figure 48. SNR and THD Across Gain Settings

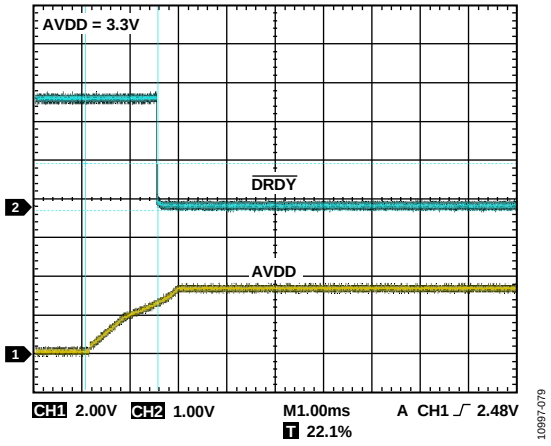


Figure 49. Power Up AVDD Line to $\overline{DRDY}$ Going Low (Ready)

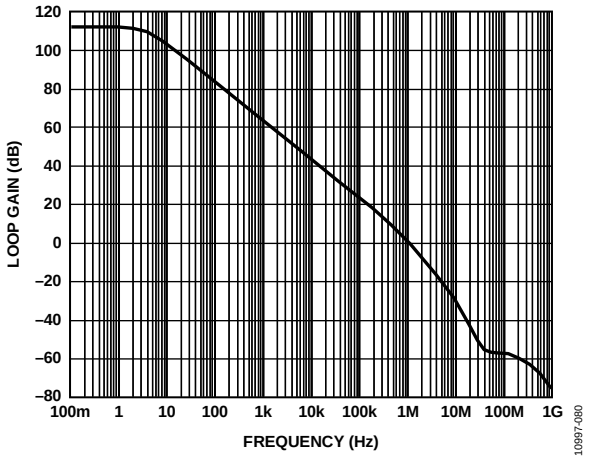


Figure 50. Open-Loop Gain Response of Right Leg Drive Amplifier Without Loading

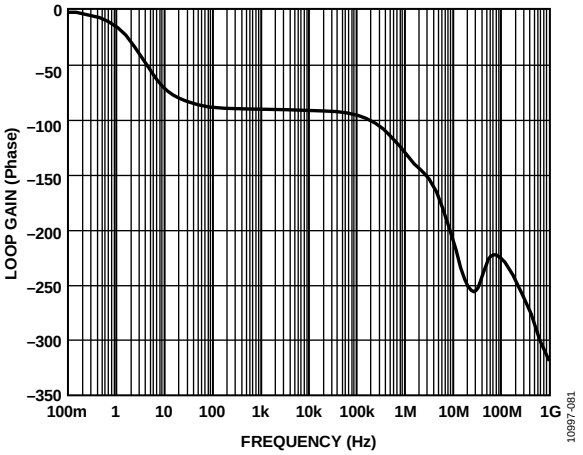


Figure 51. Open-Loop Phase Response of Right Leg Drive Amplifier Without Loading

APPLICATIONS INFORMATION

OVERVIEW

The ADAS1000-3/ADAS1000-4 are electro cardiac (ECG) front-end solutions targeted at a variety of medical applications. In addition to ECG measurements, the ADAS1000-3/ADAS1000-4 also measure thoracic impedance (respiration) and detect pacing artifacts, providing all the measured information to the host controller in the form of a data frame supplying either lead/vector or electrode data at programmable data rates. The ADAS1000-3/ADAS1000-4 are designed to simplify the task of acquiring ECG signals for use in both monitor and diagnostic applications. Value-added cardiac post processing may be executed externally on a DSP, microprocessor, or FPGA. The ADAS1000-3/ADAS1000-4 are designed for operation in both low power, portable telemetry applications and line powered systems; therefore, the parts offer power/noise scaling to ensure suitability to these varying requirements.

The devices also offer a suite of dc and ac test excitation via a calibration DAC feature and CRC redundancy checks in addition to readback of all relevant register address space.

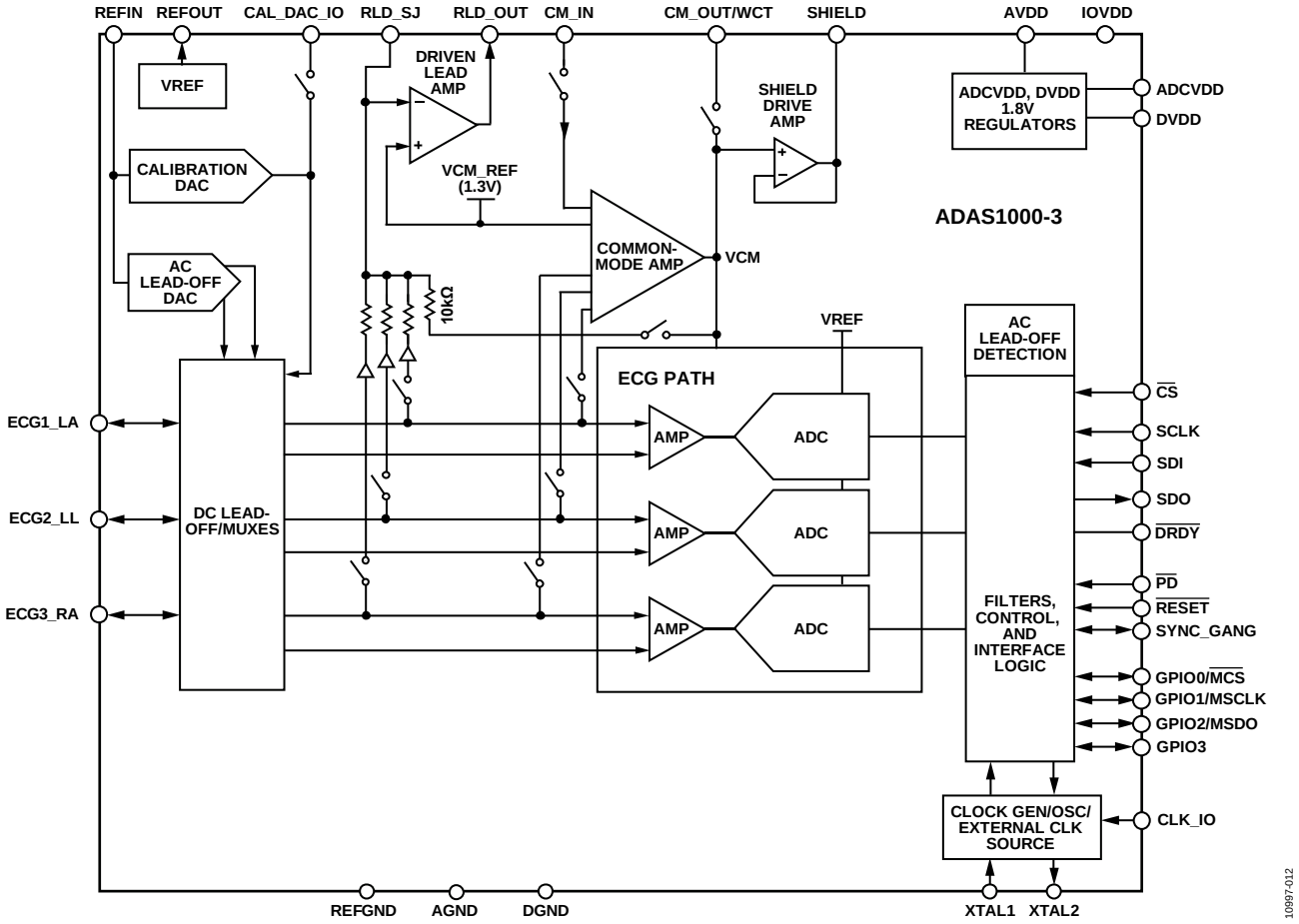


Figure 52. ADAS1000-3 Simplified Block Diagram

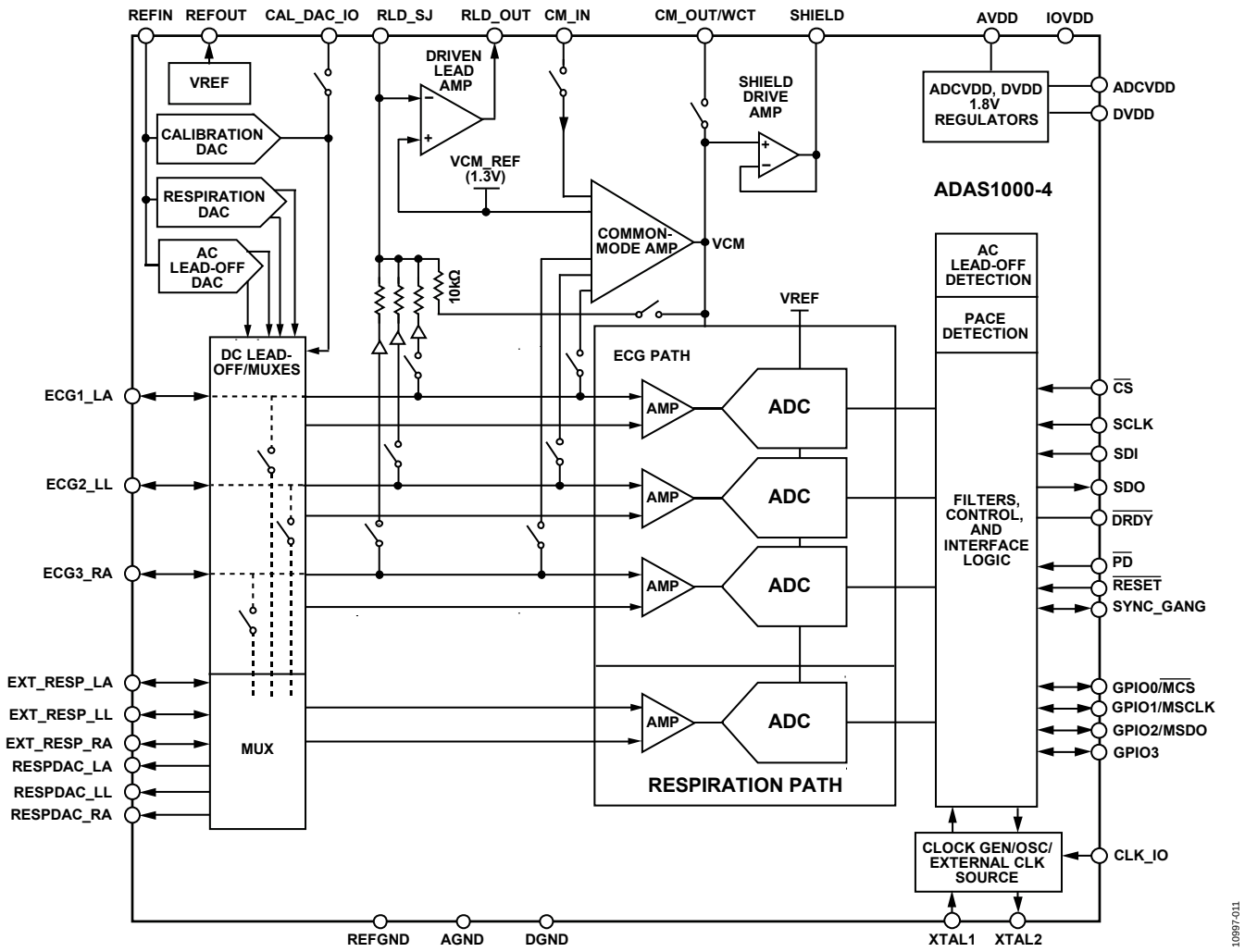


Figure 53. ADAS1000-4 Simplified Block Diagram

ECG INPUTS—ELECTRODES/LEADS

The ADAS1000-3/ADAS1000-4 ECG product consists of three ECG inputs and a reference drive, RLD (right leg drive). In a typical 3-lead/vector application, three of the ECG inputs (ECG3_RA, ECG1_LA, ECG2_LL) are used in addition to the RLD path.

In a 3-lead system, the ADAS1000-3/ADAS1000-4 can be arranged to provide Lead I, Lead II, and Lead III data or electrode data directly via the serial interface at all frame rates. Note that in 128 kHz data rate, lead data is only available when configured in analog lead mode. Digital lead mode is not available for this data rate.

Should the user have a need for increased electrode counts, then there are other products within the ADAS1000 family that may be suitable. For example, a derived 12-lead (8-electrode) system can be achieved using one ADAS1000-3 or ADAS1000-4 device ganged together with one ADAS1000-2 slave device as described in the Gang Mode Operation section. Similarly, a 12-lead (10-electrode) system can be achieved using one ADAS1000 or ADAS1000-1 device ganged together with one ADAS1000-2 slave device as described in the Gang Mode Operation section. Here, nine ECG electrodes and one RLD electrode achieve the 10 electrode system, again leaving one spare ECG channel that could be used for alternate purposes as suggested previously. In such a system, having nine dedicated electrodes benefits the user by delivering lead information based on electrode measurements and calculations rather than deriving leads from other lead measurements.

Table 10 outlines the calculation of the leads (vector) from the individual electrode measurements when using either the ADAS1000-3 or ADAS1000-4.

Table 10. Lead Composition

Device	Lead Name	Composition	Equivalent
ADAS1000-3 or ADAS1000-4	I	LA – RA	
	II	LL – RA	
	III	LL – LA	
	aVR[1]	RA – 0.5 × (LA + LL)	−0.5 × (I + II)
	aVL[1]	LA – 0.5 × (LL + RA)	0.5 × (I − III)
	aVF[1]	LL – 0.5 × (LA + RA)	0.5 × (II + III)

[1] These augmented leads are not calculated within the ADAS1000-3/ADAS1000-4, but can be derived in the host DSP/microcontroller/FPGA.

ECG CHANNEL

The ECG channel consists of a programmable gain, low noise, differential preamplifier; a fixed gain anti-aliasing filter; buffers; and an ADC (see Figure 54). Each electrode input is routed to its PGA noninverting input. Internal switches allow the PGA's inverting inputs to be connected to other electrodes and/or the Wilson Central Terminal to provide differential analog processing (analog lead mode), to a computed average of some or all electrodes, or to the internal 1.3 V common-mode reference (VCM_REF). The latter two modes support digital lead mode (leads computed on-chip) and electrode mode (leads calculated off-chip). In all cases, the internal reference level is removed from the final lead data.

The ADAS1000-3/ADAS1000-4 implementation uses a dc-coupled approach, which requires that the front end be biased to operate within the limited dynamic range imposed by the relatively low supply voltage. The right leg drive loop performs this function by forcing the electrical average of all selected electrodes to the internal 1.3 V level, VCM_REF, maximizing each channel's available signal range.

All ECG channel amplifiers use chopping to minimize 1/f noise contributions in the ECG band. The chopping frequency of ~250 kHz is well above the bandwidth of any signals of interest. The 2-pole anti-aliasing filter has ~65 kHz bandwidth to support digital pace detection while still providing greater than 80 dB of attenuation at the ADC's sample rate. The ADC is a 14-bit, 2 MHz SAR converter; 1024 × oversampling helps achieve the required system performance. The ADC's full-scale input range is 2 × VREF, or 3.6 V, although the analog portion of the ECG channel limits the useful signal swing to about 2.8 V. The ADAS1000 contains flags to indicate whether the ADC data is out of range, indicating a hard electrode off state. Programmable overrange and underrange thresholds are shown in the LOFFUTH and LOFFLTH registers (see Table 39 and Table 40, respectively). The ADC out of range flag is contained in the header word (see Table 53).

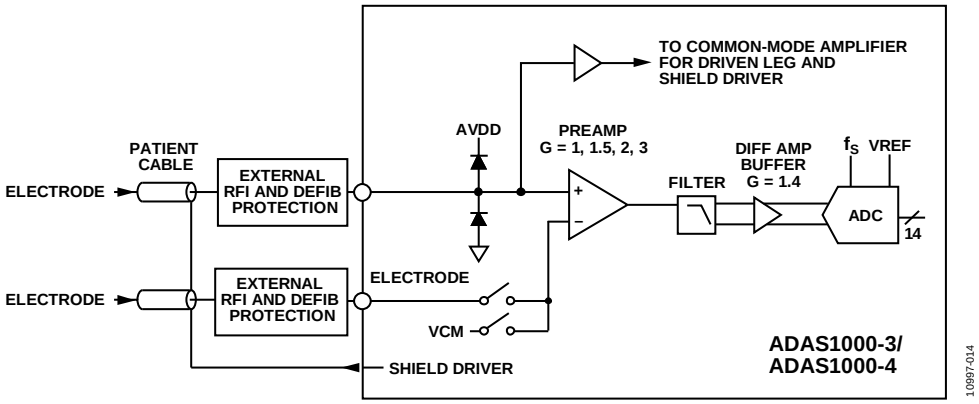


Figure 54. Simplified Schematic of a Single ECG Channel

ELECTRODE/LEAD FORMATION AND INPUT STAGE CONFIGURATION

The input stage of the ADAS1000-3/ADAS1000-4 can be arranged in several different manners. The input amplifiers are differential amplifiers and can be configured to generate the leads in the analog domain, before the ADCs. In addition to this, the digital data can be configured to provide either electrode or lead format under user control as described in Table 37. This allows maximum flexibility of the input stage for a variety of applications.

Analog Lead Mode and Calculation

Leads are configured in the analog input stage when CHCONFIG = 1, as shown in Figure 56. This uses a traditional in-amp structure where lead formation is performed prior to digitization, with WCT created using the common-mode amplifier. While this results in the inversion of Lead II in the analog domain, this is digitally corrected so output data have the proper polarity.

Digital Lead Mode and Calculation

When the ADAS1000-3/ADAS1000-4 are configured for digital lead mode (see the FRMCTL register, 0x0A[4], Table 37), the digital core will calculate each lead from the electrode signals. This is straightforward for Lead I/ Lead II/Lead III. Calculating V1' and V2' requires WCT, which is also computed internally for this purpose. This mode ignores the common-mode configuration specified in the CMREFCTL register (Register 0x05). Digital lead calculation is only available in 2 kHz and 16 kHz data rates (see Figure 57).

Electrode Mode: Single-Ended Input Electrode Configuration

In this mode, the electrode data are digitized relative to the common-mode signal, VCM, which can be arranged to be any combination of the contributing ECG electrodes. Common-mode generation is controlled by the CMREFCTL register as described in Table 32 (see Figure 59).

Electrode Mode: Common Electrode A and Common Electrode B Configurations

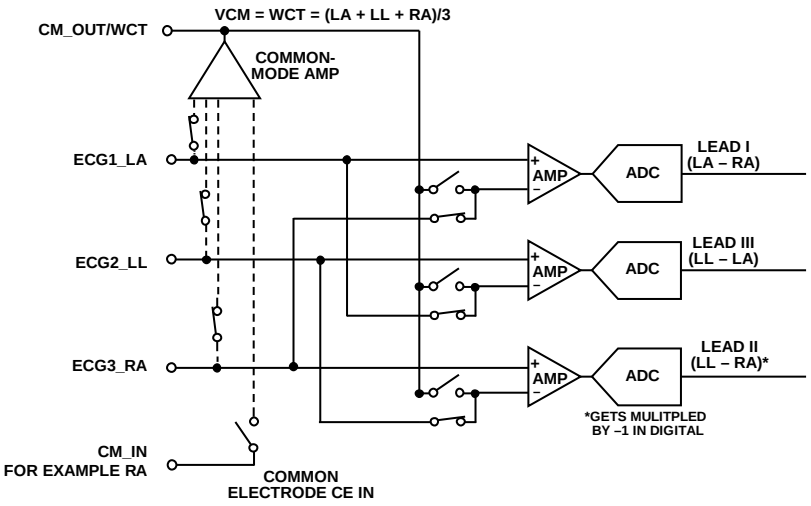
In this mode, all electrodes are digitized relative to a common electrode (CE), for example, RA. Standard leads must be calculated by post processing the output data of the ADAS1000/ ADAS1000-1/ADAS1000-2 (see Figure 58 and Figure 60).

MODE	COMMENT	WORD1	WORD2	WORD3	0x0A [4][1]	0x01 [10][2]	0x05 [8][3]
ANALOG LEAD	ANALOG LEAD	LEAD I (LA − RA)	LEAD II (LL − RA)	LEAD III (LL − LA)	0	1	0
DIGITAL LEAD	SINGLE-ENDED INPUT, DIGITALLY CALCULATED LEADS	LEAD I (LA − RA)	LEAD II (LL − RA)	LEAD III (LL − LA)	0	0	0
COMMON ELECTRODE A	COMMON ELECTRODE (CE) LEADS (HERE RA ELECTRODE IS CONNECTED TO THE CE ELECTRODE (CM_IN) AND V1 IS ON ECG3 INPUT)	LEAD I (LA − RA)	LEAD II (LL − RA)	V1' $\frac{(V1 - RA) - (LA - RA) - (LL - RA)}{3}$	0	0	1
SINGLE-ENDED INPUT ELECTRODE	SINGLE-ENDED INPUT ELECTRODE RELATIVE TO VCM	LA − VCM	LL − VCM	RA − VCM	1	0	0
COMMON ELECTRODE B	LEADS FORMED RELATIVE TO A COMMON ELECTRODE (CE)	LA − CE	LL − CE	V1 − CE	1	0	1

[1]REGISTER FRMCTL, BIT DATAFMT: 0 = LEAD/VECTOR MODE; 1 = ELECTRODE MODE.
[2]REGISTER ECGCTL, BIT CHCONFIG: 0 = SINGLE ENDED INPUT (DIGITAL LEAD MODE OR ELECTRODE MODE); 1 = DIFFERENTIAL INPUT (ANALOG LEAD MODE).
[3]REGISTER CMREFCTL, BIT CEREFEN: 0 = CE DISABLED; 1 = CE ENABLED.

10997-155

Figure 55. Electrode and Lead Configurations

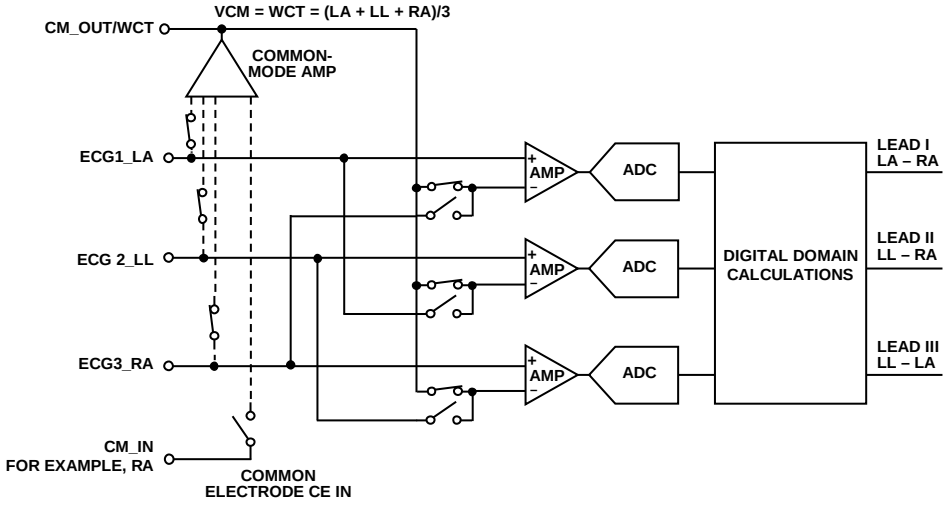


MODE	COMMENT	WORD1	WORD2	WORD3	0x0A [4][1]	0x01 [10][2]	0x05 [8][3]
ANALOG LEAD	ANALOG LEAD	LEAD I (LA − RA)	LEAD II (LL − RA)	LEAD III (LL − LA)	0	1	0

[1]REGISTER FRMCTL, BIT DATAFMT: 0 = LEAD/VECTOR MODE; 1 = ELECTRODE MODE.
[2]REGISTER ECGCTL, BIT CHCONFIG: 0 = SINGLE ENDED INPUT (DIGITAL LEAD MODE OR ELECTRODE MODE); 1 = DIFFERENTIAL INPUT (ANALOG LEAD MODE).
[3]REGISTER CMREFCTL, BIT CEREFEN: 0 = CE DISABLED; 1 = CE ENABLED.

10997-156

Figure 56. Electrode and Lead Configurations, Analog Lead Mode

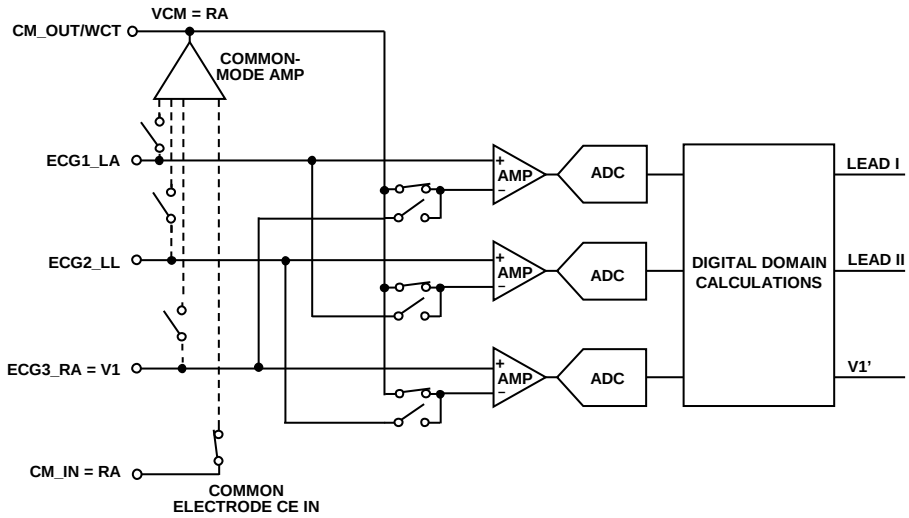


MODE	COMMENT	WORD1	WORD2	WORD3	0x0A [4][1]	0x01 [10][2]	0x05 [8][3]
DIGITAL LEAD	SINGLE-ENDED INPUT, DIGITALLY CALCULATED LEADS	LEAD I (LA − RA)	LEAD II (LL − RA)	LEAD III (LL − LA)	0	0	0

[1]REGISTER FRMCTL, BIT DATAFMT: 0 = LEAD/VECTOR MODE; 1 = ELECTRODE MODE.
[2]REGISTER ECGCTL, BIT CHCONFIG: 0 = SINGLE ENDED INPUT (DIGITAL LEAD MODE OR ELECTRODE MODE); 1 = DIFFERENTIAL INPUT (ANALOG LEAD MODE).
[3]REGISTER CMREFCTL, BIT CEREFEN: 0 = CE DISABLED; 1 = CE ENABLED.

10997-157

Figure 57. Electrode and Lead Configurations, Digital Lead Mode

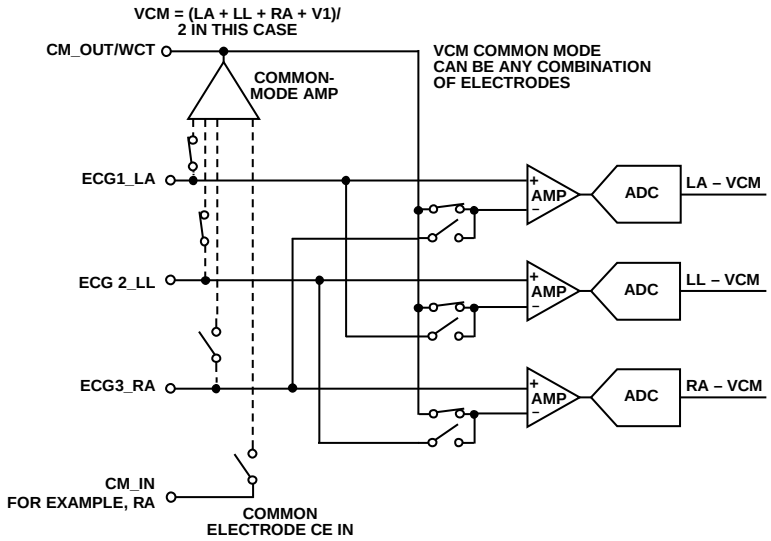


MODE	COMMENT	WORD1	WORD2	WORD3	0x0A [4][1]	0x01 [10][2]	0x05 [8][3]
COMMON ELECTRODE A	COMMON ELECTRODE (CE) LEADS (HERE RAELECTRODE IS CONNECTED TO THECE ELECTRODE (CM_IN) AND V3 IS ON ECG3 INPUT)	LEAD I (LA − RA)	LEAD II (LL − RA)	V3' $\frac{(V3 - RA) - (LA - RA) - (LL - RA)}{3}$	0	0	1

[1]REGISTER FRMCTL, BIT DATAFMT: 0 = LEAD/VECTOR MODE; 1 = ELECTRODE MODE.
[2]REGISTER ECGCTL, BIT CHCONFIG: 0 = SINGLE ENDED INPUT (DIGITAL LEAD MODE OR ELECTRODE MODE); 1 = DIFFERENTIAL INPUT (ANALOG LEAD MODE).
[3]REGISTER CMREFCTL, BIT CEREFEN: 0 = CE DISABLED; 1 = CE ENABLED.

10997-158

Figure 58. Electrode and Lead Configurations, Common Electrode A

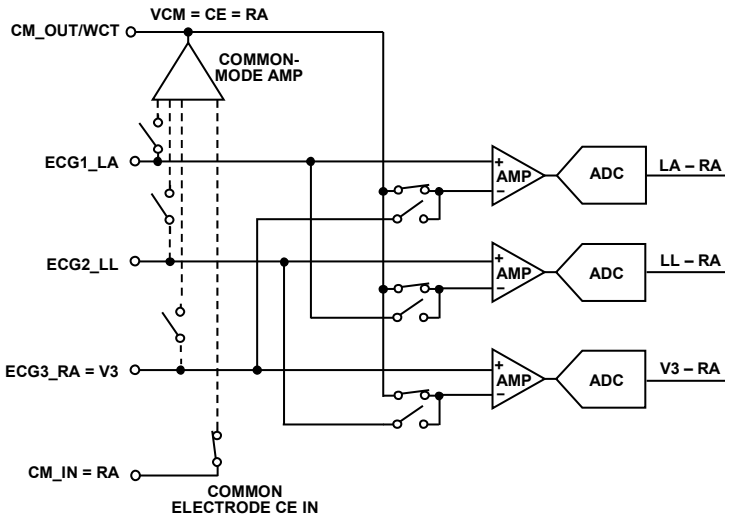


MODE	COMMENT	WORD1	WORD2	WORD3	0x0A [4][1]	0x01 [10][2]	0x05 [8][3]
SINGLE-ENDED INPUT ELECTRODE	SINGLE-ENDED INPUT ELECTRODE RELATIVE TO VCM	LA − VCM	LL − VCM	RA − VCM	1	0	0

[1]REGISTER FRMCTL, BIT DATAFMT: 0 = LEAD/VECTOR MODE; 1 = ELECTRODE MODE.
[2]REGISTER ECGCTL, BIT CHCONFIG: 0 = SINGLE ENDED INPUT (DIGITAL LEAD MODE OR ELECTRODE MODE); 1 = DIFFERENTIAL INPUT (ANALOG LEAD MODE).
[3]REGISTER CMREFCTL, BIT CEREFEN: 0 = CE DISABLED; 1 = CE ENABLED.

10997-159

Figure 59. Electrode and Lead Configurations, Single-Ended Input Electrode



MODE	COMMENT	WORD1	WORD2	WORD3	0x0A [4][1]	0x01 [10][2]	0x05 [8][3]
COMMON ELECTRODE B	LEADS FORMED RELATIVE TO A COMMON ELECTRODE (CE)	LA − CE	LL − CE	V1 − CE	1	0	1

[1]REGISTER FRMCTL, BIT DATAFMT: 0 = LEAD/VECTOR MODE; 1 = ELECTRODE MODE.
[2]REGISTER ECGCTL, BIT CHCONFIG: 0 = SINGLE ENDED INPUT (DIGITAL LEAD MODE OR ELECTRODE MODE); 1 = DIFFERENTIAL INPUT (ANALOG LEAD MODE).
[3]REGISTER CMREFCTL, BIT CEREFEN: 0 = CE DISABLED; 1 = CE ENABLED.

10997-160

Figure 60. Electrode and Lead Configurations, Common Electrode B

DEFIBRILLATOR PROTECTION

The ADAS1000-3/ADAS1000-4 do not include defibrillation protection on chip. Any defibrillation protection required by the application requires external components. Figure 61 and Figure 62 show examples of external defibrillator protection, which is required on each ECG channel, in the RLD path, and in the CM_IN path if using the CE input mode. Note that, in both cases, the total ECG path resistance is assumed to be 5 kΩ. The 22 MΩ resistors shown connected to RLD are optional and used to provide a safe termination voltage for an open ECG electrode; they may be larger in value. Note that, if using these resistors, the dc lead-off feature works best with the highest current setting.

ESIS FILTERING

The ADAS1000-3/ADAS1000-4 do not include electrosurgical interference suppression (ESIS) protection on chip. Any ESIS protection required by the application requires external components.

ECG PATH INPUT MULTIPLEXING

As shown in Figure 63, signal paths for numerous functions are provided on each ECG channel (except respiration, which only connects to the ECG1_LA, ECG2_LL, and ECG3_RA pins). Note that the channel enable switch occurs after the RLD amplifier connection, thus allowing the RLD to be connected (redirected into any one of the ECG paths). The CM_IN path is treated the same as the ECG signals.

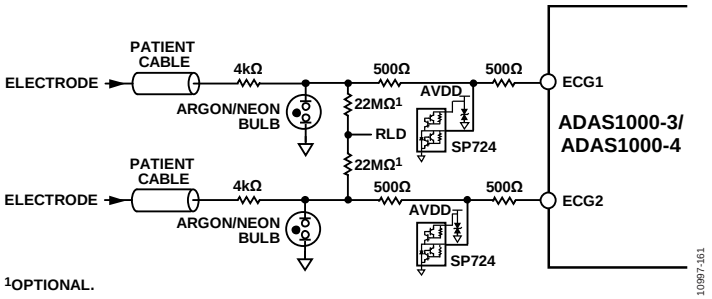


Figure 61. Possible Defibrillation Protection on ECG Paths Using Neon Bulbs

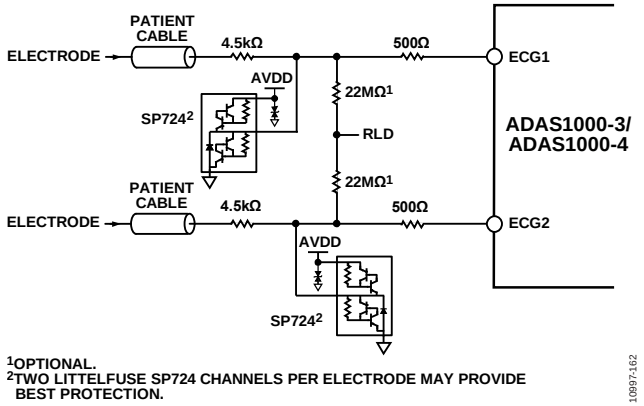


Figure 62. Possible Defibrillation Protection on ECG Paths Using Diode Protection

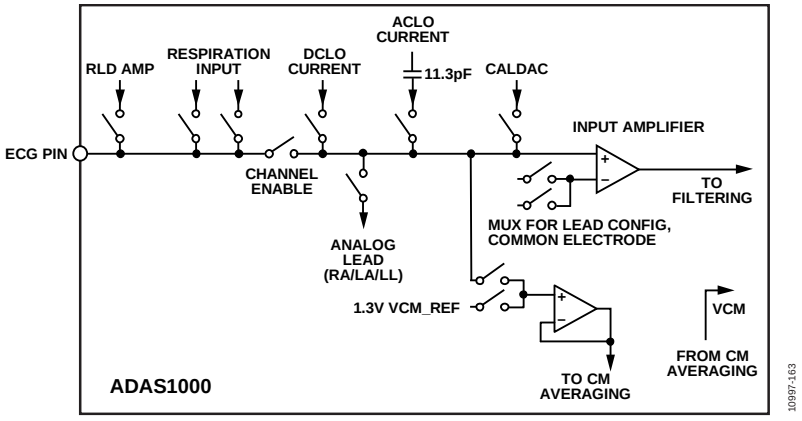


Figure 63. Typical ECG Channel Input Multiplexing

COMMON-MODE SELECTION AND AVERAGING

The common-mode signal can be derived from any combination of one or more electrode channel inputs, the fixed internal common-mode voltage reference, VCM_REF, or an external source connected to the CM_IN pin. One use of the latter arrangement is in gang mode where the master device creates the Wilson Central Terminal for the slave device(s). The fixed reference option is useful when measuring the calibration DAC test tone signals or while attaching electrodes to the patient, where it allows a usable signal to be obtained from just two electrodes.

The flexible common-mode generation allows complete user control over the contributing channels. It is similar to, but independent of, circuitry that creates the right leg drive (RLD) signal. Figure 64 shows a simplified version of the common-mode block. If the physical connection to each electrode is buffered, these buffers are omitted for clarity.

There are several restrictions on the use of the switches:

- If SW1 is closed, SW7 must be open.
- If SW1 is open, at least one electrode switch (SW2 to SW7) must be closed.
- SW7 can be closed only when SW2 to SW6 are open, so that the 1.3 V VCM_REF is summed in only when all ECG channels are disconnected.

The CM_OUT output is not intended to supply current or drive resistive loads, and its accuracy is degraded if it is used to drive anything other than the slave ADAS1000-2 devices. An external buffer is required if there is any loading on the CM_OUT pin.

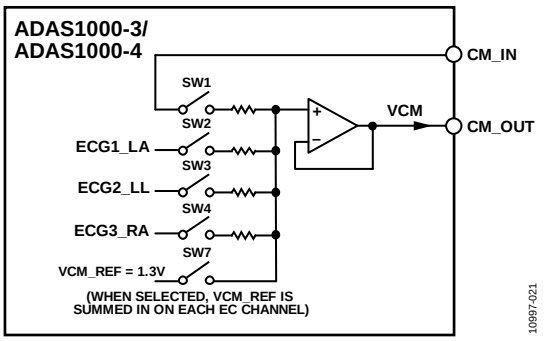


Figure 64. Common-Mode Generation Block

Table 11. Truth Table for Common-Mode Selection

ECGCTL Address 0x01[1]	CMREFCTL Address 0x05[2]						
PWREN	**DRVCM**	**EXTCM**	**LACM**	**LLCM**	**RACM**	**On Switch**	**Description**
0	X	X	X	X	X		Powered down, paths disconnected
1	X	0	0	0	0	SW7	Internal VCM_REF = 1.3 V is selected
1	0	0	1	0	0	SW2	Internal CM selection: LA contributes to VCM
1	0	0	1	1	0	SW2, SW3	Internal CM selection: LA and LL contribute to VCM
1	0	0	1	1	1	SW2, SW3, SW4	Internal CM selection: LA, LL, and RA contribute to VCM (WCT)
.	.	.	.	.	.	.	.
1	X	1	X	X	X	SW1	External VCM selected

[1] See Table 28.
[2] See Table 32.

WILSON CENTRAL TERMINAL (WCT)

The flexibility of the common-mode selection averaging allows the user to achieve a Wilson Central Terminal voltage from the ECG1_LA, ECG2_LL, ECG3_RA electrodes.

RIGHT LEG DRIVE/REFERENCE DRIVE

The right leg drive amplifier or reference amplifier is used as part of a feedback loop to force the patient's common-mode voltage close to the internal 1.3 V reference level (VCM_REF) of the ADAS1000-3/ADAS1000-4. This centers all the electrode inputs relative to the input span, providing maximum input dynamic range. It also helps to reject noise and interference from external sources such as fluorescent lights or other patient-connected instruments, and absorbs the dc or ac lead-off currents injected on the ECG electrodes.

The RLD amplifier can be used in a variety of ways as shown in Figure 65. Its input can be taken from the CM_OUT signal using an external resistor. Alternatively, some or all of the electrode signals can be combined using the internal switches.

The dc gain of the RLD amplifier is set by the ratio of the external feedback resistor (RFB) to the effective input resistor, which can be set by an external resistor, or alternatively, a function of the number of selected electrodes as configured in the CMREFCTL register (see Table 32). In a typical case, using the internal resistors for R_{IN}, all active electrodes would be used to derive the right leg drive, resulting in a 2 kΩ effective input resistor. Achieving a typical dc gain of 40 dB would thus require a 200 kΩ feedback resistor.

The dynamics and stability of the RLD loop depend on the chosen dc gain and the resistance and capacitance of the patient cabling. In general, loop compensation using external components is required, and must be determined experimentally for any given instrument design and cable set.

In some cases, adding lead compensation will prove necessary, while in others lag compensation may be more appropriate. The RLD amplifier's summing junction is brought out to a package pin (RLD_SJ) to facilitate compensation.

The RLD amplifier's short circuit current capability exceeds regulatory limits. A patient protection resistor is required to achieve compliance.

Within the RLD block, there is lead-off comparator circuitry that monitors the RLD amplifier output to determine whether the patient feedback loop is closed. An open-loop condition, typically the result of the right leg electrode (RLD_OUT) becoming detached, tends to drive the amplifier's output low. This type of fault is flagged in the header word (see Table 53), allowing the system software to take action by notifying the user, redirecting the reference drive to another electrode via the internal switches of the ADAS1000-3/ADAS1000-4, or both. The detection circuitry is local to the RLD amplifier and remains functional with a redirected reference drive. Table 32 provides details on reference drive redirection.

While reference drive redirection may be useful in the event that the right leg electrode cannot be reattached, some precautions must be observed. Most important is the need for a patient protection resistor. Because this is an external resistor, it does not follow the redirected reference drive; some provision for continued patient protection is needed external to the ADAS1000-3/ADAS1000-4. Any additional resistance in the ECG paths will certainly interfere with respiration measurement and may also result in an increase in noise and decrease in CMRR.

The RLD amplifier is designed to stably drive a maximum capacitance of 5 nF based on the gain configuration (see Figure 65) and assuming a 330 kΩ patient protection resistor.

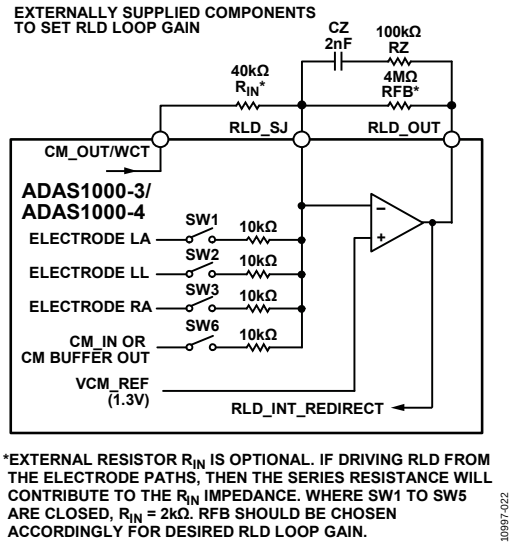


Figure 65. Right Leg Drive—Possible External Component Configuration

CALIBRATION DAC

Within the ADAS1000-3/ADAS1000-4, there are a number of calibration features.

The 10-bit calibration DAC can be used to correct channel gain errors (to ensure channel matching) or to provide several test tones. The options are as follows:

- DC voltage output (range: 0.3 V to 2.7 V). The DAC transfer function for dc voltage output is

$$0.3\text{ V} + \left(2.4\text{ V} \times \frac{code}{(2^{10}-1)}\right)$$

- 1 mV p-p sine wave of 10 Hz or 150 Hz
- 1 mV 1 Hz square wave

Internal switching allows the calibration DAC signals to be routed to the input of each ECG channel (see Figure 63). Alternatively, it can be driven out from the CAL_DAC_IO pin, enabling measurement and correction for external error sources in the entire ECG signal chain.

To ensure a successful update of the calibration DAC (see Table 36), the host controller must issue four additional SCLK cycles after writing the new calibration DAC register word.

GAIN CALIBRATION

The gain for each ECG channel can be adjusted to correct for gain mismatches between channels. Factory trimmed gain correction coefficients are stored in nonvolatile memory on-chip for GAIN 0, GAIN 1, and GAIN 2; there is no factory calibration for GAIN 3. The default gain values can be over-written by user gain correction coefficients, which are stored in volatile memory and available by addressing the appropriate gain control registers (see Table 50). The gain calibration applies to the ECG data available on the standard interface and applies to all data rates.

LEAD-OFF DETECTION

An ECG system must be able to detect if an electrode is no longer connected to the patient. The ADAS1000-3/ADAS1000-4 support two methods of lead-off detection, ac lead-off detection and dc lead-off detection. The two systems are independent and can be used singly or together under the control of the serial interface (see Table 29).

A lead-off event sets a flag in the frame header word (see Table 53). Identification of which electrode is off is available as part of the data frame or as a register read from the lead-off status register (Register LOFF, see Table 47). In the case of ac lead-off, information about the amplitude of the lead-off signal or signals can be read back through the serial interface (see Table 51).

In a typical ECG configuration, the electrodes RA, LA, and LL are used to generate a common mode of Wilson Central Terminal (WCT). If one of these electrodes is off, this affects the WCT signal and any lead measurements that it contributes to. As a result, the ECG measurements on these signals are expected to degrade. The user has full control over the common-mode amplifier and can adjust the common-mode configuration to remove that electrode from the common-mode generation. In this way, the user can continue to make measurements on the remaining connected leads.

DC Lead-Off Detection

This method injects a small programmable dc current into each input electrode. When an electrode is properly connected, the current flows into the right leg (RLD_OUT) and produces a minimal voltage shift. If an electrode is off, the current charges that pin's capacitance, causing the voltage at the pin to float positive and create a large voltage change that is detected by the comparators in each channel. These comparators use fixed, gain-independent upper and lower threshold voltages of 2.4 V and 0.2 V, respectively. If the input exceeds either of these levels, the lead-off flag is raised. The lower threshold is included in the event that something pulls the electrode down to ground.

The dc lead-off detection current can be programmed via the serial interface. Typical currents range from 10 nA to 70 nA in 10 nA steps. All input pins (RA, LA, LL, V1, V2, and CM_IN) use identical dc lead-off detection circuitry.

Detecting if the right-leg electrode has fallen off is necessarily different as RLD_OUT is a low impedance amplifier output. A pair of fixed threshold comparators monitor the output voltage to detect amplifier saturation that would indicate a lead-off condition. This information is available in the DCLEAD-OFF register (Register 0x1E) along with the lead-off status of all the input pins.

The propagation delay for detecting a dc lead-off event depends on the cable capacitance and the programmed current. It is approximately

Delay = *Voltage* × *Cable Capacitance*/*Programmed Current*

For example:

Delay = 1.2 V × (200 pF/70 nA) = 3.43 ms

DC Lead-Off and High Gains

Using dc lead-off at high gains can result in failure of the circuit to flag a lead-off condition. The chopping nature of the input amplifier stage contributes to this situation. When the electrode is off, the electrode is pulled up; however, in this gain setting, the first stage amplifier goes into saturation before the input signal crosses the DCLO upper threshold, resulting in no lead-off flag. This affects the gain setting GAIN 3 (4.2) and partially GAIN 2 (2.8).

Increasing the AVDD voltage raises the voltage at which the input amplifiers saturate, allowing the off electrode voltage to rise high enough to trip the DCLO comparator (fixed upper threshold of 2.4 V). The ADAS1000 operates over a voltage range of 3.15 V to 5.5 V. If using GAIN 2/GAIN 3 and dc lead-off, an increased AVDD supply voltage (minimum 3.6 V) allows dc lead-off to flag correctly at higher gains.

AC Lead-Off Detection

The alternative method of sensing if the electrodes are connected to the patient is based on injecting ac currents into each channel and measuring the amplitudes of the resulting voltages. The system uses a fixed carrier frequency at 2.039 kHz, which is high enough to be removed by the ADAS1000-3/ ADAS1000-4 on-chip digital filters without introducing phase or amplitude artifacts into the ECG signal.

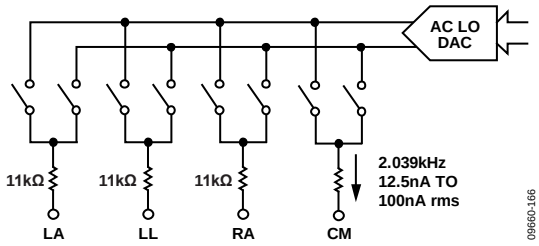


Figure 66. Simplified AC Lead-Off Configuration

The amplitude of the signal is nominally 2 V p-p and is centered on 1.3 V relative to the chip AGND level. It is ac-coupled into each electrode. The polarity of the ac lead-off signal can be configured on a per-electrode basis through Bits[23:18] of the LOFFCTL register (see Table 29). All electrodes can be driven in phase, and some can be driven with reversed polarity to minimize the total injected ac current. Drive amplitude is also programmable. AC lead-off detection functions only on the input pins (LA, LL, RA, and CM_IN) and is not supported for the RLD_OUT pin.

The resulting analog input signal applied to the ECG channels is I/Q demodulated and amplitude detected. The resulting amplitude is low pass filtered and sent to the digital threshold detectors.

AC lead-off detection offers user programmable dedicated upper and lower threshold voltages (see Table 39 and Table 40). Note that these programmed thresholds voltage vary with the ECG channel gain. The threshold voltages are not affected by the current level that is programmed. All active channels use the same detection thresholds.

A properly connected electrode has a very small signal as the drive current flows into the right leg (RL), whereas a disconnected electrode has a larger signal as determined by a capacitive voltage divider (source and cable capacitance).

If the signal measured is larger than the upper threshold, then the impedance is high, so a wire is probably off. Selecting the appropriate threshold setting depends on the particular cable/ electrode/protection scheme, as these parameters are typically unique for the specific use case. This can take the form of starting with a high threshold and ratcheting it down until a lead-off is detected, then increasing the threshold by some safety margin. This gives simple dynamic thresholding that automatically compensates for many of the circuit variables.

The lower threshold is added for cases where the only ac lead-off is in use and for situations where an electrode cable has been off for a long time. In this case, the dc voltage has saturated to a rail, or the electrode cable has somehow shorted to a supply. In either case, there is no ac signal present, yet the electrode may not be connected. The lower threshold checks for a minimum signal level.

In addition to the lead-off flag, the user can also read back the resulting voltage measurement available on a per channel basis. The measured amplitude for each of the individual electrodes is available in Register 0x31 through Register 0x35 (LOAMxx registers, see Table 51).

The propagation delay for detecting an ac lead-off event is <10 ms.

Note that the ac lead-off function is disabled when the calibration DAC is enabled.

ADC Out of Range

When multiple leads are off, the input amplifiers may run into saturation. This results in the ADC outputting out of range data with no carrier to the leads off algorithm. The ac lead-off algorithm then reports little or no ac amplitude. The ADAS1000 contains flags to indicate if the ADC data is out of range, indicating a hard electrode off state. There are programmable overrange and under-range thresholds that can be seen in the LOFFUTH and LOFFLTH registers (see Table 39 and Table 40, respectively). The ADC out of range flag is contained in the header word (see Table 53).

SHIELD DRIVER

The shield drive amplifier is a unity-gain amplifier. Its purpose is to drive the shield of the ECG cables. For power consumption purposes, it can be disabled if not in use. Note that, the SHIELD pin is shared with the respiration pin function, where it can be muxed to be one of the pins for external capacitor connection. If the pin is being used for the respiration feature, the shield function is not available. In this case, if the application requires a shield drive, an external amplifier connected to the CM_OUT pin can be used.

RESPIRATION (ADAS1000-4 MODEL ONLY)

The respiration measurement is performed by driving a high frequency (programmable from 46.5 kHz to 64 kHz) differential current into two electrodes; the resulting impedance variation caused by breathing causes the differential voltage to vary at the respiration rate. The signal is ac-coupled onto the patient. The acquired signal is AM, with a carrier at the driving frequency and a shallow modulation envelope at the respiration frequency. The modulation depth is greatly reduced by the resistance of the customer-supplied RFI and ESIS protection filters, in addition to the impedance of the cable and the electrode to skin interface (see Table 12). The goal is to measure small ohm variation to sub ohm resolution in the presence of large series resistance. The circuit itself consists of a respiration DAC that drives the ac-coupled current at a programmable frequency onto the chosen pair of electrodes. The resulting variation in voltage is amplified, filtered, and synchronously demodulated in the digital domain; what results is a digital signal that represents the total thoracic or respiration impedance, including cable and electrode contributions. While it is heavily low-pass filtered on-chip, the user is required to further process it to extract the

envelope and perform the peak detection needed to establish breathing (or lack thereof).

Respiration measurement is available on one of the leads (Lead I, Lead II, or Lead III) or on an external path via a pair of dedicated pins (EXT_RESP_LA, EXT_RESP_RA, or EXT_RESP_LL). Only one lead measurement can be made at one time. The respiration measurement path is not suited for use as additional ECG measurements because the internal configuration and demodulation do not align with an ECG measurement. The respiration signal processing path is not reconfigurable for ECG measurements, as it is specifically designed for the respiration signal measurement.

Internal Respiration Capacitors

The internal respiration function uses an internal RC network (5 kΩ/100 pF), and this circuit is capable of 200 mΩ resolution (with up to 5 kΩ total path and cable impedance). The current is ac-coupled onto the same pins that the measurement is sensed back on. Figure 67 shows the measurement on Lead I, but, similarly, the measurement can be configured to measure on either Lead II or Lead III. The internal capacitor mode requires no external capacitors and produces currents of ~64 µA p-p amplitude when configured for maximum amplitude setting (±1 V) through the RESPCTRL register (see Table 30).

Table 12. Maximum Allowable Cable and Thoracic Loading

Cable Resistance	Cable Capacitance
R < 1 kΩ	C < 1200 pF
1 kΩ < R < 2.5 kΩ	C < 400 pF
2.5 kΩ < R < 5 kΩ	C < 200 pF
$R_{THORACIC}$ < 2 kΩ	

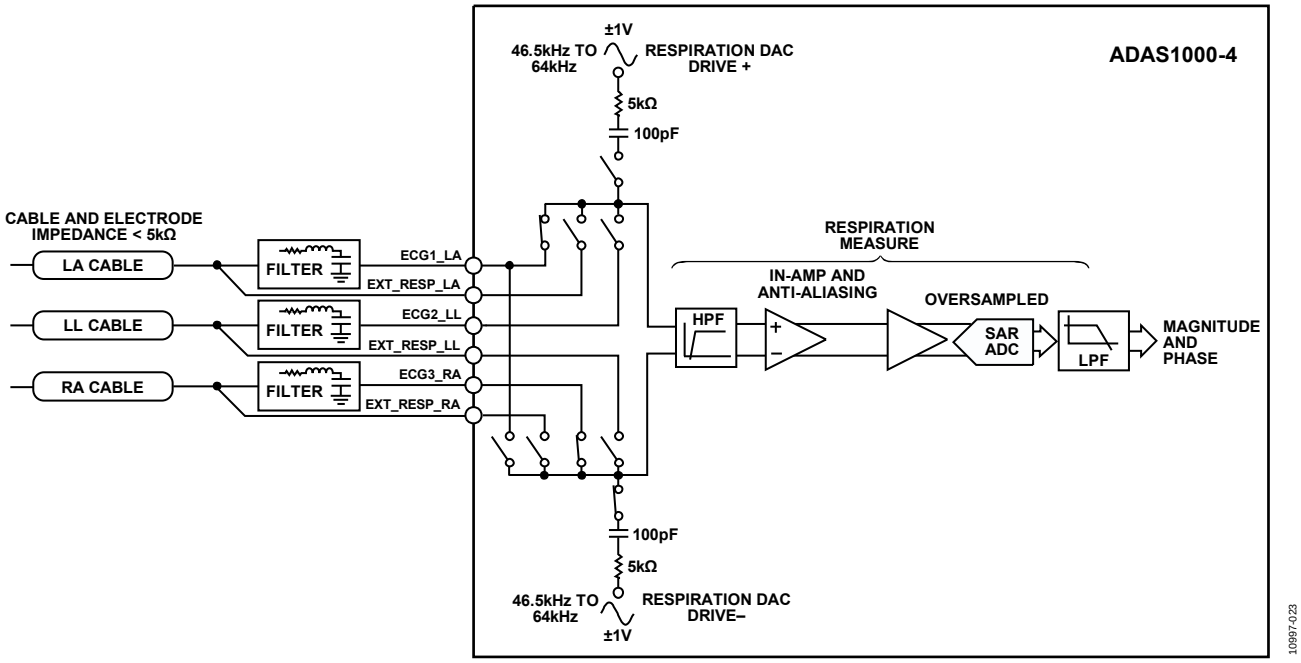


Figure 67. Simplified Respiration Block Diagram

External Respiration Path

The EXT_RESP_xx pins are provided for use either with the ECG electrode cables or, alternatively, with a dedicated external sensor independent of the ECG electrode path. Additionally, the EXT_RESP_xx pins are provided so the user can measure the respiration signal at the patient side of any input filtering on the front end. In this case, the user must continue to take precautions to protect the EXT_RESP_xx pins from any signals applied that are in excess of the operating voltage range (for example, ESIS or defibrillator signals).

External Respiration Capacitors

If necessary, the ADAS1000-4 allows the user to connect external capacitors into the respiration circuit to achieve higher resolution (<200 mΩ). This level of resolution requires that the cable impedance be ≤1 kΩ. The diagram in Figure 68 shows the connections at RESPDAC_xx paths for the extended respiration configuration. Again, the EXT_RESP_xx paths can be connected at the patient side of any filtering circuit; however, the user must provide protection for these pins. While this external capacitor mode requires external components, it can deliver a larger signal-to-noise ratio. Note again that respiration can be measured on only one lead (at one time); therefore, only one pair of external respiration paths (and external capacitors) may be required.

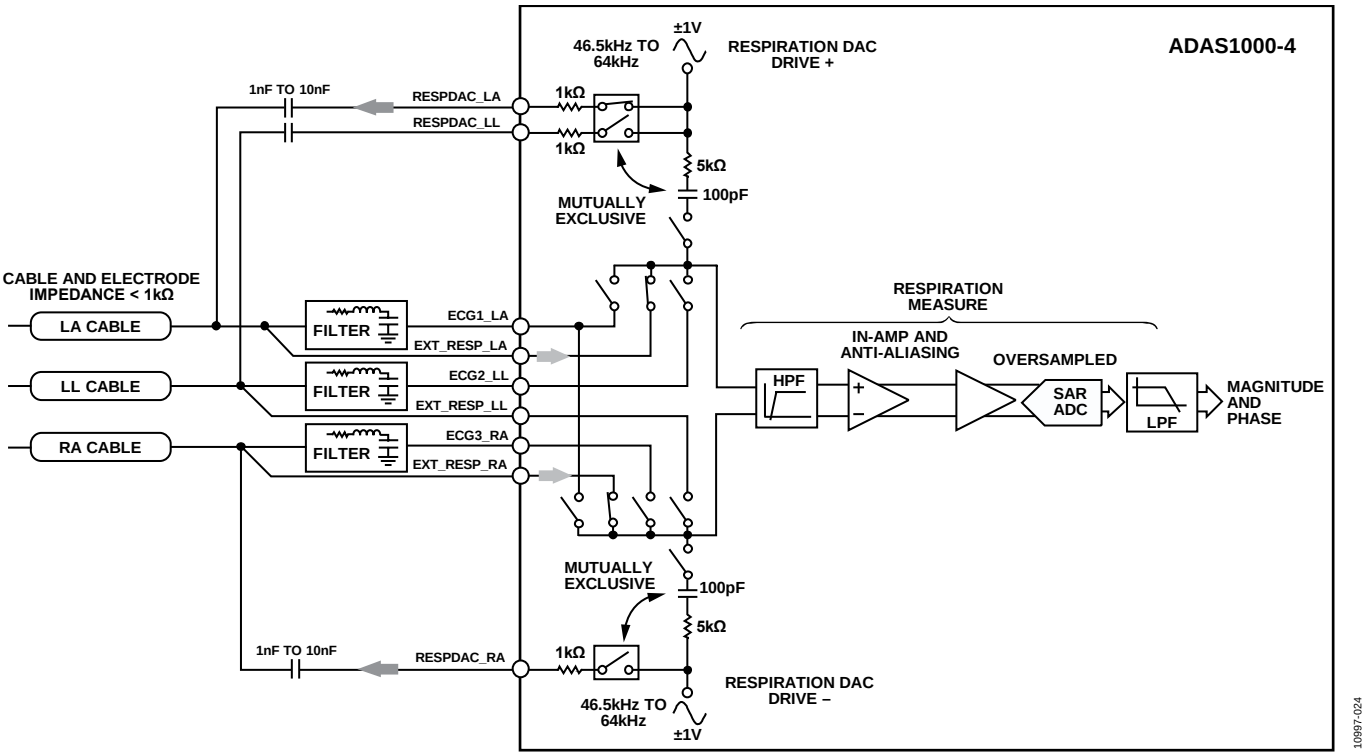


Figure 68. Respiration Measurement Using External Capacitor

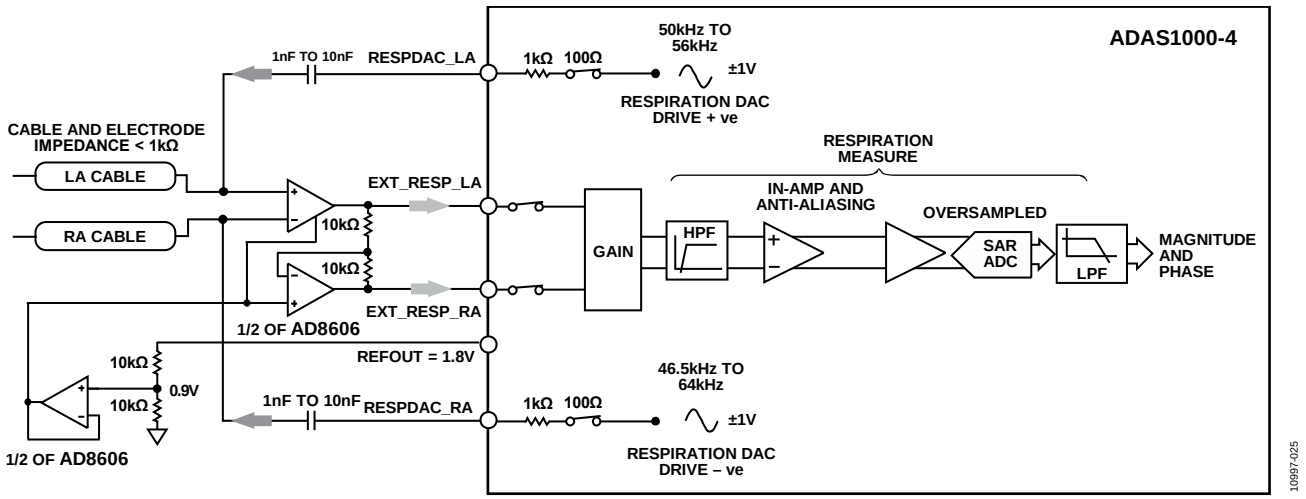


Figure 69. Respiration Using External Capacitor and External Amplifiers

If required, further improvements in respiration performance may be possible with the use of an instrumentation amplifier and op amp external to the ADAS1000-4. The instrumentation amplifier must have sufficiently low noise performance to meet the target performance levels. This mode uses the external capacitor mode configuration and is shown in Figure 69. Bit 14 of the RESPCTL register (Table 30) allows the user to bypass the on-chip amplifier when using an external instrumentation amplifier.

Respiration Carrier Frequency

The frequency of the respiration carrier is programmable and can be varied through the RESPCTL register (Address 0x03, see Table 30). The status of the HP bit in the ECGCTL register also has an influence on the carrier frequency as shown in Table 13.

Table 13. Control of Respiration Carrier Frequencies

RESPALT-FREQ[1]	RESPEXT-SYNC[1]	HP[2]	RESP-FREQ[1]	Respiration Carrier Frequency
0	0	1	00	56
0	0	1	01	54
0	0	1	10	52
0	0	1	11	50
0	0	0	00	56
0	0	0	01	54
0	0	0	10	52
0	0	0	11	50
1	X[3]	1	00	64
1	X[3]	1	01	56.9
1	X[3]	1	10	51.2
1	X[3]	1	11	46.5
1	X[3]	0	00	32
1	X[3]	0	01	28
1	X[3]	0	10	25.5
1	X[3]	0	11	23

[1] Control bits from RESPCTL (Register 0x03).
[2] Control bit from ECGCTL (Register 0x01).
[3] X = don't care.

In applications where an external signal generator is used to develop a respiration carrier signal, that external signal source can be synchronized to the internal carrier using the signal available on GPIO3 when Bit 7, RESPEXTSEL, is enabled in the respiration control register (see Table 30).

Table 14. Control of Respiration Carrier Frequency Available on GPIO3

RESPALT-FREQ[1]	RESPEXT-SYNC[1]	HP[2]	RESP-FREQ[1]	Respiration Carrier Frequency on GPIO3
0	1	X[3]	XX[3]	64
1	1	1	00	64
1	1	1	01	56
1	1	1	10	51.2
1	1	1	11	46.5
1	1	0	00	32
1	1	0	01	28
1	1	0	10	25.5
1	1	0	11	23

[1] Control bits from RESPCTL (Register 0x03).
[2] Control bit from ECGCTL (Register 0x01).
[3] X = don't care.

EVALUATING RESPIRATION PERFORMANCE

ECG simulators offer a convenient means of studying the ADAS1000-3/ADAS1000-4's performance. While many simulators offer a variable-resistance respiration capability, care must be taken when using this feature.

Some simulators use electrically-programmable resistors, often referred to as digiPOTs, to create the time-varying resistance to be measured by the respiration function. The capacitances at the digitPOT's terminals are often unequal and code-dependent, and these unbalanced capacitances can give rise to unexpectedly large or small results on different leads for the same programmed resistance variation. Best results are obtained with a purpose-built fixture that carefully balances the capacitance presented to each ECG electrode.

PACING ARTIFACT DETECTION FUNCTION (ADAS1000-4 ONLY)

The pacing artifact validation function qualifies potential pacing artifacts and measures the width and amplitude of valid pulses. These parameters are stored in and available from any of the pace data registers (Address 0x1A, Address 0x3A to Address 0x3C). This function runs in parallel with the ECG channels. Digital detection is performed using a state machine operating on the 128 kHz 16-bit data from the ECG decimation chain. The main ECG signals are further decimated before appearing in the 2 kHz output stream so that detected pace signals are not perfectly time-aligned with fully-filtered ECG data. This time difference is deterministic and may be compensated for.

The pacing artifact validation function can detect and measure pacing artifacts with widths from 100 µs to 2 ms and with amplitudes of <400 µV to >1000 mV. Its filters are designed to reject heartbeat, noise, and minute ventilation pulses. The flowchart for the pace detection algorithm is shown in Figure 71.

The ADAS1000-4 pace algorithm can operate with the ac lead-off and respiration impedance measurement circuitry enabled.

Once a valid pace has been detected in the assigned leads, the pace-detected flags appear in the header word (see Table 53) at the start of the packet of ECG words. These bits indicate that a pace was qualified. Further information on height and width of pace is available by reading the contents of Address 0x1A (Register PACEDATA, see Table 44). This word can be included in the ECG data packet/frame as dictated by the frame control register (see Table 37). The data available in the PACEDATA register is limited to seven bits total for width and height information; therefore, if more resolution is required on the pace height and width, this is available by issuing read commands of the PACExDATA registers (Address 0x3A to Address 0x3C) as shown in Table 52.

The on-chip filtering contributes some delay to the pace signal (see the Pace Latency section).

Choice of Leads

Three identical and independent state machines are available and can be configured to run on up to three of four possible leads (Lead I, Lead II, Lead III, and aVF) for pacing artifact detection. Any necessary lead calculations are performed internally and are independent of EGG channel settings for output data rate, low-pass filter cutoff, and mode (electrode, analog lead, common electrode). These calculations take into account the available front-end configurations as detailed in Table 15.

The pace detection algorithm searches for pulses by analyzing samples in the 128 kHz ECG data stream. The algorithm searches for a leading edge, a peak, and a trailing edge as defined by values in the PACEEDGETH, PACEAMPTH, and PACELVLTH registers, along with fixed width qualifiers. The post-reset default register values can be overwritten via the SPI bus, and different values can be used for each of the three pace detection state machines.

Some users may not want to use three pace leads for detection. In this case, Lead II is the vector of choice, because this lead is likely to display the best pacing artifact. The other two pace instances can be disabled if not in use.

The first step in pace detection is to search the data stream for a valid leading edge. Once a candidate edge has been detected, the algorithm begins searching for a second, opposite-polarity edge that meets with pulse width criteria and passes the (optional) noise filters. Only those pulses meeting all the criteria are flagged as valid pace pulses. Detection of a valid pace pulse sets the flag(s) in the frame header register and stores amplitude and width information in the PACEDATA register (Address 0x1A; see Table 44). The pace algorithm looks for a negative or positive pulse

Table 15. Pace Lead Calculation

			0x04 [8:3][3]			
			00	**01**	**10**	**11**
0x01 [10][1]	**0x05 [8][2]**	**Configuration**	**Lead I (LA – RA)**	**Lead II (LL – RA)**	**Lead III (LL – LA)**	**aVF (Lead II + Lead III)/2**
0	0	Digital leads	LA – RA CH1 – CH3	LL – RA CH2 – CH3	LL – LA CH2 – CH1	LL – (LA + RA)/2 CH2 – (CH1 + CH3)/2
0	1	Common Electrode Lead A	Lead I CH1	Lead II CH2	Lead II – Lead I CH2 – CH1	Lead II – 0.5 × Lead I CH2 – 0.5 × CH1
1	X	Analog leads	Lead I CH1	Lead II – CH3	Lead III CH2	Lead II – 0.5 × Lead I – CH3 – 0.5 × CH1

[1] Register ECGCTL, Bit CHCONFIG, see Table 28.
[2] Register CMREFCTL, Bit CEREFEN, see Table 32.
[3] Register PACECTL, Bit PACExSEL [1:0], see Table 31.

Detection Algorithm Overview

The pace pulse amplitude and width varies over a wide range, while its shape is affected by both the internal filtering arising from the decimation process and the low pass nature of the electrodes, cabling, and components used for defibrillation and ESIS protection. The ADAS1000-4 provides user programmable variables to optimize the performance of the algorithm within the ECG system, given all these limiting elements. The default parameter values are probably not optimal for any particular system design; experimentation and evaluation are needed to ensure robust performance.

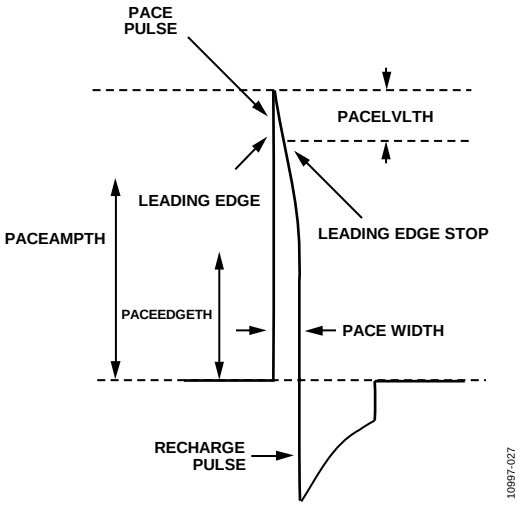


Figure 70. Typical Pace Signal

The first step in pace detection is to search the data stream for a valid leading edge. Once a candidate edge is detected, the algorithm verifies that the signal looks like a pulse and then begins searching for a second, opposite polarity edge that meets the pulse width and amplitude criteria and passes the optional noise filters. Only the pulses meeting all requirements are flagged as valid pace pulses. Detection of a valid pace pulse sets the flag or flags in the frame header register and stores amplitude and width information in the PACEDATA register (Address 0x1A; see Table 34).

The pace algorithm detects pulses of both negative and positive polarity using a single set of parameters by tracking the slope of the leading edge and making the necessary adjustments to internal parameter signs. This frees the user to concentrate on determining appropriate threshold values based on pulse shape without concern for pulse polarity.

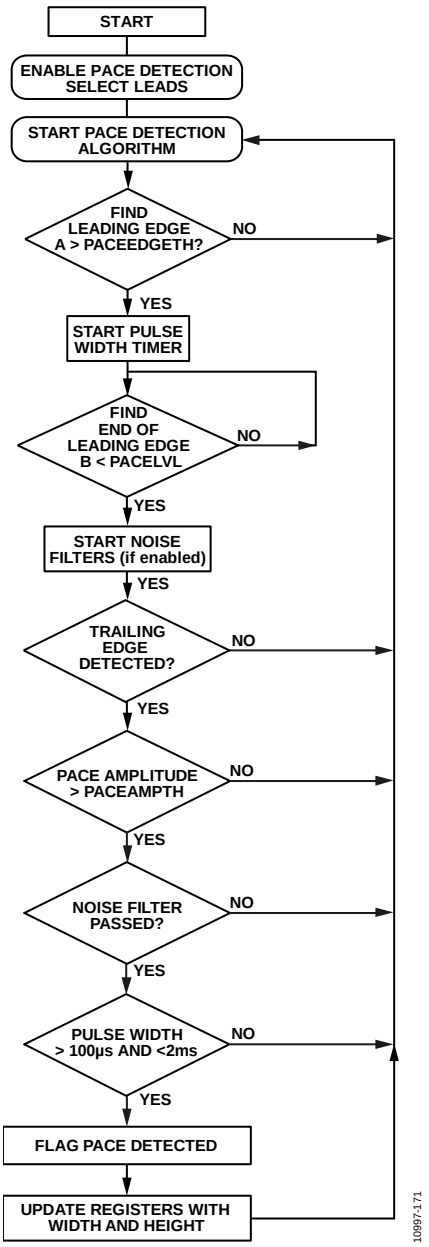


Figure 71. Overview of Pace Algorithm

The three user controlled parameters for the pace detection algorithm are Pace Amplitude Threshold (PACEAMPTH), Pace Level Threshold (PACELVLTH), and Pace Edge Threshold (PACEEDGETH).

Pace Edge Threshold

This programmable level (Address 0x0E, see Table 41) is used to find a leading edge, signifying the start of a potential pace pulse. A candidate edge is one in which the leading edge crosses a threshold PACEEDGETH from the recent baseline. PACEEDGETH can be assigned any value between 0 and 255. Setting PACEEDGETH to 0 forces it to the value PACEAMPTH/2 (see the following equation). Non-zero values give the following:

$$PACEEDGETH\ setting = \frac{N \times VREF}{GAIN \times 2^{16}}$$

where:
N is the 8-bit programmed PACEEDGETH value (1 ≤ N ≤ 255).
VREF is the ADAS1000-4 reference voltage of 1.8 V.
GAIN is the programmed gain of the ECG channel.

The minimum threshold for ×1.4 gain is 19.6 µV, while the maximum for the same gain setting is 5.00 mV.

Pace Level Threshold

This programmable level (Address 0x0F, see Table 42) is used to detect when the leading edge of a candidate pulse ends. In general, a pace pulse is not perfectly square, and the top, meaning the portion after the leading edge, may continue to increase slightly or droop back towards the baseline. PACELVLTH defines an allowable slope for this portion of the candidate pulse, where the slope is defined as the change in value over an internally-fixed interval after the pace edge is qualified.

PACELVLTH is an 8-bit, twos complement number. Positive values represent movement away from the baseline (pulse amplitude is still increasing) while negative values represent droop back towards the baseline.

$$PACELVLTH\ setting = \frac{N \times VREF}{GAIN \times 2^{16}}$$

where:
N is the 8-bit programmed PACELVLTH value (−128 ≤ N ≤ 127).
VREF is the ADAS1000-4 reference voltage of 1.8 V.
GAIN is the programmed gain of the ECG channel.

The minimum value for ×1.4 gain is 9.8 µV, while the maximum for the same gain setting is 2.50 mV.

An additional qualification step, performed after PACELVLTH is satisfied, rejects pulses with a leading edge transition time greater than about 156 µs. This filter improves immunity to motion and other artifacts and cannot be disabled. Overly aggressive ESIS filtering causes this filter to disqualify valid pace pulses. In such cases, increasing the value of PACEEDGETH provides more robust pace pulse detection. Although counterintuitive, this change forces a larger initial deviation from the recent baseline before the pace detection algorithm starts, reducing the time until PACELVLTH comes into play and shortening the apparent leading edge transition. Increasing the value of PACEEDGETH may require a reduction in PACEAMPTH.

Pace Amplitude Threshold

This register (Address 0x07, see Table 34) sets the minimum valid pace pulse amplitude. PACEAMPTH is an unsigned 8-bit number. The programmed height is given by:

$$PACEAMPTH\ setting = \frac{2 \times N \times VREF}{GAIN \times 2^{16}},$$

where:
N is the 8-bit programmed PACEAMPTH value (1 ≤ N ≤ 255).
VREF is the ADAS1000-4 reference voltage of 1.8 V.
GAIN is the programmed gain of the ECG channel.

The minimum threshold for ×1.4 gain is 19.6 µV, while the maximum for the same gain setting is 5.00 mV. PACEAMPTH is typically set to the minimum expected pace amplitude and must be larger than the value of PACEEDGETH.

The default register setting of N = 0x24 results in 706 µV for a gain = 1 setting. An initial PACEAMPTH setting between 700 µV and 1 mV provides a good starting point for both unipolar and biventricular pacing detection. Values below 250 µV are not recommended because they greatly increase sensitivity to ambient noise from the patient. The amplitude may need to be adjusted much higher than 1 mV when other medical devices are connected to the patient.

Pace Validation Filters

A candidate pulse that successfully passes the combined tests of PACEEDGETH, PACELVLTH, and PACEAMPTH is next passed through two optional validation filters. These filters are used to reject sub-threshold pulses such as minute ventilation (MV) pulse and signals from inductively coupled implantable telemetry systems. These filters perform different tests of pulse shape using a number of samples. Both filters are enabled by default; Filter 1 is controlled by Bit 9 in the PACECTL register (see Table 31) and Filter 2 is controlled by Bit 10 in the same register. These filters are not available on a lead by lead basis; if enabled, they are applied to all leads being used for pace detection.

Pace Width Filter

A candidate pulse that successfully passes the edge, amplitude, and noise filters is finally checked for width. When this final filter is enabled, it checks that the candidate pulse is between 100 µs and 2 ms wide. When a valid pace width is detected, the width is stored. Disabling this filter affects only the minimum width (100 µs) determination; the maximum width detection portion of the filter is always active. This filter is controlled by the PACECTL register, Bit 11 (see Table 31).

BIVENTRICULAR PACERS

As described previously, the pace algorithm expects the pace pulse to be less than 2 ms wide. In a pacer where both ventricles are paced, they can be paced simultaneously. Where they fall within the width and height limits programmed into the algorithm, a valid pace will be flagged, but only one pace pulse may be visible.

With the pace width filter enabled, the pace algorithm seeks pace pulse widths within a 100 µs to 2 ms window. Assuming that this filter is enabled and in a scenario where two ventricle pacer pulses fire at slightly different times, resulting in the pulse showing in the lead as one large, wider pulse, a valid pace is flagged so long as the total width does not exceed 2 ms.

PACE DETECTION MEASUREMENTS

Design verification of the ADAS1000-4 digital pace algorithm includes detection of a range of simulated pace signals in addition to using the ADAS1000-4 and evaluation board with one pacemaker device connected to various simulated loads (approximately 200 Ω to over 2 kΩ) and covering the following four waveform corners.

- Minimum pulse width (100 µs), minimum height (to <300 µV)
- Minimum pulse width (100 µs), maximum height (up to 1.0 V)
- Maximum pulse width (2 ms), minimum height (to <300 µV)
- Maximum pulse width (2 ms), maximum height (up to 1.0 V)

These scenarios passed with acceptable results. The use of the ac lead-off function had no obvious impact on the recorded pace height, width, or the ability of the pace detection algorithm to identify a pace pulse. The pace algorithm was also evaluated with the respiration carrier enabled; again, no differences in the threshold or pacer detect were noted from the carrier.

While these experiments validate the pace algorithm over a confined set of circumstances and conditions, they do not replace end system verification of the pacer algorithm. This can be performed in only the end system, using the system manufacturer's specified cables and validation data set.

EVALUATING PACE DETECTION PERFORMANCE

ECG simulators offer a convenient means of studying the performance and ability of the ADAS1000-4 to capture pace signals over the range of widths and heights defined by the various regulatory standards. While the pace detection algorithm of the ADAS1000 is designed to conform to medical instrument standards (pace widths of 100 µs to 2.00 ms and with amplitudes of <400 µV to >1000 mV), some simulators put out signals wider or narrower than called for in the standards. The pace detection algorithm has been designed to measure a maximum pace widths of 2 ms with a margin of 0.25 ms to allow for simulator variations.

PACE WIDTH

The ADAS1000-4 is capable of measuring pace widths of 100 µs to 2.00 ms. The measured pace width is available through the PACExDATA registers. These registers have limited resolution. The minimum pace width is 101.56 µs and the maximum is 2.00 ms. The pace detection algorithm always returns a width greater than what is measured at the 50% point, ensuring that the algorithm is capable of measuring a narrow 100 µs pulse. A valid pulse width of 100 µs is reported as 101.56 µs. Any valid pace pulses ≥2.00 ms and ≤ 2.25 ms are reported as 2.00 ms.

PACE LATENCY

The pace algorithm always examines 128 kHz, 16-bit ECG data, regardless of the selected frame rate and ECG filter setting. A pace pulse is qualified when a valid trailing edge is detected and is flagged in the next available frame header. Pace and ECG data is always correctly time-aligned at the 128 kHz frame rate, but the additional filtering inherent in the slower frame rates delays the frame's ECG data relative to the pace pulse flag. These delays are summarized in Table 16 and must be taken into account to enable correct positioning of the pace event relative to the ECG data.

There is an inherent one-frame-period uncertainty in the exact location of the pace trailing edge.

PACE DETECTION VIA SECONDARY SERIAL INTERFACE

The ADAS1000-3/ADAS1000-4 provide a second serial interface for users to implement their own pace detection schemes. This interface is configured as a master interface. It provides ECG data at the 128 kHz data rate only. The purpose of this interface is to allow the user to access the ECG data at a rate sufficient to allow them to run their own pace algorithm, while maintaining all the filtering and decimation of the ECG data that the ADAS1000-3/ADAS1000-4 offer on the standard serial interface (2 kHz and 16 kHz data rates). This dedicated pace interface uses three of the four GPIO pins, leaving one GPIO pin available even when the secondary serial interface is enabled. Note that the on-chip digital calibration to ensure channel gain matching does not apply to data that is available on this interface. This interface is discussed in more detail in the Secondary Serial Interface section.

FILTERING

Figure 72 shows the ECG digital signal processing. The ADC sample rate is programmable. In high performance mode, it is 2.048 MHz; in low power mode, the sampling rate is reduced to 1.024 MHz. The user can tap off framing data at one of three data rates, 128 kHz, 16 kHz, or 2 kHz. Note that although the data-word width is 24 bits for the 2 kHz and 16 kHz data rate, the usable bits are 19 and 18, respectively.

The amount of decimation depends on the selected data rate, with more decimation for the lower data rates.

Four selectable low-pass filter corners are available at the 2 kHz data rate.

Filters are cleared by a reset. Table 16 shows the filter latencies at the different data rates.

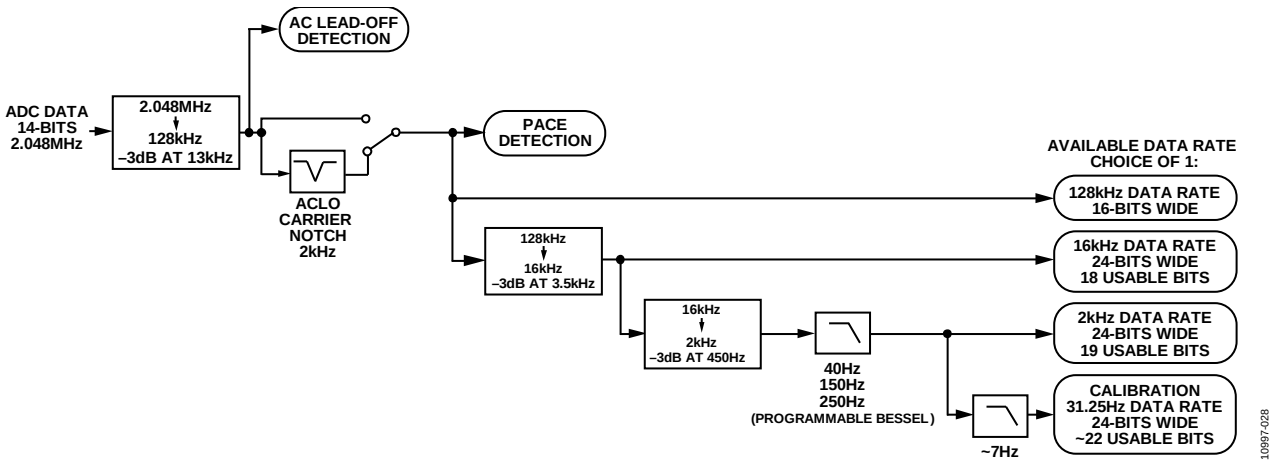


Figure 72. ECG Channel Filter Signal Flow

Table 16. Relationship of ECG Waveform to Pace Indication[1, 2, 3]

Data Rate	Conditions	Apparent Delay of ECG Data Relative to Pace Event[4]
2 kHz	450 Hz ECG bandwidth	0.984 ms
	250 Hz ECG bandwidth	1.915 ms
	150 Hz ECG bandwidth	2.695 ms
	40 Hz ECG bandwidth	7.641 ms
16 kHz		109 µs
128 kHz		0

[1] ECG waveform delay is the time required to reach 50% of final value following a step input.
[2] Guaranteed by design, not subject to production test.
[3] There is an unavoidable residual uncertainty of 8 µs in determining the pace pulse trailing edge.
[4] Add 38 µs to obtain the absolute delay for any setting.

VOLTAGE REFERENCE

The ADAS1000-3/ADAS1000-4 have a high performance, low noise, on-chip 1.8 V reference for use in the ADC and DAC circuits. The REFOUT of one device is intended to drive the REFIN of the same device. The internal reference is not intended to drive significant external current; for optimum performance in gang operation with multiple devices, each device should use its own internal reference.

An external 1.8 V reference can be used to provide the required VREF. In such cases, there is an internal buffer provided for use with external reference. The REFIN pin is a dynamic load with an average input current of approximately 100 µA per enabled channel, including respiration. When the internal reference is used, the REFOUT pin requires decoupling with a 10 µF capacitor with low ESR (0.2 Ω maximum) in parallel with 0.1 µF capacitor to REFGND, these capacitors should be placed as close to the device pins as possible and on the same side of the PCB as the device.

GANG MODE OPERATION

Increasing the number of ECG channels enables the user to measure an increased number of patient electrodes. Typically a 12-lead system would require nine electrodes (and one right leg drive reference electrode), but a derived arrangement is possible by using just eight electrodes (and one right leg drive reference electrode). As such, mating a 5-electrode ADAS1000, ADAS1000-1, or ADAS1000-2 with either a ADAS1000-3 or ADAS1000-4 device delivers the required eight electrodes. The approach used is a master slave arrangement, where one device is designated as master, and any others are designated as slaves. It is important that multiple devices operate well together; with this in mind, the pertinent inputs/outputs to interface between master and slave devices have been made available.

Note that when using multiple devices, the user must collect the ECG data directly from each device. If using a traditional 12-lead arrangement where the Vx leads are measured relative to WCT, the user should configure the master device in lead mode with the slave device configured for electrode mode. The LSB size for electrode and lead data differs (see Table 43 for details).

In gang mode, all devices must be operated in the same power mode (either high performance or low power) and the same data rate.

Master/Slave

Any of the ADAS1000, ADAS1000-1, ADAS1000-3, or ADAS1000-4 can be configured as a master or slave, while the ADAS1000-2 can only be configured as a slave. A device is selected as a master or slave using Bit 5, master, in the ECGCTL register (see Table 28). Gang mode is enabled by setting Bit 4, gang, in the same register. When a device is configured as a master, the SYNC_GANG pin is automatically set as an output.

When a device is configured as a slave (ADAS1000-2), the SYNC_GANG and CLK_IO pins are set as inputs.

Synchronizing Devices

The ganged devices need to share a common clock to ensure that conversions are synchronized. One approach is to drive the slave CLK_IO pins from the master CLK_IO pin. Alternatively, an external 8.192 MHz clock can be used to drive the CLK_IO pins of all devices. The CLK_IO powers up high impedance until configured in gang mode.

In addition, the SYNC_GANG pin is used to synchronize the start of the ADC conversion across multiple devices. The SYNC_GANG pin is automatically driven by the master and is an input to all the slaves. SYNC_GANG is in high impedance until enabled via gang mode.

When connecting devices in gang mode, the SYNC_GANG output is triggered once when the master device starts to convert. Therefore, to ensure that the slave device(s) receive this synchronization signal, configure the slave device first for operation and enable conversions, followed by issuing the conversion signal to the ECGCTL register in the master device.

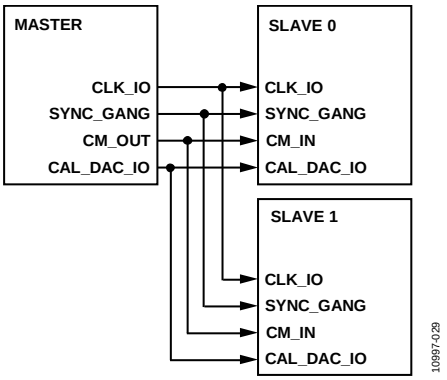


Figure 73. Master/Slave Connections in Gang Mode, Using Multiple Devices

Calibration

The calibration DAC signal from one device (master) can be output on the CAL_DAC_IO pin and used as the calibration input for other devices (slaves) when used in the gang mode of operation. This ensures that they are all being calibrated using the same signal which results in better matching across channels. This does not happen automatically in gang mode but, rather, must be configured via Table 36.

Common Mode

The ADAS1000-3/ADAS1000-4 have a dedicated CM_OUT pin serving as an output and a CM_IN pin as an input. In gang mode, the master device determines the common-mode voltage based on the selected input electrodes. This common-mode signal (on CM_OUT) can then be used by subsequent slave devices (applied to CM_IN) as the common-mode reference. All electrodes within the slave device are then measured with respect to the CM_IN signal from the master device. See the CMREFCTL register in Table 32 for more details on the control via the serial interface. Figure 74 shows the connections between a master and slave device using multiple devices.

Right Leg Drive

The right leg drive comes from the master device. If the internal RLD resistors of the slave device are to contribute to the RLD loop, tie the RLD_SJ pins of master and slave together.

Sequencing Devices into Gang Mode

When entering gang mode with multiple devices, both devices can be configured for operation, but the conversion enable bit (ECGCTL register, Bit 2, Table 28) of the master device should be set after the conversion enable bit of the slave device. When the master device conversion signal is set, the master device generates one edge on its SYNC_GANG pin. This applies to any slave SYNC_GANG inputs, allowing the devices to synchronize ADC conversions.

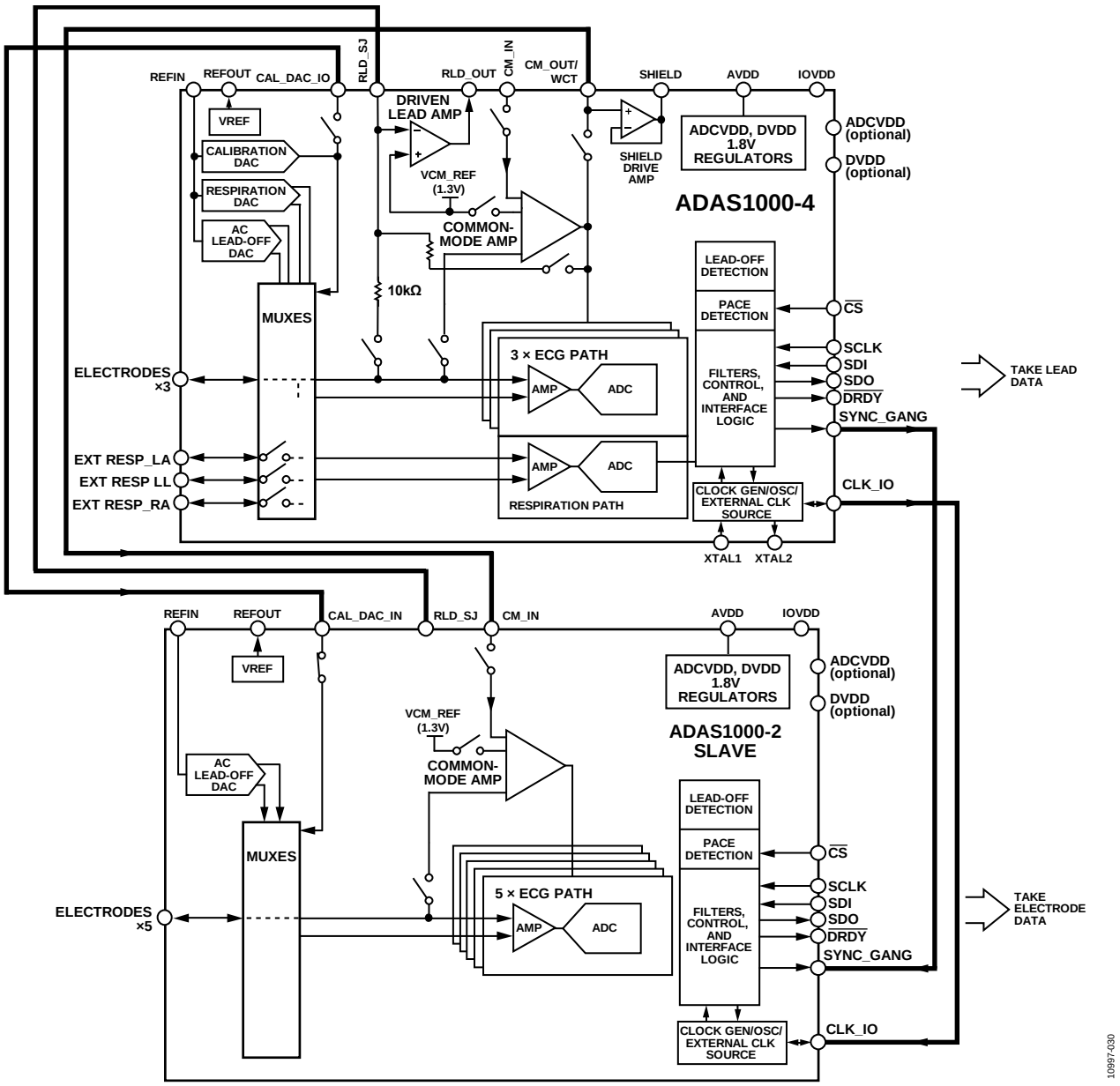


Figure 74. Configuring Multiple Devices to Extend Number of Electrodes/Leads
(This example uses ADAS1000-4 as master and ADAS1000-2 as slave; other arrangements possible.)

Table 17. Some Possible Arrangements for Gang Operation

Master	Slave 1	Slave 2	Features	Number of Electrodes	Number of Leads
ADAS1000	ADAS1000-2		ECG, respiration, pace	10 ECG, CM_IN, RLD	12-lead + spare ADC channel
ADAS1000	ADAS1000-2	ADAS1000-2	ECG, respiration, pace	15 ECG, CM_IN, RLD	15-lead + 3 spare ADC channels
ADAS1000	ADAS1000-3		ECG, respiration, pace	8 ECG, CM_IN, RLD	12-lead (derived leads)
ADAS1000-3	ADAS1000-2		ECG	8 ECG, CM_IN, RLD	12-lead (derived leads)
ADAS1000-4	ADAS1000-2		ECG, respiration, pace	8 ECG, CM_IN, RLD	12-lead (derived leads)

INTERFACING IN GANG MODE

As shown in Figure 74, when using multiple devices, the user must collect the ECG data directly from each device. The example shown in Figure 75 illustrates one possibility of how to approach interfacing to a master and slave device.

Note that SCLK, SDO, and SDI are shared here with individual $\overline{CS}$ lines. This requires the user to read the data on both devices twice as fast to ensure that they can capture all the data to maintain the chosen data rate and ensure they have the relevant synchronized data. Alternative methods might use individual controllers for each device or separate SDO paths.

For some applications, digital isolation is required between the host and the ADAS1000-3/ADAS1000-4. The example shown illustrates a means to ensure that the number of lines requiring isolation is minimized.

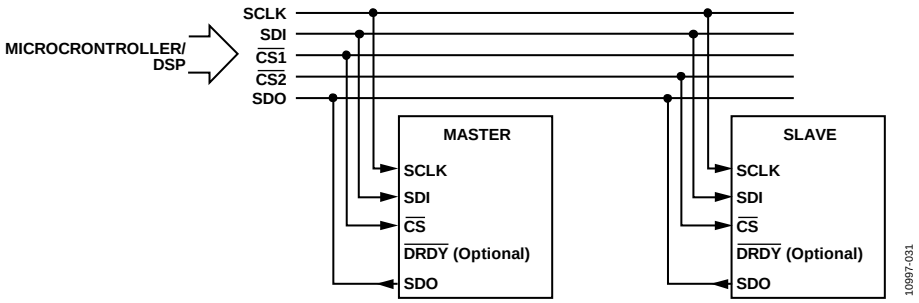


Figure 75. One Method of Interfacing to Multiple Devices

SERIAL INTERFACES

The ADAS1000-3/ADAS1000-4 are controlled via a standard serial interface allowing configuration of registers and readback of ECG data. This is an SPI-compatible interface that can operate at SCLK frequencies up to 40 MHz.

The ADAS1000-3/ADAS1000-4 also provide an optional secondary serial interface that is capable of providing ECG data at the 128 kHz data rate for users wishing to apply their own digital pace detection algorithm. This is a master interface that operates with an SCLK of 20.48 MHz.

STANDARD SERIAL INTERFACE

The standard serial interface is LVTTL-compatible when operating from a 2.3 V to 3.6 V IOVDD supply. This is the primary interface for controlling the ADAS1000-3/ADAS1000-4 reading and writing registers, and reading frame data containing all the ECG data-words and other status functions within the device.

The SPI is controlled by the following five pins:

- $\overline{CS}$ (frame synchronization input). Asserting $\overline{CS}$ low selects the device. When $\overline{CS}$ is high, data on the SDI pin is ignored. If $\overline{CS}$ is inactive, the SDO output driver is disabled so that multiple SPI devices can share a common SDO pin. The $\overline{CS}$ pin can be tied low to reduce the number of isolated paths required. When $\overline{CS}$ is tied low, there is no frame around the data-words; therefore, the user must be aware of where they are within the frame. All data-words with 2 kHz and 16 kHz data rates contain register addresses at the start of each word within the frame. Users can resynchronize the interface by holding SDI high for 64 SCLK cycles, followed by a read of any register so that SDI is brought low for the first bit of the following word.
- SDI (serial data input pin). Data on SDI is clocked into the device on the rising edges of SCLK.
- SCLK (clocks data in and out of the device). SCLK should idle high when $\overline{CS}$ is high.
- SDO (serial data output pin for data readback). Data is shifted out on SDO on the falling edges of SCLK. The SDO output driver is high-Z when $\overline{CS}$ is high.
- $\overline{DRDY}$ (data ready, optional). Data ready when low, busy when high. Indicates the internal status of the ADAS1000-3/ADAS1000-4 digital logic. It is driven high/busy during reset. If data frames are enabled and the frame buffer is empty, this pin is driven busy/high. If the frame buffer is full, this pin is driven low/ready. If data frames are not enabled, this pin is driven low to indicate that the device is ready to accept register read/write commands. When reading packet data, the entire packet must be read to allow the $\overline{DRDY}$ return back high.

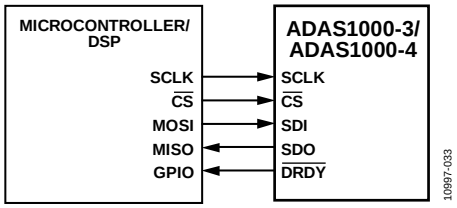


Figure 76. Serial Interface

Write Mode

The serial word for a write is 32 bits long, MSB first. The serial interface works with both a continuous and a burst (gated) serial clock. The falling edge of $\overline{CS}$ starts the write cycle. Serial data applied to SDI is clocked into the ADAS1000-3/ADAS1000-4 on rising SCLK edges. At least 32 rising clock edges must be applied to SCLK to clock in 32 bits of data before $\overline{CS}$ is taken high again. The addressed input register is updated on the rising edge of $\overline{CS}$. For another serial transfer to take place, $\overline{CS}$ must be taken low again. Register writes are used to configure the device. Once the device is configured and enabled for conversions, frame data can be initiated to start clocking
out ECG data on SDO at the programmed data rate. Normal operation for the device is to send out frames of ECG data. Typically, register reads and writes should be needed only during start-up configuration. However, it is possible to write new configuration data to the device while in framing mode. A new write command is accepted within the frame and, depending on the nature of the command, there may be a need to flush out the internal filters (wait periods) before seeing usable framing data again.

Write/Read Data Format

Address, data, and the read/write bits are all in the same word. Data is updated on the rising edge of $\overline{CS}$ or the first cycle of the following word. For all write commands to the ADAS1000-3/ADAS1000-4, the data-word is 32 bits, as shown in Table 18. Similarly, when using data rates of 2 kHz and 16 kHz, each word is 32 bits (address bits and data bits).

Table 18. Serial Bit Assignment (Applies to All Register Writes, 2 kHz and 16 kHz Reads)

B31	[B30:B24]	[B23:B0]
$\overline{R}$/W	Address Bits[6:0]	Data Bits[23:0] (MSB first)

For register reads, data is shifted out during the next word, as shown in Table 19.

Table 19. Read/Write Data Stream

Digital Pin	Command 1	Command 2	Command 2
SDI	Read Address 1	Read Address 2	Write Address 3
SDO		Address 1	Address 2
		Read Data 1	Read Data 2

In the 128 kHz data rate, all write words are still 32-bit writes but the read words in the data packet are now 16 bits (upper 16 bits of register). There are no address bits, only data bits. Register space that is larger than 16 bits spans across 2 × 16-bit words (for example, pace and respiration).

Data Frames/Packets

The general data packet structure is shown in Table 18. Data can be received in two different frame formats. For the 2 kHz and 16 kHz data rates, a 32-bit data format is used (where the register address is encapsulated in the upper byte, identifying the word within the frame) (see Table 22). For the 128 kHz data rate, words are provided in 16-bit data format (see Table 23).

When the configuration is complete, the user can begin reading frames by issuing a read command to the frame header register (see Table 53). The ADAS1000-3/ADAS1000-4 continue to make frames available until another register address is written (read or write command). To continue reading frame data, continue to write all zeros on SDI, which is a write of the NOP register (Address 0x00). A frame is interrupted only when another read or write command is issued.

Each frame can be a large amount of data plus status words. $\overline{CS}$ can toggle between each word of data within a frame, or it can be held constantly low during the entire frame.

Reading all the data-words creates a frame containing 10 × 32 bit words when reading at 2 kHz or 16 kHz data rates; similarly, a frame contains 13 × 16-bit words when reading at 128 kHz. Additionally any words not required can be excluded from the frame. To arrange the frame with the words of interest, configure the appropriate bits in the frame control register (see Table 37). The complete set of words per frame are 10 × 32-bit words for the 2 kHz or 16 kHz data rates, or 13 × 16-bit words at 128 kHz.

Any data not available within the frame can be read between frames. Reading a register interrupts the frame and requires the user to issue a new read command of Address 0x40 (see Table 53) to start framing again.

Read Mode

Although the primary reading function within the ADAS1000-3/ADAS1000-4 is the output of the ECG frame data, the devices also allow reading of all configuration registers. To read a register, the user must first address the device with a read command containing the particular register address. If the device is already in data framing mode, the read register command can be interleaved between the frames by issuing a read register command during the last word of frame data. Data shifted out during the next word is the register read data. To return to framing mode, the user must re-enable framing by issuing a read of the frame header register (Address 0x40) (see Table 53). This register write can be used to flush out the register contents from the previous read command.

Table 20. Example of Reading Registers and Frames

SDI	…..	NOP	Read Address N	Read frames	NOP	NOP	…..
SDO	…..	Frame data	Frame CRC	Register Data N	Frame header	Frame data	…..

Regular register reads are always 32 bits long and MSB first.

Serial Clock Rate

The SCLK can be up to 40 MHz, depending on the IOVDD voltage level as shown in Table 5. The minimum SCLK frequency is set by the requirement that all frame data be clocked out before the next frame becomes available.

SCLK (min) = *frame_rate* × *words_per_frame* × *bits_per_word*

The minimum SCLK for the various frame rates is shown in Table 21.

Table 21. SCLK Clock Frequency vs. Packet Data/Frame Rates

Frame Rate	Word Size	Maximum Words/Frame[1]	Minimum SCLK
128 kHz	16 bits	13 words	26.62 MHz
16 kHz	32 bits	10 words	5.12 MHz
2 kHz	32 bits	10 words	640 kHz

[1] This is the full set of words that a frame contains. It is programmable and can be configured to provide only the words of interest. See Table 37.

Table 22. Default 2 kHz and 16 kHz Data Rate: 32-Bit Frame Word Format

Register	Header	Lead I/LA	Lead II/LL	Lead III/RA	PACE	RESPM	RESPPH	LOFF	GPIO	CRC
Address	0x40	0x11	0x12	0x13	0x1A	0x1B	0x1C	0x1D	0x06	0x41

Table 23. Default 128 kHz Data Rate: 16-Bit Frame Word Format

Register	Header	Lead I/LA	Lead II/LL	Lead III/RA	PACE1	PACE2	RESPM1	RESPM2	RESPH1	RESPH2	LOFF	GPIO	CRC
Address	0x40	0x11	0x12	0x13	0x1A		0x1B		0x1C		0x1D	0x06	0x41

Internal operations are synchronized to the internal master clock at either 2.048 MHz or 1.024 MHz (ECGCTL[3]: HP = 1 and HP = 0, respectively, see Table 28). Because there is no guaranteed relationship between the internal clock and the SPI's SCLK signal, an internal handshaking scheme is used to ensure safe data transfer between the two clock domains. A full handshake requires three internal clock cycles and imposes an upper speed limit on the SCLK frequency when reading frames with small word counts. This is true for all data frame rates.

SCLK (max) = (1.024 MHz × (1 + HP) × words_per_frame × bits_per_word)/3; or 40 MHz, whichever is lower.

Exceeding the maximum SCLK frequency for a particular operating mode causes erratic behavior in the $\overline{\text{DRDY}}$ signal and results in the loss of data.

Data Rate and Skip Mode

Although the standard frame rates available are 2 kHz, 16 kHz, and 128 kHz, there is also a provision to skip frames to further reduce the data rate. This can be configured in the frame control register (see Table 37).

Data Ready ($\overline{\text{DRDY}}$)

The $\overline{\text{DRDY}}$ pin is used to indicate that a frame composed of decimated data at the selected data rate is available to read. It is high when busy and low when ready. Send commands only when the status of $\overline{\text{DRDY}}$ is low or ready. During power-on, the status of $\overline{\text{DRDY}}$ is high (busy) while the device initializes itself. When initialization is complete, $\overline{\text{DRDY}}$ goes low and the user can start configuring the device for operation. When the device is configured and enabled for conversions by writing to the conversion bit (CNVEN) in the ECGCTL register, the ADCs start to convert and the digital interface starts to make data available, loading them into the buffer when ready. If conversions are enabled and the buffer is empty, the device is not ready and $\overline{\text{DRDY}}$ goes high. Once the buffer is full, $\overline{\text{DRDY}}$ goes low to indicate that data is ready to be read out of the device. If the device is not enabled for conversions, the $\overline{\text{DRDY}}$ ignores the state of the buffer full status.

When reading packets of data, the entire data packet must be read; otherwise, $\overline{\text{DRDY}}$ stays low.

There are three methods of detecting $\overline{\text{DRDY}}$ status.

- $\overline{\text{DRDY}}$ pin. This is an output pin from the ADAS1000-3/ADAS1000-4 that indicates the device read or busy status. No data is valid while this pin is high. The $\overline{\text{DRDY}}$ signals that data is ready to be read by driving low and remaining low until the entire frame has been read. It is cleared when the last bit of the last word in the frame is clocked onto SDO. The use of this pin is optional.
- SDO pin. The user can monitor the voltage level of the SDO pin by bringing $\overline{\text{CS}}$ low. If SDO is low, data is ready; if high, busy. This does not require clocking the SCLK input. (CPHA = CPOL = 1 only).
- One of the first bits of valid data in the header word available on SDO is a data ready status bit (see Table 43). Within the configuration of the ADAS1000-3/ADAS1000-4, the user can set the header to repeat until the data is ready. See Bit 6 (RDYRPT) in the frame control register in Table 37.

The host controller must read the entire frame to ensure $\overline{\text{DRDY}}$ returns low and ready. If the host controller treats the $\overline{\text{DRDY}}$ as an edge triggered signal and then misses a frame or underruns, the $\overline{\text{DRDY}}$ remains high because there is still data available to read. The host controller must treat the $\overline{\text{DRDY}}$ signal as level triggered, ensuring that whenever it goes low, it generates an interrupt which can initiate a SPI frame transfer. On completion of the transfer the $\overline{\text{DRDY}}$ returns high.

Detecting Missed Conversion Data

To ensure that the current data is valid, the entire frame must be read at the selected data rate. If a read of the entire frame takes longer than the selected data rate allows, the internal buffer is not loaded with the latest conversion data. The frame header register (see Table 53) provides four settings to indicate an overflow of frame data. The settings of Bits[29:28] report how many frames have been missed since the last valid frame read. A missed frame may occur as a result of the last read taking too long. The data in the current frame is valid data, but it is not the current data. It is the calculation made directly after the last valid read.

To clear such an overflow, the user must read the entire frame.

CRC Word

Framed data integrity is provided by CRCs. For the 128 kHz frame rates, the 16-bit CRC-CCITT polynomial is used. For the 2 kHz and 16 kHz frame rates, the 24-bit CRC polynomial used.

In both cases, the CRC residue is preset to all 1s and inverted before being transmitted. The CRC parameters are summarized in Table 24. To verify that data was correctly received, software should compute a CRC on both the data and the received checksum. If data and checksum are received correctly, the resulting CRC residue should equal the check constant shown in Table 24. Note that data is shifted through the generator polynomial MSB first, the same order that it is shifted out serially. The bit and byte order of the CRC that is appended to the frame is such that the MSB of the CRC is shifted through the generator polynomial first in the same order as the data so that the CRC residue XOR'd with the inverted CRC at the end of the frame is all 1s (which is why the check constant is identical for all messages). The CRC is based only on the data that is sent out.

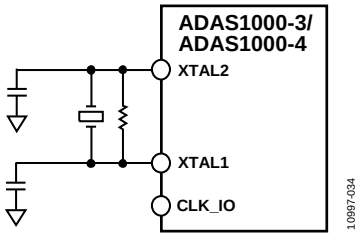


Figure 77. Input Clock

Clocks

The ADAS1000-3/ADAS1000-4 run from an external crystal or clock input frequency of 8.192 MHz. The external clock input is provided for use in gang mode so conversions between the two devices are synchronized. In this mode, the CLK_IO pin is an output from the master and an input from the slave. To reduce power, the CLK_IO is disabled when not in gang mode.

All features within the ADAS1000-3/ADAS1000-4 are a function of the frequency of the externally applied clock. Using a frequency other than the 8.192 MHz previously noted causes scaling of the data rates, filter corners, ac leads-off frequency, respiration frequency, and pace algorithm corners accordingly.

Table 24. CRC Polynomials

Frame Rate	CRC Size	Polynomial	Polynomial in Hex	Check Constant
2 kHz, 16 kHz	24 bits	$x^{24} + x^{22} + x^{20} + x^{19} + x^{18} + x^{16} + x^{14} + x^{13} + x^{11} + x^{10} + x^8 + x^7 + x^6 + x^3 + x^1 + x^0$	0x15D6DCB	0x15A0BA
128 kHz	16 bits	$x^{16} + x^{12} + x^5 + x^0$	0x11021	0x1D0F

SECONDARY SERIAL INTERFACE

This second serial interface is an optional interface that can be used for the user's own pace detection purposes. This interface contains ECG data at 128 kHz data rate only. If using this interface, the ECG data is still available on the standard interface discussed previously at lower rates with all the decimation and filtering applied. If this interface is inactive, it draws no power.

Data is available in 16-bit words, MSB first.

This interface is a master interface, with the ADAS1000-3/ ADAS1000-4 providing the SCLK, $\overline{CS}$, SDO. Is it shared across some of the existing GPIO pins as follows:

- GPIO1/MSCLK
- GPIO0/$\overline{MCS}$
- GPIO2/MSDO

This interface can be enabled via the GPIO register (see Table 33).

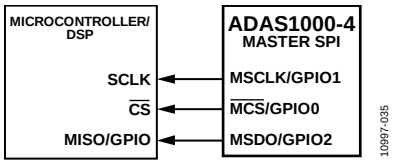


Figure 78. Master SPI Interface for External Pace Detection Purposes

The data format of the frame starts with a header word, three ECG data-words, two words filled with zeros and completes with the same CRC word as documented in Table 24 for the 128 kHz rate. All words are 16 bits. MSCLK runs at approximately 20 MHz and the $\overline{MCS}$ function is asserted for the entire frame with the data available on MSDO on the falling edge of MSCLK. MSCLK idles high when $\overline{MCS}$ is deasserted.

The data format for this interface is fixed and not influenced by the FRMCTL register settings. All six words are output, even if the individual channels are not enabled.

The header word consists of four bits of all 1s followed by a 12-bit sequence counter. This sequence counter increments after every frame is sent, thereby allowing the user to tell if any frames have been missed and how many.

$\overline{RESET}$

There are two methods of resetting the ADAS1000-3/ADAS1000-4 to power-on default. Bringing the $\overline{RESET}$ line low or setting the SWRST bit in the ECGCTL register (Table 28) resets the contents of all internal registers to their power-on reset state. The falling edge of the $\overline{RESET}$ pin initiates the reset process; $\overline{DRDY}$ goes high for the duration, returning low when the $\overline{RESET}$ process is complete. This sequence takes 1.5 ms maximum. Do not write to the serial interface while $\overline{DRDY}$ is high handling a $\overline{RESET}$ command. When $\overline{DRDY}$ returns low, normal operation resumes and the status of the $\overline{RESET}$ pin is ignored until it goes low again. Software reset using the SWRST bit (see Table 28) requires that a NOP (no operation) command be issued to complete the reset cycle.

$\overline{PD}$ FUNCTION

The $\overline{PD}$ pin powers down all functions in low power mode. The digital registers maintain their contents. The power-down function is also available via the serial interface (ECG control register, see Table 28).

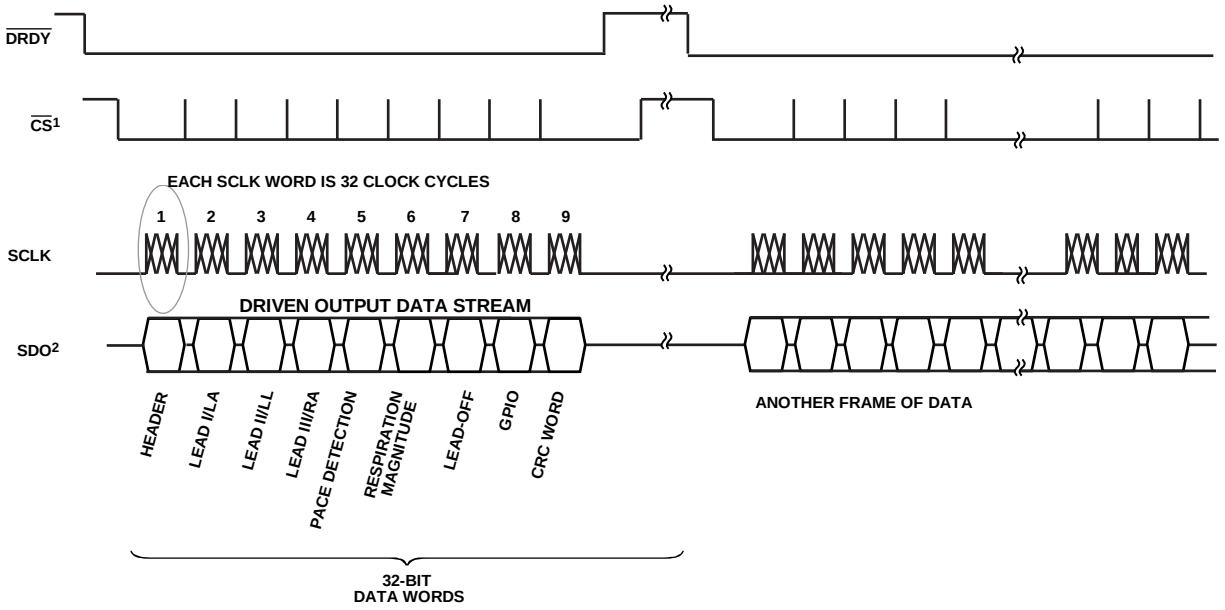
Table 25. Master SPI Frame Format; All Words are 16 Bits

Mode\Word	1	2	3	4	5	6	7
Electrode mode[1]	Header	ECG1_LA	ECG2_LL	ECG3_RA	All 0's	All 0's	CRC
Analog lead mode[1]	Header	LEAD I	LEAD III	–LEAD II (RA-LL)	All 0's	All 0's	CRC

[1] As set by the FRMCTL register data DATAFMT, Bit [4], see Table 37.

SPI OUTPUT FRAME STRUCTURE (ECG AND STATUS DATA)

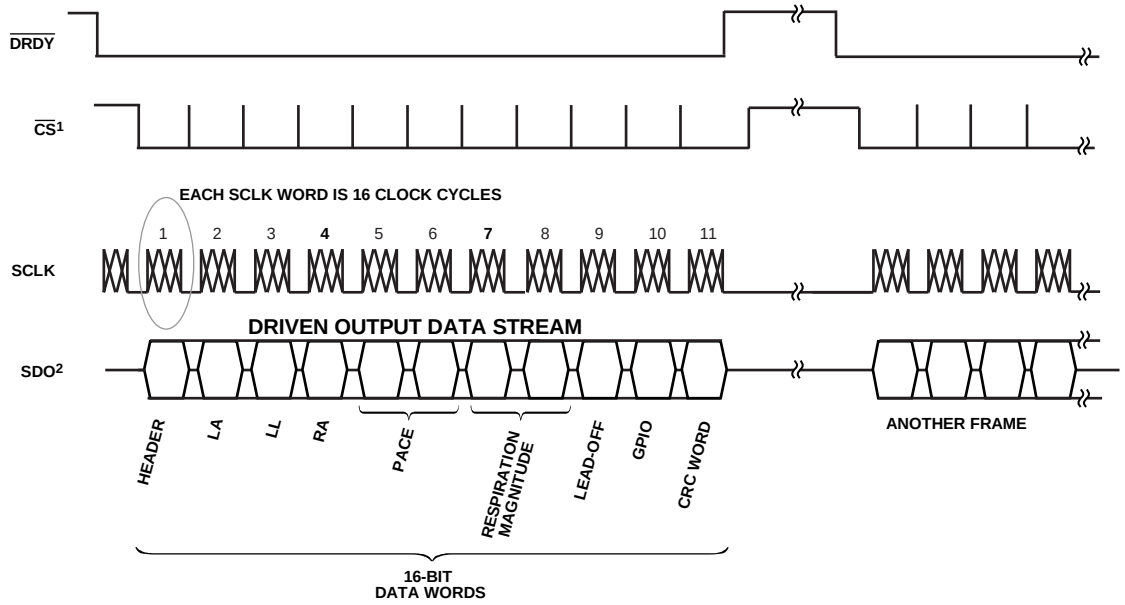
Three data rates are offered for reading ECG data: low speed 2 kHz/16 kHz rates for electrode/lead data (32-bit words) and a high speed 128 kHz for electrode/lead data (16-bit words).



1 $\overline{CS}$ MAY BE USED IN ONE OF THE FOLLOWING WAYS:
A) HELD LOW ALL THE TIME.
B) USED TO FRAME THE ENTIRE PACKET OF DATA.
C) USED TO FRAME EACH INDIVIDUAL 32-BIT WORD.
2 FULL WORD COUNT = 10 (RESPIRATION PHASE EXCLUDED HERE). WORDS MAY BE EXCLUDED, SEE THE FRMCTL REGISTER.

10997-036

Figure 79. Output Frame Structure for 2 kHz and 16 kHz Data Rates with SDO Data Configured for Electrode or Lead Data



1 $\overline{CS}$ MAY BE USED IN ONE OF THE FOLLOWING WAYS:
A) HELD LOW ALL THE TIME.
B) USED TO FRAME THE ENTIRE PACKET OF DATA.
C) USED TO FRAME EACH INDIVIDUAL 16-BIT WORD.
2 FULL WORD COUNT = 13 (RESPIRATION PHASE EXCLUDED HERE). WORDS MAY BE EXCLUDED, SEE THE FRMCTL REGISTER.

10997-037

Figure 80. Output Frame Structure for 128 kHz Data Rate with SDO Data Configured for Electrode Data
(The 128 kHz Data Rate Can Provide Single-Ended Electrode Data or Analog Lead Mode Data Only. Digital Lead Mode Is Not Available at 128 kHz Data Rate.)

SPI REGISTER DEFINITIONS AND MEMORY MAP

In 2 kHz and 16 kHz data rates, data takes the form of 32-bit words. Bit A6 to Bit A0 serve as word identifiers. Each 32-bit word has 24 bits of data. A third high speed data rate is also offered: 128 kHz with data in the form of 16-bit words (all 16 bits as data).

Table 26. SPI Register Memory Map

$\overline{R}/W$[1]	A[6:0]	D[23:0]	Register Name	Table	Register Description	Reset Value
R	0x00	XXXXXX	NOP		NOP (no operation)	0x000000
R/W	0x01	dddddd	ECGCTL	Table 28	ECG control	0x000000
R/W	0x02	dddddd	LOFFCTL	Table 29	Lead-off control	0x000000
R/W	0x03	dddddd	RESPCTL	Table 30	Respiration control[2]	0x000000
R/W	0x04	dddddd	PACECTL	Table 31	Pace detection control	0x000F88
R/W	0x05	dddddd	CMREFCTL	Table 32	Common-mode, reference, and shield drive control	0xE00000
R/W	0x06	dddddd	GPIOCTL	Table 33	GPIO control	0x000000
R/W	0x07	dddddd	PACEAMPTH	Table 34	Pace amplitude threshold[2]	0x242424
R/W	0x08	dddddd	TESTTONE	Table 35	Test tone	0x000000
R/W	0x09	dddddd	CALDAC	Table 36	Calibration DAC	0x002000
R/W	0x0A	dddddd	FRMCTL	Table 37	Frame control	0x079000
R/W	0x0B	dddddd	FILTCTL	Table 38	Filter control	0x000000
R/W	0x0C	dddddd	LOFFUTH	Table 39	AC lead-off upper threshold	0x00FFFF
R/W	0x0D	dddddd	LOFFLTH	Table 40	AC lead-off lower threshold	0x000000
R/W	0x0E	dddddd	PACEEDGETH	Table 41	Pace edge threshold[2]	0x000000
R/W	0x0F	dddddd	PACELVLTH	Table 42	Pace level threshold[2]	0x000000
R	0x11	XXXXXX	LADATA	Table 43	LA or Lead I data	0x000000
R	0x12	XXXXXX	LLDATA	Table 43	LL or Lead II data	0x000000
R	0x13	XXXXXX	RADATA	Table 43	RA or Lead III data	0x000000
R	0x1A	XXXXXX	PACEDATA	Table 44	Read pace detection data/status[2]	0x000000
R	0x1B	XXXXXX	RESPMAG	Table 45	Read respiration data—magnitude[2]	0x000000
R	0x1C	XXXXXX	RESPPH	Table 46	Read respiration data—phase[2]	0x000000
R	0x1D	XXXXXX	LOFF	Table 47	Lead-off status	0x000000
R	0x1E	XXXXXX	DCLEAD-OFF	Table 48	DC lead-off	0x000000
R	0x1F	XXXXXX	OPSTAT	Table 49	Operating state	0x000000
R/W	0x21	dddddd	CALLA	Table 50	User gain calibration LA	0x000000
R/W	0x22	dddddd	CALLL	Table 50	User gain calibration LL	0x000000
R/W	0x23	dddddd	CALRA	Table 50	User gain calibration RA	0x000000
R	0x31	dddddd	LOAMLA	Table 51	Lead-off amplitude for LA	0x000000
R	0x32	dddddd	LOAMLL	Table 51	Lead-off amplitude for LL	0x000000
R	0x33	dddddd	LOAMRA	Table 51	Lead-off amplitude for RA	0x000000
R	0x3A	dddddd	PACE1DATA	Table 52	Pace1 width and amplitude[2]	0x000000
R	0x3B	dddddd	PACE2DATA	Table 52	Pace2 width and amplitude[2]	0x000000
R	0x3C	dddddd	PACE3DATA	Table 52	Pace3 width and amplitude[2]	0x000000
R	0x40	dddddd	FRAMES	Table 53	Frame header	0x800000
R	0x41	XXXXXX	CRC	Table 54	Frame CRC	0xFFFFFF
x	Other	XXXXXX	Reserved[3]		Reserved	XXXXXX

[1] R/W = register both readable and writable; R = read only.
[2] ADAS1000-4 model only, ADAS1000-3 model does not contain these features.
[3] Reserved bits in any register are undefined. In some cases, a physical (but unused) memory bit may be present—in other cases not. Do not issue commands to reserved registers/space. Read operations of unassigned bits are undefined.

CONTROL REGISTERS DETAILS

For each register address, the default setting is noted in a default column in addition to being noted in the function column by "(default)"; this format applies throughout the register map.

Table 27. Serial Bit Assignment

B31	[B30:B24]	[B23:B0]
$\overline{R}$/W	Address bits	Data bits (MSB first)

Table 28. ECG Control Register (ECGCTL) Address 0x01, Reset Value = 0x000000

$\overline{R}$/W	Default	Bit	Name	Function
R/W R/W R/W	0 0 0	23 22 21	LAEN LLEN RAEN	ECG channel enable; shuts down power to the channel; the input becomes high-Z. 0 (default) = disables ECG channel. When disabled, the entire ECG channel is shut down and dissipates minimal power. 1 = enables ECG channel.
R/W	0	[20:11]	Reserved	Reserved, set to 0.
R/W	0	10	CHCONFIG	Setting this bit selects the differential analog front-end (AFE) input. See Figure 56. 0 (default) = single-ended input (digital lead mode or electrode mode). 1 = differential input (analog lead mode).
R/W	00	[9:8]	GAIN [1:0]	Preamplifier and anti-aliasing filter overall gain. 00 (default) = GAIN 0 = ×1.4. 01 = GAIN 1 = ×2.1. 10 = GAIN 2 = ×2.8. 11 = GAIN 3 = ×4.2 (user gain calibration is required for this gain setting).
R/W	0	7	VREFBUF	VREF buffer enable. 0 (default) = disabled. 1 = enabled (when using the internal VREF, VREFBUF must be enabled).
R/W	0	6	CLKEXT	Use external clock instead of crystal oscillator. The crystal oscillator is automatically disabled if configured as a slave in gang mode and the slave device should receive the clock from the master device. 0 (default) = XTAL is clock source. 1 = CLK_IO is clock source.
R/W	0	5	Master	In gang mode, this bit selects the master (SYNC_GANG pin is configured as an output). When in single channel mode (gang = 0), this bit is ignored. 0 (default) = slave. 1 = master.
R/W	0	4	Gang	Enable gang mode. Setting this bit causes CLK_IO and SYNC_GANG to be activated. 0 (default) = single channel mode. 1 = gang mode.
R/W	0	3	HP	Selects the noise/power performance. This bit controls the ADC sampling frequency. See the Specifications section for further details. This bit also affects the respiration carrier frequency as discussed in the Respiration Carrier Frequency section. 0 (default) = 1 MSPS, low power. 1 = 2 MSPS, high performance/low noise.
R/W	0	2	CNVEN	Conversion enable. Setting this bit enables the ADC conversion and filters. 0 (default) = idle. 1 = conversion enable.
R/W	0	1	PWREN	Power enable. Clearing this bit powers down the device. All analog blocks are powered down and the external crystal is disabled. The register contents are retained during power down as long as DVDD is not removed. 0 (default) = power down. 1 = power enable.
R/W	0	0	SWRST	Software reset. Setting this bit clears all registers to their reset value. This bit automatically clears itself. The software reset requires a NOP command to complete the reset. 0 (default) = NOP. 1 = reset.

Table 29. Lead-Off Control Register (LOFFCTL) Address 0x02, Reset Value = 0x000000

R/$\overline{W}$	Default	Bit	Name	Function
R/W	0	23	LAPH	AC lead-off phase.
R/W	0	22	LLPH	0 (default) = in phase.
R/W	0	21	RAPH	1 = 180° out of phase.
R/W	0	[20:19]	Reserved	Reserved, set to 0.
R/W	0	18	CEPH	AC lead-off phase. 0 (default) = in phase. 1 = 180° out of phase.
R/W	0	17	LAACLOEN	Individual electrode ac lead-off enable. AC lead-off enables are the OR of ACSEL and the individual ac lead-off channel enables.
R/W	0	16	LLACLOEN	0 (default) = ac lead-off disabled.
R/W	0	15	RAACLOEN	1 = ac lead-off enabled.
R/W	0	[14:13]	Reserved	Reserved, set to 0.
R/W	0	12	CEACLOEN	Individual electrode ac lead-off enable. AC lead-off enables are the OR of ACSEL and the individual ac lead-off channel enables. 0 (default) = ac lead-off disabled. 1 = ac lead-off enabled.
R/W	0	[11:9]	Reserved	Reserved, set to 0.
R/W	00	[8:7]	ACCURRENT	Set current level for ac lead-off. 00 (default) = 12.5 nA rms. 01 = 25 nA rms. 10 = 50 nA rms. 11 = 100 nA rms.
R/W	00	[6:5]	Reserved	Reserved, set to 0.
R/W	000	[4:2]	DCCURRENT	Set current level for dc lead-off (active only for ACSEL = 0). 000 (default) = 0 nA. 001 = 10 nA. 010 = 20 nA. 011 = 30 nA. 100 = 40 nA. 101 = 50 nA. 110 = 60 nA. 111 = 70 nA.
R/W	0	1	ACSEL	DC or AC (out-of-band) lead-off detection. ACSEL acts as a global ac lead-off enable for RA, LL, LA, electrodes (CE ac lead-off is not enabled using ACSEL). AC lead-off enables are the OR of ACSEL and the individual ac lead-off channel enables. If LOFFEN = 0, this bit is don't care. If LOFFEN = 1, 0 (default) = dc lead-off detection enabled. (Individual ac lead-off can be enabled through Bits[17:12].) 1 = dc lead-off detection disabled. AC lead-off detection enabled (all electrodes except CE electrode). When the calibration DAC is enabled, ac lead-off is disabled.
R/W	0	0	LOFFEN	Enable lead-off detection. 0 (default) = lead-off disabled. 1 = lead-off enabled.

Table 30. Respiration Control Register (RESPCTL) Address 0x03, Reset Value = 0x000000[1]

R/W	Default	Bit	Name	Function
		[23:17]	Reserved	Reserved, set to 0.
R/W	0	16	RESPALTFREQ	Setting this bit to 1 makes the respiration waveform on the GPIO3 pin periodic every cycle. Use in conjunction with RESFREQ to select drive frequency. 0 (default) = periodic every N cycles (default). 1 = periodic every cycle.
R/W	0	15	RESPEXTSYNC	Set this bit to 1 to drive the MSB of the respiration DAC out onto the GPIO3 pin. This signal can be used to synchronize an external generator to the respiration carrier. It is a constant period only when RESPALTFREQ = 1. 0 (default) = normal GPIO3 function. 1 = MSB of RESPDAC driven onto the GPIO3 pin.
R/W	0	14	RESPEXTAMP	For use with an external instrumentation amplifier with respiration circuit. Bypasses the on-chip amplifier stage and input directly to the ADC. See Figure 69. 0 (default) = disabled. 1 = enabled.
R/W	0	13	RESPOUT	Selects external respiration drive output. RESPDAC_RA is automatically selected when RESPCAP = 1 0 (default) = RESPDAC_LL and RESPDAC_RA. 1 = RESPDAC_LA and RESPDAC_RA.
R/W	0	12	RESPCAP	Selects source of respiration capacitors. 0 (default) = use internal capacitors. 1 = use external capacitors.
R/W	0000	[11:8]	RESPGAIN [3:0]	Respiration in amp gain (saturates at 10). 0000 (default) = ×1 gain. 0001 = ×2 gain. 0010 = ×3 gain. … 1000 = ×9 gain. 1001 = ×10 gain. 11xx = ×10 gain.
R/W	0	7	RESPEXTSEL	Selects between EXT_RESP _LA or EXT_RESP_LL paths. Applies only if the external respiration is selected in RESPSEL. EXT_RESP_RA is automatically enabled. 0 (default) = EXT_RESP_LL. 1 = EXT_RESP_LA.
R/W	00	[6:5]	RESPSEL [1:0]	Set leads for respiration measurement. 00 (default) = Lead I. 01 = Lead II. 10 = Lead III. 11 = external respiration path.
R/W	00	[4:3]	RESPAMP	Set the test tone amplitude for respiration drive signal. 00 (default) = amplitude/8. 01 = amplitude/4. 10 = amplitude/2. 11 = amplitude.
R/W	00	[2:1]	RESPFREQ	Set frequency for respiration.

RESPFREQ	RESPALTFREQ = 0	RESPALTFREQ = 1 (periodic)
00 (default)	56 kHz	64 kHz
01	54 kHz	56.9 kHz
10	52 kHz	51.2 kHz
11	50 kHz	46.5 kHz

R/W	0	0	RESPEN	Enable respiration. 0 (default) = respiration disabled. 1 = respiration enabled.

[1] ADAS1000-4 model only, ADAS1000-3 model does not contain this feature.

Table 31. Pace Detection Control Register (PACECTL) Address 0x04, Reset Value = 0x000F88[1]

R/W	Default	Bit	Name	Function
		[23:12]	Reserved	Reserved, set to 0
R/W	1	11	PACEFILTW	Pace width filter 0 = filter disabled 1 (default) = filter enabled
R/W	1	10	PACETFILT2	Pace Validation Filter 2 0 = filter disabled 1 (default) = filter enabled
R/W	1	9	PACETFILT1	Pace Validation Filter 1 0 = filter disabled 1 (default) = filter enabled
R/W R/W R/W	11 00 01	[8:7] [6:5] [4:3]	PACE3SEL [1:0] PACE2SEL [1:0] PACE1SEL [1:0]	Set lead for pace detection measurement 00 = Lead I 01 = Lead II 10 = Lead III 11 = Lead aVF
R/W R/W R/W	0 0 0	2 1 0	PACE3EN PACE2EN PACE1EN	Enable pace detection algorithm 0 (default) = pace detection disabled 1 = pace detection enabled

[1] ADAS1000-4 model only, ADAS1000-3 model does not contain this feature.

Table 32. Common-Mode, Reference, and Shield Drive Control Register (CMREFCTL) Address 0x05, Reset Value = 0xE00000

R/W	Default	Bit	Name	Function
R/W	1	23	LACM	Common-mode electrode select.
R/W	1	22	LLCM	Any combination of the five input electrodes can be used to create the common-mode signal, VCM. Bits[23:19] are ignored when Bit 2 is selected. Common mode is the average of the selected electrodes. When a single electrode is selected, common mode is the signal level of that electrode alone. The common-mode signal can be driven from the internal VCM_REF (1.3 V) when Bits [23:19] = 0.
R/W	1	21	RACM	0 = does not contribute to the common mode. 1 = contributes to the common mode.
R/W	0	[20:15]	Reserved	Reserved, set to 0.
R/W	0	14	LARLD	RLD summing junction.
R/W	0	13	LLRLD	0 (default) = does not contribute to RLD input.
R/W	0	12	RARLD	1 = contributes to RLD input.
R/W	0	[11:10]	Reserved	Reserved, set to 0.
R/W	0	9	CERLD	RLD summing junction. 0 (default) = does not contribute to RLD input. 1 = contributes to RLD input.
R/W	0	8	CEREFEN	Common electrode (CE) reference, see Figure 56. 0 (default) = common electrode disabled. 1 = common electrode enabled.
R/W	0000	[7:4]	RLDSEL [3:0]	Select electrode for reference drive. 0000 (default) = RLD_OUT. 0001 = LA. 0010 = LL. 0011 = RA. 0100 to 1111 = reserved.
R/W	0	3	DRVCM	Common-mode output. When set, the internally derived common-mode signal is driven out of the common-mode pin. This bit has no effect if an external common mode is selected. 0 (default) = common mode is not driven out. 1 = common mode is driven out of the external common-mode pin.
R/W	0	2	EXTCM	Select the source of common mode (use when operating multiple devices together). 0 (default) = internal common mode selected. 1 = external common mode selected (all the internal common-mode switches are off).
R/W	0	1	RLDSEL	Enable right leg drive reference electrode. 0 (default) = disabled. 1 = enabled.
R/W	0	0	SHLDEN	Enable shield drive. 0 (default) = shield drive disabled. 1 = shield drive enabled.

Table 33. GPIO Control Register (GPIOCTL) Address 0x06, Reset Value = 0x000000

R/$\overline{W}$	Default	Bit	Name	Function
	0	[23:19]	Reserved	Reserved, set to 0
R/W	0	18	SPIFW	Frame secondary SPI words with chip select 0 (default) = $\overline{MCS}$ asserted for entire frame 1 = $\overline{MCS}$ asserted for individual word
R/W	0	17	Reserved	Reserved, set to 0
R/W	0	16	SPIEN	Secondary SPI enable; SPI interface providing ECG data at 128 kHz data rate for external digital pace algorithm detection, uses GPIO0, GPIO1, GPIO2 pins 0 (default) = disabled 1 = enabled; the individual control bits for GPIO0, GPIO1, GPIO2 are ignored; GPIO3 is not affected by SPIEN
R/W	00	[15:14]	G3CTL [1:0]	State of GPIO3 pin 00 (default) = high impedance 01 = input 10 = output 11 = open drain
R/W	0	13	G3OUT	Output value to be written to GPIO3 when the pin is configured as an output or open drain 0 (default) = low value 1 = high value
R	0	12	G3IN	Read only; input value read from GPIO3 when the pin is configured as an input 0 (default) = low value 1 = high value
R/W	00	[11:10]	G2CTL [1:0]	State of GPIO2 pin 00 (default) = high impedance 01 = input 10 = output 11 = open drain
R/W	0	9	G2OUT	Output value to be written to GPIO2 when the pin is configured as an output or open drain 0 (default) = low value 1 = high value
R	0	8	G2IN	Read only Input value read from GPIO2 when the pin is configured as an input 0 (default) = low value 1 = high value
R/W	00	[7:6]	G1CTL [1:0]	State of GPIO1 pin 00 (default) = high impedance 01 = input 10 = output 11 = open drain
R/W	0	5	G1OUT	Output value to be written to GPIO1 when the pin is configured as an output or open drain 0 (default) = low value 1 = high value
R	0	4	G1IN	Read only; input value read from GPIO1 when the pin is configured as an input 0 (default) = low value 1 = high value
R/W	00	[3:2]	G0CTL [1:0]	State of the GPIO0 pin 00 (default) = high impedance 01 = input 10 = output 11 = open drain
R/W	0	1	G0OUT	Output value to be written to GPIO0 when the pin is configured as an output or open drain 0 (default) = low value 1 = high value
R	0	0	G0IN	(Read only) input value read from GPIO0 when the pin is configured as an input 0 (default) = low value 1 = high value

Table 34. Pace Amplitude Threshold Register (PACEAMPTH) Address 0x07, Reset Value = 0x242424[1]

R/W	Default	Bit	Name	Function
R/W	0010 0100	[23:16]	PACE3AMPTH	Pace amplitude threshold
R/W	0010 0100	[15:8]	PACE2AMPTH	Threshold = N × 2 × VREF/GAIN/2^{16}
R/W	0010 0100	[7:0]	PACE1AMPTH	

[1] ADAS1000-4 model only, ADAS1000-3 model does not contain these features.

Table 35. Test Tone Register (TESTTONE) Address 0x08, Reset Value = 0x000000

R/W	Default	Bit	Name	Function
R/W	0	23	TONLA	Tone select
R/W	0	22	TONLL	0 (default) = 1.3 V VCM_REF
R/W	0	21	TONRA	1 = 1 mV sine wave or square wave for TONINT = 1, no connect for TONINT = 0
R/W	0	[20:5]	Reserved	Reserved, set to 0
R/W	00	[4:3]	TONTYPE	00 (default) = 10 Hz sine wave 01 = 150 Hz sine wave 1x = 1 Hz, 1 mV square wave
R/W	0	2	TONINT	Test tone internal or external 0 (default) = external test tone; test tone to be sent out through CAL_DAC_IO and applied externally to enabled channels 1 = internal test tone; disconnects external switches for all ECG channels and connects the calibration DAC test tone internally to all ECG channels; in gang mode, the CAL_DAC_IO is connected, and the slave disables the calibration DAC
R/W	0	1	TONOUT	Test tone out enable 0 (default) = disconnects test tone from CAL_DAC_IO during internal mode only 1 = connects CAL_DAC_IO to test tone during internal mode
R/W	0	0	TONEN	Enables an internal test tone to drive entire signal chain, from preamplifier to SPI interface; this tone comes from the calibration DAC and goes to the preamplifier through the internal mux; when TONEN (calibration DAC) is enabled, ac lead-off is disabled 0 (default) = disable the test tone 1 = enable the 1 mV sine wave test tone (calibration mode has priority)

Table 36. Calibration DAC Register (CALDAC) Address 0x09, Reset Value = 0x002000[1]

R/W	Default	Bit	Name	Function
	0	[23:14]	Reserved	Reserved, set to 0.
R/W	1	13	CALCHPEN	Calibration chop clock enable. The calibration DAC output (CAL_DAC_IO) can be chopped to lower 1/f noise. Chopping is performed at 256 kHz. 0 = disabled. 1 (default) = enabled.
R/W	0	12	CALMODEEN	Calibration mode enable. 0 (default) = disable calibration mode. 1 = enable calibration mode; connect CAL DAC_IO, begin data acquisition on ECG channels.
R/W	0	11	CALINT	Calibration internal or external. 0 (default) = external calibration to be performed externally by looping CAL_DAC_IO around into ECG channels. 1 = internal calibration; disconnects external switches for all ECG channels and connects calibration DAC signal internally to all ECG channels.
R/W	0	10	CALDACEN	Enable 10-bit calibration DAC for calibration mode or external use. 0 (default) = disable calibration DAC. 1 = enable calibration DAC. If a master device and not in calibration mode, also connects the calibration DAC signal out to the CAL_DAC_IO pin for external use. If in slave mode, the calibration DAC is disabled to allow master to drive the slave CAL_DAC_IO pin. When the calibration DAC is enabled, ac lead-off is disabled.
R/W	0000000000	[9:0]	CALDATA[9:0]	Set the calibration DAC value.

[1] To ensure successful update of the calibration DAC, the serial interface must issue four additional SCLK cycles after writing the new calibration DAC register word.

Table 37. Frame Control Register (FRMCTL) Address 0x0A, Reset Value = 0x079000

R/W	Default	Bit	Name	Function
R/W	0	23	LEAD I/LADIS	Include/exclude word from ECG data frame. If the electrode/lead is included in the data-word and the electrode falls off, the data-word is undefined. 0 (default) = included in frame. 1 = exclude from frame.
R/W	0	22	LEADII/LLDIS	
R/W	0	21	LEADIII/RADIS	
R/W	1111	[20:15]	Reserved	Reserved, set to 111111.
R/W	0	14	PACEDIS[1]	Pace detection. 0 (default) = included in frame. 1 = exclude from frame.
R/W	0	13	RESPMDIS[1]	Respiration magnitude. 0 (default) = included in frame. 1 = exclude from frame.
R/W	1	12	RESPPHDIS[1]	Respiration phase. 0 = included in frame. 1 (default) = exclude from frame.
R/W	0	11	LOFFDIS	Lead-off status. 0 (default) = included in frame. 1 = exclude from frame.
R/W	0	10	GPIODIS	GPIO word disable. 0 (default) = included in frame. 1 = exclude from frame.
R/W	0	9	CRCDIS	CRC word disable. 0 (default) = included in frame. 1 = exclude from frame.
R/W	0	8	Reserved	Reserved, set to 0.
R/W	0	7	ADIS	Automatically excludes PACEDIS[14], RESPMDIS[13], LOFFDIS[11] words if their flags are not set in the header. 0 (default) = fixed frame format. 1 = autodisable words (words per frame changes).
R/W	0	6	RDYRPT	Ready repeat. If this bit is set and the frame header indicates data is not ready, the frame header is continuously sent until data is ready. 0 (default) = always send entire frame. 1 = repeat frame header until ready.
R/W	0	5	Reserved	Reserved, set to 0.
R/W	0	4	DATAFMT	Sets the output data format, see Figure 56. 0 (default) = digital lead/vector format (available only in 2 kHz and 16 kHz data rates). 1 = electrode format.
R/W	00	[3:2]	SKIP[1:0]	Skip interval. This field provides a way to decimate the data. 00 (default) = output every frame. 01 = output every other frame. 1× = output every 4th frame.
R/W	00	[1:0]	FRMRATE[1:0]	Sets the output data rate. 00 (default) = 2 kHz output data rate. 01 = 16 kHz output data rate. 10 = 128 kHz output data rate (DATAFMT must be set to 1). 11 = 31.25 Hz.

[1] ADAS1000-4 model only, ADAS1000-3 model does not contain these features.

Table 38. Filter Control Register (FILTCTL) Address 0x0B, Reset Value = 0x000000

R/W	Default	Bit	Name	Function
R/W	0	[23:6]	Reserved	Reserved, set to 0
R/W	0	5	MN2K	2 kHz notch bypass for SPI master 0 (default) = notch filter bypassed 1 = notch filter present
R/W	0	4	N2KBP	2 kHz notch bypass 0 (default) = notch filter present 1 = notch filter bypassed
R/W	00	[3:2]	LPF[1:0]	00 (default) = 40 Hz 01 = 150 Hz 10 = 250 Hz 11 = 450 Hz
R/W	00	[1:0]	Reserved	Reserved, set to 0

Table 39. AC Lead-Off Upper Threshold Register (LOFFUTH) Address 0x0C, Reset Value = 0x00FFFF

R/W	Default	Bit	Name	Function
	0	[23:20]	Reserved	Reserved, set to 0
R/W	0	[19:16]	ADCOVER[3:0]	ADC overrange threshold An ADC out-of-range error is flagged if the ADC output is greater than the overrange threshold; the overrange threshold is offset from the maximum value *Threshold = max_value – ADCOVER[3:0]* × 2^6 0000 = maximum value (disabled) 0001 = max_value – 64 0010 = max_value – 128 … 1111 = max_value – 960
R/W	0xFFFF	[15:0]	LOFFUTH[15:0]	Applies to ac lead-off upper threshold only; lead-off is detected if the output is ≥ N × 2 × VREF/gain/2^{16} 0 = 0 V

Table 40. AC Lead-Off Lower Threshold Register (LOFFLTH) Address 0x0D, Reset Value = 0x000000

R/W	Default	Bit	Name	Function
	0	[23:20]	Reserved	Reserved, set to 0
R/W	0	[19:16]	ADCUNDR[3:0]	ADC underrange threshold An ADC out-of-range error is flagged if the ADC output is less than the underrange threshold *Threshold = min_value + ADCUNDR[3:0]* × 2^6 0000 = minimum value (disabled) 0001 = min_value + 64 0010 = min_value + 128 … 1111 = min_value + 960
R/W	0	[15:0]	LOFFLTH[15:0]	Applies to ac lead-off lower threshold only; lead-off is detected if the output is ≤ N × 2 × VREF/GAIN/2^{16} 0 = 0 V

Table 41. Pace Edge Threshold Register (PACEEDGETH) Address 0x0E, Reset Value = 0x000000[1]

R/W	Default	Bit	Name	Function
R/W	0	[23:16]	PACE3EDGTH	Pace edge trigger threshold 0 = PACEAMPTH/2 1 = VREF/gain/2^{16} N = N × VREF/gain/2^{16}
R/W	0	[15:8]	PACE2EDGTH	
R/W	0	[7:0]	PACE1EDGTH	

[1] ADAS1000-4 model only, ADAS1000-3 model does not contain these features.

Table 42. Pace Level Threshold Register (PACELVLTH) Address 0x0F, Reset Value = 0x000000[1]

R/W	Default	Bit	Name	Function
R/W	0	[23:16]	PACE3LVLTH[7:0]	Pace level threshold; This is a signed value −1 = 0xFF = −VREF/gain/2^{16} 0 = 0x00 = 0 V +1 = 0x01 = +VREF/gain/2^{16} N = N × VREF/gain/2^{16}
R/W	0	[15:8]	PACE2LVLTH[7:0]	
R/W	0	[7:0]	PACE1LVLTH[7:0]	

[1] ADAS1000-4 model only, ADAS1000-3 model does not contain these features.

Table 43. Read Electrode/Lead Data Registers (Electrode/Lead) Address 0x11 to 0x13, Reset Value = 0x000000[1]

R/W	Default	Bit	Name	Function
		[31:24]	Address [7:0]	0x11: LA or Lead I. 0x12: LL or Lead II. 0x13: RA or Lead III.
R	0	[23:0]	ECG data	Channel data value. Data left justified (MSB) irrespective of data rate. The input stage can be configured into different modes (electrode, analog lead, or digital lead). In electrode mode and analog lead mode, the digital result value is an unsigned integer. In digital lead/vector mode, the value is a signed twos complement integer format and has a 2× range compared to electrode format because it can swing from +VREF to –VREF; therefore, the LSB size is doubled. Electrode mode and analog lead mode: Minimum value (000…) = 0 V Maximum value (1111….) = VREF/GAIN $LSB = (2 \times VREF/GAIN)/(2^N - 1)$ $ECG\ (voltage) = ECG\ Data \times (2 \times VREF/GAIN)/(2^N - 1)$ Digital lead mode: Minimum value (1000…) = −(VREF/GAIN) Maximum value (0111….) = +VREF/GAIN $LSB = (4 \times VREF/GAIN)/(2^N - 1)$ $ECG\ (voltage) = ECG\ Data \times (4 \times VREF/GAIN)/(2^N - 1)$ where N = number of data bits: 16 for 128 kHz data rate or 24 for 2 kHz/16 kHz data rate.

[1] If using 128 kHz data rate in frame mode, only the upper 16 bits are sent. If using the 128 kHz data rate in regular read/write mode, all 32 bits are sent.

Table 44. Read Pace Detection Data/Status Register (PACEDATA) Address 0x1A, Reset Value = 0x000000[1, 2, 3]

R/W	Default	Bit	Name	Function
R	0	23	Pace 3 detected	Pace 3 detected. This bit is set once a pace pulse is detected. This bit is set on the trailing edge of the pace pulse. 0 = pace pulse not detected in current frame. 1 = pace pulse detected in this frame.
R	000	[22:20]	Pace Channel 3 width	This bit is $\log_2$ (width) − 1 of the pace pulse. Width = 2^{N+1}/128 kHz.
R	0000	[19:16]	Pace Channel 3 height	This bit is the $\log_2$ (height) of the pace pulse. Height = $2^N \times$ VREF/gain/2^{16}.
R	0	15	Pace 2 detected	Pace 2 detected. This bit is set once a pace pulse is detected. This bit is set on the trailing edge of the pace pulse. 0 = pace pulse not detected in current frame. 1 = pace pulse detected in this frame.
R	000	[14:12]	Pace Channel 2 width	This bit is $\log_2$ (width) − 1 of the pace pulse. Width = 2^{N+1}/128 kHz.
R	0000	[11:8]	Pace Channel 2 height	This bit is the $\log_2$ (height) of the pace pulse. Height = $2^N \times$ VREF/gain/2^{16}.
R	0	7	Pace 1 detected	Pace 1 detected. This bit is set once a pace pulse is detected. This bit is set on the trailing edge of the pace pulse. 0 = pace pulse not detected in current frame. 1 = pace pulse detected in this frame.
R	000	[6:4]	Pace Channel 1 width	This bit is $\log_2$ (width) − 1 of the pace pulse. Width = 2^{N+1}/128 kHz.
R	0000	[3:0]	Pace Channel 1 height	This bit is the $\log_2$ (height) of the pace pulse. Height = $2^N \times$ VREF/gain/2^{16}.

[1] If using 128 kHz data rate in frame mode, this word is stretched over two 16-bit words. If using the 128 kHz data rate in regular read/write mode, all 32 bits are sent.
[2] Log data for width and height is provided here to ensure that it fits in one full 32-bit data-word. As a result, there may be some amount of error in the resulting value. For more accurate reading, read the 0x3A, 0x3B, 0x3C registers (see Table 52).
[3] ADAS1000-4 model only, ADAS1000-3 model does not contain these features.

Table 45. Read Respiration Data—Magnitude Register (RESPMAG) Address 0x1B, Reset Value = 0x000000[1, 2]

R/W	Default	Bit	Name	Function
R	0	[23:0]	Respiration Magnitude[23:0]	Magnitude of respiration signal. This is an unsigned value. $4 \times$ (VREF/(1.6468 × respiration gain))/(2^{24} − 1).

[1] If using 128 kHz data rate in frame mode, this word is stretched over two 16-bit words. If using the 128 kHz data rate in regular read/write mode, all 32 bits are sent.
[2] ADAS1000-4 model only, ADAS1000-3 model does not contain these features.

Table 46. Read Respiration Data—Phase Register (RESPPH) Address 0x1C, Reset Value = 0x000000[1, 2]

R/W	Default	Bit	Name	Function
R	0	[23:0]	Respiration Phase[23:0]	Phase of respiration signal. Can be interpreted as either signed or unsigned value. If unsigned, the range is from 0 to 2π. If signed, the range is from − π to +π. 0x000000 = 0. 0x000001 = 2π/2^{24}. 0x400000 = π/2. 0x800000 = +π = − π. 0xC00000 = +3π/2 = − π/2. 0xFFFFFF = +2π(1 − 2^{-24}) = −2π/2^{24}.

[1] This register is not part of framing data, but may be read by issuing a register read command of this address.
[2] ADAS1000-4 model only, ADAS1000-3 model does not contain these features.

Table 47. Lead-Off Status Register (LOFF) Address 0x1D, Reset Value = 0x000000

R/W	Default	Bit	Name	Function
R	0	23 22 21 20 13	RLD lead-off Status LA lead-off status LL lead-off status RA lead-off status CELO	Electrode connection status. If either dc or ac lead-off is enabled, these bits are the corresponding lead-off status. If both dc and ac lead-off are enabled, these bits reflect only the ac lead-off status. DC lead-off is available in the DCLEAD-OFF register (see Table 48). The common electrodes have only dc lead-off detection. An ac lead-off signal can be injected into the common electrode, but there is no ADC input to measure its amplitude. If the common electrode is off, it affects the ac lead-off amplitude of the other electrodes. These bits accumulate in the frame buffer and are cleared when the frame buffer is loaded into the SPI buffer. 0 = electrode is connected. 1 = electrode is disconnected.
R	0	[19:14]	Reserved	Reserved.
R	0	12 11 10	LAADCOR LLADCOR RAADCOR	ADC out of range error. These status bits indicate the resulting ADC code is out of range. These bits accumulate in the frame buffer and are cleared when the frame buffer is loaded into the SPI buffer.
R	0	[9:0]	Reserved	Reserved.

Table 48. DC Lead-Off Register (DCLEAD-OFF) Address 0x1E, Reset Value = 0x000000[1]

R/W	Default	Bit	Name	Function
R	0	23 22 21 20 13	RLD input overrange LA input overrange LL input overrange RA input overrange CE input overrange	The dc lead-off detection is comparator based and compares to a fixed level. Individual electrode bits flag indicate if the dc lead-off comparator threshold level has been exceeded. 0 = electrode < overrange threshold, 2.4 V. 1 = electrode > overrange threshold, 2.4 V.
R	0	[19:14] [8:3]	Reserved	Reserved.
R	0	12 11 10 9 2	RLD input underrange LA input underrange LL input underrange RA input underrange CE input underrange	The dc lead-off detection is comparator based and compares to a fixed level. Individual electrode bits indicate if the dc lead-off comparator threshold level has been exceeded. 0 = electrode > underrange threshold, 0.2 V. 1 = electrode < underrange threshold, 0.2 V.
R	0	[1:0]	Reserved	

[1] This register is not part of framing data, but can be read by issuing a register read command of this address.

Table 49. Operating State Register (OPSTAT) Address 0x1F, Reset Value = 0x000000[1]

R/W	Default	Bit	Name	Function
R	0	[23:4]	Reserved	Reserved.
R	0	3	Internal error	Internal digital failure. This is set if an error is detected in the digital core.
R	0	2	Configuration status	This bit is set after a reset indicating that the configuration has not been read yet. Once the configuration is set, this bit is ready. 0 = ready. 1 = busy.
R	0	1	PLL lock	PLL lock lost. This bit is set if the internal PLL loses lock after it is enabled and locked. This bit is cleared once this register is read or the PWREN bit (Address 0x01[1]) is cleared. 0 = PLL locked. 1 = PLL lost lock.
R	0	0	PLL locked status	This bit indicates the current state of the PLL locked status. 0 = PLL not locked. 1 = PLL locked.

[1] This register is not part of framing data, but can be read by issuing a register read command of this address. This register assists support efforts giving insight into potential areas of malfunction within a failing device.

Table 50. User Gain Calibration Registers (CALxx) Address 0x21 to Address 0x23, Reset Value = 0x000000

R/W	Default	Bit	Name	Function
		[31:24]	Address [7:0]	0x21: calibration LA. 0x22: calibration LL. 0x23: calibration RA.
R/W	0	23	USRCAL	User can choose between default calibration values or user calibration values for GAIN 0, GAIN 1, GAIN 2. Note that for GAIN 3, there is no factory calibration. 0 = default calibration values (factory calibration). 1 = user calibration values.
R/W	0	[22:12]	Reserved	Reserved, set to 0.
R/W	0	[11:0]	CALVALUE	Gain calibration value. Result = data × (1 + gain × 2^{-17}). The value read from this register is the current gain calibration value. If the USRCAL bit is set to 0, this register returns the default value for the current gain setting. 0x7FF (+2047) = ×1.00000011111111111b. 0x001 (+1) = ×1.00000000000000001b. 0x000 (0) = ×1.00000000000000000b. 0xFFF (−1) = ×0.11111111111111111b. 0x800 (−2048) = ×0.11111100000000000b.

Table 51. Read AC Lead-Off Amplitude Registers (LOAMxx) Address 0x31 to Address 0x33, Reset Value = 0x000000[1]

R/W	Default	Bit	Name	Function
		[31:24]	Address [7:0]	0x31: LA ac lead-off amplitude. 0x32: LL ac lead-off amplitude. 0x33: RA ac lead-off amplitude.
R/W	0	[23:16]	Reserved	Reserved.
R	0	[15:0]	LOFFAM	Measured amplitude. When ac lead-off is selected, the data is the average of the rectified 2 kHz band-pass filter with an update rate of 8 Hz and cutoff frequency at 2 Hz. The output is the amplitude of the 2 kHz signal scaled by 2/π approximately = 0.6 (average of rectified sine wave). To convert to rms, scale the output by π/(2√2). Lead-off (unsigned). Minimum 0x0000 = 0 V. LSB 0x0001= VREF/GAIN/2^{16}. Maximum 0xFFFF = VREF/GAIN. RMS = [π/(2√2)] × [(Code × VREF)/(GAIN × 2^{16})] Peak-to-peak = π × [(Code × VREF)/(GAIN × 2^{16})]

[1] This register is not part of framing data, but can be read by issuing a register read command of this address.

Table 52. Pace Width and Amplitude Registers (PACExDATA) Address 0x3A to Address 0x3C, Reset Value = 0x000000[1, 2]

R/W	Default	Bit	Name	Function
		[31:24]	Address [7:0]	0x3A: PACE1DATA 0x3B: PACE2DATA 0x3C: PACE3DATA
R	0	[23:8]	Pace height	Measured pace height in signed twos complement value 0 = 0 1 = VREF/gain/2^{16} N = N × VREF/gain/2^{16}
R	0	[7:0]	Pace width	Measured pace width in 128 kHz samples N: (N + 1)/128 kHz = width 12: (12 + 1)/128 kHz = 101.56 µs (minimum when pace width filter enabled) 255: (255 + 1)/128 kHz = 2.0 ms Disabling the pace width filter allows the pace measurement system to return values of N < 12, that is, pulses narrower than 101.56 µs.

[1] These registers are not part of framing data but can be read by issuing a register read command of these addresses.
[2] ADAS1000-4 model only, ADAS1000-3 model does not contain these features.

Table 53. Frame Header (FRAMES) Address 0x40, Reset Value = 0x800000[1]

R/W	Default	Bit	Name	Function
R	1	31	Marker	Header marker, set to 1 for the header.
R	0	30	Ready bit	Ready bit indicates if ECG frame data is calculated and ready for reading. 0 = ready, data frame follows. 1 = busy.
R	0	[29:28]	Overflow [1:0]	Overflow bits indicate that since the last frame read, a number of frames have been missed. This field saturates at the maximum count. The data in the frame including this header word is valid but old if the overflow bits are >0. When using skip mode (FRMCTL register (0x0A), Bits[3:2]), the overflow bit acts as a flag, where a nonzero value indicates an overflow. 00 = 0 missed. 01 = 1 frame missed. 10 = 2 frames missed. 11 = 3 or more frames missed.
R	0	27	Fault	Internal device error detected. 0 = normal operation. 1 = error condition.
R	0	26	Pace 3 detected	Pace 3 indicates pacing artifact was qualified at most recent point. 0 = no pacing artifact. 1 = pacing artifact present.
R	0	25	Pace 2 detected	Pace 2 indicates pacing artifact was qualified at most recent point. 0 = no pacing artifact. 1 = pacing artifact present.
R	0	24	Pace 1 detected	Pace 1 indicates pacing artifact was qualified at most recent point. 0 = no pacing artifact. 1 = pacing artifact present.
R	0	23	Respiration	0 = no new respiration data. 1 = respiration data updated.
R	0	22	Lead-off detected	If both dc and ac lead-off are enabled, this bit is the OR of all the ac lead-off detect flags. If only ac or dc lead-off is enabled, this bit reflects the OR of all dc and ac lead-off flags. 0 = all leads connected. 1 = one or more lead-off detected.
R	0	21	DC lead-off detected	0 = all leads connected. 1 = one or more lead-off detected.
R	0	20	ADC out of range	0 = ADC within range. 1 = ADC out of range.
	0	[19:0]	Reserved	Reserved.

[1] If using 128 kHz data rate in frame mode, only the upper 16 bits are sent. If using the 128 kHz data rate in regular read/write mode, all 32 bits are sent.

Table 54. Frame CRC Register (CRC) Address 0x41, Reset Value = 0xFFFFFF[1]

R/W	Bit	Name	Function
R	[23:0]	CRC	Cyclic redundancy check

[1] The CRC register is a 32-bit word for 2 kHz and 16 kHz data rate and a 16-bit word for 128 kHz rate. See Table 24 for more details.

INTERFACE EXAMPLES

The following examples show register commands required to configure the ADAS1000-3/ADAS1000-4 devices into particular modes of operation and to start framing ECG data.

Example 1: Initialize the Device for ECG Capture and Start Streaming Data

1. Write 1 configures the CMREFCTL register for CM = WCT = (LA + LL + RA)/3; RLD is enabled onto the RLD_OUT electrode. The shield amplifier is enabled.
2. Write 2 configures the FRMCTL register to output seven words per frame/packet. The frame/packet of words consist of the header, three ECG words, pace, respiration magnitude, and lead-off. The frame is configured to always send, irrespective of ready status. The device is in analog lead mode with a data rate of 2 kHz.
3. Write 3 addresses the ECGCTL register, enabling all channels into a gain of 1.4, low noise mode, and differential input, which configures the device for analog lead mode. This register also configures the device as a master, using the external crystal as the input source to the XTALx pins. The device is also put into conversion mode in this write.
4. Write 4 issues the read command to start putting the converted data out on the SDO pin.
5. Continue to issue SCLK cycles to read the converted data at the configured packet data rate (2 kHz). The SDI input should be held low when reading back the conversion data because any commands issued to the interface during read of frame/packet are understood to be a change of configuration data and will stop the ADC conversions to allow the interface to process the new command.

Example 2: Enable Respiration and Stream Conversion Data (Applies to ADAS1000-4 Only)

1. Write 1 configures the RESPCTL register with a 56 kHz respiration drive signal, gain = 1, driving out through the respiration capacitors and measuring on Lead I.
2. Write 2 issues the read command to start putting the converted data out on the SDO pin.
3. Continue to issue SCLK cycles to read the converted data at the configured packet data rate.
4. Note that this example assumes that the FRMCTL register has already been configured such that the respiration magnitude is available in the data frame, as arranged in Write 2 of Example 1.

Example 3: DC Lead-Off and Stream Conversion Data

1. Write 1 configures the LOFFCTL register with a dc lead-off enabled for a lead-off current of 50 nA.
2. Write 2 issues the read command to start putting the converted data out on the SDO pin.
3. Continue to issue SCLK cycles to read the converted data at the configured packet data rate.
4. Note that this example assumes that the FRMCTL register has already been configured such that the dc lead-off word is available in the data frame, as arranged in Write 2 of Example 1.

Table 55. Example 1: Initialize the Device for ECG Capture and Start Streaming Data

Write Command	Register Addressed	Read/Write Bit	Register Address	Data	32-Bit Write Command
Write 1	CMREFCTL	1	000 0101	1110 0000 0000 0000 0000 1011	0x85E0000B
Write 2	FRMCTL	1	000 1010	0001 1111 1001 0110 0000 0000	0x8A1F9600
Write 3	ECGCTL	1	000 0001	1110 0000 0000 0100 1010 1110	0x81E004AE
Write 4	FRAMES	0	100 0000	0000 0000 0000 0000 0000 0000	0x40000000

Table 56. Example 2: Enable Respiration and Stream Conversion Data (Applies to ADAS1000-4 Only)

Write Command	Register Addressed	Read/Write Bit	Register Address	Data	32-Bit Write Command
Write 1	RESPCTL	1	000 0011	0000 0000 0010 0000 1001 1001	0x83002099
Write 2	FRAMES	0	100 0000	0000 0000 0000 0000 0000 0000	0x40000000

Table 57. Example 3: Enable DC Lead-Off and Stream Conversion Data

Write Command	Register addressed	Read/Write Bit	Register Address	Data	32-Bit Write Command
Write 1	LOFFCTL	1	000 0010	0000 0000 0000 0000 0001 0101	0x82000015
Write 2	FRAMES	0	100 0000	0000 0000 0000 0000 0000 0000	0x40000000

Example 4: Configure 150 Hz Test Tone Sine Wave on Each ECG Channel and Stream Conversion Data

1. Write 1 configures the CMREFCTL register to VCM_REF = 1.3 V (no electrodes contribute to VCM). RLD is enabled to RLD_OUT, and the shield amplifier enabled.
2. Write 2 addresses the TESTTONE register to enable the 150 Hz sine wave onto all electrode channels.
3. Write 3 addresses the FILTCTL register to change the internal low-pass filter to 250 Hz to ensure that the 150 Hz sine wave can pass through.
4. Write 4 configures the FRMCTL register to output nine words per frame/packet. The frame/packet of words consists of the header and three ECG words, pace, respiration magnitude, and lead-off. The frame is configured to always send, irrespective of ready status. The device is in electrode format mode with a data rate of 2 kHz. Electrode format is required to see the test tone signal correctly on each electrode channel.
5. Write 5 addresses the ECGCTL register, enabling all channels into a gain of 1.4, low noise mode. It configures the device as a master and driven from the XTAL input source. The device is also put into conversion mode in this write.
6. Write 6 issues the read command to start putting the converted data out on the SDO pin.
7. Continue to issue SCLK cycles to read the converted data at the configured packet data rate.

Example 5: Enable Pace Detection and Stream Conversion Data (Applies to ADAS1000-4 Only)

1. Write 1 configures the PACECTL register with all three pace detection instances enabled, PACE1EN detecting on Lead II, PACE2EN detecting on Lead I, and PACE3EN detecting on Lead aVF. The pace width filter and validation filters are also enabled.
2. Write 2 issues the read command to start putting the converted data out on the SDO pin.
3. Continue to issue SCLK cycles to read the converted data at the configured packet data rate. When a valid pace is detected, the detection flags are confirmed in the header word and the PACEDATA register contains information on the width and height of the measured pulse from each measured lead.
4. Note that the PACEAMPTH register default setting is 0x242424, setting the amplitude of each of the pace instances to 1.98 mV/gain.
5. Note that this example assumes that the FRMCTL register has already been configured such that the PACEDATA word is available in the data frame, as arranged in Write 2 of Example 1.

Table 58. Example 4: Configure 150 Hz Test Tone Sine Wave on Each ECG Channel and Stream Conversion Data

Write Command	Register Addressed	Read/Write Bit	Register Address	Data	32-Bit Write Command
Write 1	CMREFCTL	1	000 0101	0000 0000 0000 0000 0000 1011	0x8500000B
Write 2	TESTTONE	1	000 1000	1110 0000 0000 0000 0000 1101	0x88E0000D
Write 3	FILTCTL	1	000 1011	0000 0000 0000 0000 0000 1000	0x8B000008
Write 4	FRMCTL	1	000 1010	0001 1111 1001 0110 0001 0000	0x8A1F9610
Write 5	ECGCTL	1	000 0001	1110 0000 0000 0000 1010 1110	0x81E000AE
Write 6	FRAMES	0	100 0000	0000 0000 0000 0000 0000 0000	0x40000000

Table 59. Example 5: Enable Pace Detection and Stream Conversion Data (Applies to ADAS1000-4 Only)

Write Command	Register Addressed	Read/Write Bit	Register Address	Data	32-Bit Write Command
Write 1	PACECTL	1	000 0100	0000 0000 0000 1111 1000 1111	0x84000F8F
Write 2	FRAMES	0	100 0000	0000 0000 0000 0000 0000 0000	0x40000000

Example 6: Writing to Master and Slave Devices and Streaming Conversion Data

This example uses the ADAS1000-3 as the slave device and the ADAS1000 as the master device to achieve a configuration with eight input electrodes and one right leg drive.

Slave Configuration (ADAS1000-3)

1. Write 1 configures the FRMCTL register to output five words per frame/packet. The frame/packet of words consists of the header, three ECG words, and lead-off. The frame is configured to always send, irrespective of ready status. The slave ADAS1000-3 is in electrode mode format with a data rate of 2 kHz.
2. Write 2 configures the CMREFCTL register to receive an external common mode from the master.
3. Write 3 addresses the ECGCTL register, enabling all channels into a gain of 1.4, low noise mode. It configures the device as a slave, in gang mode and driven from the CLK_IN input source (derived from master ADAS1000). The ADAS1000-3 slave is also put into conversion mode in this write, but waits for the SYNC_GANG signal from the master device before it starts converting.

Master Configuration (ADAS1000)

- Write 4 configures the FRMCTL register to output seven words per frame/packet (note that this differs from the number of words in a frame available from the slave device). The frame/packet of words consists of the header, five ECG words, pace, respiration magnitude, and lead-off. In this example, the frame is configured to always send irrespective of ready status. The master, ADAS1000, is in vector mode format with a data rate of 2 kHz. Similar to the slave device, the master could be configured for electrode mode; the host controller would then be required to make the lead calculations.

1. Write 5 configures the CMREFCTL register for CM = WCT = (LA + LL + RA)/3; RLD is enabled onto RLD_OUT electrode. The shield amplifier is enabled. The CM = WCT signal is driven out of the master device (CM_OUT) into the slave device (CM_IN).
2. Write 6 addresses the ECGCTL register, enabling all channels into a gain of 1.4, low noise mode. It configures the device as a master in gang mode and driven from the XTAL input source. The ADAS1000 master is set to differential input, which places it in analog lead mode. This ECGCTL register write puts the master into conversion mode, where the device sends an edge on the SYNC_GANG pin to the slave device to trigger the simultaneous conversions of both devices.
3. Write 7 issues the read command to both devices to start putting the converted and decimated data out on the respective SDO pins.
4. Continue to issue SCLK cycles to read the converted data at the configured packet data rate.

Table 60. Example 6: Writing to Master and Slave Devices and Streaming Conversion Data

Device	Write Command	Register Addressed	R/W	Register Address	Data	32-Bit Write Command
Slave	Write 1	FRMCTL	1	000 1010	0001 1111 1111 0110 0001 0000	0x8A1FF610
	Write 2	CMREFCTL	1	000 0101	0000 0000 0000 0000 0000 0100	0x85000004
	Write 3	ECGCTL	1	000 0001	1110 0000 0000 0000 1101 1110	0x81E000DE
Master	Write 4	FRMCTL	1	000 1010	0001 1111 1001 0110 0000 0000	0x8A1F9600
	Write 5	CMREFCTL	1	000 0101	1110 0000 0000 0000 0000 1011	0x85E0000B
	Write 6	ECGCTL	1	000 0001	1110 0000 0000 0100 1011 1110	0x81E004BE
Master and Slave	Write 7	FRAMES	0	100 0000	0000 0000 0000 0000 0000 0000	0x40000000

SOFTWARE FLOWCHART

Figure 81 shows a suggested sequence of steps to be taken to interface to multiple devices.

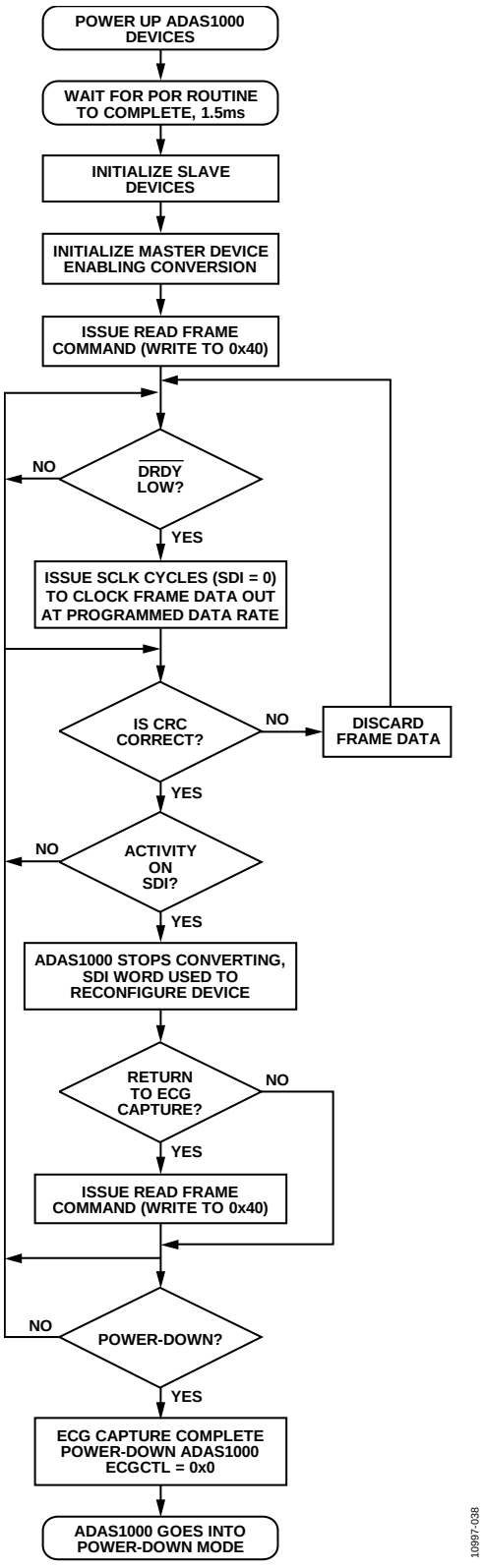


Figure 81. Suggested Software Flowchart for Interfacing to Multiple Devices

POWER SUPPLY, GROUNDING, AND DECOUPLING STRATEGY

The ADAS1000-3/ADAS1000-4 should have ample supply decoupling of 0.01 µF on each supply pin located as close to the device pin as possible, ideally right up against the device. In addition, there should be one 4.7 µF capacitor for each of the power domains, AVDD and IOVDD, again located as close to the device as possible. IOVDD is best split from AVDD due to its noisy nature.

Similarly, the ADCVDD and DVDD power domains each require one 2.2 µF capacitor with ESR in the range of 0.5 Ω to 2 Ω. The ideal location for each 2.2 µF capacitor is dependent on package type. For the LQFP package and DVDD decoupling, the 2.2 µF capacitor is best placed between Pin 30 and Pin 31, while for ADCVDD, the 2.2 µF capacitor should be placed between Pin 55 and Pin 56. Similarly for the LFCSP package, the DVDD 2.2 µF capacitor is ideal between Pin 43 and Pin 44, and between Pin 22 and Pin 23 for ADCVDD. A 0.01 µF capacitor is recommended for high frequency decoupling at each pin. The 0.01 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESL), such as the common ceramic capacitors that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

Digital lines running under the device should be avoided because these couple noise onto the device. The analog ground plane should be allowed to run under the device to avoid noise coupling. The power supply lines should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. It is essential to minimize noise on VREF lines. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough throughout the board. As is the case for all thin packages, take care to avoid flexing the package and to avoid a point load on the surface of this package during the assembly process.

During layout of board, ensure that bypass capacitors are placed as close to the relevant pin as possible, with short, wide traces ideally on the topside.

AVDD

While the ADAS1000-3/ADAS1000-4 are designed to operate from a wide supply rail, 3.15 V to 5.5 V, the performance is similar over the full range, but overall power increases with increasing voltage.

ADCVDD AND DVDD SUPPLIES

The AVDD supply rail powers the analog blocks in addition to the internal 1.8 V regulators for the ADC and the digital core. If using the internal regulators, connect the VREG_EN pin to AVDD and then use the ADCVDD and DVDD pins for decoupling purposes.

The DVDD regulator can be used to drive other external digital circuitry as required; however, the ADCVDD pin is purely provided for bypassing purposes and does not have available current for other components.

Where overall power consumption must be minimized, using external 1.8 V supply rails for both ADCVDD and DVDD would provide a more efficient solution. The ADCVDD and DVDD inputs have been designed to be driven externally and the internal regulators may be disabled by tying VREG_EN pin directly to ground.

UNUSED PINS/PATHS

In applications where not all ECG paths or functions might be used, the preferred method of biasing the different functions is as follows:

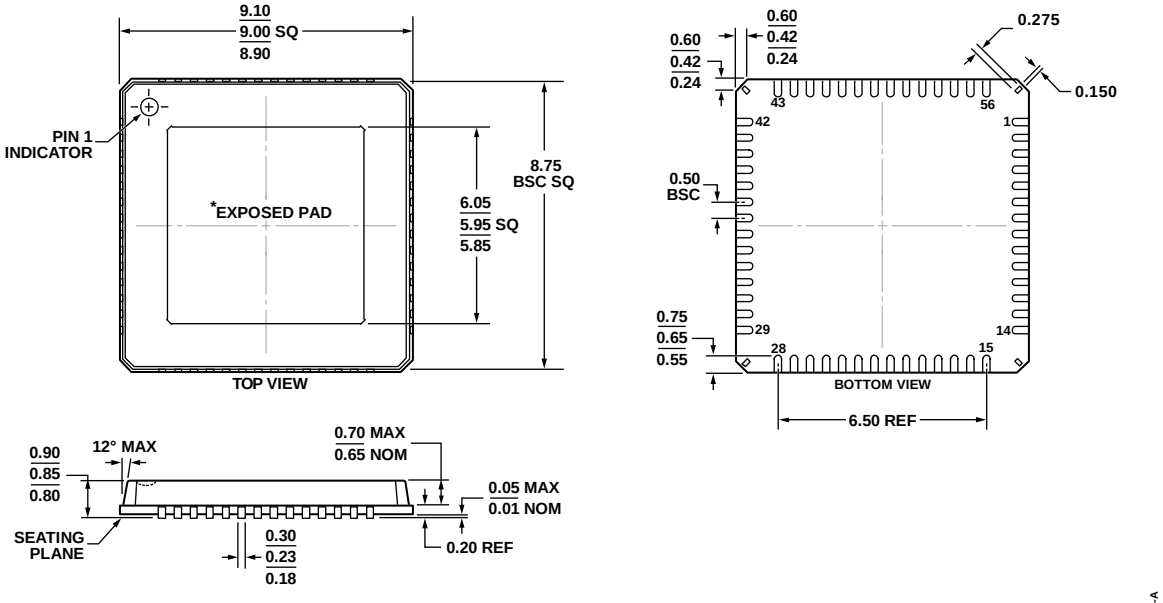
- Unused ECG paths power up disabled. For low power operation, they should be kept disabled throughout operation. Ideally, these pins should be connected to RLD_OUT if not being used.
- Unused external respiration inputs can be tied to ground if not in use.
- If unused, the shield driver can be disabled and output left to float.
- CM_OUT, CAL_DAC_IO, $\overline{\text{DRDY}}$, GPIOx, CLK_IO, SYNC_GANG can be left open.

LAYOUT RECOMMENDATIONS

To maximize CMRR performance, pay careful attention to the ECG path layout for each channel. All channels should be identical to minimize difference in capacitance across the paths.

Place all decoupling as close to the ADAS1000-3/ADAS1000-4 devices as possible, with an emphasis on ensuring that the VREF decoupling be prioritized, with VREF decoupling on the same side as the ADAS1000-3/ADAS1000-4devices, where possible.

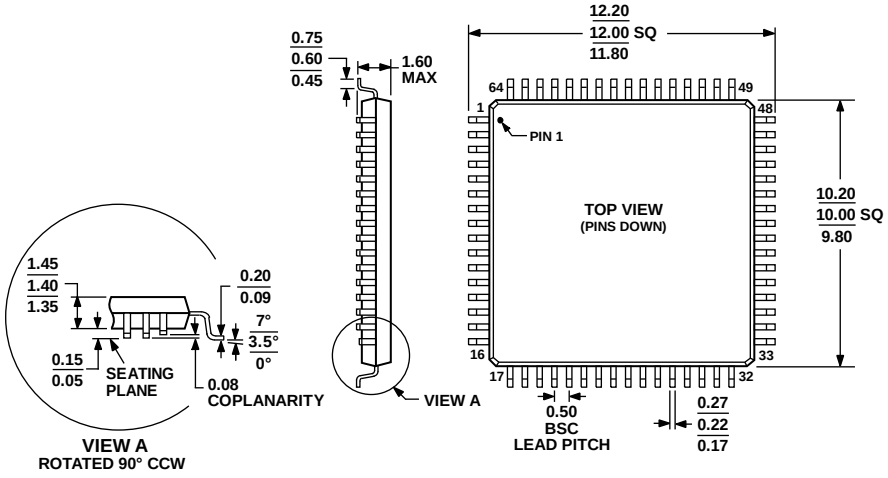
OUTLINE DIMENSIONS



*FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

06-20-2012-A

Figure 82. 56-Lead, Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-56-7)
Dimensions shown in millimeters



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051706-A

Figure 83. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Option	Description	Temperature Range	Package Description	Package Option
ADAS1000-3BSTZ	Tray	3 ECG Channels	−40°C to +85°C	64-Lead LQFP	ST-64-2
ADAS1000-3BSTZ-RL	Reel, 1000		−40°C to +85°C	64-Lead LQFP	ST-64-2
ADAS1000-3BCPZ	Tray		−40°C to +85°C	56-Lead LFCSP_VQ	CP-56-7
ADAS1000-3BCPZ-RL	Reel, 2500		−40°C to +85°C	56-Lead LFCSP_VQ	CP-56-7
ADAS1000-4BSTZ	Tray	3 ECG Channels, Pace Algorithm, Respiration Circuit	−40°C to +85°C	64-Lead LQFP	ST-64-2
ADAS1000-4BSTZ-RL	Reel, 1000		−40°C to +85°C	64-Lead LQFP	ST-64-2
ADAS1000-4BCPZ	Tray		−40°C to +85°C	56-Lead LFCSP_VQ	CP-56-7
ADAS1000-4BCPZ-RL	Reel, 2500		−40°C to +85°C	56-Lead LFCSP_VQ	CP-56-7
EVAL-ADAS1000SDZ		ADAS1000 Evaluation Board		Evaluation Kit[2]	
EVAL-SDP-CB1Z		System Demonstration Board (SDP), used as a controller board for data transfer via USB interface to PC		Controller Board[3]	

[1] Z = RoHS Compliant Part.
[2] This evaluation kit consists of ADAS1000BSTZ × 2 for up to 12-lead configuration. Because the ADAS1000 contains all features, it is the evaluation vehicle for all ADAS1000 variants.
[3] This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the SD designator.

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