MAX14670-MAX14673

Bidirectional Current-Blocking, High-Input Overvoltage Protector with Adjustable OVLO

General Description

The MAX14670–MAX14673 provide protection to valuable consumer circuits against positive voltage faults up to $\pm 28 \rm V_{DC}$. An internal clamp also protects the devices from surges up to $\pm 100 \rm V$. The device is able to disconnect the system from its output terminal when wrong input conditions are detected.

The MAX14670–MAX14673 overvoltage protection devices feature low $65m\Omega$ (typ), WLP package on-resistance (R_{ON}) internal FETs, effectively minimizing the voltage drop across the device. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components.

The overvoltage protection threshold can be adjusted with optional external resistors to any voltage between 5V and 22V. The devices automatically choose the accurate internal trip thresholds when the overvoltage lockout input (OVLO) is set lower than the external OVLO select voltage. The internal OVLO are preset to typical 6.8V (MAX14670), 15.5V (MAX14671), 5.825V (MAX14672), or 22V (MAX14673).

The MAX14670–MAX14673 feature reverse bias blocking capability. Unlike other overvoltage protectors, when the MAX14670–MAX14673 are disabled, the voltage applied to OUT does not feed back into IN. These devices also feature an OTG enable pin that allows OUT voltage to supply IN. The MAX14670–MAX14673 also have thermal shutdown protection against over load conditions.

The MAX14670–MAX14673 are specified over the extended -40°C to +85°C temperature range. The MAX14670/MAX14671 are available in a 15-bump WLP package and the MAX14672/MAX14673 are available in a 10-pin TDFN package.

Ordering Information/Selector Guide and Typical Operating Circuit appear at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX14670.related.

Benefits and Features

- Protect High-Power Portable Devices
 - Wide Operating Input Voltage Protection from +3V to +28V
 - +100V Surge Capability
 - 4.5A Continuous Current Capability (WLP Package)
 - Integrated $65m\Omega$ (typ) n-Channel MOSFET Switch (WLP Package)
- Flexible Overvoltage Protection Design
 - Wide +5V to +22V Adjustable OVLO Threshold Range
 - ACOK and ACOK Indicate Input is in Range
 - · OTG Enable Allows OUT to Supply IN
 - · Preset Accurate Internal OVLO Thresholds:

6.8V ±3% (MAX14670) 15.5V ±3% (MAX14671) 5.825V ±3% (MAX14672) 22V ±3% (MAX14673)

- Additional Protection Features Increase System Reliability
 - · OUT-IN Reverse Bias Blocking Capability
 - · Soft-Start to Minimize Inrush Current
 - · Internal 15ms Startup Debounce
 - · Thermal Shutdown Protection
- Space Saving
 - 15-Bump, 1.6mm x 2.1mm, WLP Package
 - 10-Pin, 3mm x 3mm, TDFN Package

Applications

- Tablets
- Smart Phones
- E-Readers
- PC Notebooks
- Charging USB Hosts



MAX14670-MAX14673

Bidirectional Current-Blocking, High-Input Overvoltage Protector with Adjustable OVLO

Absolute Maximum Ratings

(All voltages referenced to GND.)		Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
IN (Note 1)	0.3V to +29V	WLP (derate 16.4mW/°C above +70°C)	1312mW
OUT	0.3V to +26V	TDFN (derate 24.4mW/°C above +70°C)	1951mW
IN - OUT	26V to +29V	Operating Temperature Range	40°C to +85°C
OTG_EN, ACOK, ACOK	0.3V to +6V	Storage Temperature Range	65°C to +150°C
OVLO	0.3V to +26V	Lead Temperature (soldering, 10s)	+300°C
Continuous Current into IN, OUT		Soldering Temperature (reflow)	+260°C
WLP (Note 2)			
TDFN	±3.2A		

- **Note 1:** Survives burst pulses up to 100V with 2Ω series resistance and hot plug events. Above the input clamp voltage, the IN must be a surge in nature with a limited energy.
- Note 2: Limited by the PCB thermal design.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 3)

WLP	TDFN
Junction-to-Ambient Thermal Resistance (θ _{JA})52°C/W	Junction-to-Ambient Thermal Resistance (θ _{JA})41°C/W
	Junction-to-Case Thermal Resistance (θ _{JC})9°C/W

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

 $(V_{IN} = +3V \text{ to } +28V, V_{OUT} = +3V \text{ to } +24V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{IN} = +5V, T_A = +25^{\circ}\text{C}.)$ (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Startup Voltage	V _{INBT}			2.17	3	٧
Input Sustaining Voltage	V _{INBU}	I _{OUT} = 0A		1.5	2.3	V
Input Clamp Voltage	V _{IN_CLAMP}	I _{IN} = 10mA, T _A = +25°C		33.7		V
Input Supply Current	I _{IN}	V _{OVLO} = 0V, V _{IN} = 5V, ACOK is unconnected, I _{OUT} = 0mA		100	190	μΑ
Output Startup Voltage	V _{OUTBT}			2.15	3	V
Output Sustaining Voltage	V _{OUTBU}	I _{IN} = 0A		1.5	2.3	V
Output Supply Current	l _{OUT}	V _{OVLO} = 0V, V _{OUT} = 5V, I _{IN} = 0mA, V _{OTG_EN} = 1.8V		83	170	μΑ
Output Shutdown Current		$V_{OVLO} = 3V$, $V_{OUT} = 5V$, $V_{IN} = 0V$, $V_{OTG_EN} = 0V$		6	12	μΑ
IN Leakage Voltage		V _{OUT} = 21V, IN unconnected, V _{OTG_EN} = 0V		0.001	0.1	٧
IN Discharge Current		V _{IN} = V _{OUT} = 5V, IN discharge current after an OTG_EN transition from high to low		100	150	mA

Electrical Characteristics (continued)

 $(V_{IN} = +3V \text{ to } +28V, V_{OUT} = +3V \text{ to } +24V, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{IN} = +5V, T_A = +25^{\circ}\text{C}.)$ (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVP (IN TO OUT)	,						
On-Resistance (IN to OUT)		$V_{IN} = 5V,$ $WLP, T_A = +25^{\circ}C$ $TDFN, T_A = +25^{\circ}C$	WLP, T _A = +25°C		65	87	m0
on resistance (iiv to our)	R _{ON}		TDFN, T _A = +25°C		85	110	mΩ
		MAX14670	V _{IN} rising	6.6	6.8	7.0	
		IVIAX 14070	V _{IN} falling	6.5			
latara al Ovaca salta da Tria I aval		MAX14671	V _{IN} rising	15.0	15.5	16.0	
Internal Overvoltage Trip Level	V _{IN} OVLO	V _{IN} fa	V _{IN} falling	14.5			V
		MAY44670	V _{IN} rising	5.65	5.825	6.0	
		MAX14672	V _{IN} falling	5.55			
OVLO Set Threshold	V _{OVLO_TH}			1.18	1.221	1.26	V
Adjustable OVLO Threshold Range	V _{OVLO_EXT}			5		22	V
External OVLO Select Threshold	V _{OVLO_SEL}			0.2	0.25	0.3	V
DIGITAL SIGNALS (ACOK, ACO	K, OTG_EN)						
ACOK Output High Voltage	V _{ACOK}	I _{SOURCE} ≤ 100μA, V _{IN} > 3V		1.6	1.8	2.0	V
ACOK Leakage Current		Pull down to ground, V _{OUT} = 5V, OTG_EN = high, ACOK deasserted				1	μA
ACOK Output Low Voltage	V _{OL}	V _{IO} = 3.3V, I _{SINK} = 1mA				0.4	V
ACOK Leakage Current		V _{IO} = 3.3V, ACOK deasserted				1	μA
OTG_EN Input Logic-High	V _{IH}			1.6			V
OTG_EN Input Logic-Low	V _{IL}					0.4	V
OTG_EN Input Leakage Current	I _{IN}	$0V \le V_{IN} \le V_{IL}$ and $V_{IH} \le V_{IN} \le V_{CC}$, $V_{CC} = 5.5V$		-1		+1	μA
TIMING CHARACTERISTICS (Fig	gure 1)						
IN Debounce Time	t _{DEB}	V_{IN} = 5V to charge p of V_{IN}), R_{LOAD} = 100	ump on (V _{OUT} = 10% Ω Ω, C _{LOAD} = 10 μ F		20		ms
IN/OUT Soft-Start Time	t _{SS}	V_{IN} = 5V to V_{OUT} = 90% of V_{IN} , R_{LOAD} = 100 Ω , C_{LOAD} = 10 μ F			25		ms
IN OVP Turn-On Time During Soft-Start	t _{ON}	V_{IN} = 5V, R_{LOAD} = 100 Ω , C_{LOAD} = 10 μ F, V_{OUT} = 20% of V_{IN} to 80% of V_{IN}			1.5		ms
IN OVP Turn-Off Response Time	t _{OFF}	From $V_{IN} > V_{OVLO}$ to $V_{OUT} = 80\%$ of V_{IN} , $R_{LOAD} = 100\Omega$			1		μs
OTG Turn-On Time	t _{OTG_ON}	Time from OTG_EN high to V_{IN} = 80% of V_{OUT} , V_{OUT} = 5V, C_{IN} = 10 μ F			1.4		ms
In-Discharge Pulse Duration		V _{IN} = V _{OUT} = 5V, current pulse duration after an OTG_EN transition from high to low			1.1		ms

Electrical Characteristics (continued)

 $(V_{IN} = +3V \text{ to } +28V, V_{OUT} = +3V \text{ to } +24V, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{IN} = +5V, T_A = +25^{\circ}\text{C}.)$ (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL PROTECTION						
Thermal Shutdown	T _{SHDN}			150		°C
Thermal Hysteresis	T _{HYST}			20		°C
ESD PROTECTION						
Human Body Model		IN pin		±15		kV
IEC 61000-4-2 Contact Discharge		IN pin		±8		kV
IEC 61000-4-2 Air-Gap Discharge		IN pin		±8		kV

Note 4: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

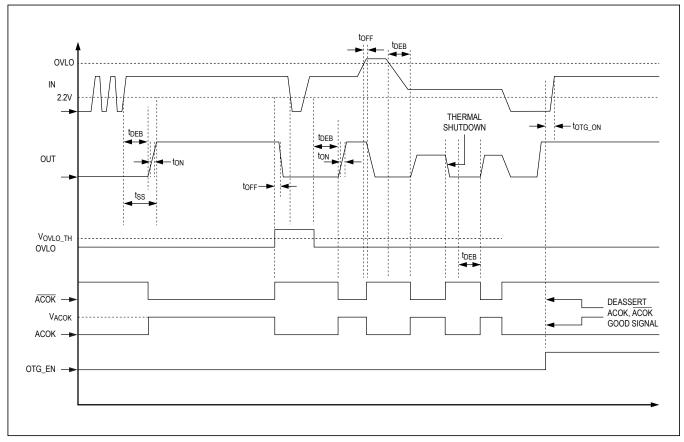
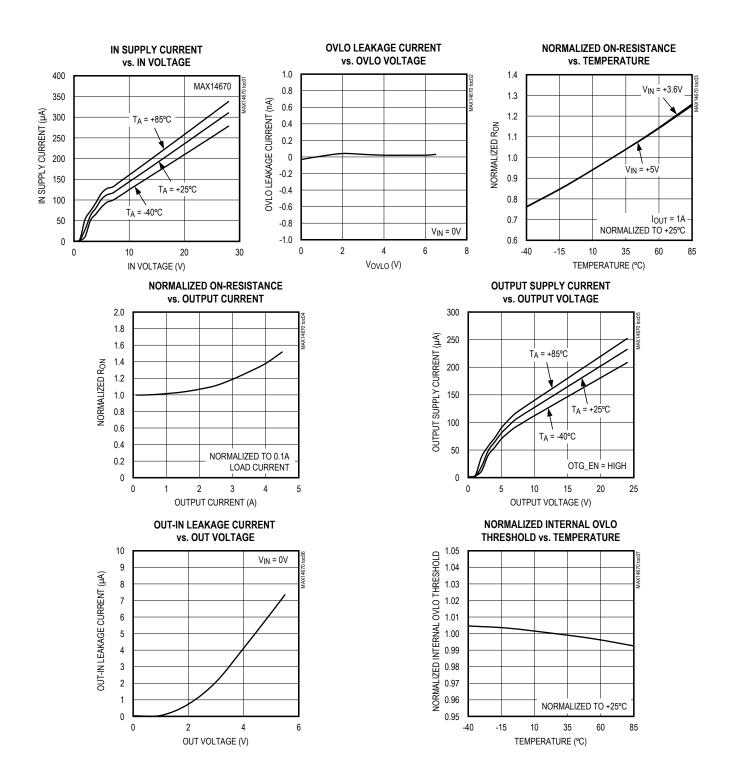


Figure 1. Timing Diagram

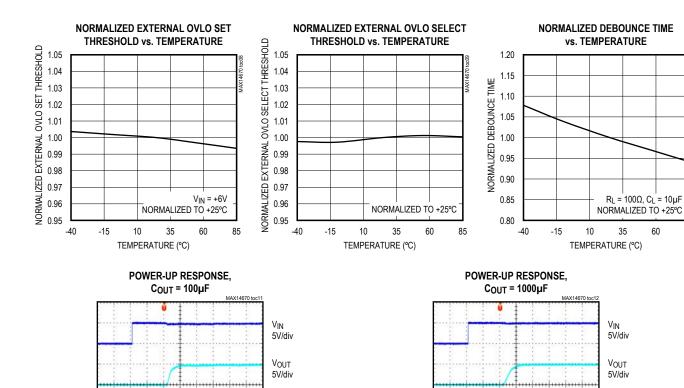
Typical Operating Characteristics

(V_{IN} = +5V, OVLO = GND, C_{IN} = 0.1 μ F, C_{OUT} = 1 μ F, T_A = +25°C, unless otherwise noted.)



Typical Operating Characteristicsc (continued)

 $(V_{IN}$ = +5V, OVLO = GND, C_{IN} = 0.1 μ F, C_{OUT} = 1 μ F, T_A = +25°C, unless otherwise noted.)



VACOK

2V/div

I_{OUT} = 500mA

 $C_{OUT} = 100 \mu F$

10ms/div

VACOK

2V/div

I_{OUT} = 500mA

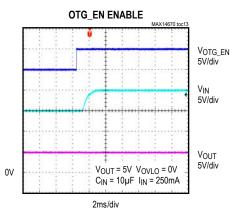
 $C_{OUT} = 1000 \mu F$

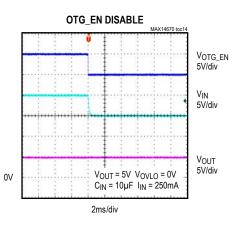
10ms/div

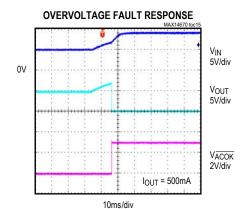
85

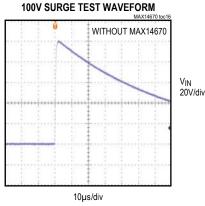
Typical Operating Characteristicsc (continued)

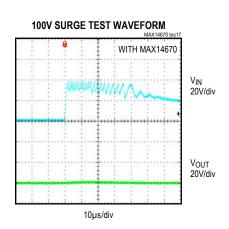
 $(V_{IN}$ = +5V, OVLO = GND, C_{IN} = 0.1 μ F, C_{OUT} = 1 μ F, T_A = +25°C, unless otherwise noted.)



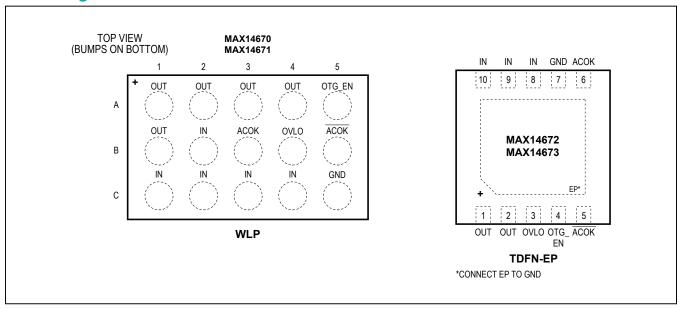








Pin Configurations

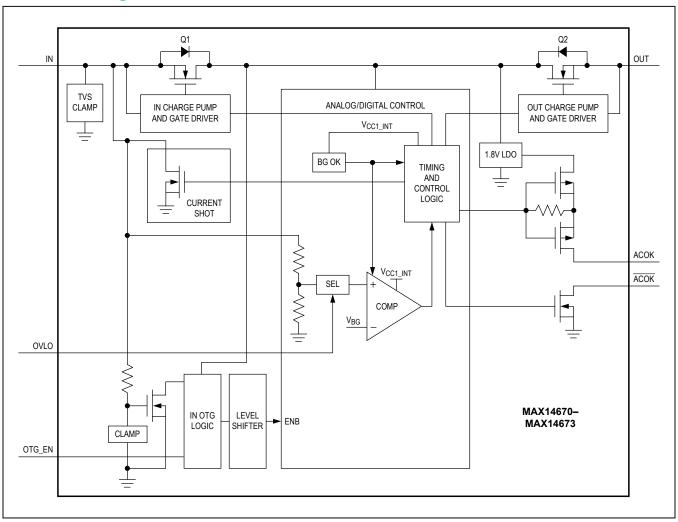


Pin Descriptions

BUMP	PIN			
MAX14670/ MAX14671	MAX14672/ MAX14673	NAME	FUNCTION	
A1, B1	1, 2	OUT	Overvoltage Protection Output. Bypass OUT with a 1µF ceramic capacitor. Externally connect all OUT together.	
A5	4	OTG_EN	Enable Input for OTG Supply Operation	
B2, C1-C4	8–10	IN	Overvoltage Protection Input. If desired, bypass IN with a 0.1µF ceramic capacitor as close to the device as possible. Externally connect all IN together.	
В3	6	ACOK	1.8V Logic Output. ACOK is driven high after input voltage is stable between minimum V_{IN} and V_{OVLO} when OTG_EN = 0. Connect a pulldown resistor from ACOK to ground.	
B4	3	OVLO	Overvoltage Lockout Input. Connect OVLO to GND to use internal OVLO threshold. Connect OVLO to a resistor-divider for a different voltage threshold.	
B5	5	ACOK	Open-Drain Flag Output. \overline{ACOK} is driven low after input voltage is stable between minimum V _{IN} and V _{OVLO} when OTG_EN = 0. Connect a pullup resistor from \overline{ACOK} to the logic I/O voltage of the host system.	
C5	7	GND	Ground	
_	_	EP	Exposed Pad (TDFN Only). Connect EP to ground.	

Bidirectional Current-Blocking, High-Input Overvoltage Protector with Adjustable OVLO

Functional Diagram



Bidirectional Current-Blocking, High-Input Overvoltage Protector with Adjustable OVLO

Detailed Description

The MAX14670–MAX14673 overvoltage protection (OVP) devices feature low on-resistance (R_{ON}) internal FETs (Q1+Q2) and protect low-voltage systems against voltage faults up to +28V $_{DC}$. An internal clamp also protects the devices from surges up to +100V. If the input voltage exceeds the overvoltage threshold, the output is disconnected from the input to prevent damage to the protected components. The 15ms debounce time prevents false turn-on of the internal FETs during startup.

Soft-Start

To minimize inrush current, the devices feature a soft-start capability to slowly turn on Q1 and Q2. Soft-start begins when ACOK/ACOK is asserted and ends after 15ms (typ).

Overvoltage Lockout (OVLO)

Connect OVLO to ground to use the internal OVLO comparator with the internally set OVLO value. When IN goes above the overvoltage lockout threshold (V_{IN_OVLO}), OUT is disconnected from IN and \overline{ACOK} / ACOK is deasserted. When IN drops below V_{IN_OVLO} , the debounce time starts counting. After the debounce time, OUT follows IN again and \overline{ACOK} /ACOK is asserted.

External OVLO Adjustment Functionality

When an external resistor-divider is connected to OVLO and V_{OVLO} exceeds the OVLO select voltage (V_{OVLO_SEL}), the internal OVLO comparator reads IN by the external resistor-divider.

R1 = $1M\Omega$ is a good starting value for minimum current consumption. Since V_{IN_OVLO} , V_{OVLO_TH} , and R1 are known, R2 can be calculated from the following formula:

$$V_{IN_OVLO} = V_{OVLO_TH} \times \left[1 + \frac{R1}{R2}\right]$$

This external resistor-divider is completely independent from the internal resistor-divider.

Reverse Bias Blocking

The ICs feature reverse bias blocking. When IN voltage is below input startup voltage and OTG_EN is low, the switch between IN and OUT is open and the two back-to-back diodes of the two series switches block reverse bias. Therefore, when the voltage is applied at the output, current does not travel back to the input. When OVLO is high, the parts block against reverse bias as well.

OTG Enable

The devices feature reverse turn-on capability. OTG_EN can be used to turn on the switch for OUT to feed back to IN when the voltage applied at OUT is above the minimum startup voltage. When OTG_EN is high, ACOK and ACOK are deasserted. During the OTG operation, if IN goes above OVLO, the OVP switch turns off. It is recommended that the power is supplied to OUT prior to OTG operation and also the power is removed from OUT prior to disable OTG operation.

Thermal Shutdown Protection

The devices feature thermal shutdown protection to protect the devices from overheating. The internal FETs turn off when the junction temperature exceeds +150°C (typ), and the device returns to normal operation after the temperature drops by approximately 20°C (typ).

Applications Information

IN Bypass Capacitor

If desired, bypass IN to GND with a $0.1\mu F$ ceramic capacitor as close to the device as possible. If the power source has significant inductance due to long lead length, the device prevents overshoots due to the LC tank circuit and provides protection by clamping the overshooting.

Output Capacitor

The slow turn-on time provides a soft-start function that allows the devices to charge an output capacitor up to $1000\mu F$ without turning off due to an overcurrent condition. Bypass OUT to GND with a minimum of $1\mu F$ ceramic capacitor.

Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (Human Body Model) encountered during handling and assembly. IN is further protected against ESD up to ±15kV (HBM), ±15kV (Air-Gap Discharge method described in IEC 61000-4-2) and ±8kV (Contact Discharge Method described in IEC 61000-4-2) without damage.

The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14670–MAX14673 continue to function without latchup.

Bidirectional Current-Blocking, High-Input Overvoltage Protector with Adjustable OVLO

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model ESD Protection

<u>Figure 2</u> shows the HBM and <u>Figure 3</u> shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a $1.5k\Omega$ resistor.

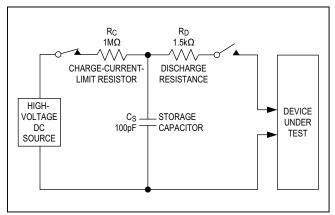


Figure 2. Human Body ESD Test Model

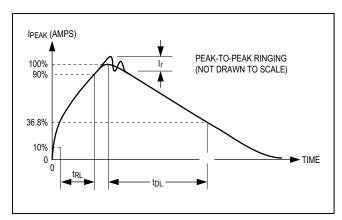


Figure 3. Human Body Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 4 shows the IEC 61000-4-2 model, and Figure 5 shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

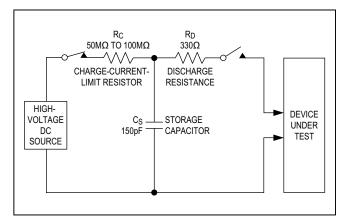


Figure 4. IEC 61000-4-2 ESD Test Model

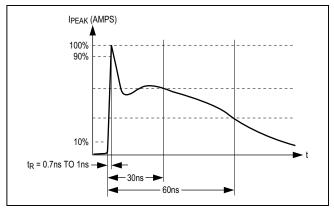
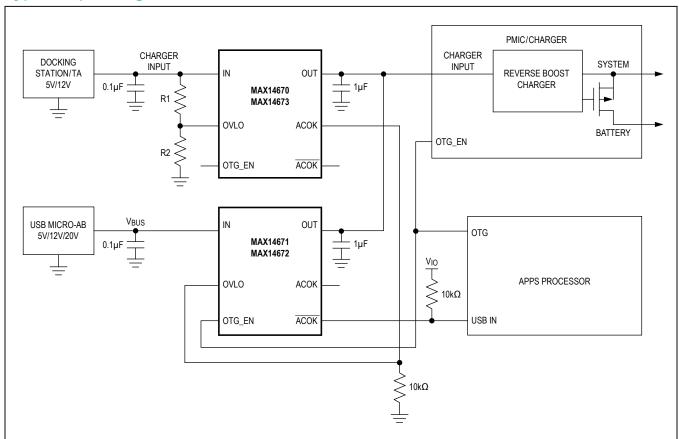


Figure 5. IEC 61000-4-2 ESD Generator Current Waveform

Typical Operating Circuit



Ordering Information/Selector Guide

PART	OVLO (V)	TOP MARK	PIN- PACKAGE
MAX14670EWL+T	6.8	+14670EWL	15 WLP
MAX14671EWL+T	15.5	+14671EWL	15 WLP
MAX14672ETB+T	5.825	AZF	10 TDFN-EP*
MAX14673ETB+T**	22	AZG	10 TDFN-EP*

Note: All devices are specified over -40°C to +85°C operating temperature range.

Chip Information

PROCESS: BICMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN	T1033+1	21-0137	90-0003
15 WLP	W151C2+1	21-0686	Refer to Application Note 1891

⁺Denotes a lead(Pb)-free package/RoHS-compliant package. T = Tape and reel.

^{*}EP = Exposed pad.

^{**}Future product—contact factory for availability.

MAX14670-MAX14673

Bidirectional Current-Blocking, High-Input Overvoltage Protector with Adjustable OVLO

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/13	Initial release	_
1	7/13	Update Functional Diagram	9
2	8/13	Included soldering lead time; corrected nFET and pFET arrows in Functional Diagram	2, 9
3	10/13	Updated Functional Diagram	9
4	1/14	Updated data sheet to reflect 100V surge protection capability	1, 2, 7, 10

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

ПОСТАВКА ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9