STW82102B

RF down converter with embedded integer-N synthesizer

Datasheet – production data

Features

- High linearity:
  - IIP3: +25.5 dBm
  - 2FRF-2FLO spurious rejection: 85 dBc
- Noise figure:
  - NF: 10.5 dB
- Conversion gain
  - CG: 8 dB
- RF range: 1425 MHz to 1910 MHz
- Wide IF amplifier frequency range: 70 MHz to 400 MHz
- Integrated RF balun with internal matching
- Dual differential integrated VCOs with automatic center frequency calibration:
  - LOA: 1500 to 1800 MHz
  - LOB: 1900 to 2200 MHz
- Embedded integer-N synthesizer
  - Dual modulus programmable prescaler (16/17 or 19/20)
  - Programmable reference frequency divider (10 bits)
  - Adjustable charge pump current
  - Digital lock detector
  - Excellent integrated phase noise
  - Fast lock time: 150 µs
- Integrated DAC with dual current output
- Supply: 3.3 V and 5 V analog, 3.3 V Digital
- Dual digital bus interface: SPI and I^2C bus (fast mode) with 3 bit programmable address ($1101A_2A_1A_0$)
- Process: 0.35 µm BICMOS SiGe
- Operating temperature range -40 to +85°C
- 44-lead exposed pad VFQFPN package 7x7x1.0 mm

VFQFPN-44

Applications

- Cellular infrastructure equipment:
  - IF sampling receivers
  - Digital PA linearization loops
- Other wireless communication systems.

Table 1. Device summary

Part number	Package	Packaging
STW82102B	VFQFPN-44	Tray
STW82102BTR	VFQFPN-44	Tape and reel

Description

The STMicroelectronics STW82102B is an integrated down converter providing 8 dB of gain, 10.5 dB NF, and a very high input linearity by means of its passive mixer.

Embedding two wide band auto calibrating VCOs and an integer-N synthesizer, the STW82102B is suitable for both Rx and Tx requirements for cellular infrastructure equipment.

The integrated RF balun and internal matching permit direct 50 ohm single-ended interface to RF port. The IF output is suitable for driving 200-ohm impedance filters.

By embedding a DAC with dual current output to drive an external PIN diode attenuator, the STW82102B replaces several costly discrete components and offers a significant footprint reduction.

The STW82102B device is designed with STMicroelectronics advanced 0.35 µm SiGe process. Its performance is specified over a -40 °C to +85 °C temperature range.

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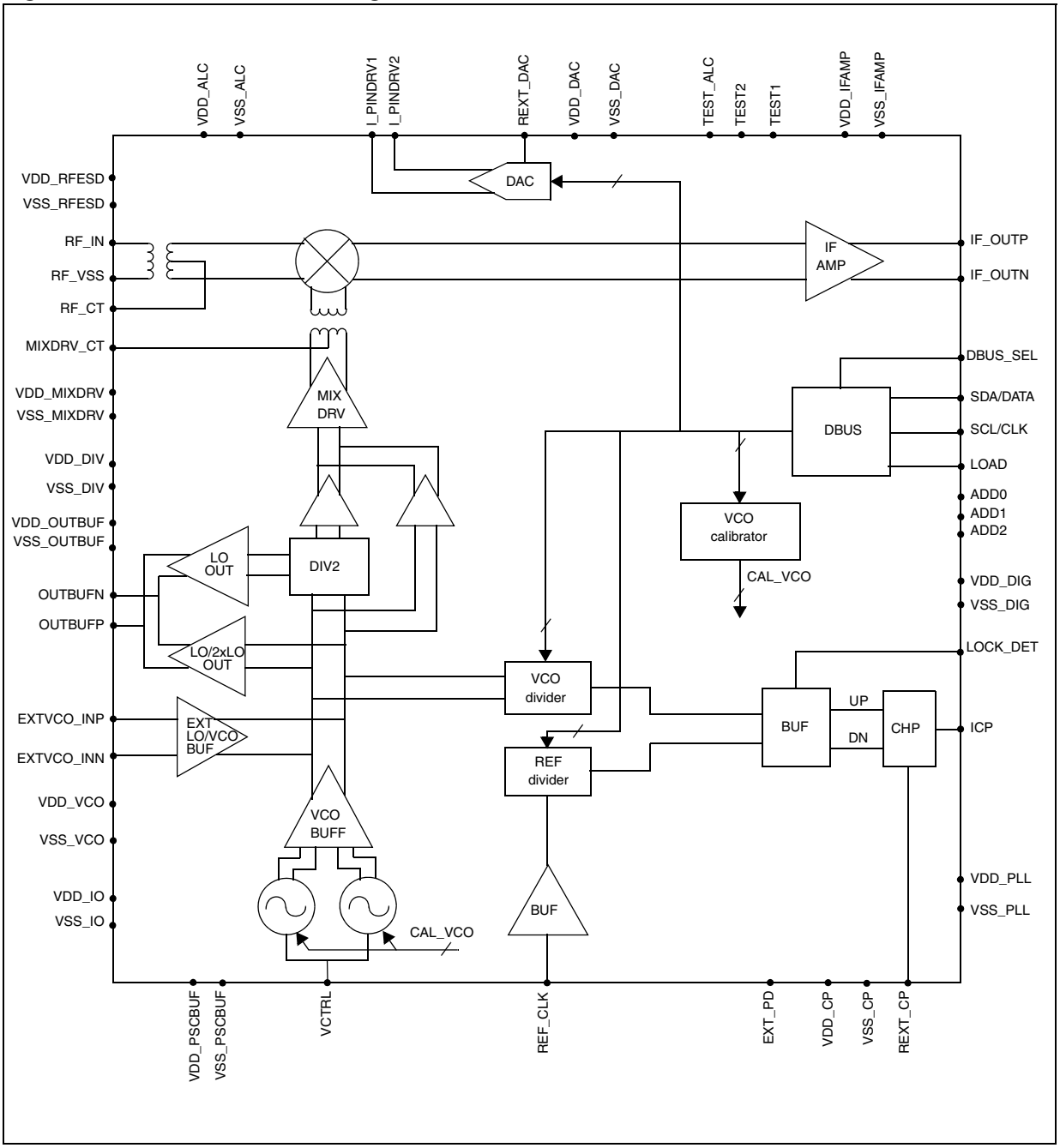
1 Block diagram

Figure 1. STW82102B block diagram



2 Pin description

Figure 2. STW82102B pin configuration

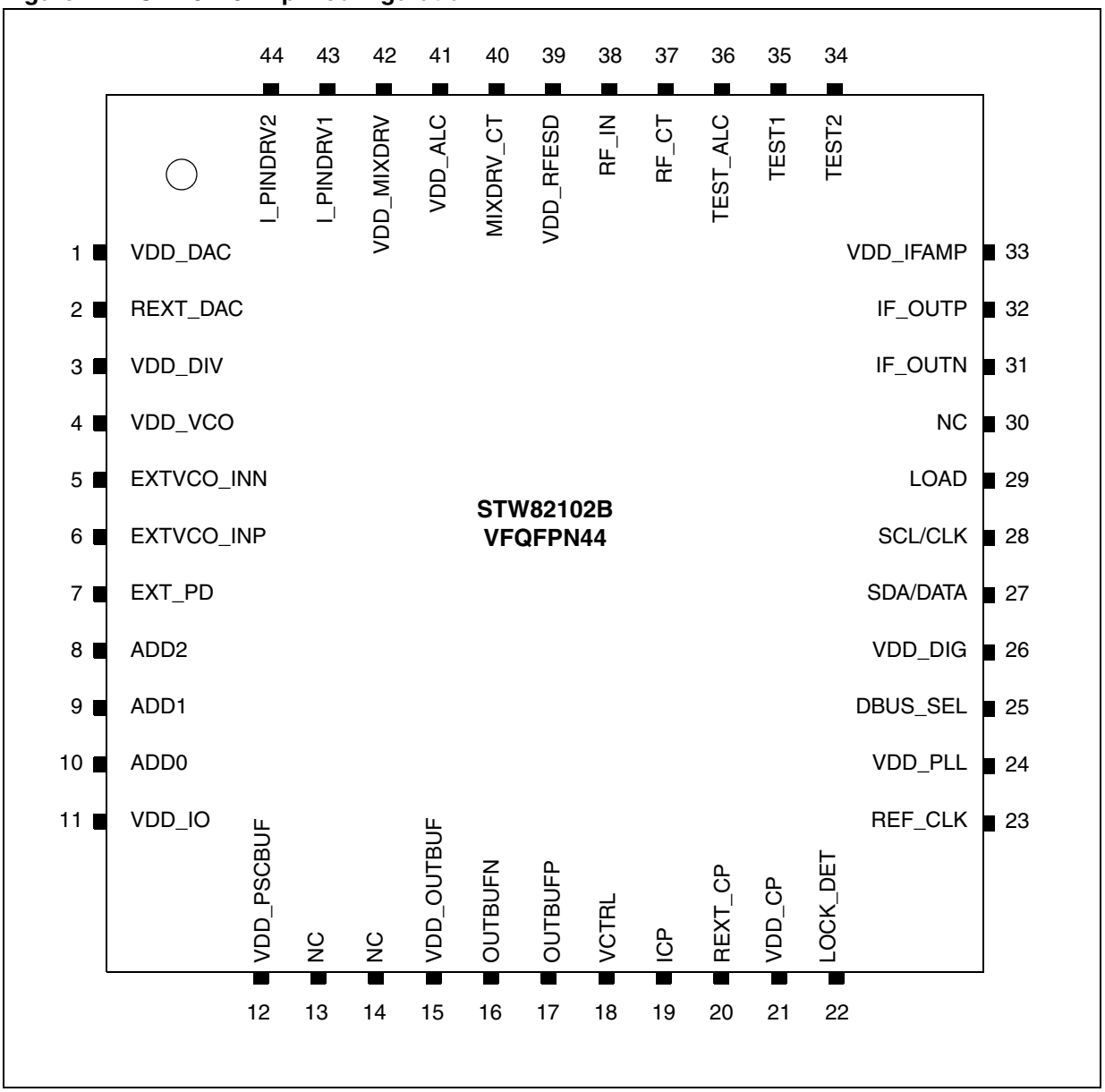


Table 2. Pin list

Pin No	Name	Description	Observation
1	VDD_DAC	DAC power supply	Vsupply analog1= 3.3 V
2	REXT_DAC	External resistance connection for DAC	-
3	VDD_DIV	Divider by 2 power supply	Vsupply analog1= 3.3 V
4	VDD_VCO	VCOs and External VCO Buffer power supply	Vsupply analog1= 3.3 V
5	EXTVCO_INN	External VCO (LO) negative input	Diversity Slave Mode and External VCO Modes; otherwise it must be connected to GND
6	EXTVCO_INP	External VCO (LO) positive input	Diversity Slave Mode and External VCO Modes; otherwise it must be connected to GND
7	EXT_PD	Hardware power down: '0' device ON; '1' device OFF	CMOS Input
8	ADD2	I^2CBUS address select pin	CMOS Input
9	ADD1	I^2CBUS address select pin	CMOS Input
10	ADD0	I^2CBUS address select pin	CMOS Input
11	VDD_IO	Digital IO power supply	Vsupply digital = 3.3 V
12	VDD_PSCBUF	Prescaler input buffer power supply	Vsupply analog1= 3.3 V
13	NC	Not connected	-
14	NC	Not connected	-
15	VDD_OUTBUF	Power supply for LO buffer	Vsupply analog1=3.3 V
16	OUTBUFN	LO Output buffer negative output	Open collector @3.3 V
17	OUTBUFP	LO Output buffer positive output	Open collector @ 3.3 V
18	VCTRL	Control voltage for VCOs	-
19	ICP	PLL charge pump output	-
20	REXT_CP	External resistance connection for PLL charge pump current	-
21	VDD_CP	Power supply for charge pump	Vsupply analog1= 3.3 V
22	LOCK_DET	Lock detector	CMOS Output
23	REF_CLK	Reference frequency input	-
24	VDD_PLL	PLL digital power supply	Vsupply analog1= 3.3 V
25	DBUS_SEL	Digital Bus Interface select	CMOS Input
26	VDD_DIG	Power supply for digital bus interface	Vsupply digital = 3.3 V
27	SDA/DATA	I^2CBUS /SPI data line	CMOS Bidir Schmitt triggered
28	SCL/CLK	I^2CBUS /SPI clock line	CMOS Input Schmitt triggered
29	LOAD	SPI load line	CMOS Input Schmitt triggered
30	NC	Not connected	-
31	IF_OUTN	IF amplifier negative output	Open collector @ 5 V(1)

Table 2. Pin list (continued)

Pin No	Name	Description	Observation
32	IF_OUTP	IF Amplifier positive output	Open collector @ 5 V(1)
33	VDD_IFAMP	IF Amplifier power supply	Vsupply analog1 = 3.3 V
34	TEST2	Test input 2	Test purpose only; it must be connected to GND
35	TEST1	Test input 1	Test purpose only; it must be connected to GND
36	TEST_ALC	Test output	Test purpose only; it must be connected to GND
37	RF_CT	RF balun central tap	-
38	RF_IN	RF input	-
39	VDD_RFESD	RF ESD positive rail power supply	Vsupply analog1 = 3.3 V
40	MIXDRV_CT	Mixer driver balun central tap	Vsupply analog2 = 5 V(1)
41	VDD_ALC	ALC power supply	Vsupply analog1 = 3.3 V
42	VDD_MIXDRV	Mixer driver power supply	Vsupply analog1 = 3.3 V
43	I_PINDRV1	DAC current output for external PIN Diode attenuator	PMOS Open drain
44	I_PINDRV2	DAC current output for external PIN Diode attenuator	PMOS Open drain

1. Supply voltage @ 3.3 V in low-current mode operation

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AVCC1	Analog Supply voltage	0 to 4.6	V
AVCC2	Analog Supply voltage	0 to 6	V
DVCC	Digital Supply voltage	0 to 4.6	V
Tstg	Storage temperature	+150	°C
ESD (Electro-static discharge)	HBM on pins 16, 17, 31, 32	0.8	kV
	HBM on pin 37, 38, 40	1	
	HBM on all remaining pins	2	
	CDM-JEDEC Standard on pin 38	0.25	
	CDM-JEDEC Standard on all remaining pins	0.5	
	MM on pins 16,17	0.15	
	MM on all remaining pins	0.2	

4 Operating conditions

Table 4. Operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AVCC1	Analog Supply voltage	-	3.15	3.3	3.45	V
AVCC2	Analog Supply voltage	-	4.75	5	5.25	V
DVCC	Digital Supply voltage	-	3.15	3.3	3.45	V
$I_{CC3.3V}$	Current Consumption at 3.3 V	Standard mode	-	130	150	mA
		External VCO standard mode	-	110	130	mA
		Diversity slave mode	-	105	120	mA
		Diversity master mode	-	155	180	mA
		External VCO diversity master mode	-	140	160	mA
I_{CC5V}	Current Consumption	High current mode at 5 V	-	160	185	mA
		Low current mode at 3.3 V	-	95	110	mA
T_A	Operating ambient temperature	-	-40		85	°C
T_J	Maximum junction temperature	-	-		125	°C
Θ_{JA}	Junction to ambient package thermal resistance(1)	Multi-layer JEDEC board	-	33	-	°C/W
Θ_{JB}	Junction to board package thermal resistance(1)	Multi-layer JEDEC board	-	19	-	°C/W
Θ_{JC}	Junction to case package thermal resistance(1)	Multi-layer JEDEC board	-	3	-	°C/W
Ψ_{JB}	Thermal characterization parameter junction to board(1)	Multi-layer JEDEC board	-	18	-	°C/W
Ψ_{JT}	Thermal characterization parameter junction to top case(1)	Multi-layer JEDEC board	-	0.3	-	°C/W

1. Refer to JEDEC standard JESD 51-12 for a detailed description of the thermal resistances and thermal parameters. Data here presented are referring to a Multi-layer board according to JEDEC standard.
$T_J = T_A + \Theta_{JA} * Pdiss$ (in order to estimate T_J if ambient temperature T_A and dissipated power Pdiss are known)
$T_J = T_B + \Psi J_B * Pdiss$ (in order to estimate T_J if board temperature T_B and dissipated power Pdiss are known)
$T_J = T_T + \Psi J_T * Pdiss$ (in order to estimate T_J if top case temperature T_T and dissipated power Pdiss are known)

Table 5. Digital logic levels

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Vil	Low level input voltage	-	-	-	0.2*Vdd	V
Vih	High level input voltage	-	0.8*Vdd	-	-	V
Vhyst	Schmitt trigger hysteresis	-	0.8	-	-	V
Vol	Low level output voltage	-	-	-	0.4	V
Voh	High level output voltage	-	0.85*Vdd	-	-	V

5 Test conditions

Unless otherwise specified the following test conditions are applied:

- Vsupply digital = 3.3 V
- Vsupply analog1 = 3.3 V
- Vsupply analog2 = 5 V
- F_{IF} = 150 MHz
- MIX = 0111
- T ambient = 27 °C

Refer also to *Section 11: Application information*.

6 Electrical characteristics

*Note: Vsupply digital = 3.3 V, Vsupply analog1 = 3.3 V, Vsupply analog2 = 5 V, F_{RF} = 1700 MHz, F_{LO} = 1550 MHz, T_A = +25*C, RF power = 0 dBm, unless otherwise specified.*

Table 6. Down converter mixer and IF amplifier electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{RF}	RF Frequency	-	1425	-	1910	MHz
F_{LO}	LO Frequency	VCOA divided by 2	1500	-	1800	MHz
		VCOB divided by 2	1900	-	2200	MHz
F_{IF}	IF Center Frequency(2)	F_{IF} = ABS(F_{LO}-F_{RF})	70	-	400	MHz
CG	Power Conversion Gain	Rin = 50 ohm, Rout = 200 ohm RFin = 0 dBm	7.5	8	8.5	dB
$CG_{\Delta T}$	Power Conversion Gain over Temperature(3)	T= -40 to +85 °C	-	±0.6	-	dB
IP_{1dB}	Input P1dB	High current Mode	-	13.5	-	dBm
		Low current Mode	-	8	-	
IIP3	Third-order input intercept point(4)	High current Mode	25	25.5	-	dBm
		Low current Mode	19	19.5	-	
$IIP3_{\Delta T}$	IIP3 variation over temperature(3)	T= -40 to +85 °C	-	±0.5	-	dB
nF_{RF}-nF_{LO}	Spurious rejection at IF(3)	$2F_{RF}$-$2F_{LO}$ F_{RFin} = -5 dBm, F_{IF} = 150 MHz	-	85	-	dBc
		$3F_{RF}$-$3F_{LO}$ F_{RFin} = -5 dBm, F_{IF} = 150 MHz	-	76	-	dBc
NF_{SSB}	Noise figure	High-current mode, MIX = 0011	-	10.5	11	dB
		Low-current mode, MIX = 0011	-	10.5	11	dB
-	LO to IF Leakage	1xLO	-	-35	-	dBm
		2xLO		-34		
-	LO to RF Leakage	-	-	-27	-	dBm
-	RF to IF Isolation	-	-	45	-	dB
RF_{RL}	RF Return Loss	Matched to 50 ohm	-	20	-	dB
IF_{RL}	IF Return Loss	Matched to 200 ohm	-	25	-	dB
-	Gain Flatness for TX observation path(5)	Maximum deviation from F_c over ±10 MHz. For any F_c within each TX observation path band.	-0.05	-	+0.05	dB
		Maximum deviation from F_c over ±30 MHz. For any F_c within each TX observation path band.	-0.10	-	+0.10	dB

Table 6. Down converter mixer and IF amplifier electrical characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
-	Phase Flatness for TX observation path(5)	Maximum deviation from linear phase at F_c over ±10 MHz. For any F_c within each TX observation path band.	-0.3	-	+0.3	deg
		Maximum deviation from linear phase at F_c over ±30 MHz. For any F_c within each TX observation path band.	-0.7	-	+0.7	deg
-	Gain Flatness for RX path(5)	Maximum ripple over a 4 MHz band. For any F_c within each RX path band.	-	-	0.1	dB pk-pk
-	Phase Flatness for RX path(5)	Maximum ripple over a 4 MHz band. For any F_c within each RX path band.	-	-	0.6	deg pk-pk
ICC_{MD}	Mixer Driver Current Consumption	3.3 V Supply (pin 41, 42)	-	48	-	mA
		5 V Supply (pin 40)	-	50	-	mA
	Mixer Driver Current Consumption (Low Current Mode)	3.3 V Supply (pin 41, 42)	-	20	-	mA
		3.3 V Supply (pin 40)	-	35	-	mA
ICC_{IFAM}	IFAMP Current Consumption	3.3 V Supply (pin 33)	-	10	-	mA
		5 V Supply (pin 31, 32)	-	107	-	mA
	IFAMP Current Consumption (Low Current Mode)	3.3 V Supply (pin 33)	-	6	-	mA
		3.3 V Supply (pin 31, 32)	-	55	-	mA

1. All linearity and NF performances are intended at maximum LO amplitude (LO_A[1:0]=[11]), tuning capacitors (CAP[2:0]) programmed according to the selected frequency, mixer bias (MIX[3:0]) set to maximize performance and the device operated in high current mode. The performances of conversion gain, NF and linearity are intended at the SMA connectors of a typical application board.
2. The IF frequency range supported by the IF Amplifier is from 70 to 400 MHz. The exact IF frequency range supported for a specific RF frequency can be calculated as $F_{IF} = ABS(F_{LO}-F_{RF})$ where F_{LO} is inside the specified LO frequency range.
3. Guaranteed by design and characterization
4. RFin = 0 dBm/tone, RF tone spacing = 5 MHz
5. Guaranteed by design

Table 7. Pin diode attenuator driver (dual output current DAC) electrical characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
R	Resolution	-	-	10	-	Bit
DNL	Differential non linearity	-	-0.05	-	0.05	LSB
INL	Integral non linearity	-	-0.45	-	0.45	LSB
I_{FS}	Full Scale current (1)	-	0.28	-	2.8	mA
-	Current Mismatch	-	-	-	2	%
-	Output voltage compliance range	-	0	-	3	V
VR_{EXT_DAC}	Voltage Reference	-	-	1.19		V
R_{EXT_DAC}	REXT DAC Range	-	10	-	100	kΩ
Icc_{static}	Static current consumption	(Iout = 0 mA; pin 1)	-	2.5	-	mA

1. See relationship between IDAC and R_{EXT_DAC} in the Circuit Description section (Dual Output Current DAC)

Table 8. Integer-N synthesizer electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCO dividers						
N	VCO Divider Ratio (N)	Prescaler 16/17	256	-	65551	-
		Prescaler 19/20	361	-	77836	-
Reference clock and phase frequency detector						
F_{ref}	Reference input frequency	-	10	19.2	200	MHz
-	Reference input sensitivity	-	0.35	1	1.5	Vpeak
R	Reference Divider Ratio	-	2	-	1023	
F_{PFD}	PFD input frequency	-	-	-	16	MHz
F_{STEP}	Frequency step (1)	Prescaler 16/17	F_{LO}/ 65551	-	F_{LO}/ 256	Hz
		Prescaler 19/20	F_{LO}/ 77836	-	F_{LO}/ 361	Hz
Charge pump						
I_{CP}	ICP sink/source (2)	3bit programmable	-	-	5	mA
V_{OCP}	Output voltage compliance range	-	0.4	-	V_{dd}-0.3	V
-	Spurious(3)	-	-	-70	-	dBc
VCOs						
K_{VCOA}	VCOA sensitivity	Higher frequency range	-	100	-	MHz/V
		Intermediate frequency range	-	85	-	MHz/V
		Lower frequency range	-	70	-	MHz/V
K_{VCOB}	VCOB sensitivity	Higher frequency range	-	85	-	MHz/V
		Intermediate frequency range	-	70	-	MHz/V
		Lower frequency range	-	60	-	MHz/V
ΔT_{LKA}	VCOA maximum temperature variation for continuous lock(4)	CALTYPE [0]	-	-	125	°C
		CALTYPE [1]	-	-	125	°C
ΔT_{LKB}	VCOB maximum temperature variation for continuous lock (4))	CALTYPE [0]	-	-	115	°C
		CALTYPE [1]	-	-	125	°C
-	VCO A Pushing	-	-	8	-	MHz/V
	VCO B Pushing	-	-	14	-	MHz/V
V_{CTRL}	VCO control voltage	-	0.4		V_{dd}-0.3	V
-	LO Harmonic Spurious	-	-		-20	dBc
I_{VCO}	VCO and VCO buffer current consumption	Amplitude [11] (pin 4)	-	35	-	mA
I_{DIV2}	DIVIDER by 2 consumption	(pin 3)	-	20	-	mA

Table 8. Integer-N synthesizer electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
2 x LO output buffer (test purpose only)						
F_{OUT}	Frequency range	-	3.0	-	4.4	GHz
P_{OUT}	Output level	-	-	0	-	dBm
RL	Return Loss	Matched to 50ohm	-	10	-	dB
I_{2LOBUF}	Current Consumption	(pin 15, 16, 17)	-	28	-	mA
LO output buffer						
F_{OUT}	Frequency range	-	1.5	-	2.2	GHz
P_{OUT}	Output level	-	-	3	-	dBm
RL	Return Loss	Matched to 50ohm	-	12	-	dB
I_{LOBUF}	Current Consumption	(pin 15, 16, 17)	-	28	-	mA
External VCO (LO) buffer						
f_{INVCO}	Frequency range	-	1.5	-	2.2	GHz
P_{IN}	Input level	-	-	0	-	dBm
I_{EXTBUF}	Current Consumption	External VCO Buffer (pin 4)	-	25	-	mA
PLL miscellaneous						
I_{PLL}	PLL Current Consumption	Input Buffer, Prescaler, Digital Dividers, misc. (pin 24)	-	8	-	mA
I_{PRE}	Prescaler input buffer Current Consumption	(pin 12)	-	3	-	mA
I_{CP}	Charge Pump Current Consumption	CPSEL=[111], REXT_CP = 4.7 kΩ (pin 21)	-	4	-	mA
t_{LOCK}	Lock up time(5)	25 kHz PLL bandwidth; within 1ppm of frequency error	-	150	-	µs

1. The frequency step is related to the PFD input frequency as follows: $F_{STEP}=F_{PFD}/2$)
2. See relationship between ICP and R_{EXT_CP} in the Circuit Description section (Charge Pump)
3. The level of spurs may change depending on PFD frequency, Charge Pump current, selected channel and PLL loop BW.
4. When setting a specified output frequency, the VCO calibration procedure must be run first in order to select the best sub-range for the VCO covering the desired frequency. Once programmed at the initial temperature T_0 inside the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status if the temperature drift (in either direction) is within the limit specified by ΔT_{LK}, provided that the final temperature T_1 is still inside the nominal range.
5. Frequency jump form 1900 to 2050 MHz; it includes the time required by the VCO calibration procedure (7 x F_{PFD} cycles =17.5 µs with F_{PFD} =400 kHz))

Table 9. Phase noise performance(1)

Parameters	Conditions	Min.	Typ.	Max.	Unit
In band phase noise floor, closed loop(2)					
Normalized In Band Phase Noise Floor (LO)	I_{CP}=4 mA, PLL BW = 50 kHz (including reference clock contribution)	-	-230	-	dBc/Hz
In Band Phase Noise Floor (LO)		-230+20log(N)+10log(F_{PFD})			dBc/Hz
PLL integrated phase noise					
Integrated Phase Noise (single sided) 100 Hz to 40 MHz	F_{LO}=2.050 GHz, F_{STEP}=200 kHz, I_{CP}=3 mA, PLL BW = 25 kHz	-	-45.3	-	dBc
		-	0.44	-	° rms
LOA (1500 MHz to 1800 MHz) – open loop					
Phase Noise @ 1 kHz	-	-	-69	-	dBc/Hz
Phase Noise @ 10 kHz	-	-	-96	-	dBc/Hz
Phase Noise @ 100 kHz	-	-	-118	-	dBc/Hz
Phase Noise @ 1 MHz	-	-	-139	-	dBc/Hz
Phase Noise @ 10 MHz	-	-	-153	-	dBc/Hz
Phase Noise Floor @ 40 MHz	-	-	-156	-	dBc/Hz
LOB (1900 MHz to 2200 MHz) – open loop					
Phase Noise @ 1 kHz	-	-	-64	-	dBc/Hz
Phase Noise @ 10 kHz	-	-	-91	-	dBc/Hz
Phase Noise @ 100 kHz	-	-	-115	-	dBc/Hz
Phase Noise @ 1 MHz	-	-	-136	-	dBc/Hz
Phase Noise @ 10 MHz	-	-	-152	-	dBc/Hz
Phase Noise Floor @ 40 MHz	-	-	-156	-	dBc/Hz

1. Phase Noise SSB. VCO amplitude set to maximum value [11]. All the closed-loop performances are specified using a Reference Clock signal at 76.8 MHz with phase noise of -144 dBc/Hz @1 kHz offset, -157 dBc/Hz @10 kHz offset and -168 dBc/Hz of noise floor.
2. Normalized PN = Measured LO PN – 20log(N) – 10log(F_{PFD}) where N is the VCO divider ratio (N=B*P+A) and F_{PFD} is the comparison frequency at the PFD input

7 Typical performance characteristics

Note: Vsupply digital = 3.3 V, Vsupply analog1 = 3.3 V, Vsupply analog2 = 5 V, F_{IF} = 150 MHz, T_A = +25 °C, RF power = 0 dBm, unless otherwise specified.

Figure 3. Conversion gain against RF frequency

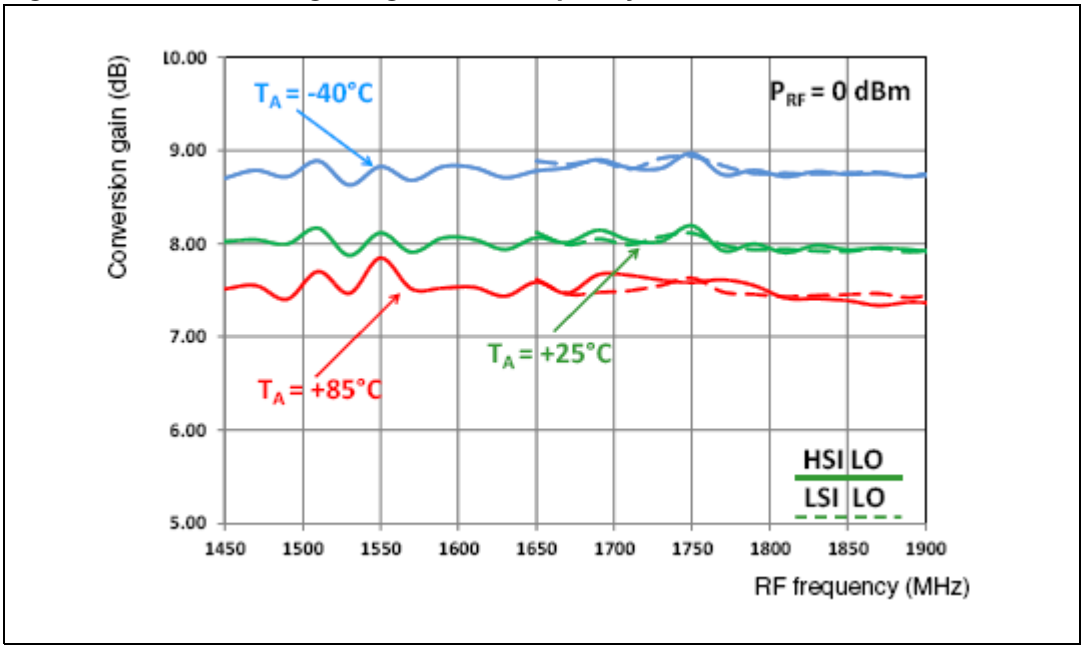


Figure 4. Noise figure against RF frequency

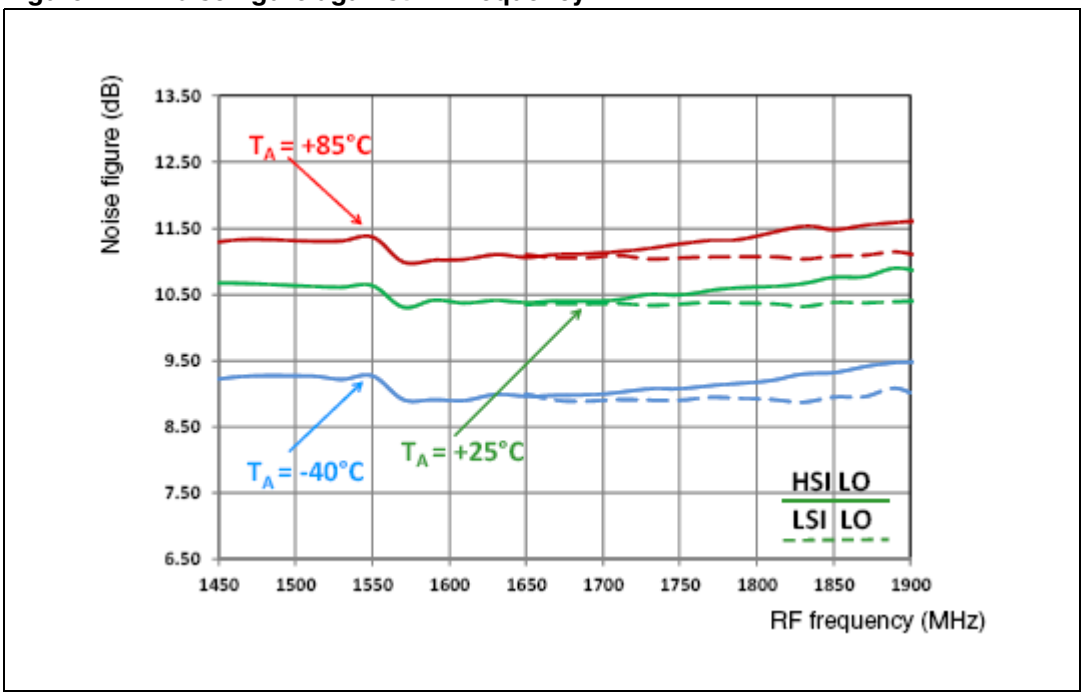


Figure 5. IIP3 against RF frequency

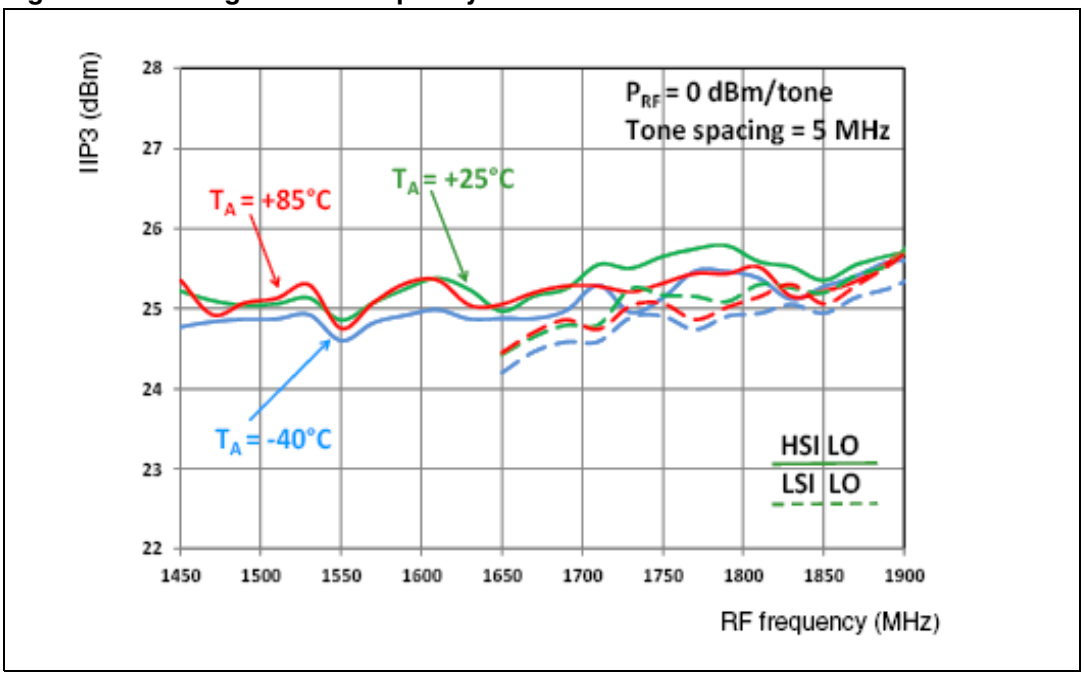


Figure 6. 2RF-2LO response against RF frequency

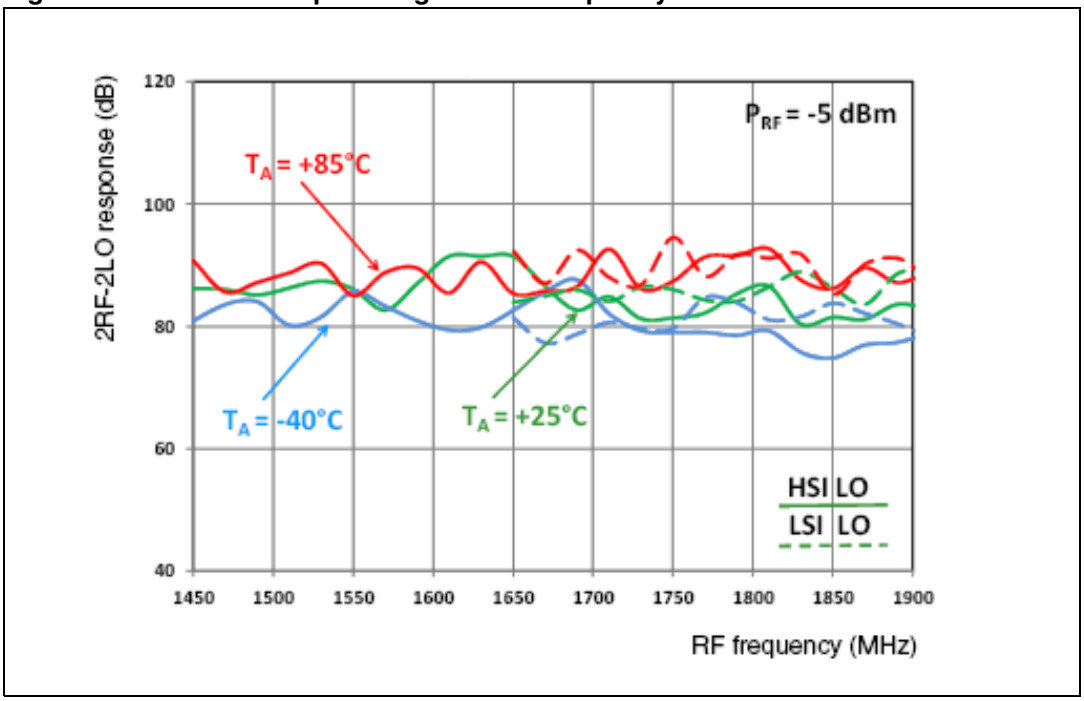


Figure 7. LOA (VCOA div. by 2) closed-loop phase noise at 1.65 GHz (F_{STEP} = 200 kHz, I_{CP} = 3 mA)

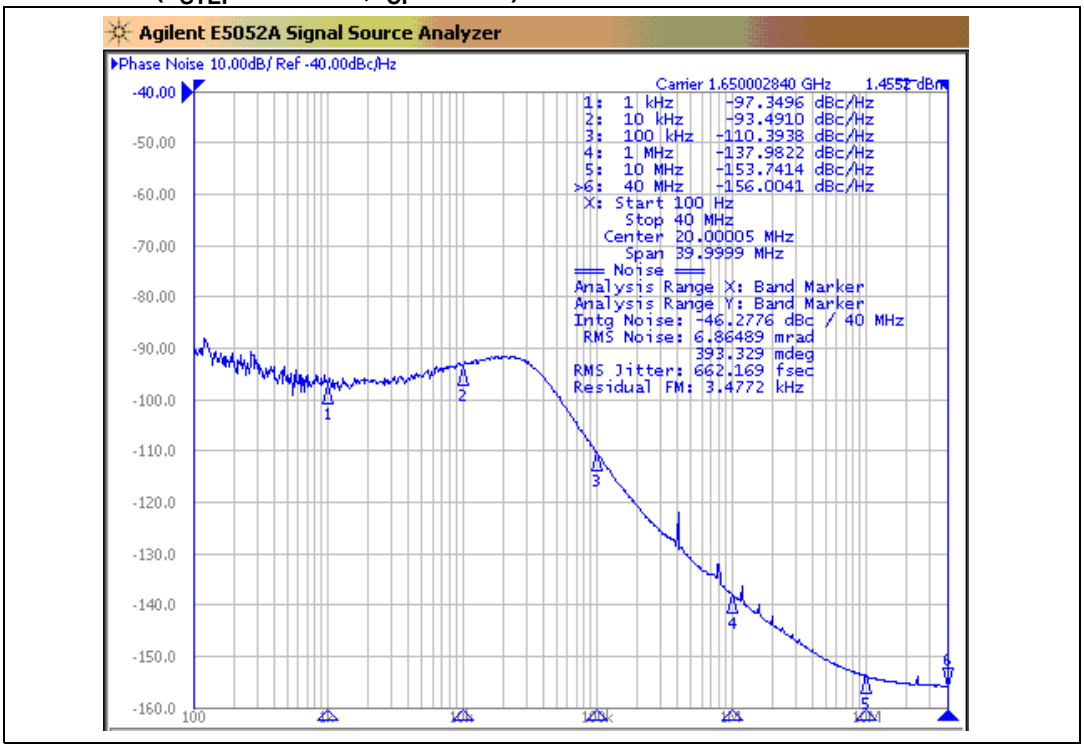
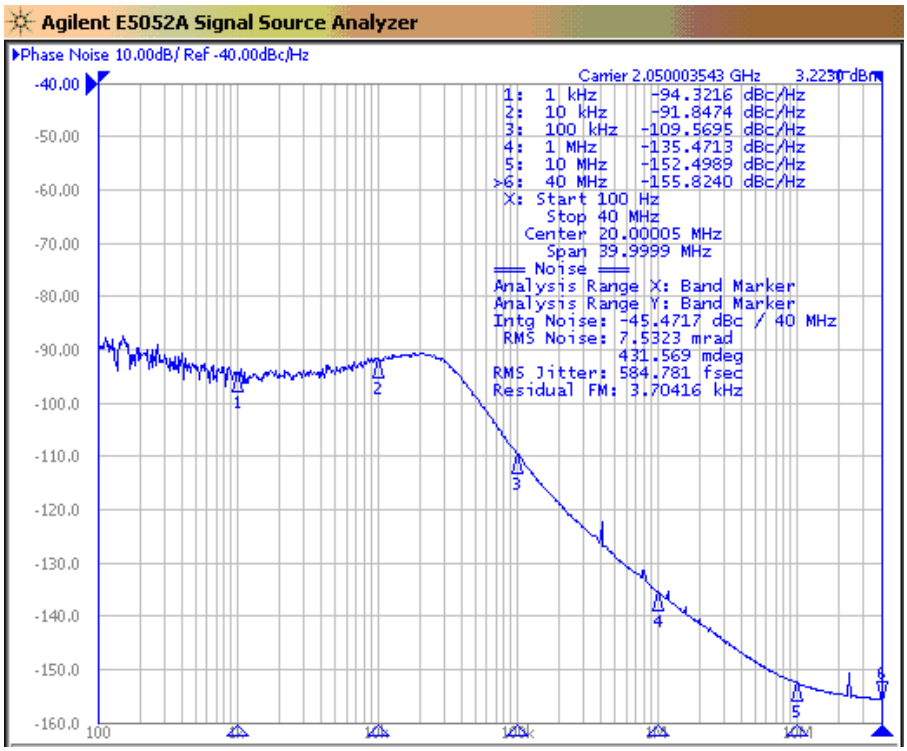


Figure 8. LOB (VCOB div. by 2) closed-loop phase noise at 2.05 GHz (F_{STEP} = 200 kHz, I_{CP} = 3 mA)



8 General description

The STW82102B (see *Figure 1: STW82102B block diagram on page 7*) consists of a high linearity passive CMOS mixer with integrated RF balun, an IF amplifier, a 10-bit current steering DAC with dual output, and an integrated integer-N synthesizer.

The synthesizer embeds 2 internal low-noise VCOs with buffer blocks, a divider by 2, a low noise PFD (Phase Frequency Detector), a precise charge pump, a 10-bit programmable reference divider, two programmable counters and a dual-modulus prescaler. The A-counter (5 bits) and B counter (12 bits) counters, in conjunction with the dual modulus prescaler P/P+1 (16/17 or 19/20), implement an N integer divider, where N = B*P+A.

The device is controlled through a digital interface (*I2C bus interface* or *SPI digital interface*).

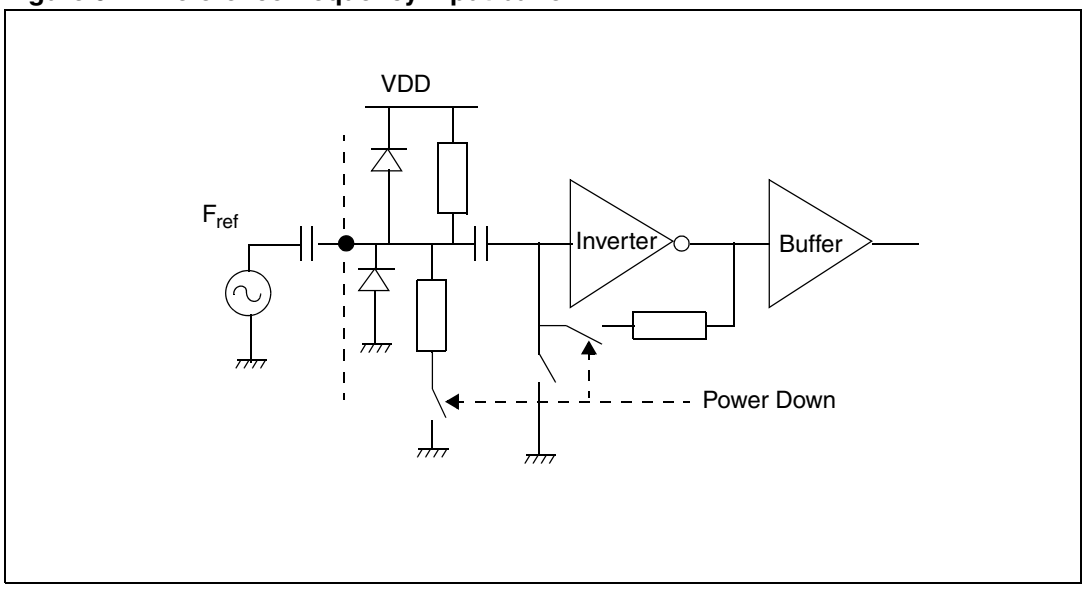
All internal devices operate with a power supply of 3.3 V except for the IF Amplifier output stage and the mixer driver stage operating at 5 V power supply in order to maximize the linearity performance. If the application requires a reduced linearity and noise figure performance the device is programmed in a low-current mode by using the minimum LO amplitude and the minimum biasing current in the IF amplifier. In low-current mode operation the device can use only the 3.3 V power supply thus dissipating less power.

8.1 Circuit description

8.1.1 Reference input stage

The reference input stage is shown in *Figure 9*. The resistor network feeds a DC bias at the F_{ref} input while the inverter used as the frequency reference buffer is AC coupled.

Figure 9. Reference frequency input buffer



8.1.2 Reference divider

The 10-bit programmable reference counter allows the input reference frequency to be divided to produce the input clock to the PFD. The division ratio is programmed through the digital interface.

8.1.3 Prescaler

The dual-modulus prescaler P/P+1 takes the CML clock from the VCO buffer and divides it down to a manageable frequency for the CMOS A and B counters. The modulus (P) is programmable and can be set to 16 or 19. It is based on a synchronous 4/5 core which division ratio depends on the state of the modulus input.

8.1.4 A and B counters

The A (5 bits) and B (12 bits) counters, in conjunction with the selected dual modulus (16/17 or 19/20) prescaler make it possible to generate output frequencies which are spaced only by the reference frequency divided by the reference division ratio. Thus, the division ratio and the VCO output frequency are given by the following formulae:

$$N = B \times P + A$$

$$F_{VCO} = \frac{(B \times P + A) \times F_{ref}}{R}$$

where:

F_{VCO}: VCO output frequency.

P: modulus of dual modulus prescaler (16 or 19 selected through the digital interface).

B: division ratio of the main counter.

A: division ratio of the swallow counter.

F_{ref}: input reference frequency.

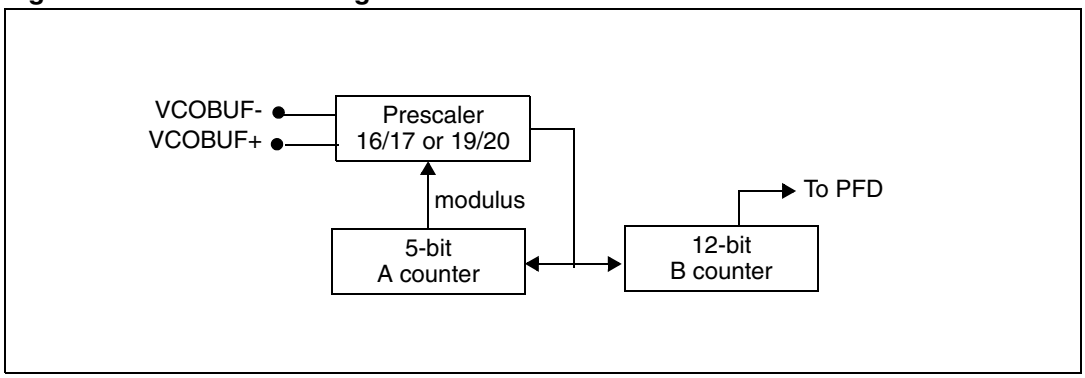
R: division ratio of the reference counter.

N: division ratio of the PLL

The following points should be noted:

- For the VCO divider to work correctly, B **must** be higher than A.
- A can take any value from 0 to 31.
- Two PLL division ratio (N) ranges are possible, depending on the value of P:
  - 256 to 65551 (when P=16)
  - 361 to 77836 (when P=19).

Figure 10. VCO divider diagram

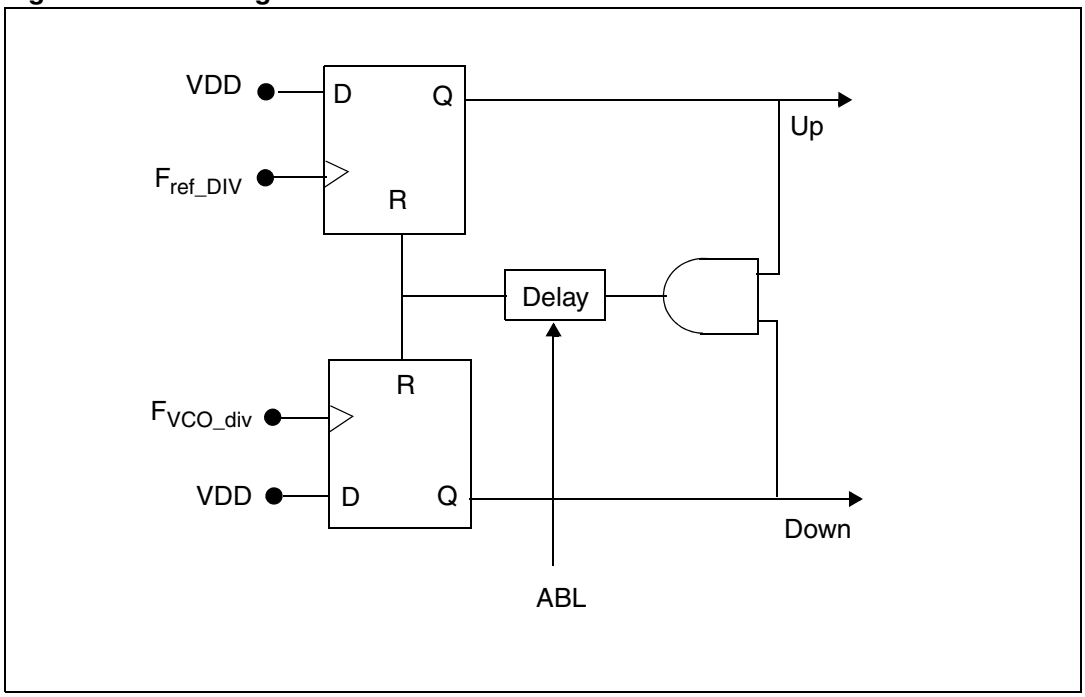


8.1.5 Phase frequency detector (PFD)

The PFD takes inputs from the reference and the VCO dividers and produces an output proportional to the phase error. The PFD includes a delay gate that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function.

Figure 11 is a simplified schematic of the PFD.

Figure 11. PFD diagram



8.1.6 Lock detect

This signal indicates that the difference between rising edges of both UP and DOWN PFD signals is found to be shorter than the fixed delay (roughly 5 ns). The Lock Detect signal is high when the PLL is locked. The Lock Detector consumes current only during PLL transients.

8.1.7 Mute until lock

This (software controlled) function shuts down the following elements until the PLL achieves the lock status:

- RF output stage
- LO output buffer
- mixer
- IF amplifier circuitry

Under this setting there is no signal at the IF output stage or the LO output during a frequency jump.

8.1.8 Charge pump

This block drives two matched current sources, Iup and Idown, which are controlled respectively by the UP and DOWN PFD outputs. The nominal value of the output current is controlled by an external resistor (to be connected to the REXT input pin) and the selection of one of 8 possible values by a 3-bit word.

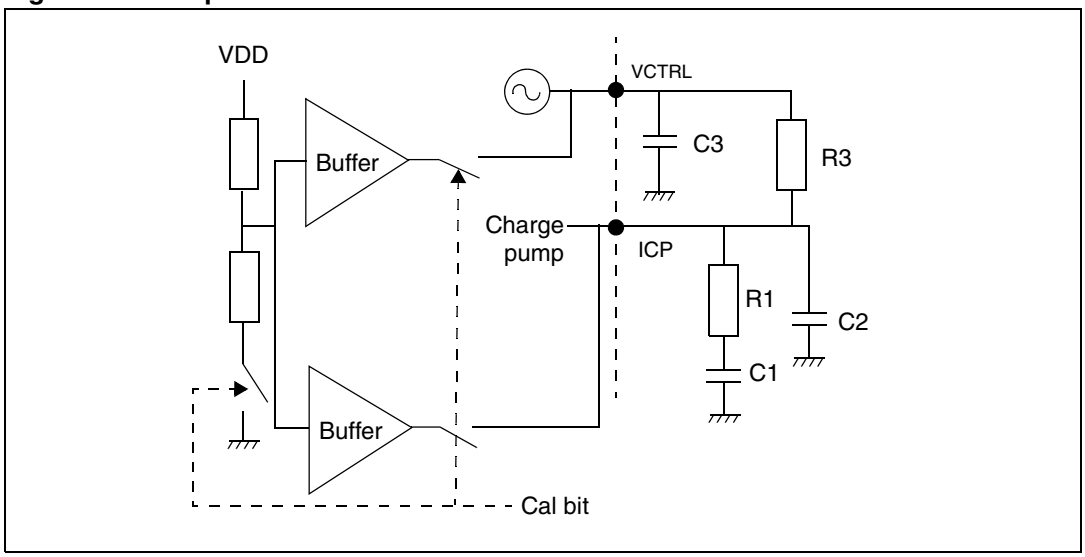
The minimum value of the output current is: IMIN = 2*VBG/REXT_CP (VBG~1.17 V)

Table 10. Current values for CPSEL[2:0] selection

CPSEL2	CPSEL1	CPSEL0	Current	Value for REXT=4.7 kΩ
0	0	0	I_{MIN}	0.5 mA
0	0	1	$2*I_{MIN}$	1.00 mA
0	1	0	$3*I_{MIN}$	1.50 mA
0	1	1	$4*I_{MIN}$	2.00 mA
1	0	0	$5*I_{MIN}$	2.50 mA
1	0	1	$6*I_{MIN}$	3.00 mA
1	1	0	$7*I_{MIN}$	3.50 mA
1	1	1	$8*I_{MIN}$	4.00 mA

Note: The current is output on pin ICP. During the VCO auto calibration, ICP and VCTRL pins are forced to VDD/2.

Figure 12. Loop filter connection



8.1.9 Voltage controlled oscillators

VCO selection

Within the STW82102B two low-noise VCOs are integrated to cover a wide band from 1500 MHz to 1800 MHz, and from 1900 MHz to 2200 MHz after the division by 2:

- VCO A frequency range is 3000 MHz to 3600 MHz
- VCO B frequency range is 3800 MHz to 4400 MHz

VCO frequency calibration

Both VCOs can operate on 32 frequency ranges that are selected by adding or subtracting capacitors to the resonator. These frequency ranges are intended to cover the wide band of operation and compensate for process variations on the VCO center frequency.

An automatic range selection is performed when the bit SERCAL rises from ‘0’ to ‘1’ . The charge pump is inhibited and the pins ICP and VCTRL are set at a fixed calibration voltage (VCAL). The frequency ranges are then tested to select the nearest one to the desired output frequency (F_{OUT}= N*F_{ref}/R) with VCAL input voltage applied. After this selection, the charge pump is once again enabled and the PLL performs a fine adjustment around VCAL on the loop filter voltage to lock F_{OUT}, thus enabling a fast settling time.

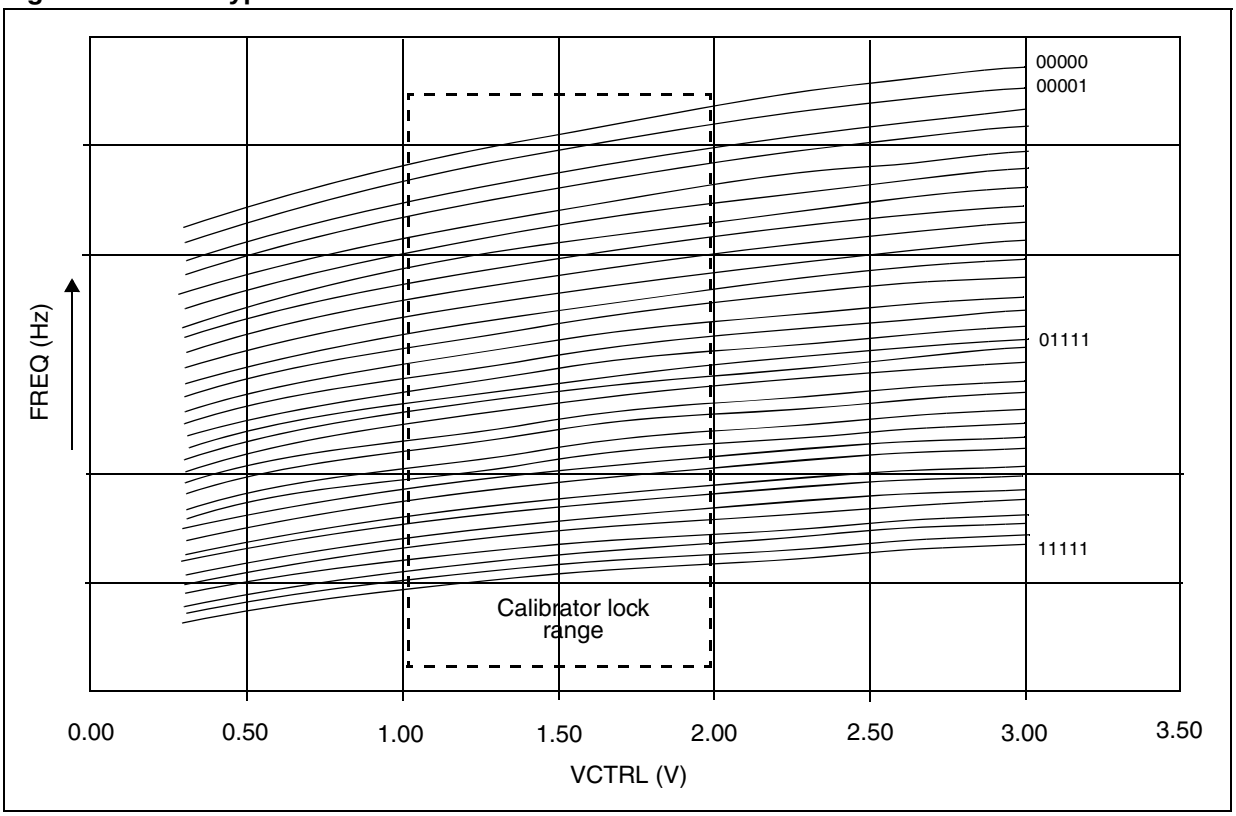
Two calibration algorithms are selectable by setting the CALTYPE bit.

Setting the CALTYPE bit to ‘1’ guarantees the PLL lock versus temperature variations. Once programmed at the initial temperature, T_0, within the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status if the temperature drift (in either direction) is within the limit specified by ΔT_{LK}, and provided that the final temperature, T_1, is still inside the nominal range.

Setting the CALTYPE bit to ‘0’ fixes VCAL to the mid point of the charge pump output (VDD/2). Optimum PLL phase noise performance versus temperature variations with a reduced ΔT_{LK} is guaranteed in this case.

The ΔT_{LK} parameter, specific to each VCO and calibration type, in the STW82102B is specified in *Table 8: Integer-N synthesizer electrical characteristics*.

Figure 13. VCO typical sub-band characteristics



The SERCAL bit should be set to '1' at each division ratio change. The calibration takes approximately 7 periods of the Comparison Frequency and the SERCAL bit is automatically reset to '0' at the end of each calibration.

The maximum allowed F_{PFD} to perform the calibration process is 1 MHz. If a higher F_{PFD} is used the following procedure should be adopted:

1. Calibrate the VCO at the desired frequency with an F_{PFD} lower than 1 MHz
2. Set the A, B and R dividers ratio for the desired F_{PFD}

For calibration details refer to *Section 9.4.1: VCO calibration procedure (I^2C interface)* or *Section 10.4.1: VCO calibration procedure (SPI interface)*.

VCO calibration auto-restart feature

The VCO Calibration Auto-Restart feature, once activated, allows the calibration procedure to be restarted when the Lock Detector reports that the PLL has moved to an unlock condition (trigger on ‘1’ to ‘0’ transition of Lock Detector signal).

This situation could happen if the device experiences a significant temperature variation and the CALTYPE bit is set for optimum PLL phase noise performance (CALTYPE [0]).

By enabling the VCO Calibration Auto-Restart feature (through the AUTO_CAL bit), the device re-selects the proper VCO frequency sub-range, without any external user command.

This feature can be enabled only when the F_{PFD} is lower than 1 MHz.

VCO voltage amplitude control

The voltage swing of the VCOs can be adjusted over 4 levels by means of two dedicated programming bits (PLL_A1 and PLL_A0). This setting trades current consumption with phase noise performances of the VCO. Higher amplitudes provide best phase noise while lower ones save power.

Table 11 and *Table 12* give the current consumption and the phase noise at 1 MHz.

Table 11. VCOA performance against amplitude setting (frequency = 3.6 GHz)

PLL_A[1:0]	Current Consumption (mA)	PN @ 1 MHz
00	23	-127
01	24	-128
10	32	-131
11	35	-132

Table 12. VCOB performance against amplitude setting (frequency = 4.3 GHz)

PLL_A[1:0]	Current Consumption (mA)	PN @ 1 MHz
00	16	-124
01	18	-126
10	27	-128
11	30	-129

8.1.10 Output stage

The differential output signal of the synthesizer after the Divider by 2 is available on pins 16 and 17.

The output stage is selected by programming the PD[4:0] bits.

The output stage is an open-collector structure which is able to meet different requirements over the desired output frequency range by proper connections on the PCB. See *Figure 27: Diversity mode operation with same LO frequencies*.

8.1.11 External VCO buffer

Although the STW82102B includes two wideband and low-noise VCOs, external VCO use capability is also provided.

The external VCO buffer can be used to manage a signal coming from an external VCO in order to build a local oscillator signal by using the STW82102B internal synthesizer as a PLL. This is only possible when External VCO standard mode or External VCO diversity master mode operation are selected. See *Figure 29: External VCO standard mode operation* and *Figure 30: External VCO diversity mode operation with same LO*.

If the STW82102B is operated in Diversity slave mode, the external VCO buffer manage the signal coming from the synthesizer output stage of another STW82102B device See *Figure 27: Diversity mode operation with same LO frequencies* and *Figure 30: External VCO diversity mode operation with same LO*.

The selection of the external VCO buffer is done by setting the PD[4:0] bits.

The external VCO signal can range from 1500 MHz to 2200 MHz and its minimum power level must be -10 dBm.

8.1.12 Mixer and IF amplifier

LO mixer driver

The LO signal is fed through a driver in order to achieve the high power level needed to drive the passive mixer for maximum performance of linearity and NF.

The LO Mixer Driver is coupled to the mixer with an integrated LO balun. The LO signal level is adjusted by means of an Automatic Level Control loop (ALC) controlled by the bits LO_A[1:0].

In low current mode the configuration LO_A[1:0]='00' (minimum LO amplitude) should be selected and the power supply on pin 40 can be set to 3.3 V.

The LO balun resonating frequency can be adjusted by means of the bits CAP[2:0] in order to match the selected LO frequency.

Table 13. Suggested CAP[2:0] values for LO Frequency range mixer

CAP[2:0]	LO frequency range
000	2100 MHz ÷ 2200 MHz
001	1970 MHz ÷ 2100 MHz
010	1870 MHz ÷ 1970 MHz
011	1770 MHz ÷ 1870 MHz
100	1700 MHz ÷ 1770 MHz
101	1620 MHz ÷ 1700 MHz
110	1550 MHz ÷ 1620 MHz
111	1500 MHz ÷ 1550 MHz

Mixer

A doubly balanced CMOS passive mixer is internally driven by the high level LO signal in order to achieve high linearity and low noise performance.

The RF integrated balun permits the removal of external components and it is internally matched to 50 ohms.

The gate bias of the CMOS devices in the mixer is programmable with 4 bits (MIX[3:0]) to optimize the input matching and the gain of the signal chain.

Higher values of gate bias (higher decimal values of MIX[3:0]) are suggested to maximize linearity and lower values to maximize the performance of Gain and NF.

IF amplifier

The integrated IF stage permits a 200-ohm load to be driven (typically a SAW filter) ensuring high linearity.

It is an open collector stage (pin 31, 32) and should be biased to 5 V with choke inductors. The typical output impedance is 200 ohms. The linearity performances are controlled by the bits IFAMP[1:0]. In low current mode the configuration IFAMP[1:0]='00' (minimum linearity) should be selected and the open collector stage can be biased to 3.3 V with choke inductors.

Table 14. Linearity performance against IFAMP[1:0] configuration (typical condition)

IFAMP[1:0]	Linearity performance
00	19.5 dB
01	21.5 dB
10	23.5 dB
11	25.5dB

8.1.13 Dual output current DAC

The STW82102B embeds a 10-bit Dual Output steering current DAC especially suited to drive an external PIN diode attenuator. This provides power level calibration capability at the RF input for the TX observation path applications.

The current sourced by the DAC is related to the R_{EXT_DAC} resistor according to the following formulae (where VR_{EXT_DAC} is approximately 1.19 V):

$$IDAC_{LSB} = \frac{1}{2} \times \frac{3 \times VR_{EXT\_DAC}}{R_{EXT\_DAC}} \times \frac{1}{64} \quad \text{LSB DAC current}$$

$$IDAC_{FS} = \frac{1}{2} \times \frac{3 \times VR_{EXT\_DAC}}{R_{EXT\_DAC}} \times \frac{1023}{64} \quad \text{Full scale current}$$

With a 10 kΩ R_{EXT_DAC} the FS current is approximately 2.8 mA.

9 I²C bus interface

The I²C bus interface is selected by hardware connection of the pin 25 (DBUS_SEL) to 0 V.

Data transmission from a microprocessor to the STW82102B takes place through the 2 wires (SDA and SCL) I²C-bus interface. The STW82102B is always a slave device.

The I²C-bus protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as receiver. The device that controls the data transfer is known as the master and the others as slaves. The master always initiates the transfer and provides the serial clock for synchronization.

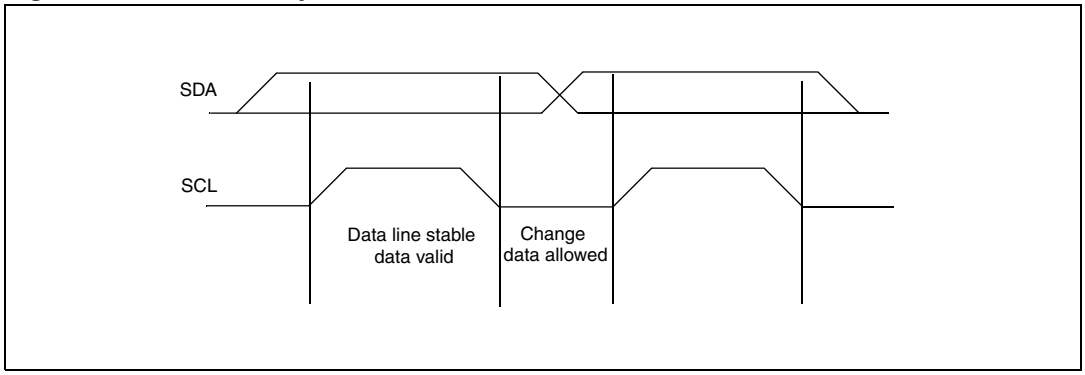
The STW82102B I²C bus supports Fast Mode operation (clock frequency up to 1 MHz).

9.1 I²C general features

9.1.1 Data validity

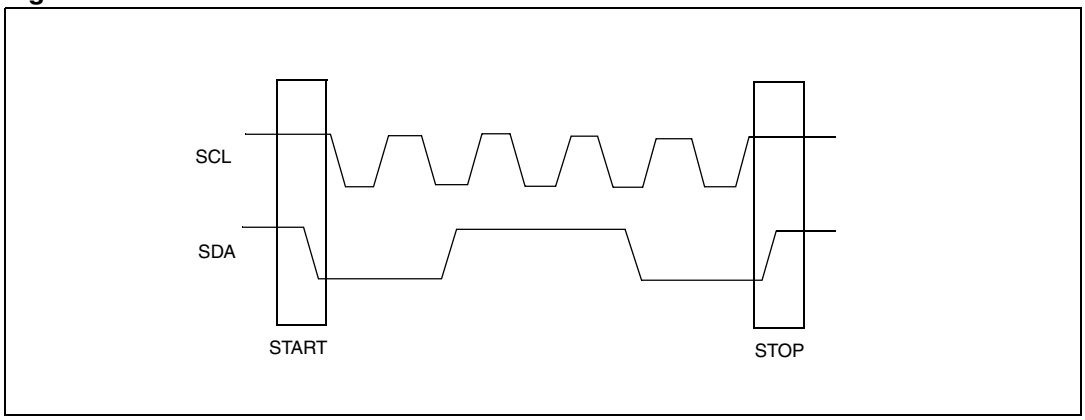
Data changes on the SDA line must only occur when the SCL is LOW. SDA transitions while the clock is HIGH identify START or STOP conditions.

Figure 14. Data validity waveform



9.1.2 START and STOP conditions

Figure 15. START and STOP condition waveform



START condition

A START condition is identified by a HIGH to LOW transition of the data bus SDA while the clock signal SCL is stable in the HIGH state. A Start condition must precede any command for data transfer.

STOP condition

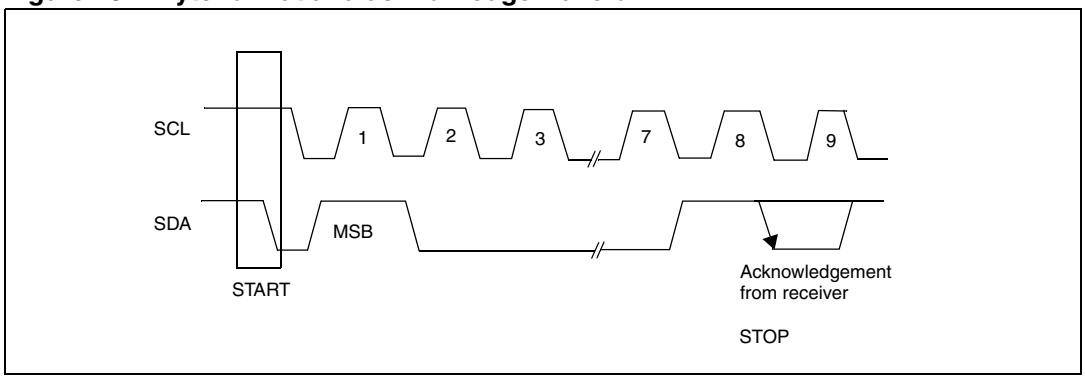
A STOP condition is identified by a transition of the data bus SDA from LOW to HIGH while the clock signal SCL is stable in the HIGH state.. A STOP condition terminates communications between the STW82102B and the Bus Master.

9.1.3 Byte format and acknowledge

Every byte (8 bits long) transferred on the SDA line must contain bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

An acknowledge bit indicates a successful data transfer. The transmitter, either master or slave, releases the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA low to acknowledge the receipt of 8 bits of data.

Figure 16. Byte format and acknowledge waveform



9.1.4 Device addressing

To start the communication between the Master and the STW82102B, the master must initiate with a START condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The first 7 MSBs are the device address identifier, corresponding to the I^2C-Bus definition. For the STW82102B the address is set as '$1101A_2A_1A_0$', 3-bits programmable. The 8th bit (LSB) is the read or write operation bit (the RW bit is set to 1 in read mode and to 0 in write mode).

After a START condition the STW82102B identifies the device address on the bus and, if matched, it acknowledge the identification on SDA bus during the 9th clock pulse.

9.1.5 Single-byte write mode

Following a START condition the master sends a device select code with the RW bit set to 0. The STW82102B gives an acknowledge and waits for the internal sub-address (1 byte). This byte provides access to any of the internal registers.

After reception of the internal byte sub-address the STW82102B again responds with an acknowledge. A single-byte write to sub-address 0x00 would affect DATA_OUT[47:40], a single-byte write with sub-address 0x04 would affect DATA_OUT[15:8] and so on.

S	$1101A_2A_1A_0$	0	ack	sub-address byte	ack	DATA IN	ack	P

9.1.6 Multi-byte write mode

The multi-byte write mode can start from any internal address. The master sends the data bytes and each one is acknowledged. The master terminates the transfer by generating a STOP condition.

The sub-address determines the starting byte. For example, a multi-byte write with sub-address 0x01 and 4 DATA_IN bytes affects 4 bytes starting at address 0x01 (registers at addresses 0x01, 0x02, 0x03 and 0x04 are modified).

S	$1101A_2A_1A_0$	0	ack	sub-address byte	ack	DATA IN	ack	..	DATA IN	ack	P

9.1.7 Current byte address read

In the current byte address read mode, following a START condition, the master sends the device address with the RW bit set to 1 (No sub-address is needed as there is only 1 byte read register). The STW82102B acknowledges this and outputs the data byte. The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

S	$1101A_2A_1A_0$	1	ack	DATA OUT	No ack	P

9.2 I²C timing specifications

9.2.1 Data and clock timing specification

Figure 17. I²C data and clock waveforms

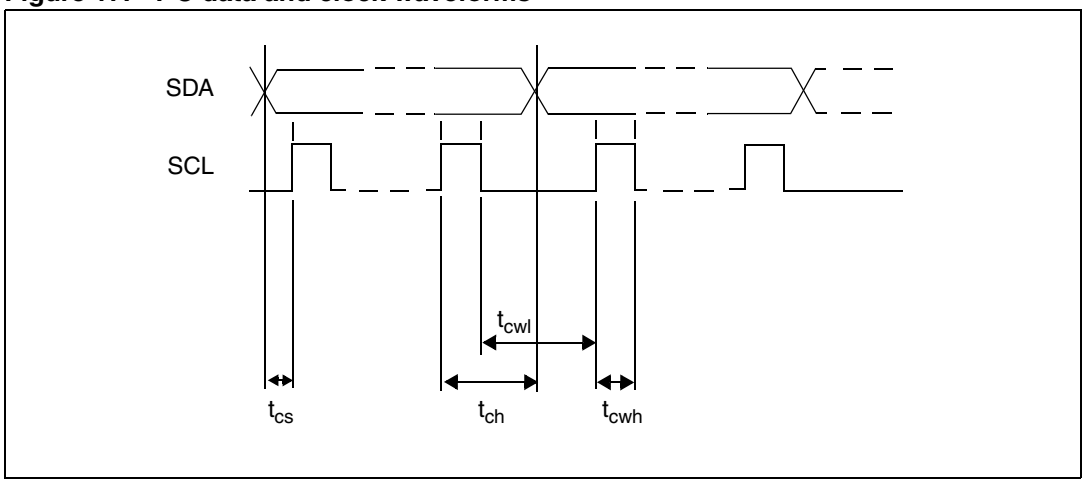


Table 15. I²C data and clock timing parameters

Symbol	Parameter	Min	Unit
T_{cs}	Data to clock set up time	2	ns
T_{ch}	Data to clock hold time	2	
T_{cwh}	Clock pulse width high	10	
T_{cwl}	Clock pulse width low	5.5	

9.2.2 I²C START and STOP timing specification

Figure 18. I²C START and STOP timing waveforms

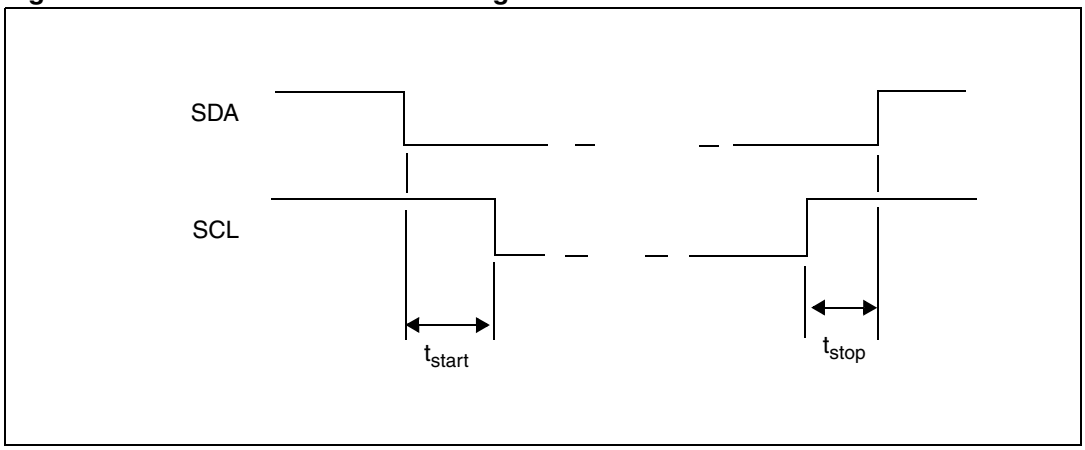


Table 16. I^2C START and STOP timing parameters

Symbol	Parameter	Min	Unit
Tstart	Clock to data start time	2	ns
Tstop	Data to clock down stop time	2	

9.2.3 I^2C acknowledge timing specification

Figure 19. I^2C acknowledge timing waveforms

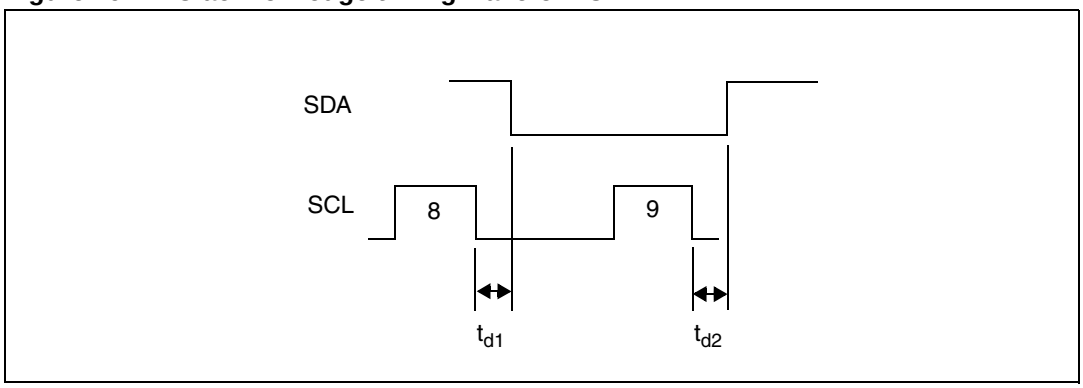


Table 17. I^2C acknowledge timing parameters

Symbol	Parameter	Max	Unit
T_{d1}	Ack begin delay	2	ns
T_{d2}	Ack end delay	2	

9.3 I²C registers

STW82102B has 9 write-only registers and 1 read-only register.

9.3.1 I²C register summary

The following table gives a short description of the write-only registers list.

Table 18. I²C register list

Offset	Register name	Description	Page
0x00	FUNCTIONAL_MODE	Functional mode register	*on page 39*
0x01	B_COUNTER	B counter register	*on page 39*
0x02	A_COUNTER	A counter register	*on page 40*
0x03	REF_DIVIDER	Reference clock divider ratio register	*on page 40*
0x04	CONTROL	PLL control register	*on page 41*
0x05	MUTE_&_CALIBRATION	Mute and calibration control register	*on page 42*
0x06	DAC_CONTROL	DAC control register	*on page 42*
0x07	MIXER_CONTROL	Mixer control register	*on page 43*
0x08	IFAMP_LO_CONTROL	IF amplifier LO control register	*on page 43*
0x09	READ_ONLY_REGISTER	Device ID and calibration status register	*on page 44*

9.3.2 I²C register definitions

FUNCTIONAL_MODE Functional mode register

7	6	5	4	3	2	1	0
ALC_PD	PKD_EN	PD[4:0]					B11
W	W	W					W

Address: 0x00

Type: W

Reset: 0x00

[7] **ALC_PD**: for test purpose only must be set to ’0’. (ALC ON)

[6] **PKD_EN**: for test purpose only must be set to ’0’. (Peak detector output on pin 36 OFF)

[5:1] **PD[4:0]**: bits used to select different functional modes for the STW82102B according to the following table

00000: (0 decimal) Power down mode

00001: (1 decimal) Standard Mode VCOA (VCOA and RX chain ON)

00010: (2 decimal) Standard Mode VCOB (VCOB and RX chain ON)

00011: (3 decimal). Diversity Slave Mode (ExtVCO/LO input buffer and RX Chain ON; internal synthesizer OFF)

00100: (4 decimal) Diversity Master Mode VCOA (VCOA, RX Chain and LO output buffer ON)

00101: (5 decimal) Diversity Master Mode VCOB (VCOB, RX Chain and LO output buffer ON)

00110: (6 decimal) External LO Standard Mode (RX Chain ON, PLL and ExtVCO/LO input buffer ON)

00111: (7 decimal) External LO Diversity Master Mode (RX Chain ON, PLL, ExtVCO/LO input buffer and LO output buffer ON)

[0] **B11**: B counter value (bits B[10:0] in the B_COUNTER and A_COUNTER registers)

B_COUNTER B counter register

7	6	5	4	3	2	1	0
B[10:3]							
W							

Address: 0x01

Type: W

Reset: 0x00

Description: Most significant bits of the B counter value

[7:0] **B[10:3]**: B counter value (bit B11 in the FUNCTIONAL_MODE register, bits B[2:0] in the A_COUNTER register)

A_COUNTER A counter register

7	6	5	4	3	2	1	0
B[2:0]			A[4:0]				
W			W				

Address: 0x02

Type: W

Reset: 0x00

Description: Least significant bits of the B-counter value. A-counter value.

[7:5] **B[2:0]**: B Counter value (bit B11 in the *FUNCTIONAL_MODE* register, bits B[10:3] in the *B_COUNTER* register).

[4:0] **A[4:0]**: A counter value

REF_DIVIDER Reference clock divider ratio register

7	6	5	4	3	2	1	0
R[9:2]							
W							

Address: 0x03

Type: W

Reset: 0x00

Description: Most significant bits of the reference clock divider ratio value.

[7:0] **R[9:2]**: Reference clock divider ratio (bits R[1:0] in the *CONTROL* register)

CONTROL PLL control register

7	6	5	4	3	2	1	0
[R1:0]		PLL_A[1:0]		CPSEL[2:0]			PSC_SEL
W		W		W			W

Address: 0x04

Type: W

Reset: 0x00

Description: Least significant bits of the reference clock divider ratio value and PLL control bits.

[7:6] **R[1:0]**: Reference clock divider ratio (bits R[9:2] in the *REF_DIVIDER* register)

[5:4] **PLL_A[1:0]**: VCO amplitude

[3:1] **CPSEL[2:0]**: Charge Pump output current

[0] **PSC_SEL**: Prescaler Modulus select (‘0’ for P=16, ‘1’ for P=19)

The LO output frequency is programmed by setting the proper value for A, B and R according to the following formula:

$$F_{LO} = D_R \cdot (B \cdot P + A) \cdot \frac{F_{ref}}{R}$$

where D_R equals 0.5 (VCOs output frequency divided by 2)
and P is the selected Prescaler Modulus

MUTE_&_CALIBRATION Mute and calibration control register

7	6	5	4	3	2	1	0
CALTYPE	SERCAL	SELEXTCAL	MUTE_EN	MUTE_TYPE	MUTE_LOOUT_EN	MUTE_MIX_EN	MUTE_IFAMP_EN
W	W	W	W	W	W	W	W

Address: 0x05

Type: W

Reset: 0x00

Description: For test purposes only

[7] **CALTYPE**: Calibration algorithm selection
0: standard calibration to optimize the phase noise versus temperature
1: enhanced calibration to maximize the ΔT_{LK} range

[6] **SERCAL**:
1: starts the VCO auto-calibration (automatically reset to ’0’ at the end of calibration)

[5] **SELEXTCAL**: test purpose only; must be set to ‘0’

[4] **MUTE_EN**:
0: mute function disabled
1: mute function enabled

[3] **MUTE_TYPE**: must be set to '1' while the mute function is enabled (mute the IF output on Unlock state)

[2] **MUTE_LOOUT_EN**:
To be set to ’1’ to mute the LO output buffer

[1] **MUTE_MIX_EN**:
To be set to ’1’ mute the Mixer circuitry

[0] **MUTE_IFAMP_EN**: To be set to '1' to mute the IF amplifier circuitry

DAC_CONTROL DAC control register

7	6	5	4	3	2	1	0
DAC[9:2]							
W							

Address: 0x06

Type: W

Reset: 0x00

Description: Most significant bits of the DAC control word

[7:0] **DAC[9:2]**: DAC input word for DAC current control (bits DAC[1:0] in the *MIXER_CONTROL* register).

MIXER_CONTROL Mixer control register

7	6	5	4	3	2	1	0
DAC[1:0]		MIX[3:0]				PD_DAC	CAL_AUTOSTART_EN
W		W				W	W

Address: 0x07

Type: W

Reset: 0x00

Description: Least significant bits of DAC control word and mixer control bit fields

[7:6] **DAC[1:0]**: DAC input word for DAC current control (bits DAC[9:2] in the *DAC_CONTROL* register)

[5:2] **MIX[3:0]**: Mixer bias control value

[1] **PD_DAC**: DAC power down

[0] **CAL_AUTOSTART_EN**: VCO calibration auto-restart enable ('1' active), permits to automatically restart the VCO calibration procedure in case of PLL unlock

IFAMP_ LO_CONTROL IF amplifier LO control register

7	6	5	4	3	2	1	0
IFAMP[1:0]		CAP[2:0]			LO_A[1:0]		LPMUX_EN
W		W			W		W

Address: 0x08

Type: W

Reset: 0x00

[7:6] **IFAMP[1:0]**: power consumption/linearity control

[5:3] **CAP[2:0]**: Tuning capacitors control

[2:1] **LO_A[1:0]**: LO amplitude control

[0] **LPMUX_EN**: for test purpose only (low power mode for MUX); must be set to '0'

READ-ONLY REGISTER Device ID and calibration status register

7	6	5	4	3	2	1	0
ID[1:0]		LOCK_DET	INTCAL[4:0]				
R		R	R				

Address: 0x09

Type: R

Reset: 0x00

Description: This register is automatically addressed in the ‘current byte address read mode’

[7:6] **ID[1:0]**: device identification ’10’ for STW82102B

[5] **LOCK_DET**: ’1’ when PLL is locked

[4:0] **INTCAL[4:0]**: internal value of the VCO calibration control word

9.4 Device calibration through the I²C interface

9.4.1 VCO calibration procedure (I²C interface)

The calibration of the VCO center frequency is activated by setting the SERCAL bit of the MUTE & CALIBRATION register to '1'.

To program the device ensuring a correct VCO calibration, the following procedure is required before every channel change:

1. Program all the Registers using a multi-byte write sequence with the desired setting:
   - Functional Mode
   - B and A counters
   - R counter
   - VCO amplitude
   - Charge Pump
   - Prescaler Modulus
   - DAC
   - Mixer and LO Control
   - all bits of the MUTE & CALIBRATION Register (0x05) set to '0'.
2. Program the MUTE & CALIBRATION register using a single-byte write sequence (sub-address 0x05) with the SERCAL bit set to '1'.

The maximum allowed PFD frequency (F_{PFD}) to perform the calibration process is 1 MHz. If the desired F_{PFD} is higher than 1 MHz the following steps are needed:

3. Perform all the step of the above calibration procedure programming the desired VCO frequency with a proper setting of R, B and A counter so that F_{PFD} results lower than 1 MHz.
4. Once calibration is completed, program all the Registers by using a multi-byte write sequence (Functional Mode, B and A counters, R counter, VCO amplitude, Charge Pump, Prescaler Modulus, DAC, Mixer and LO Control) with the proper settings for the desired VCO and PFD frequencies.

9.4.2 Power ON sequence (I²C interface)

At power-on the device is configured in power-down mode.

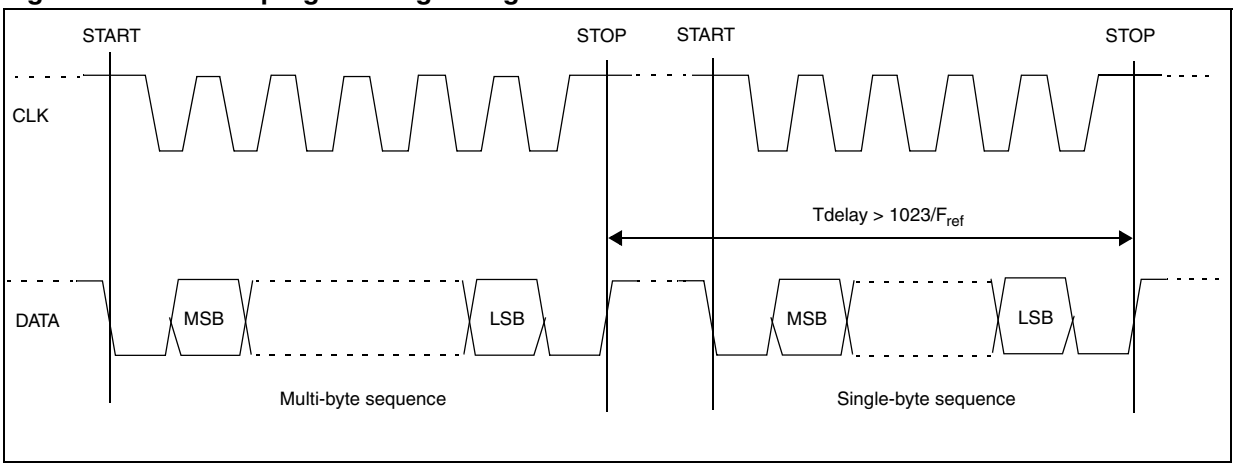
In order to guarantee correct setting of the internal circuitry after the power on, the following steps must be followed:

1. Power up the device
2. Provide the Reference clock
3. Implement the first programming sequence with a proper delay time between the STOP condition of the multi-byte write sequence and that of the single-byte write sequence (see *Figure 20*). The T_{delay} value must respect the following condition:

$$T_{delay} > 1023 \times \frac{1}{F_{ref}}$$

F_{ref} is the reference clock frequency.

Figure 20. I2C first programming timing



9.4.3 VCO calibration auto-restart procedure (I²C interface)

The VCO calibration auto-restart feature is enabled in two steps:

1. Set the desired frequency ensuring VCO calibration procedure as described above (*Section 9.4.1*).
2. Program the MIXER_CONTROL register (sub-address 0x07) using a single-byte write sequence with the CAL_AUTOSTART_EN bit set to '1' while keeping the others unchanged.

10 SPI digital interface

10.1 SPI general features

The SPI digital interface is selected by hardware connection of the pin 25 (DBUS_SEL) to 3.3 V.

The STW82102B IC is programmed by means of a high-speed serial-to-parallel interface with write option only. The 3-wires bus can be clocked at a frequency as high as 100 MHz to allow fast programming of the registers containing the data for RF IC configuration.

The programming of the chip is done through serial words with whole length of 26 bits. The first 2 MSB represent the address of the registers. The others 24 LSB represent the value of the registers.

Each data bit is stored in the internal shift register on the **rising edge** of the CLOCK signal.

On the **rising edge** of the LOAD signal the outputs of the selected register are sent to the device.

Figure 21. SPI input and output bit order

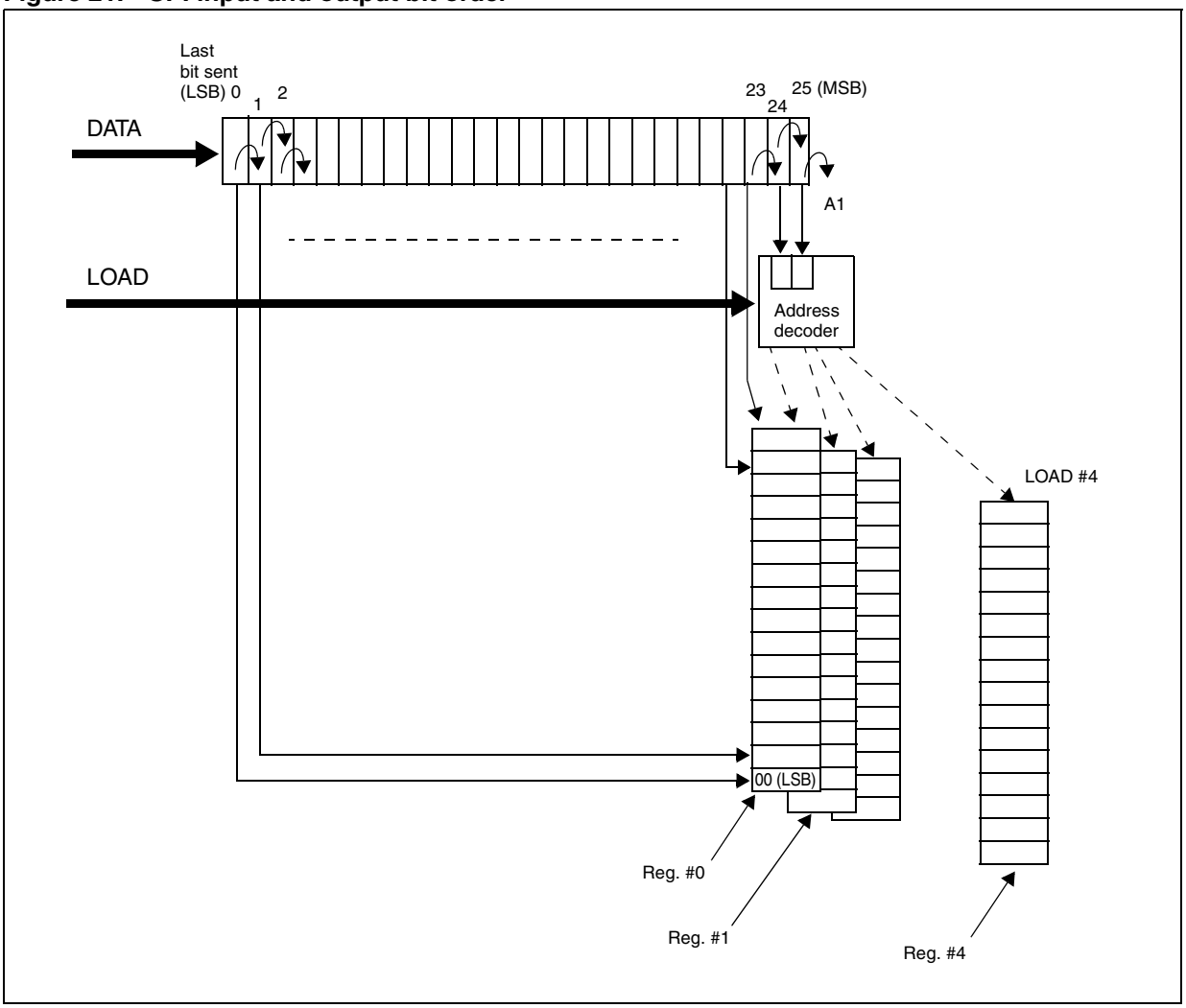


Figure 22. SPI data structure

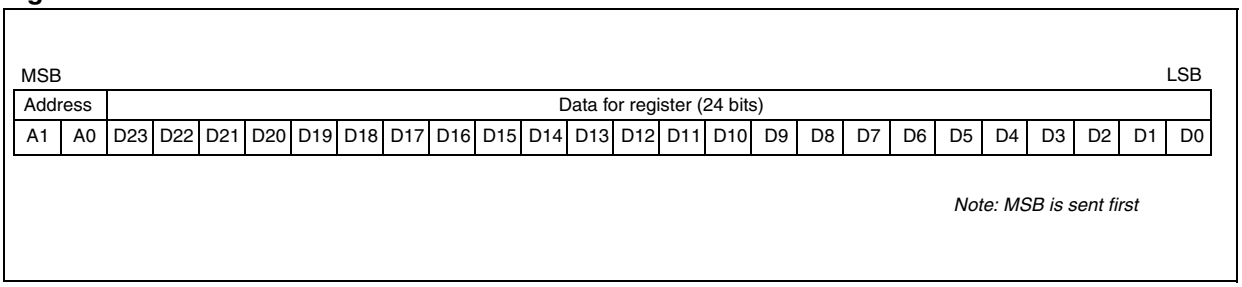


Table 19. Address decoder and outputs

Address		Outputs			
A1	**A0**	**DATABITS D23-D0**	**N°**	**Name**	**Function**
0	0	24	0	ST1	DAC, Mixer, Tuning capacitors, LO_amplitude
0	1	24	1	ST2	Reference divider, VCO amplitude, VCO Calibration, Charge Pump current, Prescaler Modulus, Mute functions
1	0	24	2	ST3	Functional modes, VCO dividers
1	1	24	3	ST4	Reserved

10.2 SPI timing specification

10.2.1 Data, clock and load timing

Figure 23. SPI timing waveforms

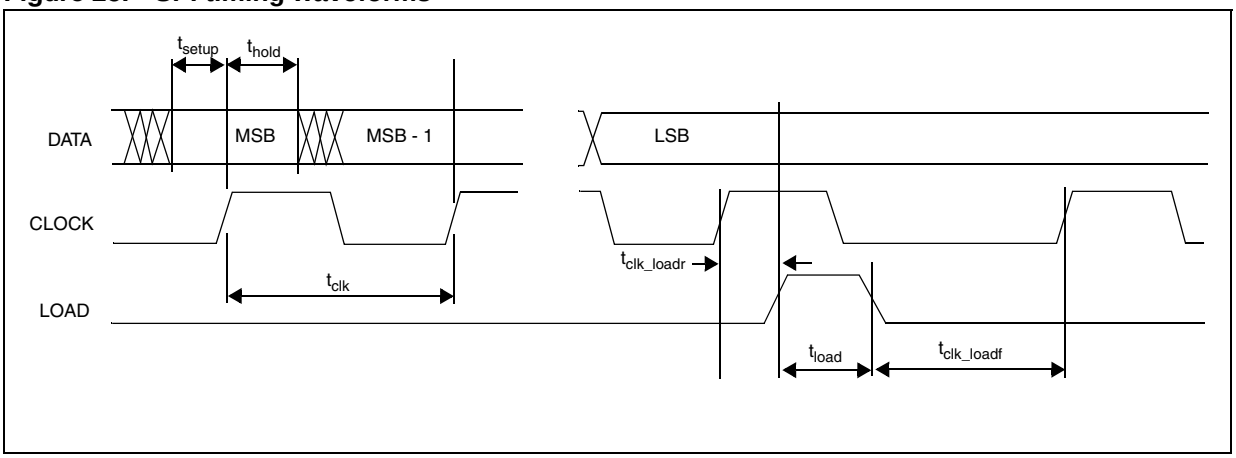


Table 20. SPI timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
t_{setup}	DATA to CLOCK setup time	1	-	-	ns
t_{hold}	DATA to clock hold time	0.5	-	-	ns
t_{clk}	CLOCK cycle period	10	-	-	ns
t_{load}	LOAD pulse width	3	-	-	ns
t_{clk_loadr}	CLOCK to LOAD rising edge	0.6	-	-	ns
t_{clk_loadf}	CLOCK to LOAD falling edge	2.5	-	-	ns

10.3 SPI registers

10.3.1 SPI register summary

Table 21. SPI register list

Offset	Register name	Description	Page
0x00	ST1	SPI register 1	*on page 50*
0x01	ST2	SPI register 2	*on page 51*
0x10	ST3	SPI register 3	*on page 52*

10.3.2 SPI register definitions

ST1 SPI register 1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC[9:0]										MIX[3:0]				PWD_DAC	CAL_AUTOSTART_EN	IF[1:0]		CAP[2:0]			LO_A[1:0]		LPMUX_EN
W										W				W	W	W		W			W		W

Address: 0x00

Type: W

Reset: 0x00

[23:14] **DAC[9:0]**: DAC input word

[13:10] **MIX[3:0]**: Mixer bias control

[9] **PWD_DAC**: DAC power down

[8] **CAL_AUTOSTART_EN**: VCO calibration auto-restart enable

[7:6] **IF[1:0]**: Power consumption/linearity control

[5:3] **CAP[2:0]**: Tuning capacitors control

[2:1] **LO_A[1:0]**: LO amplitude control

[0] **LPMUX_EN**: For test purpose only. Must be set to ‘0’

ST2 SPI register 2

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R[9:0]										PLL_A[1:0]		CPSEL[2:0]			PSC_SEL	CAL_TYPE	SERCAL	SELEXTCAL	MUTE_EN	MUTE_TYPE	MUTE_LOOUT_EN	MUTE_MIX_EN	MUTE_IFAMP_EN
W										W		W			W	W	W	W	W	W	W	W	W

Address: 0x01

Type: W

Reset: 0x00

[23:14] **R[9:0]**: Reference clock divider ratio

[13:12] **PLL_A[1:0]**: VCO amplitude control

[11:9] **CPSEL[2:0]**: Charge pump output current control

[8] **PSC_SEL**: Prescaler modulus select (‘0’ for P=16, ‘1’ for P=19)

[7] **CAL_TYPE**: Calibration algorithm selection
0: standard calibration to optimize the phase noise versus temperature
1: enhanced calibration to maximize the ΔT_{LK} range

[6] **SERCAL**:
at ‘1’ starts the VCO auto-calibration (automatically reset to ‘0’ at the end of calibration)

[5] **SELEXTCAL**: test purpose only. Must be set to ‘0’

[4] **MUTE_EN**:
0: mute function disabled
1: mute function enabled

[3] **MUTE_TYPE**: must be set to '1' while the mute function is enabled (mute IF output on Unlock state)

[2] **MUTE_LOOUT_EN**:
To be set to ’1’ to mute the LO output buffer

[1] **MUTE_MIX_EN**:
To be set to ’1’ to mute the Mixer circuitry

[0] **MUTE_IFAMP_EN**:
To be set to ’1’ to mute the IF amplifier circuitry

ST3 SPI register 3

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALC_PD	PKD_EN	PD[4:0]					B[11:0]												A[4:0]				
W	W	W					W												W				

Address: 0x10

Type: W

Reset: 0x00

[23] **ALC_PD**: Test purpose only; must be set to ‘0’ (ALC ON)

[22] **PKD_EN**: for test purpose only; must be set to ‘0’

[21:17] **PD[4:0]**:bits used to select different functional modes for the STW82102B according to the following table

00000: (0 decimal) Power down mode

00001: (1 decimal) Standard Mode VCOA (VCOA and RX chain ON)

00010: (2 decimal) Standard Mode VCOB (VCOB and RX chain ON)

00011: (3 decimal). Diversity Slave Mode (ExtVCO/LO input buffer and RX Chain ON; internal synthesizer OFF)

00100: (4 decimal) Diversity Master Mode VCOA (VCOA, RX Chain and LO output buffer ON)

00101: (5 decimal) Diversity Master Mode VCOB (VCOB, RX Chain and LO output buffer ON)

00110: (6 decimal) External LO Standard Mode (RX Chain ON, PLL and ExtVCO/LO input buffer ON)

00111: (7 decimal) External LO Diversity Master Mode (RX Chain ON, PLL, ExtVCO/LO input buffer and LO output buffer ON)

[16:5] **B[11:0]**: B counter bits

[4:0] **A[4:0]**: A Counter Bits

10.4 Device calibration through the SPI interface

10.4.1 VCO calibration procedure (SPI interface)

The calibration of the VCO center frequency is activated by setting to ’1’ the SERCAL bit (ST2 Register bit [6]).

In order to program properly the device while ensuring the VCO calibration, the following procedure is required before every channel change:

1. Program the ST1 Register with the desired setting (DAC, Mixer, LO Control)
2. Program the ST3 Register with the desired setting (Functional mode, B and A counters)
3. Program the ST2 Register with the desired setting (R counter, VCO amplitude, Charge Pump, Prescaler Modulus) and SERCAL bit set to ’1’

The maximum allowed PFD frequency (F_{PFD}) to perform the calibration process is 1 MHz; if the desired F_{PFD} is higher than 1 MHz the following steps are needed:

4. Perform all the steps of the above calibration procedure programming the desired VCO frequency with a proper setting of R, B and A counter so that F_{PFD} results lower than 1 MHz.
5. Once calibration is completed program the device with the proper setting for the desired VCO and PFD frequencies according to the following steps:
   a) Program the ST3 Register with the desired setting (Functional mode, B and A counters)
   b) Program the ST2 Register with the desired setting (R counter, VCO amplitude, Charge Pump, Prescaler Modulus) with the SERCAL bit set to ’0’.

10.4.2 Power ON sequence (SPI interface)

At power-on the device is configured in power-down mode.

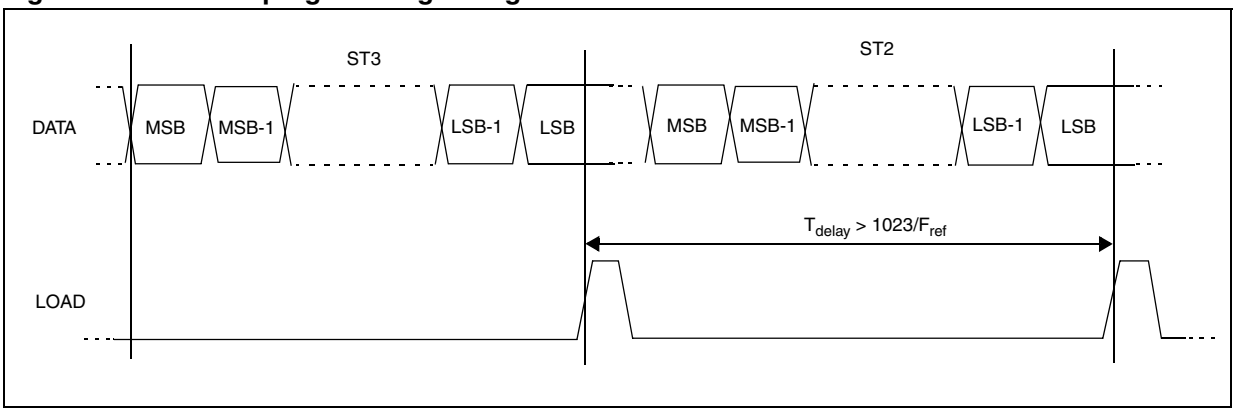
In order to guarantee correct setting of the internal circuitry after the power on, the following steps must be followed:

1. Power up the device
2. Provide the reference clock
3. Implement the first programming sequence with a proper delay time between the ST3 and ST2 load rising edges (see *Figure 24*). The T_{delay} value must respect the following condition:

$$T_{delay} > 1023 \times \frac{1}{F_{ref}}$$

F_{ref} is the reference clock frequency.

Figure 24. SPI first programming timing



10.4.3 VCO calibration auto-restart procedure (SPI interface)

The VCO calibration auto-restart feature is enabled in two steps:

1. Set the desired frequency ensuring VCO calibration as described in *Section 10.4.1*.
2. Program the ST1 register with the CAL_AUTOSTART_EN bit set to '1' while keeping unchanged the others.

11 Application information

11.1 Application circuit

Figure 25. Typical STW82102B application circuit

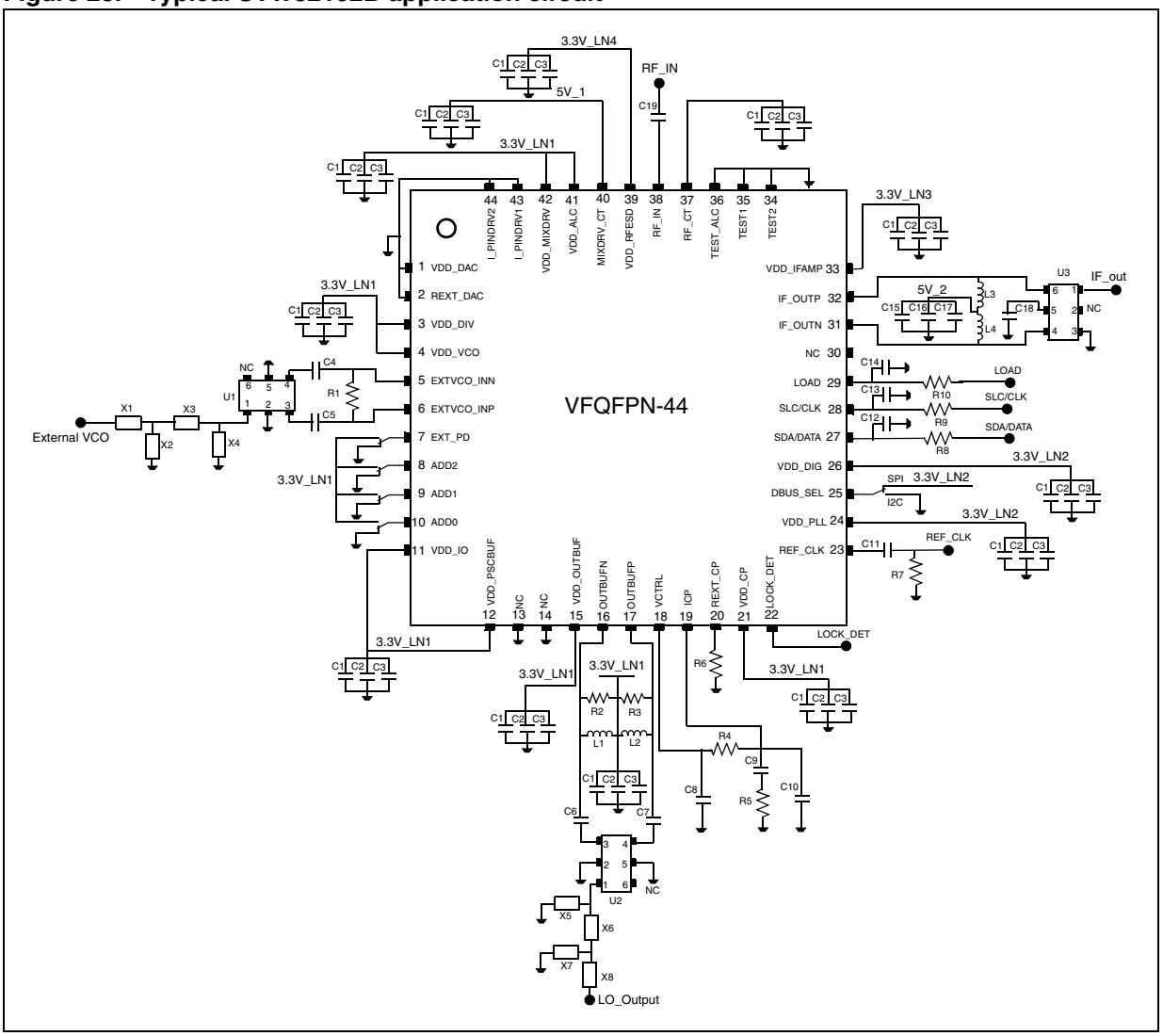


Table 22. Application circuit component values

DESIGNATION	QTY	DESCRIPTION	SUPPLIER
C1, C15	2	4.7 µF capacitors COG (0402)	Murata Manufacturing Co., Ltd
C2, C11	2	1 nF capacitors COG (0402)	
C3	1	10 pF capacitor COG (0402)	
C4, C5	2	3.6 pF capacitors COG (0402)	
C6, C7	2	6.8 pF capacitors COG (0402)	
C8	1	270 pF capacitor COG (0402)	
C9	1	2.7 nF capacitor COG (0402)	
C10	1	68 pF capacitor COG (0402)	
C12, C13, C14	3	15 pF capacitors COG (0402)	
C16	1	100 nF capacitor COG (0402)	
C17	1	100 pF capacitor COG (0402)	
C18	1	180 pF capacitor COG (0402)	
C19	1	39 pF capacitor COG (0402)	
R1, R8, R9, R10	4	100 ohm resistors (0402)	-
R2, R3, R7	3	51 ohm resistors (0402)	-
R4	1	2.2 kohm resistor (0402)	-
R5	1	8.2 kohm resistor (0402)	-
R6	1	4.7 kohm resistor (0402)	-
U1	1	Balun JTI - 2450BL15B100	JOHANSON TECHNOLOGY
U2	1	Balun JTI - 1600BL15B100	
U3	1	Balun ADT4-5WT	Mini Circuits
X1, X8	2	3.3 nH inductors CS (0402)	Coilcraft, Inc
X2	1	1.2 pF capacitor COG (0402)	Murata Manufacturing Co., Ltd
X3	1	0 ohm resistor (0402)	-
X4	0	NC	-
X5	1	1.6 pF capacitor COG (0402)	Murata Manufacturing Co., Ltd
X6	1	3.9 nH inductor CS (0402)	Coilcraft, Inc
X7	1	2 pF capacitor COG (0402)	Murata Manufacturing Co., Ltd
L1, L2	2	3.7 nH inductors HQ (0402)	Coilcraft, Inc
L3, L4	2	220 nH inductors CS (1206)	-

Note: 1 For optimum performance a low-noise 3.3 V power supply must be used.

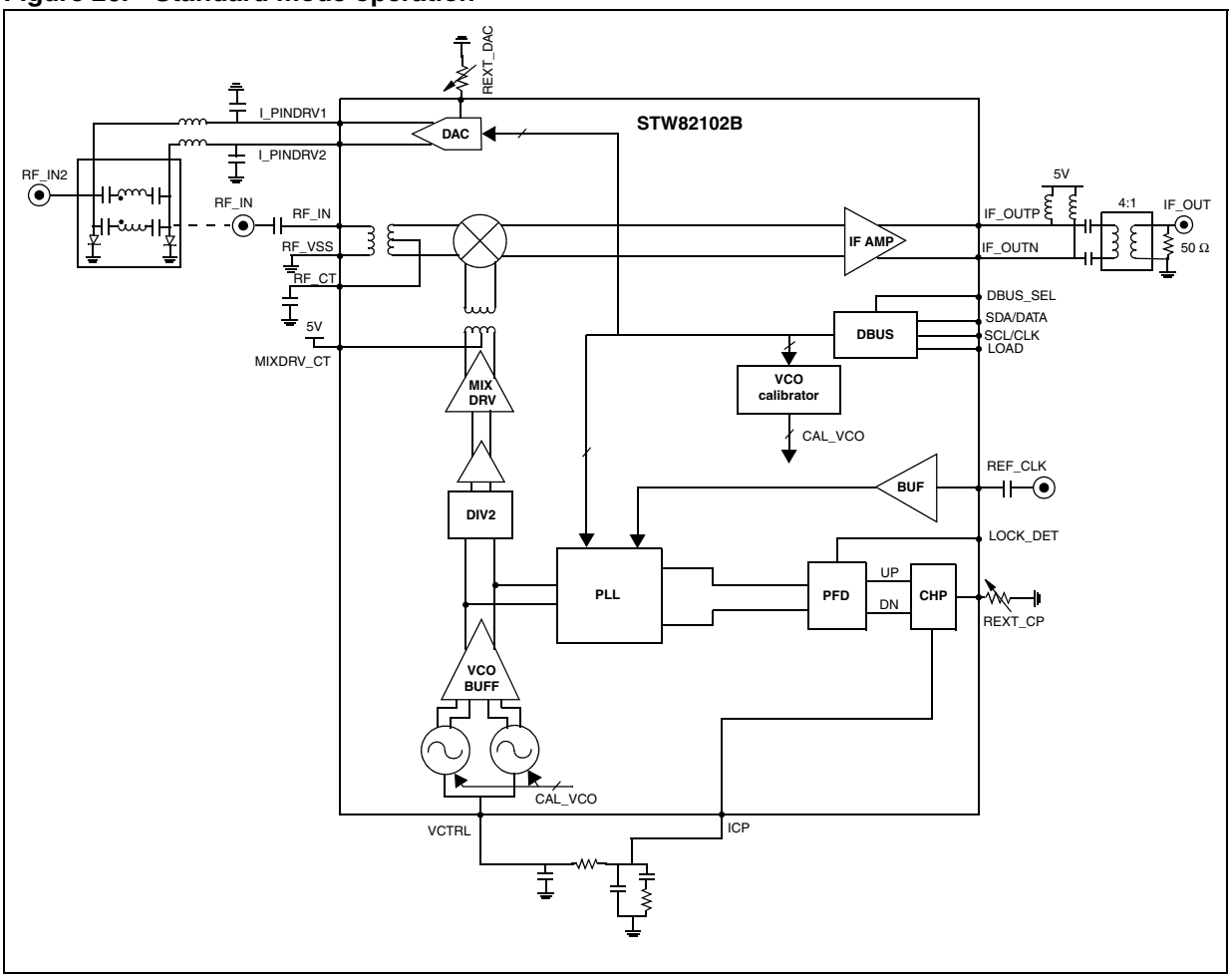
2 The 3.3 V and 5 V power supplies are split in order to maximize the isolation between RF, LO, IF and digital sections.

11.2 Standard Mode Operation

The STW82102B can be used in Standard Mode for both RX path and TX observation path (RX Chain ON and Synthesizer ON).

In such a case the 10-bit internal DAC can drive an external PIN diode attenuator in order to calibrate the signal level at the input of the device.

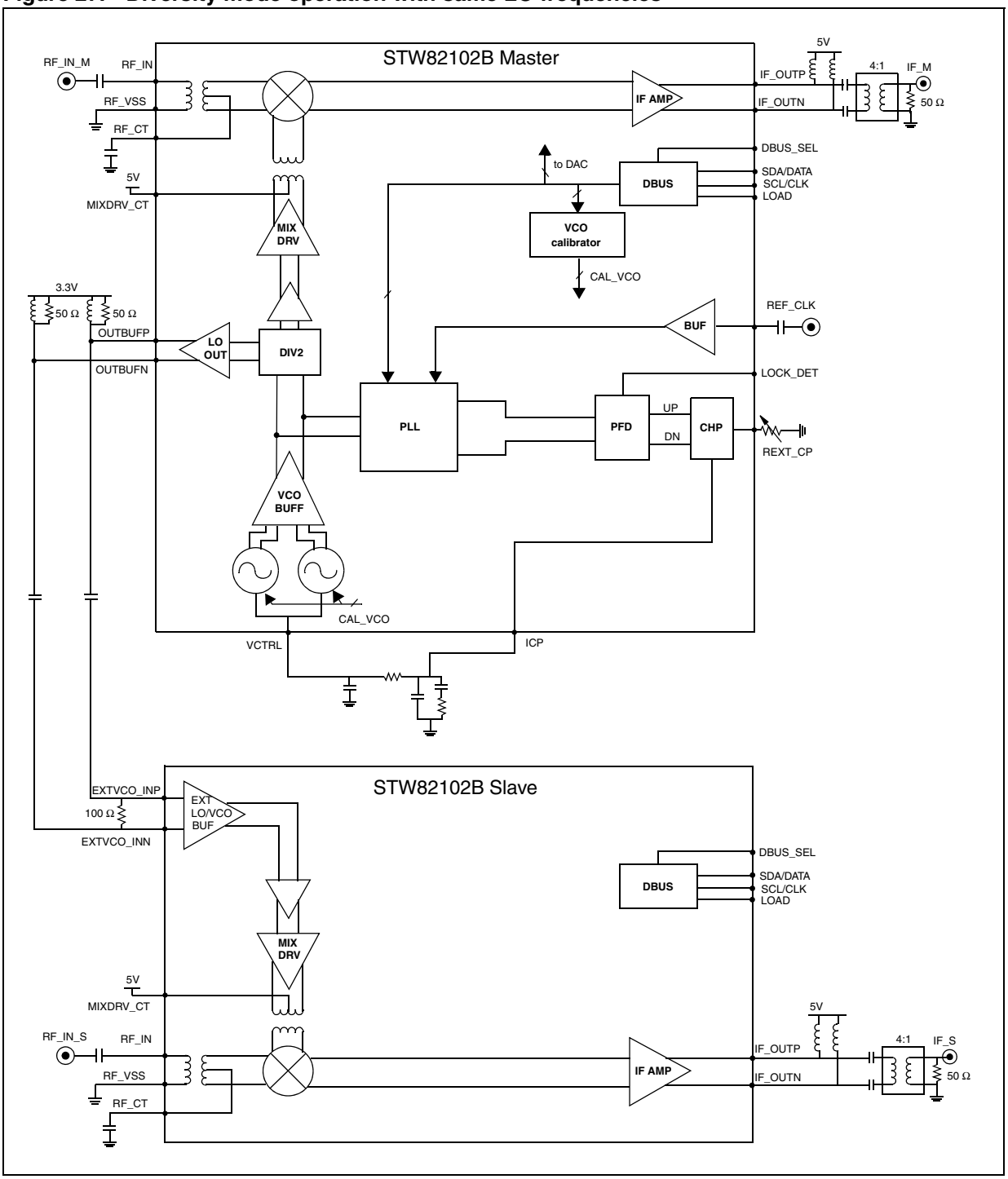
Figure 26. Standard mode operation



11.3 Diversity mode operation with same LO frequency

The STW82102B supports the Diversity mode with the same LO frequency by using one STW82102B in Master Mode (RX Chain ON, Synthesizer ON and LO output buffer ON) and the other in Slave Mode (RX Chain ON, Synthesizer OFF and EXT VCO/LO buffer ON). This operation mode is suitable for antenna diversity.

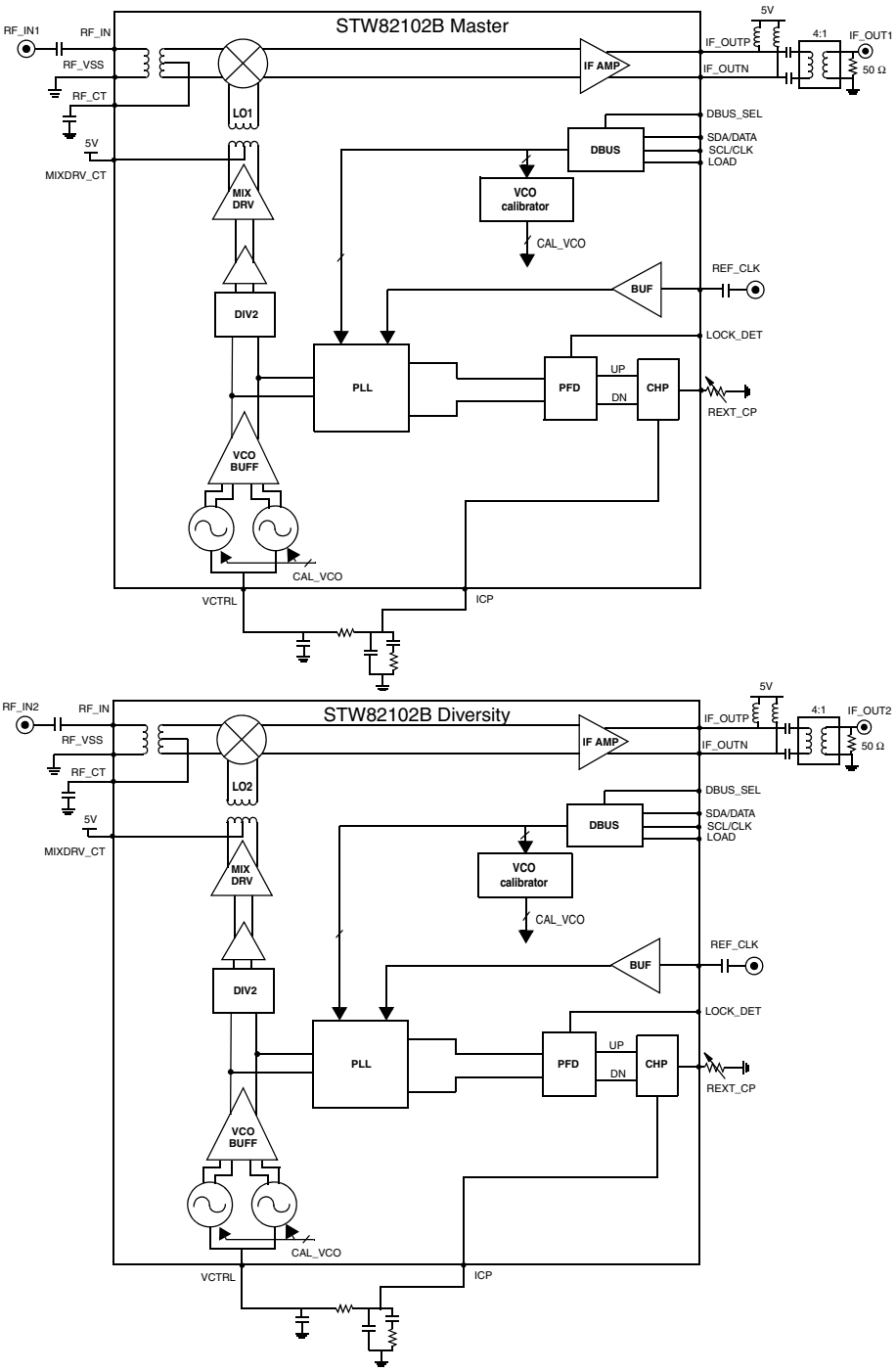
Figure 27. Diversity mode operation with same LO frequencies



11.4 Diversity mode operation with different LO frequencies

The STW82102B is particularly suitable for Diversity schemes using different LO frequencies such as the Interferer Diversity. In these schemes two STW82102Bs are used, each one set in Standard Mode and with different LO frequencies.

Figure 28. Diversity mode operation with different LO frequencies

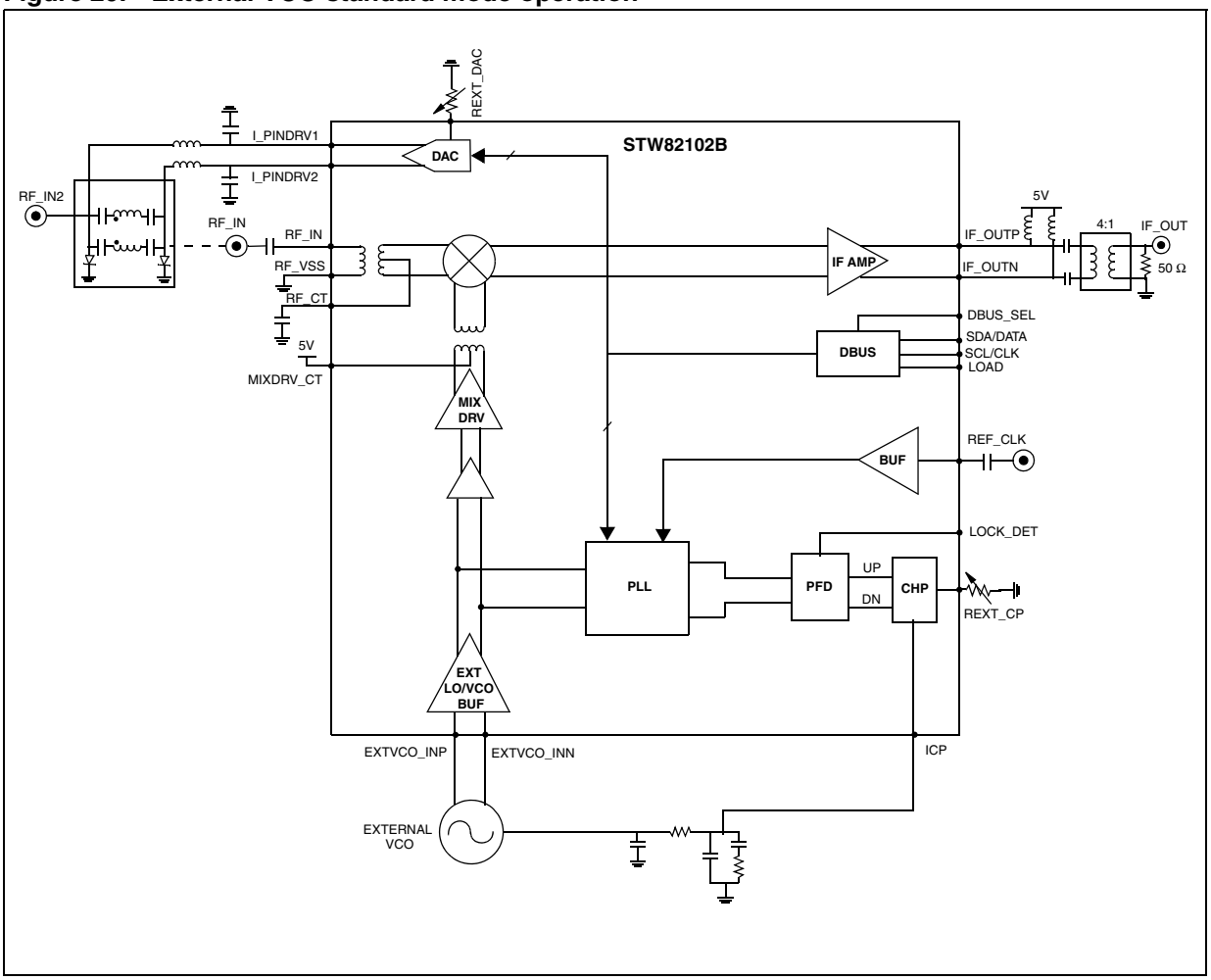


11.5 External VCO standard mode operation

The STW82102B can be used in Ext VCO Mode for both RX path and TX observation path (RX Chain ON, Synthesizer ON, EXT VCO/LO buffer ON and with an external VCO).

In such a case the 10-bit internal DAC can drive an external PIN diode attenuator in order to calibrate the signal level at the input of the device.

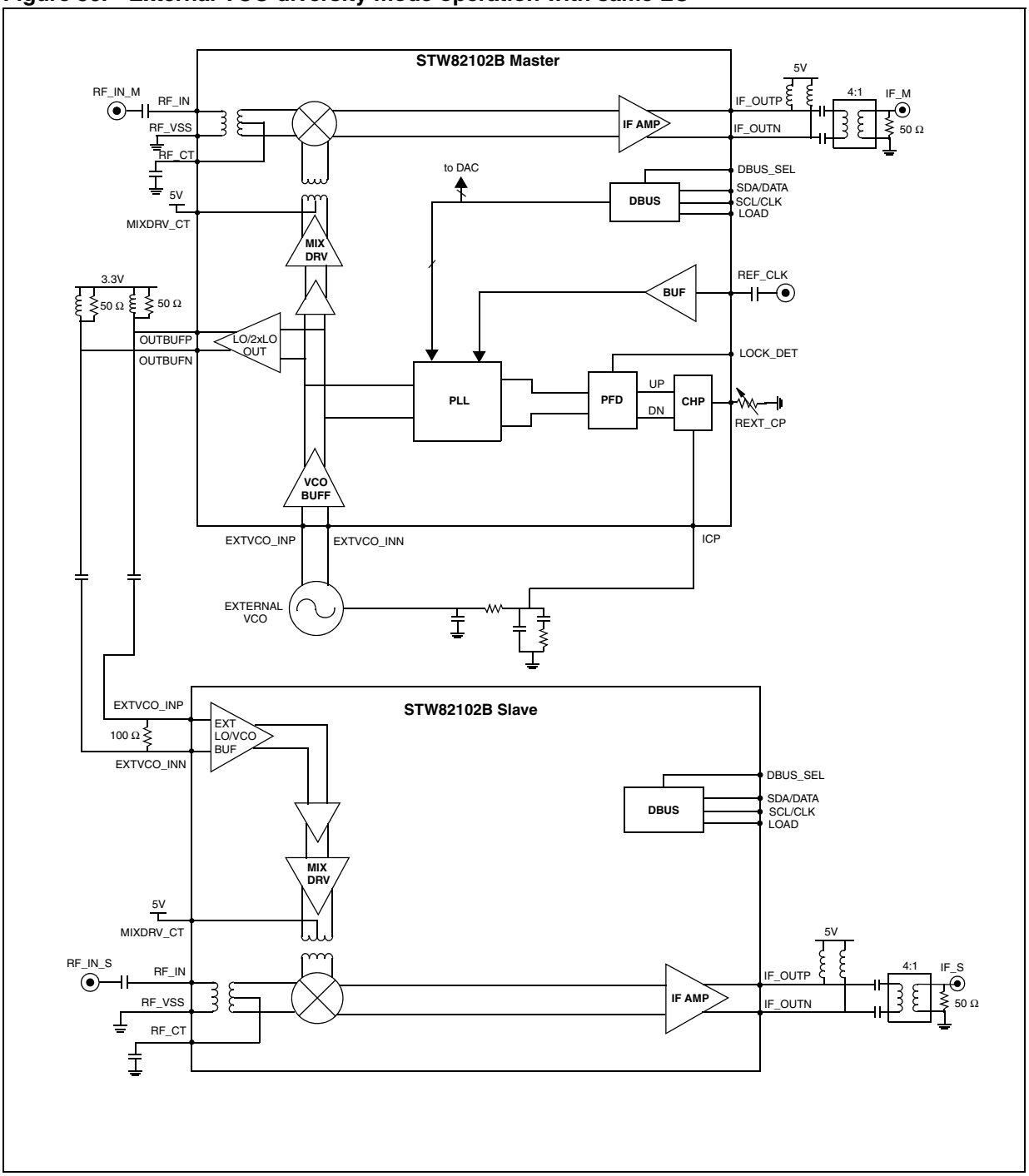
Figure 29. External VCO standard mode operation



11.6 External VCO diversity mode operation with same LO

The STW82102B can be used in Diversity mode using one STW82102B in Master Mode (RX Chain ON, Synthesizer ON, EXT VCO/LO buffer ON, LO output buffer ON and with an external VCO) and the other one in Slave Mode (RX Chain ON, Synthesizer OFF and EXT VCO/LO buffer ON).

Figure 30. External VCO diversity mode operation with same LO



12 Evaluation kit

An evaluation kit can be delivered upon request, including the following:

- Evaluation board
- GUI (graphical user interface) to program the device
- PLLSim software for PLL loop filter design and noise simulation

When ordering, please specify the following order code:

Table 23. Evaluation kit order code

Part number	Description
STW82102B-EVB	STW82102B evaluation kit, 1.4 to 1.9 GHz RF frequency range

13 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 31. VFQFPN-44 package outline

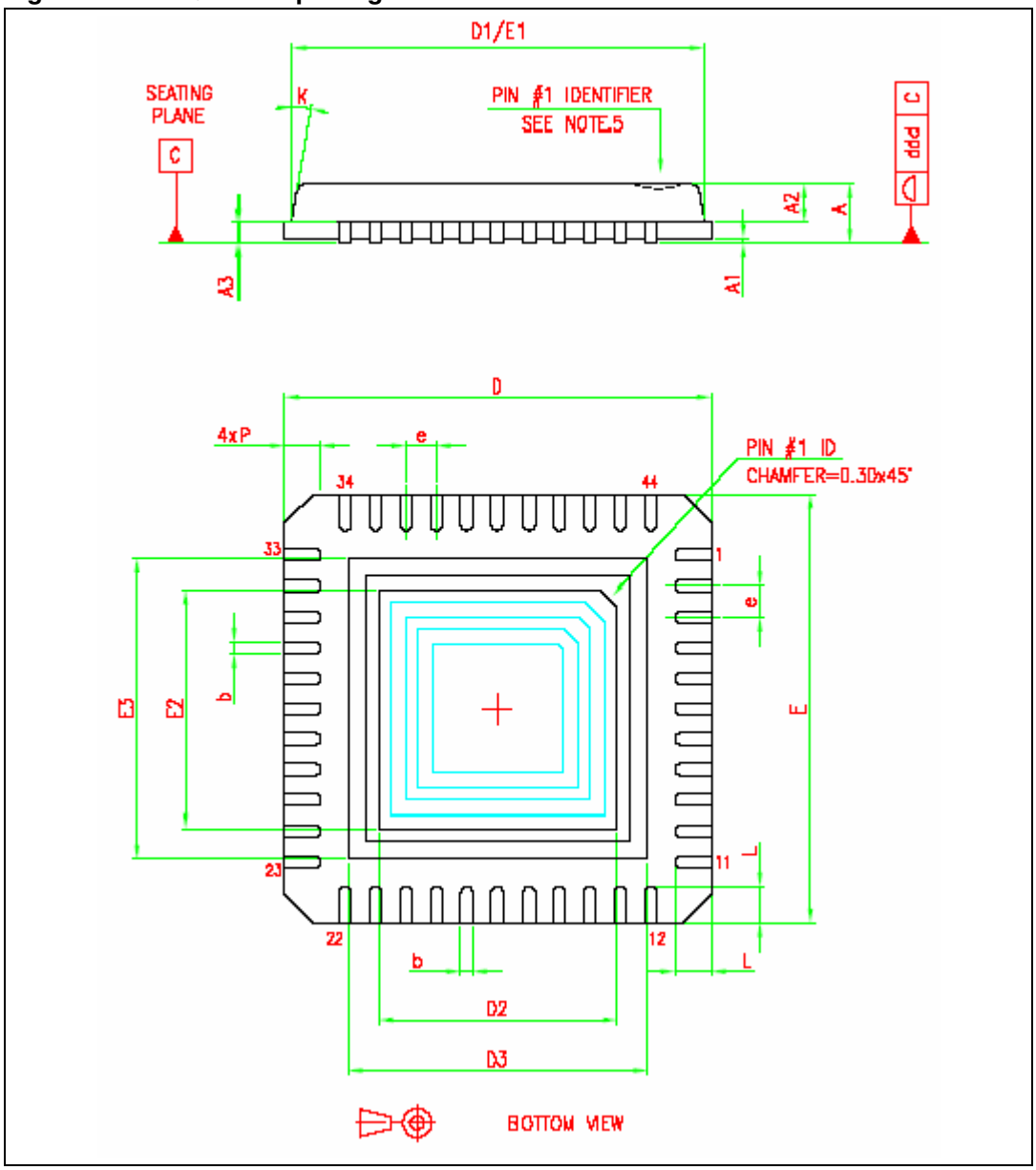


Table 24. VFQFPN-44 package dimensions

Symbol	Dimensions in mm		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	-	0.02	0.05
A2	-	0.65	1.00
A3	-	0.200	-
b	0.18	0.25	0.30
D	6.85	7.00	7.15
D1	-	6.750	-
D2	3.80	3.90	4.00
D3	-	4.90	-
E	6.85	7.00	7.15
E1	-	6.750	-
E2	3.80	3.90	4.00
E3	-	4.90	-
e	-	0.50	-
L	0.35	0.55	0.75
P	-	-	0.60
K (degree)	-	-	12
ddd	-	-	0.08

Note: 1 VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead. Very thin: A=1.00 Max.

2 Details of terminal 1 identifier are optional but must be located on the top surface of the package by using either a mold or marked features.

14 Revision history

Table 25. Document revision history

Date	Revision	Changes
07-Mar-2011	1	First release
29-Mar-2012	2	Cover page: – 2FRF-2FLO spurious rejection changed to 85 dBc – Noise figure NF changed to 10.5 dB – Removed 'Preliminary Data' tags. Added *List of tables* and *List of figures*. Table 3 moved to new *Section 3: Absolute maximum ratings* Section 2.1 becomes *Section 3: Absolute maximum ratings* Section 2.2 becomes *Section 5: Test conditions* Section 2.3 becomes *Section 6: Electrical characteristics* *Table 4: Operating conditions* updated current consumption: – $I_{CC3.3V}$. Updated typical value of diversity slave mode. Added maximum values. – I_{CC5V}. Added maximum value for high-current mode at 5.5 V. Updated typical and added maximum value for low-current mode at 3.3 V. *Section 6: Electrical characteristics*. Added note about Vsupply, RF frequency range, ambient temperature and RF power conditions. *Table 6: Down converter mixer and IF amplifier electrical characteristics* : updated: – CG added minimum and max values. – IIP3 added minimum values – nF_{RF}-nF_{LO} modified typical values – NF_{SSB} added maximum value for high-current mode, modified typical value and added maximum value for low-current mode – RF to IF isolation typical value modified – ICC_{MD} low current mode, 3.3 V on pin 41 modified typical value *Table 8: Integer-N synthesizer electrical characteristics* updated: – K_{VCOA} typical values – ΔT_{LK} split into $\Delta T_{LK\ A}$ and $\Delta T_{LK\ B}$ (for VCOA and VCOB). Specified as maximum values. – I_{PLL} typical value – modified table footnote 4 *Table 9: Phase noise performance* updated values of: – LOA open-loop phase noise @ 1 kHz, 10 kHz, 1 MHz, 10 MHz and phase noise floor @ 40 MHz – LOB open-loop phase noise @ 1 kHz, 10 kHz, 100 kHz, 10 MHz and phase noise floor @ 40 MHz Added *Section 7: Typical performance characteristics*. *Section 8.1.9: Voltage controlled oscillators*. Modified sub-sections: – *VCO frequency calibration* – *VCO calibration auto-restart feature*

Table 25. Document revision history (continued)

Date	Revision	Changes
29-Mar-2012	2	*Section 9.3.2: I²C register definitions*. Updated description of bitfield CALTYPE and MUTE_TYPE in registers *MUTE_&_CALIBRATION* Added *Section 9.4.2: Power ON sequence (I²C interface)* *Section 12: Evaluation kit*: – modified *Figure 23: SPI timing waveforms* – modified *Table 20: SPI timing parameters* minimum values of t_{clk_loadr} and t_{clk_loadf}. *Section 10.3.2: SPI register definitions*: updated – description of bitfields CALTYPE and MUTE_TYPE in register *ST2* – description of bitfield PD[4:0] in register *ST3* Added *Section 10.4.2: Power ON sequence (SPI interface)* Added *Section 12: Evaluation kit*.

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