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3.125Gbps XAUI Quad Equalizer

MAX3980

General Description

The MAX3980 quad equalizer provides compensation for transmission medium losses for four “lanes” of digital NRZ data at a 3.125Gbps data rate in one package. It is tailor-made for 10-Gigabit Ethernet (10GbE) backplane applications requiring attenuation of noise and jitter that occur in communicating from MAC to PMD or from MAC to Switch. In support of the IEEE-802.3ae for the XAUI interface, the MAX3980 adaptively allows XAUI lanes to reach up to 40in (1.0m) on FR-4 board material.

The equalizer has 100Ω differential CML data inputs and outputs.

The MAX3980 is available in a 44-pin exposed-pad QFN package. The MAX3980 consumes only 700mW at +3.3V or 175mW per channel.

Applications

IEEE-802.3ae XAUI Interface (3.125Gbps)

InfiniBandSM (2.5Gbps)

Features

- ◆ Four Differential Digital Data “Lanes” at 3.125Gbps
- ◆ Spans 40in (1.0m) of FR-4 PC Board
- ◆ Receiver Equalization Reduces Intersymbol Interference (ISI)
- ◆ Low-Power, 175mW per Channel
- ◆ Standby Mode—Power-Down State
- ◆ Single +3.3V Supply
- ◆ Signal Detect

Ordering Information

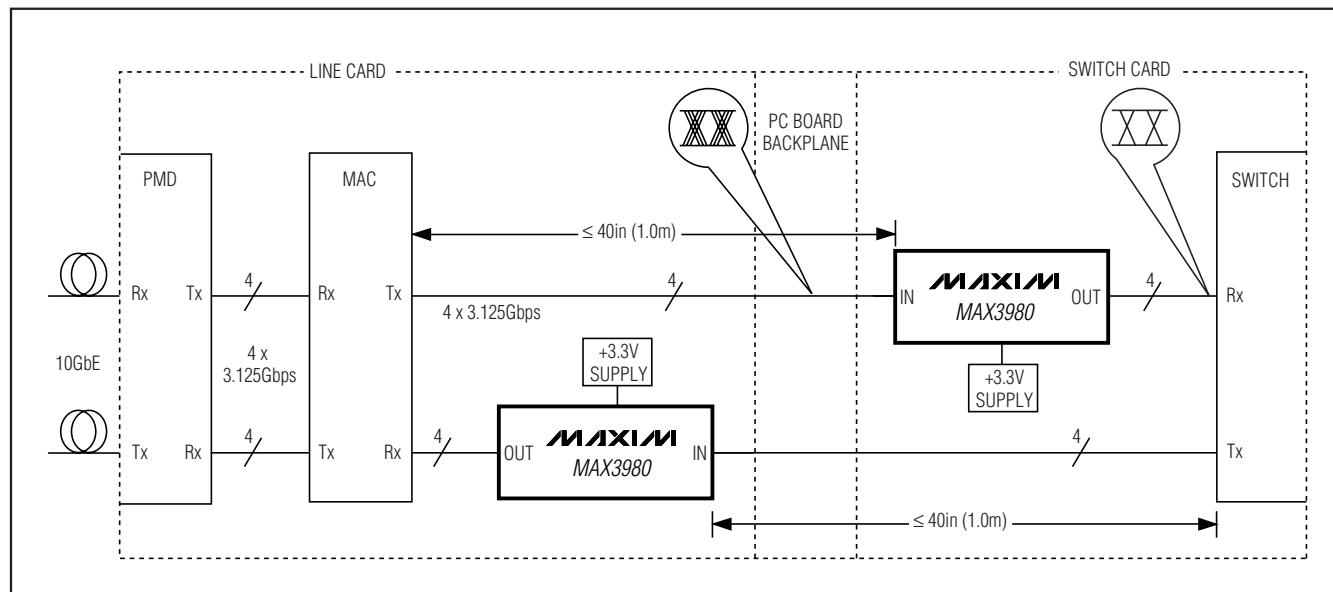
| PART | TEMP RANGE | PIN-PACKAGE |
|-------------|--------------|-------------|
| MAX3980UGH | 0°C to +85°C | 44 QFN-EP* |
| MAX3980UTH+ | 0°C to +85°C | 44 TQFN-EP* |

+Denotes a lead-free/RoHS-compliant package.

*EP = Exposed pad.

Pin Configuration appears at end of data sheet.

Typical Application Circuit



InfiniBand is a trademark and service mark of the InfiniBand Trade Association.



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} -0.5V to +4.0V
 Voltage at SDET, IN $_{\pm}$ -0.5V to ($V_{CC} + 0.5V$)
 Current Out of OUT $_{\pm}$ -25mA to +25mA
 Continuous Power Dissipation ($T_A = +85^{\circ}C$)
 44-Pin QFN-EP (derate 26.3mW/ $^{\circ}C$ above +85 $^{\circ}C$)...2105mW

Operating Ambient Temperature Range0 $^{\circ}C$ to +85 $^{\circ}C$
 Storage Temperature Range-55 $^{\circ}C$ to +150 $^{\circ}C$
 Lead Temperature (soldering, 10s)+300 $^{\circ}C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to +3.6V, input data rate = 3.125Gbps, $T_A = 0^{\circ}C$ to +85 $^{\circ}C$. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^{\circ}C$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|---|-----|----------------|------|----------|
| Supply Power | | EN = TTL low | | | 0.25 | W |
| | | EN = TTL high | | 0.7 | 0.9 | |
| Supply Noise Tolerance | | 10Hz < f < 100Hz | | 100 | | mVp-p |
| | | 100Hz < f < 1MHz | | 40 | | |
| | | 1MHz < f < 2.5GHz | | 10 | | |
| Signal Detect Assert | | Input signal level to assert SDET (Note 1) | 100 | | | mVp-p |
| Signal Detect Deassert | | Input signal level to deassert SDET (Note 1) | | | 30 | mVp-p |
| Signal Detect Delay | | | | | 10 | μs |
| Latency | | From input to output | | 0.32 | | ns |
| CML RECEIVER INPUT | | | | | | |
| Input Voltage Swing | | XAUI transmitter output measured differentially at point A, Figure 1, using K28.5 pattern | 200 | | 800 | mVp-p |
| Return Loss | | 100MHz to 2.5GHz | | 12 | | dB |
| Input Resistance | | Differential | 80 | 100 | 120 | Ω |
| EQUALIZATION | | | | | | |
| Residual Jitter | | Total jitter (Note 2) | | | 0.3 | UIp-p |
| | | Deterministic jitter | | | 0.2 | |
| Random Jitter | | (Note 2) | | 1.5 | | psRMS |
| CML TRANSMITTER OUTPUT (into 100$\Omega \pm 1\Omega$) | | | | | | |
| Output Voltage Swing | | Differential swing | 550 | | 850 | mVp-p |
| Common-Mode Voltage | | | | $V_{CC} - 0.3$ | | V |
| Transition Time | t_f, t_r | 20% to 80% (Note 3) | | 60 | 130 | ps |
| Differential Skew | | Difference in 50% crossing between OUT $_{+}$ and OUT $_{-}$ | | | 12 | ps |
| Output Resistance | | Single ended | 40 | 50 | 60 | Ω |

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, input data rate = 3.125Gbps, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|--------|----------------------|-----|-----|-----|-------|
| TTL CONTROL PINS | | | | | | |
| Input High Voltage | | | 2.0 | | | V |
| Input Low Voltage | | | | | 0.8 | V |
| Input High Current | | | | | 250 | μA |
| Input Low Current | | | | | 500 | μA |
| Output High Voltage | | Internal 10kΩ pullup | 2.4 | | | V |
| Output Low Voltage | | Internal 10kΩ pullup | | | 0.4 | V |

Note 1: K28.7 pattern is applied differentially at point A as shown in Figure 1.

Note 2: Total jitter does not include the signal source jitter. Total jitter (TJ) = [14.1 × RJ + DJ] where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for the random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss and not from clock-source modulation. Jitter is measured at 0 at point C of Figure 1.

Note 3: Using K28.7 (0011111000) pattern.

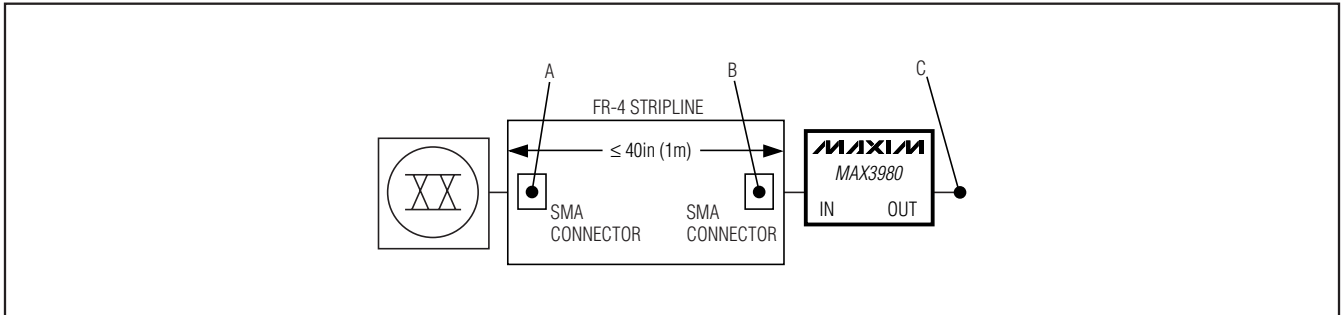


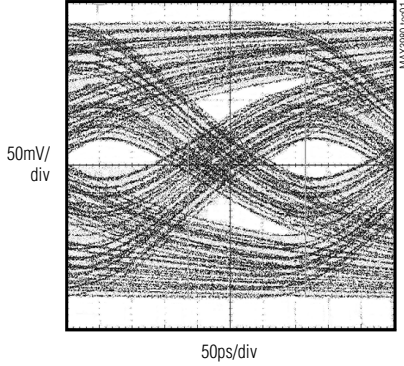
Figure 1. Test Conditions Referenced in the Electrical Characteristics Table

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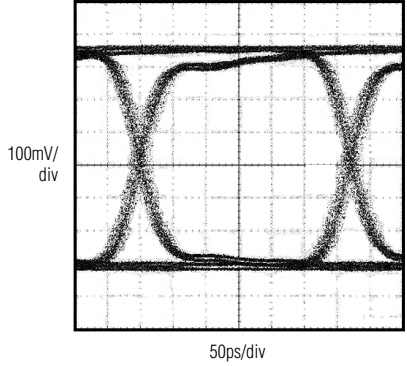
Typical Operating Characteristics

($V_{CC} = +3.3V$, 3.125Gbps, 500mVp-p board input with $2^7 - 1$ PRBS, $T_A = +25^\circ C$, unless otherwise noted.)

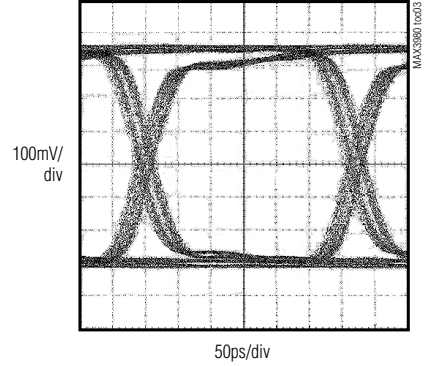
EQUALIZER INPUT EYE DIAGRAM BEFORE EQUALIZATION (40in FR-4 6mil STRIPLINE)



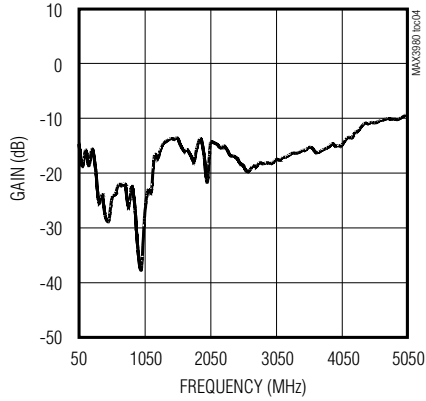
EQUALIZER OUTPUT EYE DIAGRAM AFTER EQUALIZATION (40in FR-4 6mil STRIPLINE)



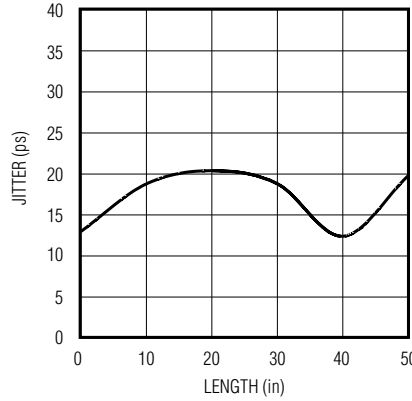
EQUALIZER OUTPUT EYE DIAGRAM (20in BACKPLANE WITH TWO TERADYNE HSD CONNECTORS AND 3in DAUGHTERBOARD)



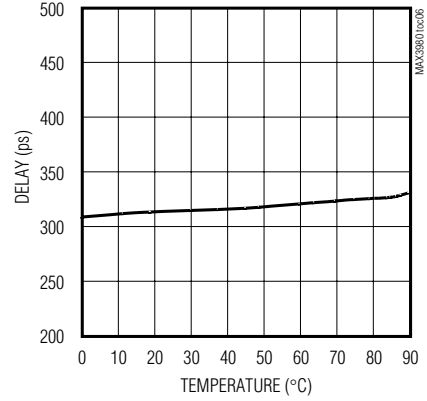
INPUT RETURN GAIN (S11, DIFFERENTIAL, INPUT SIGNAL = -60dBm, DEVICE POWERED OFF)



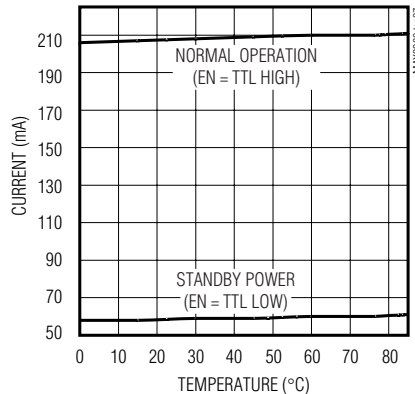
EQUALIZER DETERMINISTIC JITTER vs. LENGTH (FR-4 6mil STRIPLINE, K28.5 PATTERN)



EQUALIZER LATENCY vs. TEMPERATURE



EQUALIZER OPERATING CURRENT vs. TEMPERATURE



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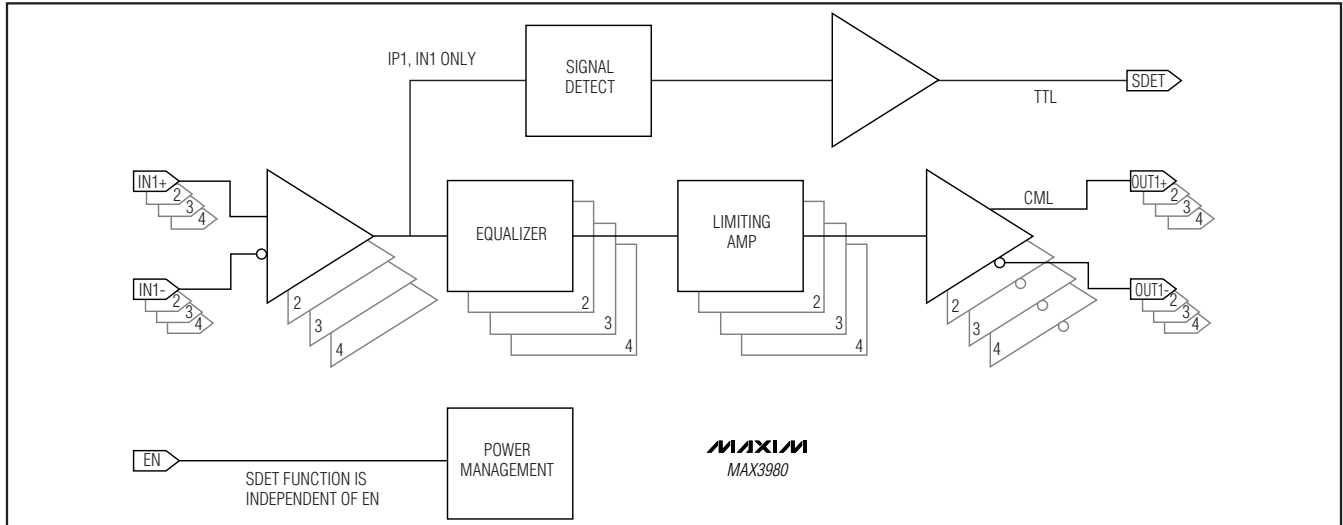
Pin Description

MAX3980

| PIN | NAME | FUNCTION |
|------------------------------|-------|--|
| 1, 5, 9, 13, 23, 27, 31, 35 | VCC | +3.3V Supply Voltage |
| 2 | IN1+ | Positive Equalizer Input Channel 1, CML |
| 3 | IN1- | Negative Equalizer Input Channel 1, CML |
| 4, 8, 12, 16, 26, 30, 34, 38 | GND | Supply Ground |
| 6 | IN2+ | Positive Equalizer Input Channel 2, CML |
| 7 | IN2- | Negative Equalizer Input Channel 2, CML |
| 10 | IN3+ | Positive Equalizer Input Channel 3, CML |
| 11 | IN3- | Negative Equalizer Input Channel 3, CML |
| 14 | IN4+ | Positive Equalizer Input Channel 4, CML |
| 15 | IN4- | Negative Equalizer Input Channel 4, CML |
| 17–22, 39–42 | N.C. | No Connection. Leave unconnected. |
| 24 | OUT4- | Negative Equalizer Output Channel 4, CML |
| 25 | OUT4+ | Positive Equalizer Output Channel 4, CML |
| 28 | OUT3- | Negative Equalizer Output Channel 3, CML |
| 29 | OUT3+ | Positive Equalizer Output Channel 3, CML |
| 32 | OUT2- | Negative Equalizer Output Channel 2, CML |
| 33 | OUT2+ | Positive Equalizer Output Channel 2, CML |
| 36 | OUT1- | Negative Equalizer Output Channel 1, CML |
| 37 | OUT1+ | Positive Equalizer Output Channel 1, CML |
| 43 | EN | Enable Equalizer Input. A TTL high selects normal operation. A TTL low selects low-power standby mode. |
| 44 | SDET | Signal Detect Output for Channel 1. Produces a TTL high output when a signal is detected. |
| — | EP | Exposed Pad. The exposed pad must be soldered to the circuit board ground plane for proper thermal and electrical performance. |

3.125Gbps XAUI Quad Equalizer

Functional Diagram



Detailed Description

Receiver and Transmitter

The receiver accepts four lanes of 3.125Gbps current-mode logic (CML) digital data signals. The adaptive equalizer compensates each received signal for dielectric and skin losses. The limiting amp shapes the output of the equalizer. The regenerated XAUI lanes are transmitted as CML signals. The source impedance and termination impedances are 100Ω differential.

General Theory of Operation

Internally, the MAX3980 comprises signal-detect circuitry, four matched equalizers, and one equalizer-control loop. The four equalizers are made up of a master equalizer and three slave equalizers. The adaptive control is generated from only channel 1. It is assumed that all channels have the same characterization in frequency content, coding, and transmission length.

The master equalizer consists of the following functions: signal detect, adaptive equalizer, equalizer control, and limiting and output drivers. The signal detect indicates input signal power. When the input signal level is sufficiently high, the SDET output is asserted. This does not directly control the operation of the part.

The equalizer core reduces intersymbol interference (ISI), compensating for frequency-dependent, media-induced loss. The equalization control detects the spectral contents of the input signal and provides a control voltage to the equalizer core, adapting it to different media. The equalizer operation is optimized for

short-run DC-balanced transmission codes such as 8b/10b codes.

CML Input and Output Buffers

The input and output buffers are implemented using CML. Equivalent circuits are shown in Figures 2 and 3. For details on interfacing with CML, see Maxim application note HFAN-1.0, *Interfacing Between CML, PECL, and LVDS*. The common-mode voltage of the input and output is above 2.5V. AC-coupling capacitors are required when interfacing this part. Values of 0.10μF or greater are recommended.

Media Equalization

Equalization at the input port compensates for the high-frequency loss encountered with up to 40in (1.0m) of FR-4 transmission lines. This part is optimized for 40in and 3.125Gbps; however, the part reduces ISI for signals spanning longer distances and functions for data rates from 2Gbps to 4Gbps, provided that short-length balanced codes, such as 8b/10b, are used.

Applications Information

Standby Mode

The power-saver standby state allows reduced-power operation. The TTL input, EN, must be set to TTL high for normal operation. A TTL low at EN forces the equalizer into the standby state. The signal EN does not affect the operation of the signal detect (SDET) function. For constant operation, connect the EN signal directly to VCC.

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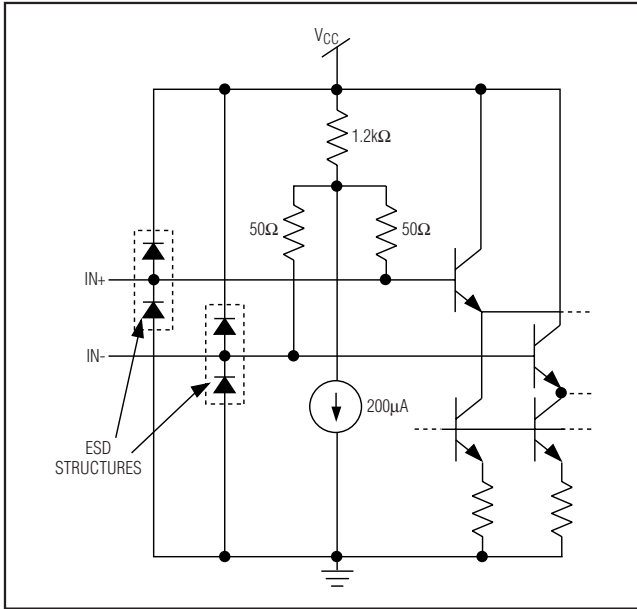


Figure 2. CML Input Buffer

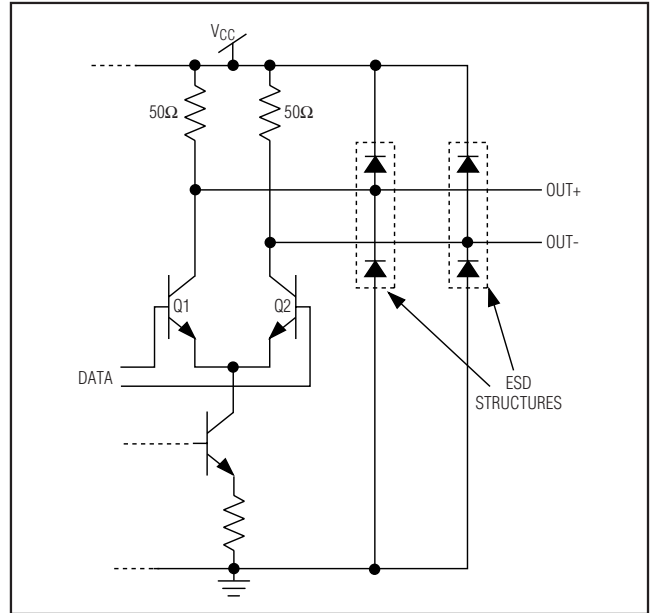


Figure 3. CML Output Buffer

Signal Detect with Standby Mode

Signal activity is detected on channel 1 only. When the peak-to-peak differential voltage at $IN1\pm$ is less than 30mVp-p, the TTL output SDET goes low. When the peak-to-peak differential voltage becomes greater than 100mVp-p, SDET is asserted high. SDET can be used to automatically force the equalizer into standby mode by connecting SDET directly to the EN input. When not used, SDET should not be connected.

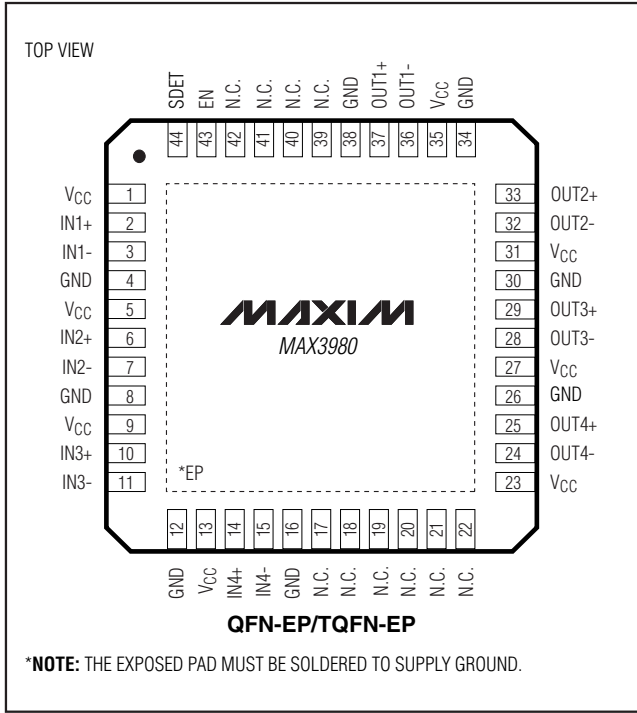
The signal-detect function continues to operate while the part is in standby mode. While connected to the EN pin, the signal detect can “wake up” the part and resume normal operation.

Layout Considerations

Circuit-board layout and design can significantly affect the MAX3980 performance. Use good high-frequency design techniques, including minimizing ground inductances and vias and using controlled-impedance transmission lines for the high-frequency data signals. Signals should be routed differentially to reduce EMI susceptibility and crosstalk. Power-supply decoupling capacitors should be placed as close as possible to the VCC pins.

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Pin Configuration



Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|--------------|--------------|-------------------------|
| 44 QFN | G4477-1 | 21-0092 |
| 44 TQFN | T4477-3 | 21-0144 |

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Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|---|---------------|
| 0 | 9/01 | Initial release. | — |
| 1 | 5/03 | Added the package code to the <i>Ordering Information</i> table. | 1 |
| | | Updated the 21-0092 package drawing in the <i>Package Information</i> section. | 8, 9 |
| 2 | 1/05 | Added the TQFN package to the <i>Ordering Information</i> table. | 1 |
| | | Added the 21-0144 package drawing to the <i>Package Information</i> section. | 10 |
| 3 | 12/08 | Changed the <i>Absolute Maximum Ratings</i> of SDET, IN _± from +5.0V to (V _{CC} to 0.5V) to -5.0V to (V _{CC} to 0.5V). | 2 |

MAX3980

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