ispClock5312S Evaluation Board

User's Guide

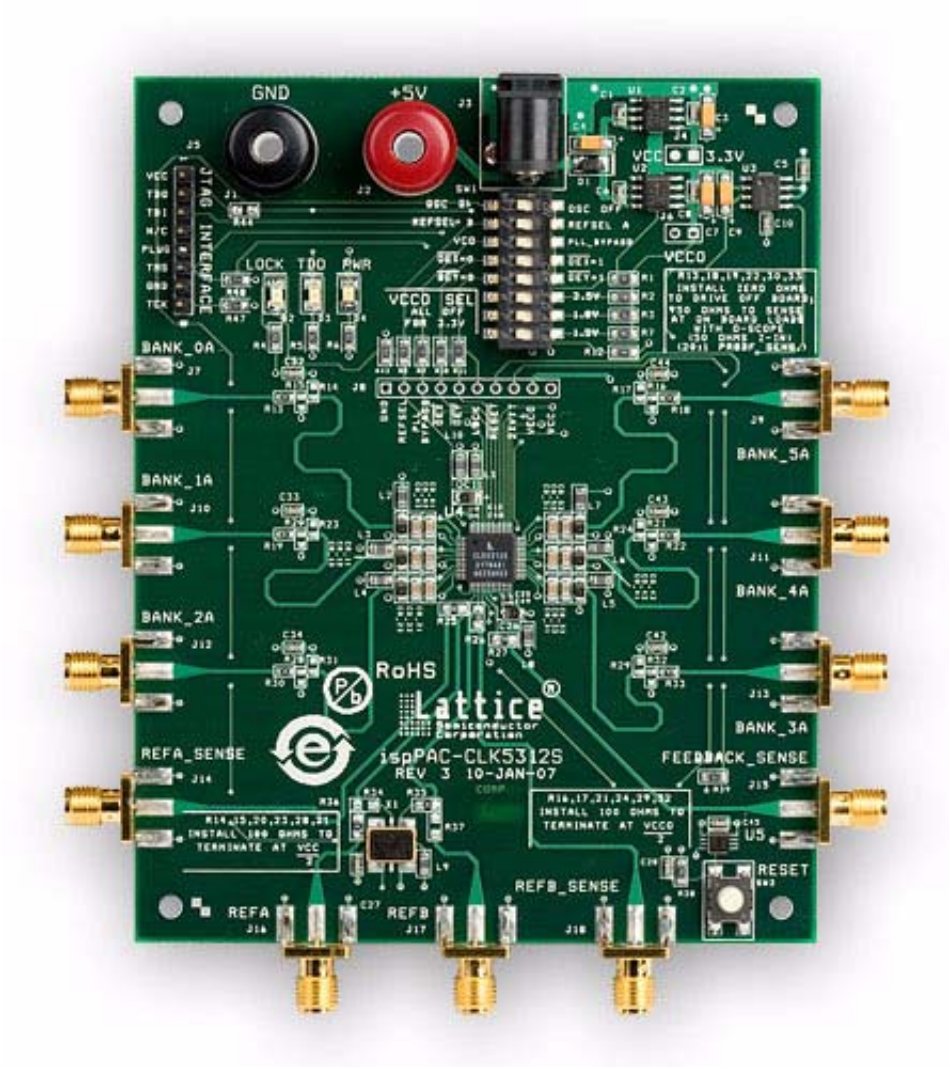
August 2007
Revision: EB32_01.0

Introduction

The family of ispClock™5300S devices from Lattice Semiconductor Corporation provide in-system-programmable zero delay universal fan-out buffers for use in clock distribution applications. Single-ended ultra low skew outputs are organized with two outputs per bank. Each pair of outputs may be independently configured to support separate I/O standards (LVTTL, LVCMOS -3.3V, 2.5V, 1.8, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on chip in non-volatile E^2CMOS® memory.

The ispClock5300S devices provide extremely low propagation delay (zero-delay) from input to output using the on-chip low jitter high-performance phase locked loop (PLL). A set of three programmable 5-bit counters can be used to generate three frequencies derived from the PLL clock. These counters are programmable in powers of 2 only (1, 2, 4, 8, 16, 32). The clock output from any of the V-dividers can then be routed to any clock output pair through the output routing matrix. The output routing matrix also enables routing of reference clock inputs directly to any output. For additional details, please refer to the ispPAC-CLK5300S Family Data Sheet.

Figure 1. ispClock5312S Evaluation Board



ispClock5312S Evaluation Board

The ispClock5312S is the first member of the ispClock5300S family with six output banks and thus has 12 single-ended ultra low skew outputs. The ispClock5312S evaluation board features this device with full support circuitry for power, programming, testing, and evaluation. The "A" output for each bank is supported with matched transmission lines, optional on-board termination, and SMA connections at the edge of the board to provide full flexibility in measurement and evaluation. Output 1B is hard-wired to the feedback input to complete the feedback loop of the PLL because, the ispClock5300S family of devices only supports external feedback. Each output bank has separate decoupling to isolate the outputs if they are configured for different frequencies. An on board 100 MHz oscillator with 3.3V CMOS output is connected to the REFB input of the ispClock5312S. The REFA input is connected to an SMA connector for testing with different input frequencies.

For a complete list of the various connections and interfaces used on the ispClock5312S evaluation board, please refer to the schematics in the appendix of this document.

Finally, the ispClock5312S evaluation board is 100% lead free and ROHS compliant as Lattice Semiconductor Corporation is sensitive to environmental issues.

Additional Resources

Additional resources relating to the ispClock5312S Evaluation Board are available on the Lattice web site. Go to: www.latticesemi/boards and navigate to "mixed signal boards" to find the appropriate link. Updates to this document can be found there, as well as sample programs and links to other related items.

PAC-Designer®

PAC-Designer is the software used to develop custom programs for the ispClock5312S device, generate programming files, and manage the download/programming of the device.

PAC-Designer is available for download from the Lattice web site at: www.latticesemi.com/pac-designer.

Programming Interface

JTAG programming is supported with the eight-pin connector J5 and either the USB download cable (HW-USBN-2A) or the parallel download cable (HW-DLN-3C). The Windows-based program PAC-Designer provides an intuitive interface for configuring the ispClock5312S and can be used to either directly program the evaluation board or to export a JEDEC file which can be used with ispVM® to program the evaluation board.

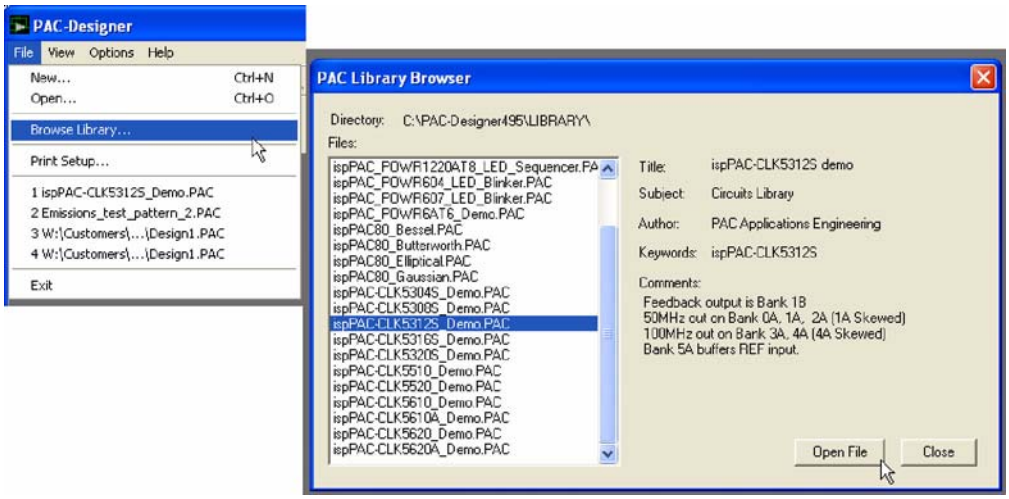
ispVM system is available for download from the Lattice web site at: www.latticesemi.com/ispvm.

Important Note: The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD® Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the ispClock5312S device and render the board inoperable.

Demo Configuration and Reprogramming

The ispClock5312S evaluation board is preprogrammed at the factory with a demonstration configuration. This demonstration configuration can be reprogrammed into the evaluation board from PAC-Designer by browsing the library files as shown in Figure 2.

Figure 2. Demonstration File in PAC-Designer's Library



Power Supply Considerations

All that is needed to power the ispClock5312S evaluation board is a 5V power supply capable of providing one ampere or more. The board can be powered either by a wall adapter with a 2.5mm coaxial power plug at J3 or from a bench supply with banana plugs at J1 and J2. Once onboard, the five volts is regulated (U1) to provide the 3.3V supply needed for VCCD, VCCA, VCCJ, and VCCO for banks zero, one, and two.

A second adjustable regulator (U2) provides the VCCO for banks three, four, and five and it is programmable using the on-board resistors and three of the DIP-switches of SW1. To bypass the on-board regulators, jumpers J4 and J6 can be cut on the bottom of the board to allow external supplies to power the ispClock5312S.

Input/Output Connections

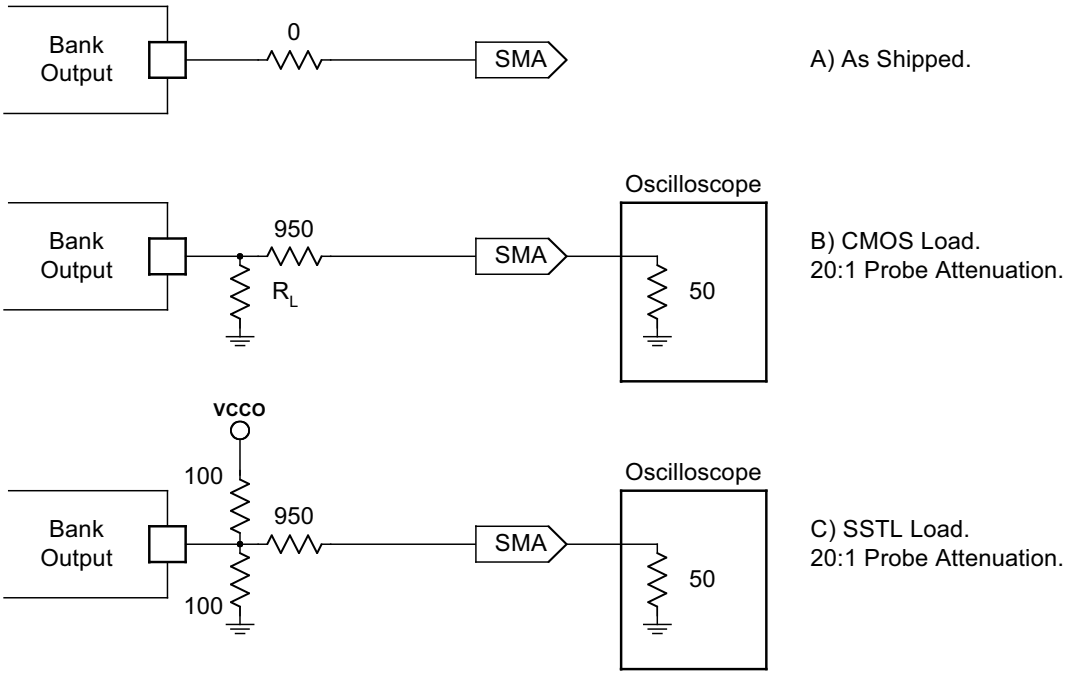
This board incorporates tapered transitions from the SMA connectors to the matched 50-ohms microstrip transmission lines. All of the output transmission lines are matched in length to the sense signals (REFA, REFB, and FEEDBACK) to support accurate timing measurements both for bank-to-bank and input to output. The header at J8 provides access to the essential control and monitor signals of the ispClock5312S such as REFSEL, PLL_BYPASS, OEX, OEY, LOCK, and RESET.

An off-board CMOS clock can be used by connecting to the REFA (J16) SMA connector. The ispClock5312S can also be driven from an external differential clock source by moving the zero-ohm resistor from the R35 location to the R37 location and connecting the clocks to both REFA and REFB inputs (J16 and J17). When an external clock source is used, switches 1 and 2 of DIP-switch SW1 should be in the left position (OSC OFF and REFSEL A).

On-Board Termination

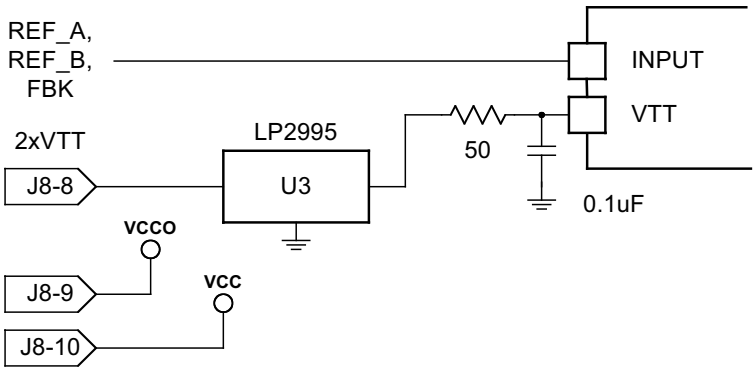
The ispClock5312S evaluation board is equipped with zero-ohm 0603 SMD resistors in series with the six outputs and their corresponding SMA connectors in order to drive an off-board CMOS loads. This is shown in Figure 3-A. However, these resistors can be replaced and additional resistors added to employ a variety of termination networks to match the desired output mode. In Figure 3-B the zero-ohm resistor is replaced with a 950-ohm sense resistor and a load resistor is added to ground. The input impedance of the oscilloscope provides a 20:1 probe attenuation. A small (5pF to 10pF) cap can be added on top of the load resistor to simulate a CMOS input. In Figure 3-C a divider network terminates the transmission line at 1/2 VCCO into a 50-ohm load and the 950-ohm resistor allows sensing by the oscilloscope with a 20:1 probe attenuation. A low value capacitor (5pF to 10pF) can be soldered on top of the 100-ohm resistor to ground to simulate an input to SSTL logic.

Figure 3. Onboard Output Termination Options



The ispClock5312S evaluation board also supports input termination for the reference clock inputs and the feedback input if they are configured as SSTL. For CMOS operation (default) nothing needs to be added to the board. For each SSTL input there is a set of pads on the backside of the board for a resistor and capacitor to terminate the input as close to the device as possible. In addition, for SSTL termination pin 8 of the header J8 needs to be connected to either pin 9 or 10 of the same header or connected off board to an adjustable supply to set the termination voltage. Note the voltage applied at pin 8 of J8 will be twice the termination voltage as U3 divides the input voltage in half, see Figure 4 and the schematic in the appendix for more details.

Figure 4. Optional Input Termination for SSTL



DIP Switch

To simplify the use of the ispClock5312S evaluation board an 8-position DIP switch (SW1) is provided for the more common adjustments. The switch can roughly be divided into four sections; reference oscillator control, PLL control, output enables, and VCCO control. Table 1 lists the switches and their respective functions. Note that for switch sections 6, 7, and 8 only one should be on at a time. The default setting with all the switches to the left (off) enables the onboard oscillator, selects that as the clock reference, and allows the PLL to lock to that frequency.

Table 1. DIP Switch Functions

Off (to the left)	SW1 - Section	ON (to the right)
Oscillator On	1	Oscillator Off
REFSEL = B	2	REFSEL = A
VCO Enabled	3	PLL-Bypass
OEX=0	4	OEX=1
OEY=0	5	OEY=1
VCCO = 3.3V	6	VCCO=2.5V
VCCO = 3.3V	7	VCCO=1.8V
VCCO = 3.3V	8	VCCO=1.5V

Measuring Zero Delay and Bank-to-Bank Skew

The transmission lines for the outputs are matched in length (and thus time) to the sense lines (FEEDBACK, REF_A, and REF_B). Thus, when matched SMA cables are used to connect the outputs to an oscilloscope the rising edges will be aligned as shown in Figure 5. Here the green trace (probe-2) displays the feedback as sensed by the on-board 950-ohm resistor (see the schematic) while the other traces illustrate the synchronization of the outputs. By double clicking the Skew Manager in PAC-Designer (see Figure 6), the skew between outputs is set to about 300ps. The ispClock5312S is then reprogrammed and the resulting measurement is shown in Figure 7. Note the feedback signal has been replaced with an output.

Figure 5. Outputs are Synchronized with the Feedback Input

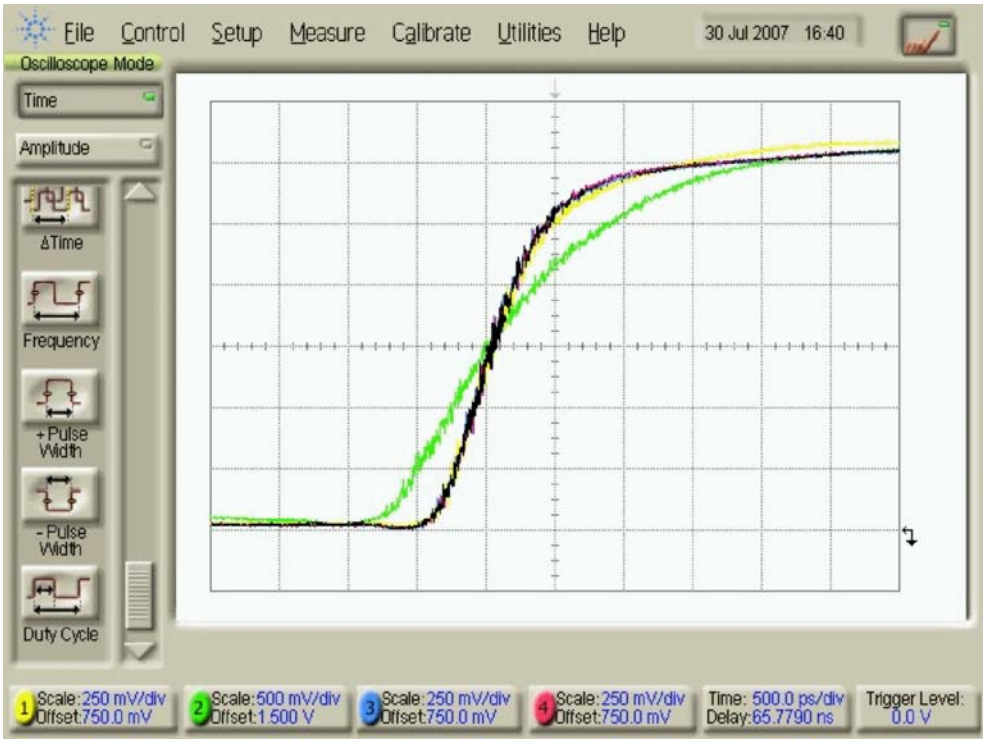


Figure 6. PAC-Designer Skew Manager and Settings Dialog

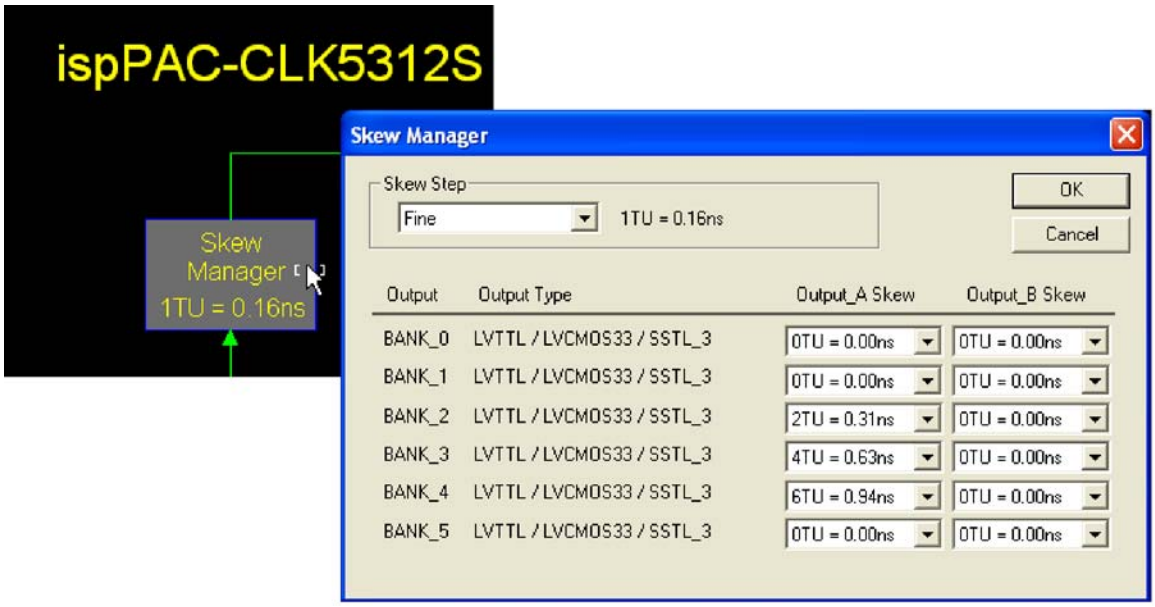
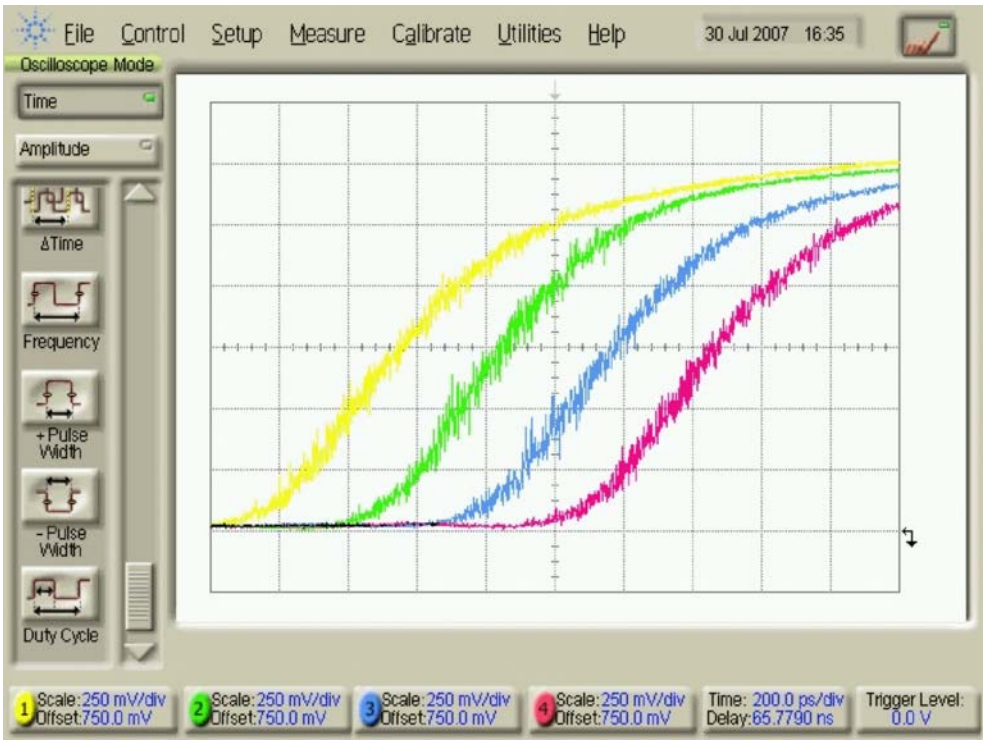


Figure 7. Outputs are Skewed 300ps



ispClock5312S Evaluation Board Bill of Materials

Quantity	Ref Des	Description	Manufacturer	Part Number
2	C12, 25	0.1uF SMD 0402 Ceramic Capacitor	Kemet	C0402C104K9PACTU
2	C48, 49	0.01uF SMD 0402 ceramic capacitor	Kemet	C0402C103K4RACTU
15	C1, 2, 5, 6, 8,10, 27, 28, 32, 33, 34, 42, 43, 44, 45	0.1uF SMD 0603 ceramic capacitor	Panasonic	ECJ-1VB1C104K
8	C11,26 CO_03, 13, 23, 33, 43, 53	6.8uF 6.3V SMD 0805 tantalum capacitor	Rohm	TCP0J685M8R
6	CO_01,11, 21, 31, 41, 51	330pF SMD 0805 ceramic capacitor	Kemet	C0805C331K5RACTU
6	CO_02, 12, 22, 32, 42, 52	3.3nF SMD 0805 ceramic capacitor	Kemet	C0805C332K5RACTU
4	C3, 4, 7, 9	10uF 10V SMD tantalum capacitor	AVX Corp.	TPSA106K010R0900
1	D1	Schottky diode SMD	ON Semi	MBR120VLSFT1G
1	D2	Blue LED SMD 1206	LiteOn	LTST-C150TBKT
1	D3	Red LED SMD 1206	LiteOn	LTST-C150KRKT
1	D4	Green LED SMD 1206	LiteOn	LTST-C150KGKT
1	J3	2.5mm DC power connector	CUI Inc.	PJ-102B
1	J2	Red banana jack	SPC Tech.	845-R
1	J1	Black banana jack	SPC Tech.	845-B
1	J5	8-position pin header	Molex	22-28-4084
11	J7,9,10-18	SMA Connector PCB End Launch	Johnson	142-0701-801
10	L1-L10	300 ohm Signal Ferrite SMD 0805	Stewart	LI0805G301R-10
1	X1	100 MHz Clock Source	ECS	ECS-3953M-1000BN
1	R1	178k 5% resistor SMD 0805	Yageo	RC0805FR-07178KL
1	R2	301k 5% resistor SMD 0805	Yageo	RC0805FR-07301KL
1	R3	73.2k 1% resistor SMD 0805	Yageo	RC0805FR-0773K2L
1	R7	31.6k 1% resistor SMD 0805	Yageo	RC0805FR-0731K6L
1	R12	100k 1% resistor SMD 0805	Yageo	RC0805FR-07100KL
3	R25,26,27	953 ohm 1% resistor SMD 0603	Yageo	RC0603FR-07953RL
2	R38, 43	10k 5% resistor SMD 0805	Yageo	RC0805JR-0710KL
8	R4, 5, 6, 8-11, 39	1k 5% resistor SMD 0805	Yageo	RC0805JR-071KL
2	R47,48	4.7k 5% resistor SMD 0805	Yageo	RC0805JR-074K7L
8	R13,18,19, 22, 30, 33, 35, 36	Zero-ohm resistor 5% SMD 0603	Yageo	RC0603JR-070RL
1	SW1	Slide Sw 8POS SMD	ITT Industries	SDA08H1SBD
1	SW2	Momentary Switch SMD	Panasonic	EVQ-QXT03W
1	U1	3.3V fixed regulator SMD 8SOIC	Texas Inst.	TPS77733D
1	U2	Adj LDO Regulator SMD 8SOIC	Texas Inst.	TPS77701D
1	U3	DDR Term Regulator SMD 8SOIC	National Semi.	LP2995M
1	U4	IspPAC-CLK5312S	Lattice	
1	U5	74LVC3G34 Triple Buffer 8-SSOP	Texas Inst.	SN74LVC3G34DCTR

References

- ispPAC-CLK5300S Family Data Sheet

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
ispClock5312S Evaluation Board	PACCLK5312S-EVN	

Technical Support Assistance

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e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
August 2007	01.0	Initial release.

Appendix A. Schematic

Figure 8. ispClock5312S Inputs, JTAG, Core and PLL

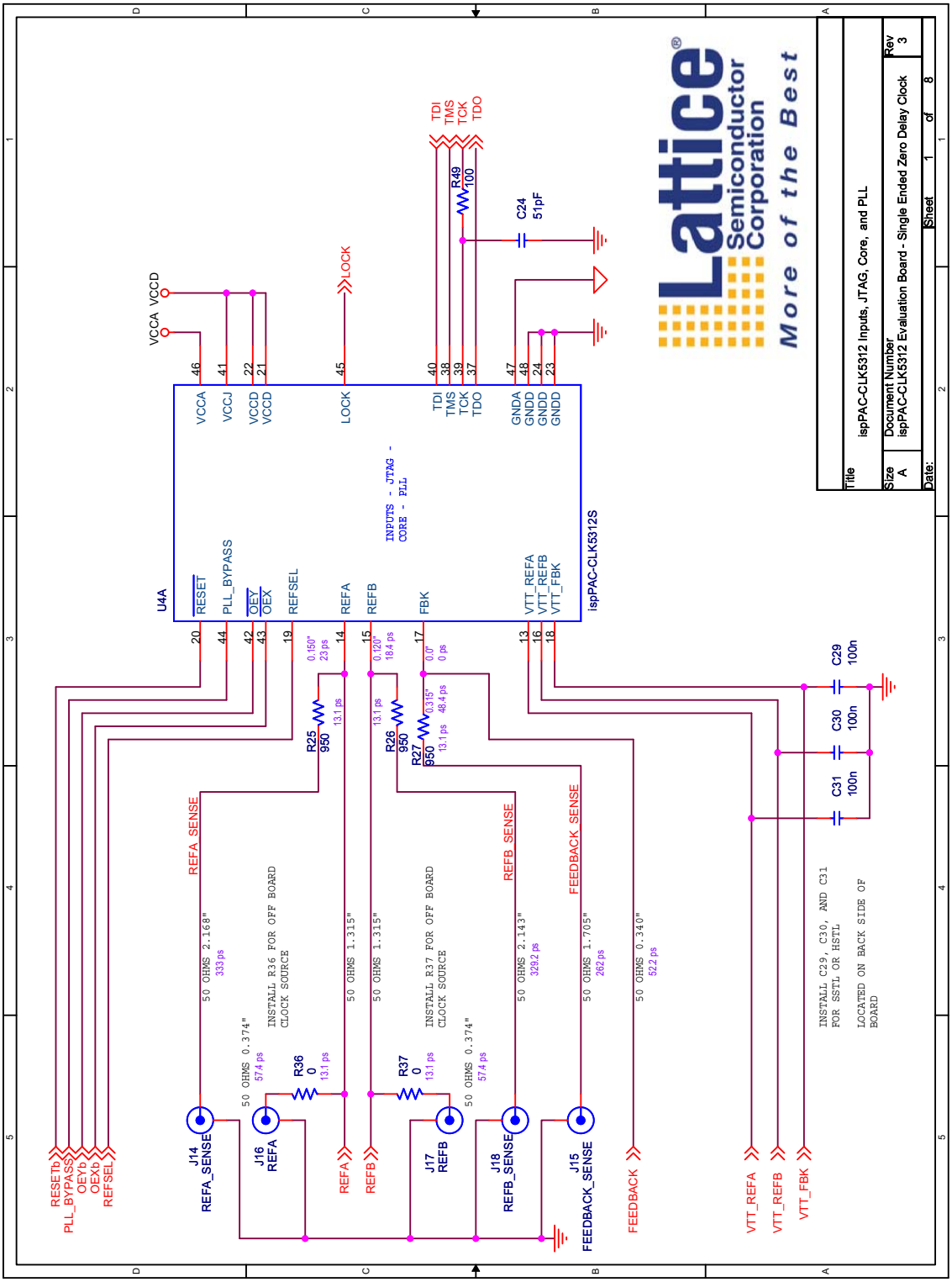


Figure 9. ispClock5312S Output Banks 0, 1 and 2

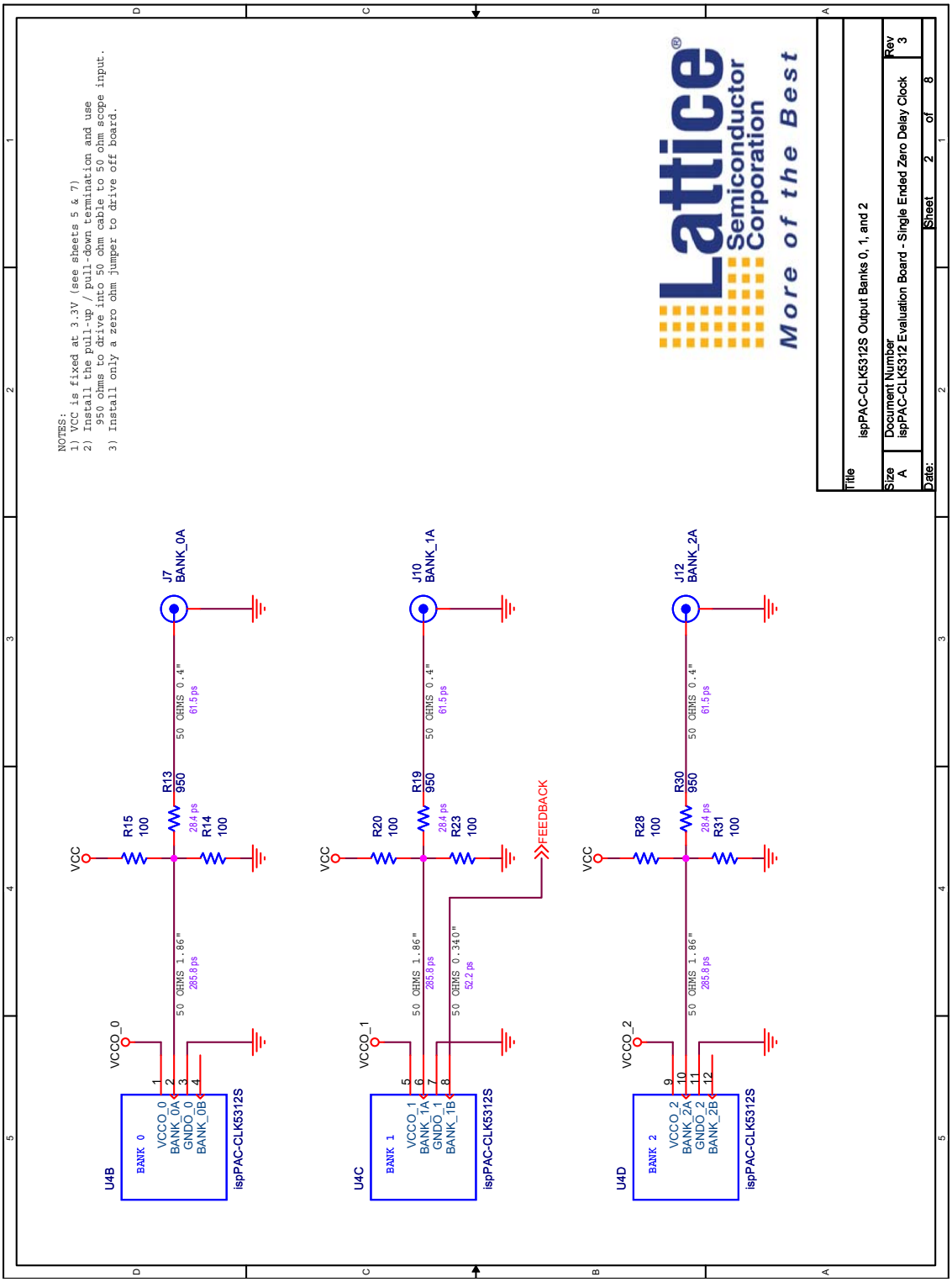


Figure 10. ispClock5312S Output Banks 3, 4 and 5

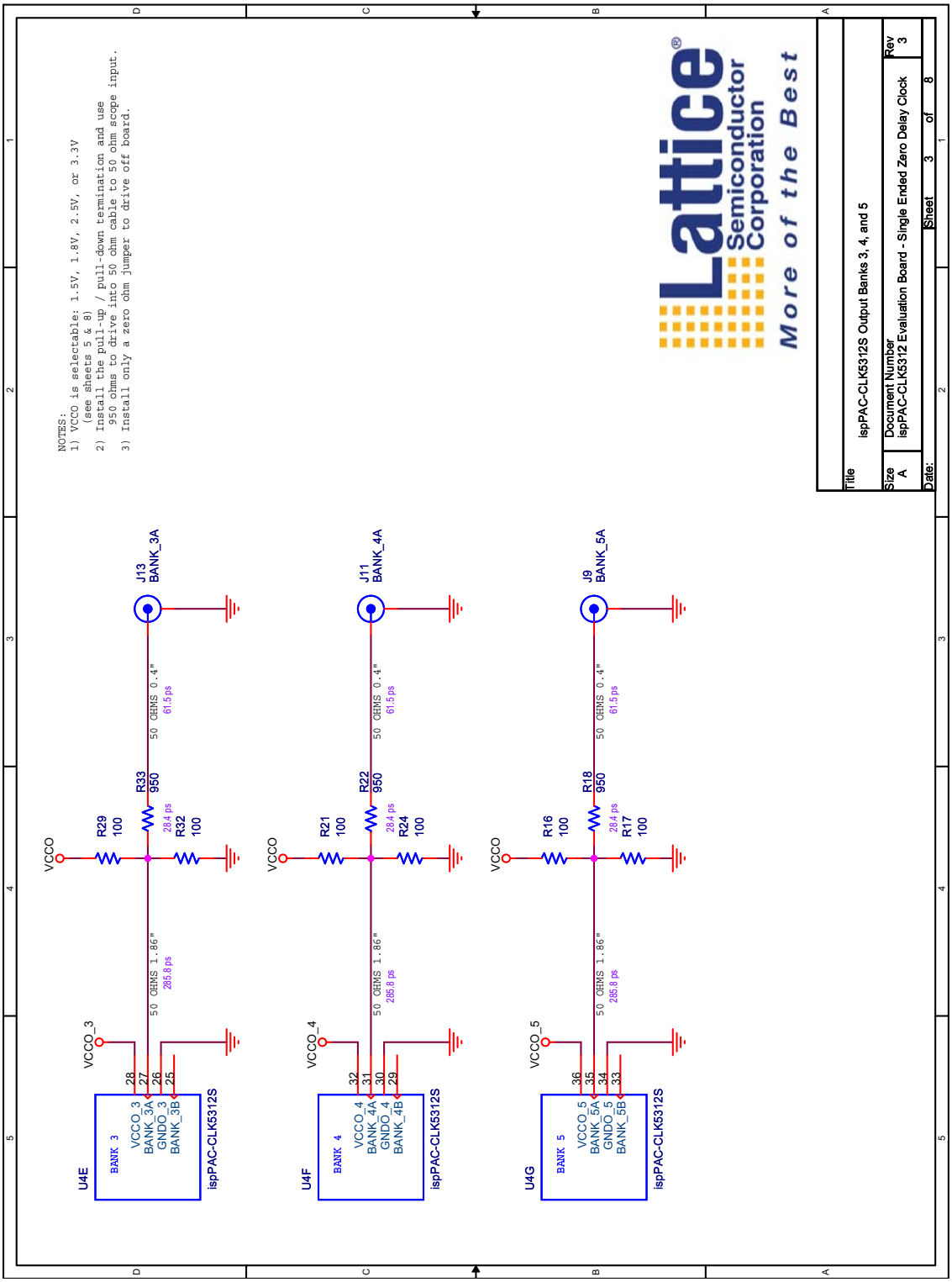


Figure 11. Connectors and Oscillator

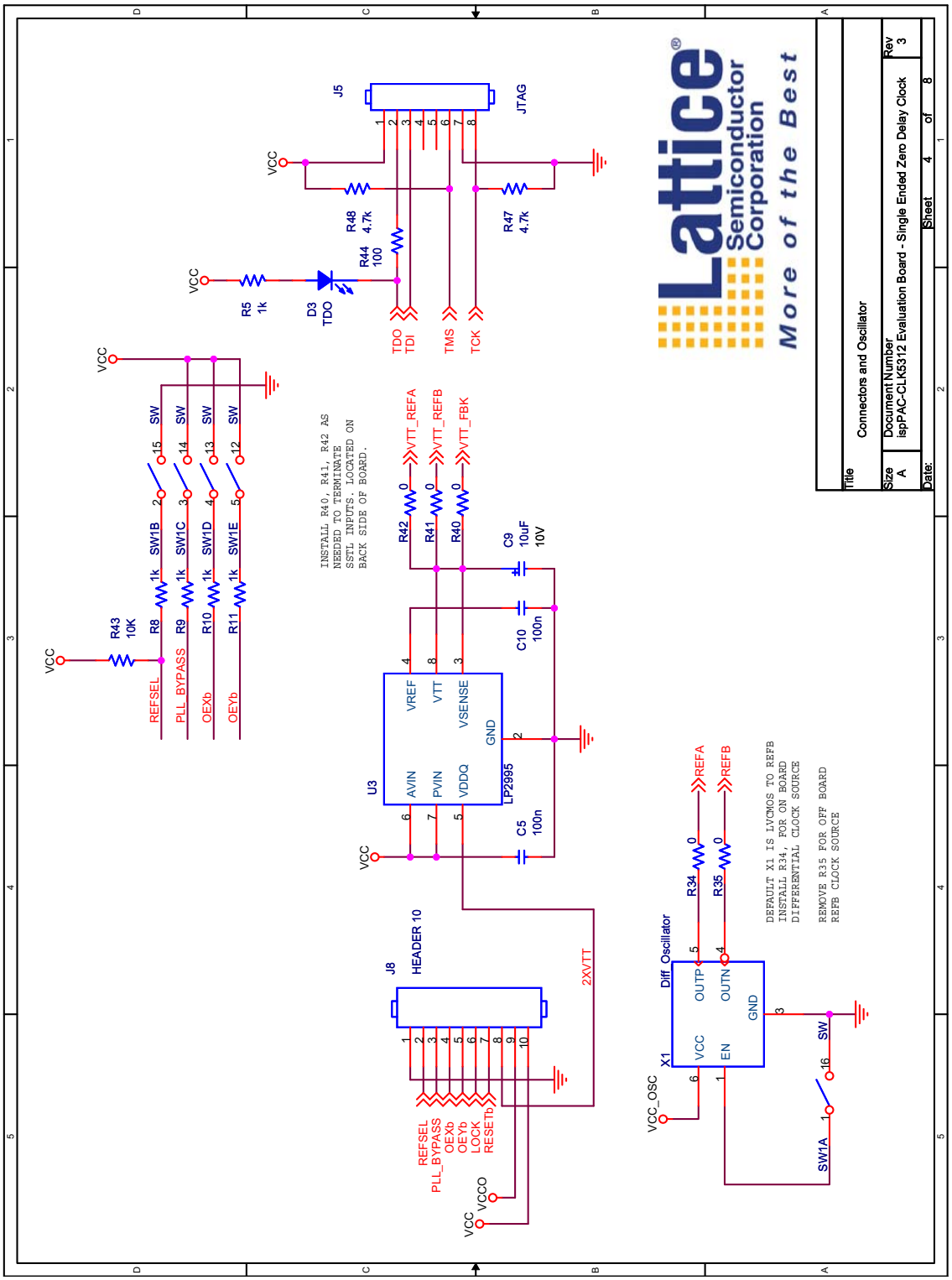


Figure 12. Power Supplies and LEDs

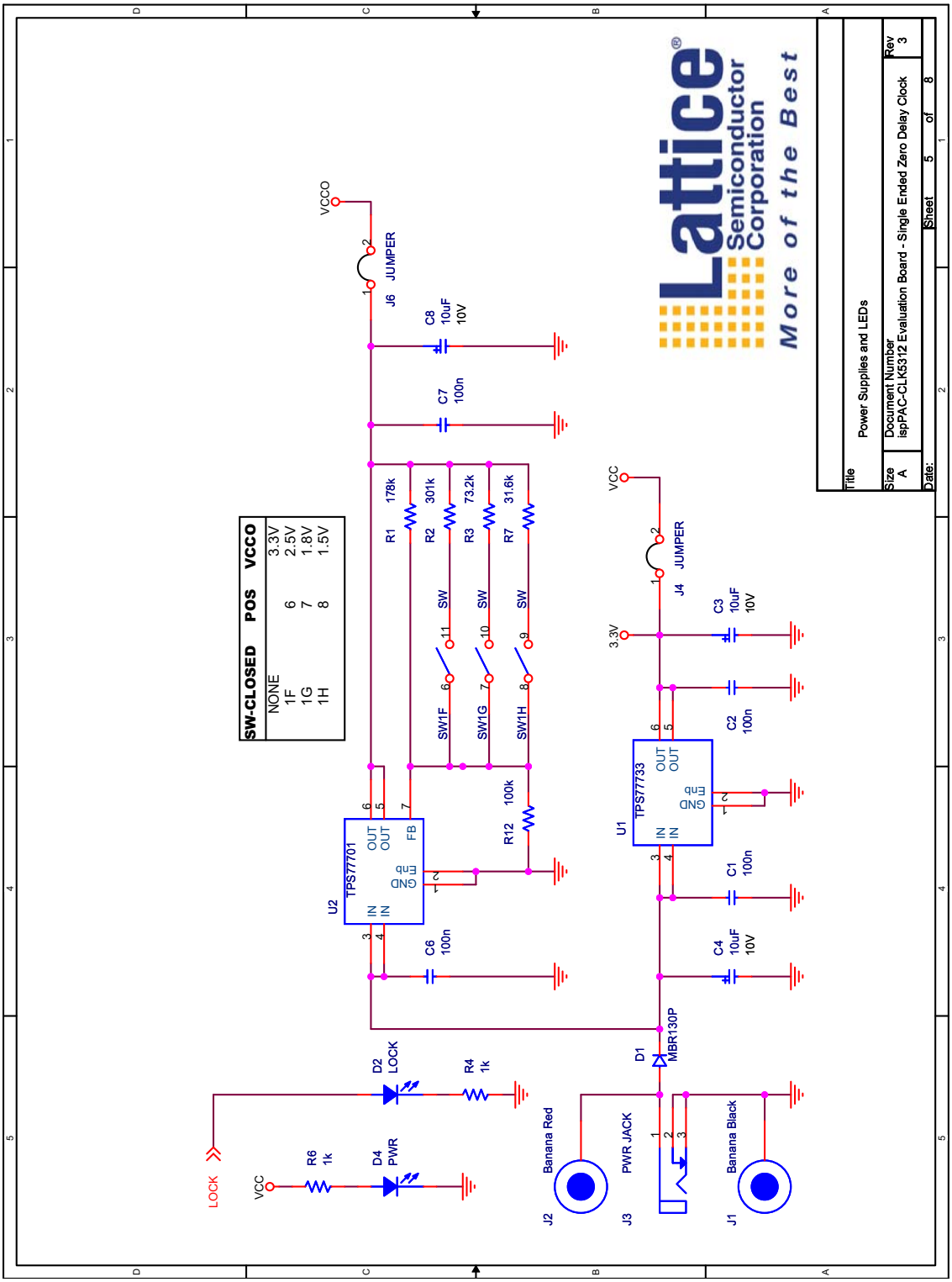


Figure 13. Power Supply Decoupling Networks and Reset Circuit

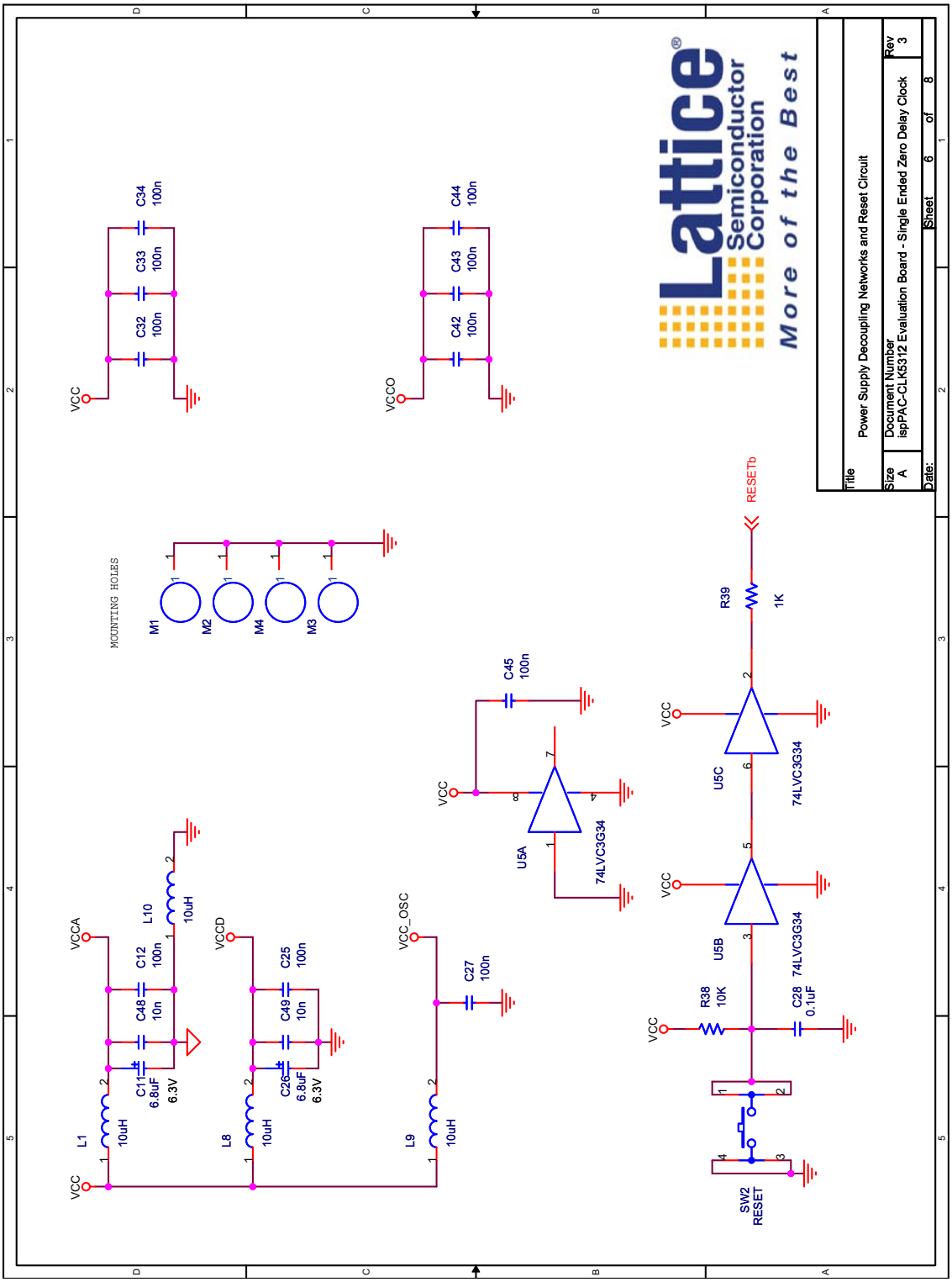


Figure 14. Banks 0, 1 and 2 Power Supply Decoupling Networks

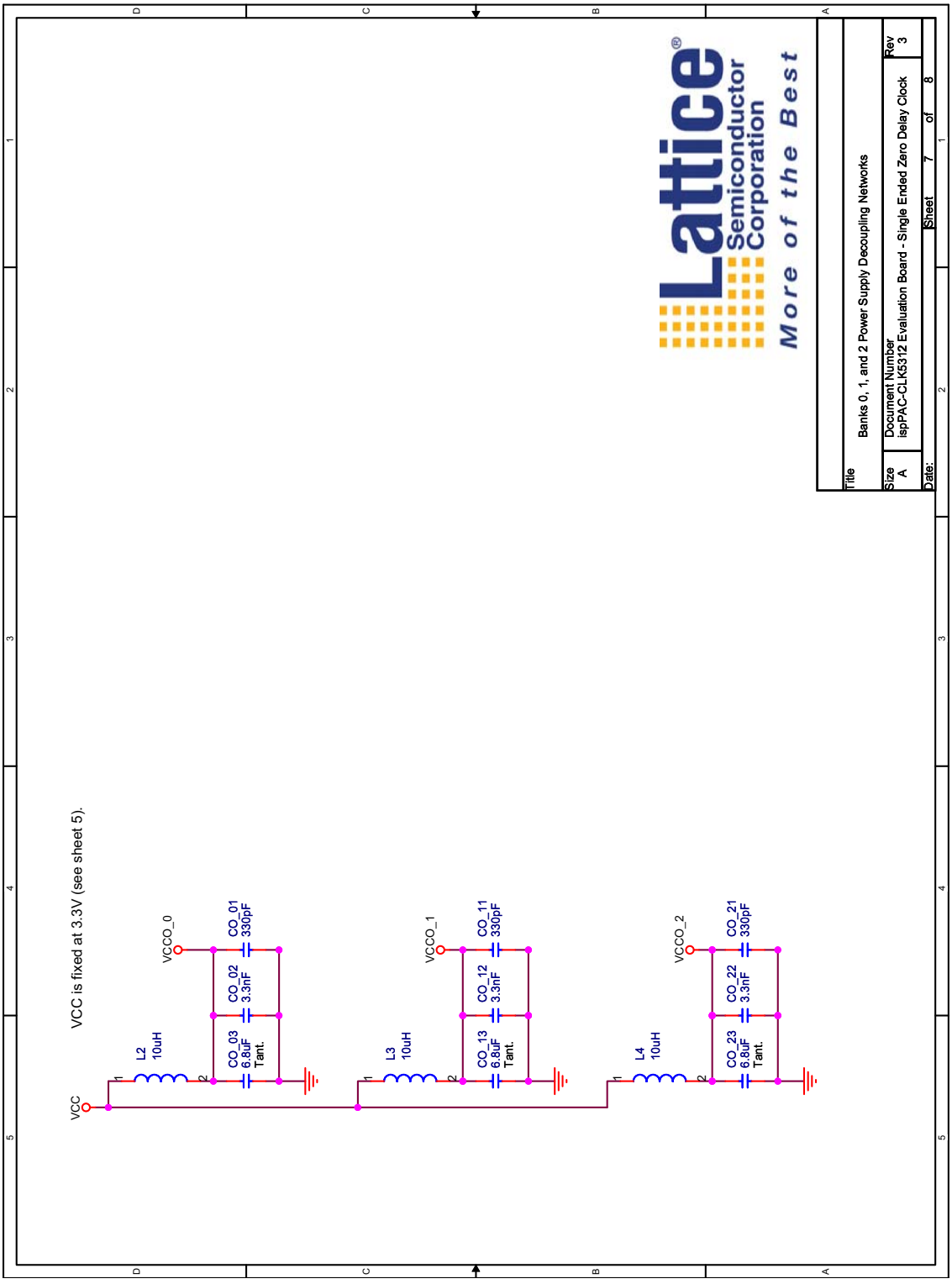
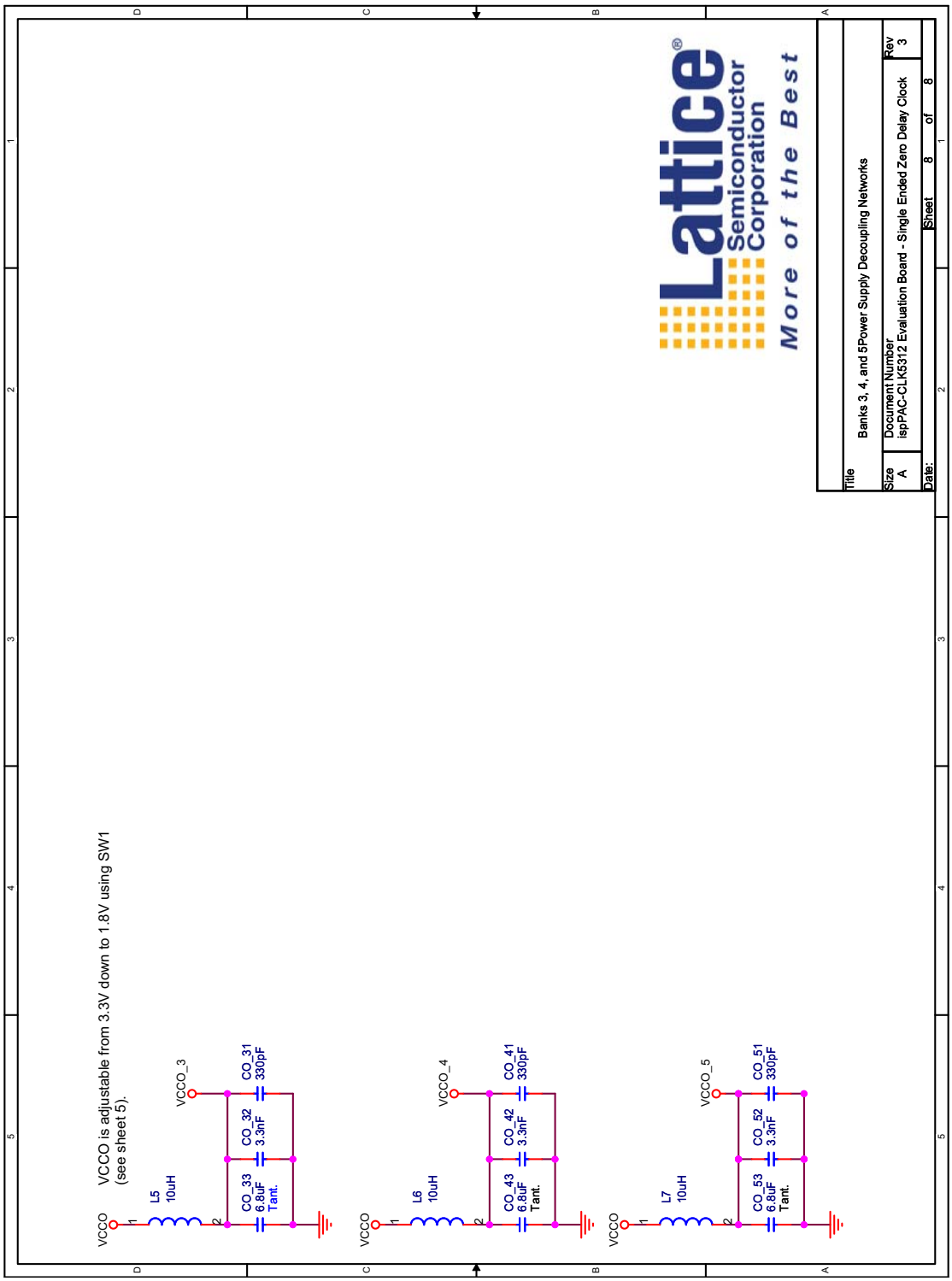


Figure 15. Banks 3, 4 and 5 Power Supply Decoupling Networks



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