ISL12008 I^2C Real Time Clock with Battery Backup

Low Power RTC with Battery ReSeal™ Function

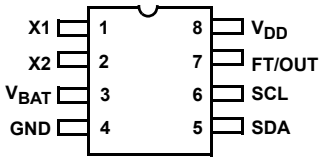
FN6690
Rev 1.00
Sep 26, 2008

The ISL12008 device is a low power real time clock/calendar that is pin compatible and functionally equivalent to the ST M41T00S and Maxim DS1340 with timing and crystal compensation. The device additionally provides power-fail indicator, software alarm and intelligent battery backup.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Pinout

ISL12008
(8 LD SOIC)
TOP VIEW



Ordering Information

PART NUMBER (Note)	PART MARKING	V_{DD} RANGE (V)	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL12008IB8Z	12008 IBZ	2.7 to 5.5	-40 to +85	8 Ld SOIC	M8.15
ISL12008IB8Z-T*	12008 IBZ	2.7 to 5.5	-40 to +85	8 Ld SOIC	M8.15

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

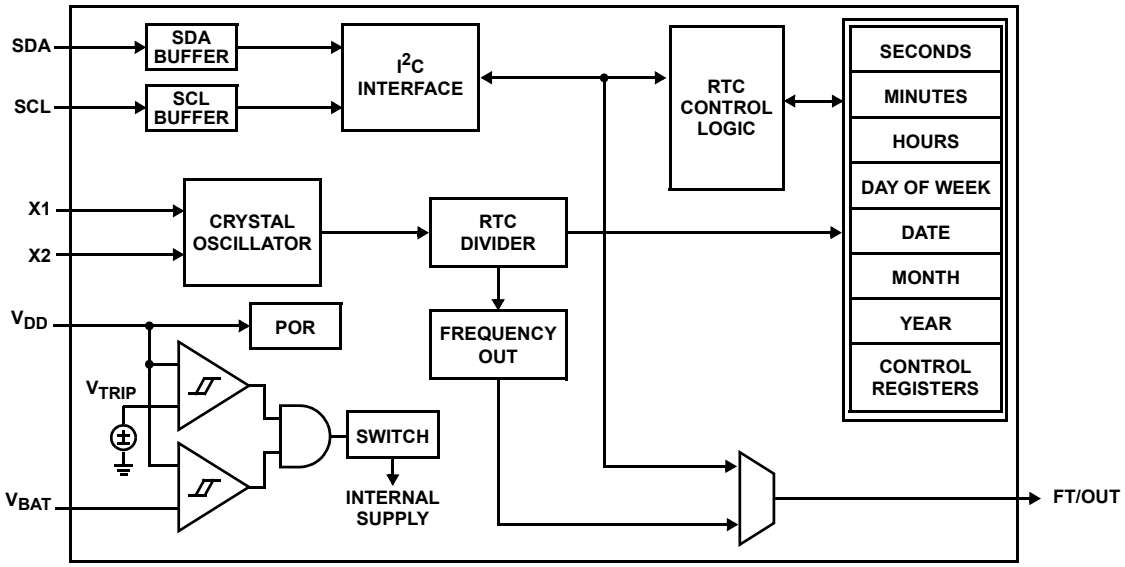
Features

- **Pin Compatible to ST M41T00S and Maxim DS1340**
- **Functionality Equivalent to ST M41T00S and Maxim DS1340**
- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes, Seconds and Sub-seconds
  - Day of the Week, Day, Month, and Year
- 512Hz Frequency Outputs for On-Chip Crystal Compensation
- Software Alarm
  - Settable to the Second, Minute, Hour, Day of the Week, Day, or Month
- Automatic Low-Drop Battery Switch for Longest Backup Life
- Power Failure Detection
- Battery ReSeal™ for Long Shelf Life
- I^2C Bus™
  - 400kHz Data Transfer Rate
- 800nA Battery Supply Current
- Small Package Option
  - 8 Ld SOIC
- Pb-Free (RoHS Compliant)

Applications

- Utility Meters
- HVAC Equipment
- Audio/Video Components
- Set-Top Box/Television
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- POS Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Home Appliances
- Computer Products
- Other Industrial/Medical/Automotive

Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	X1	The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X1 can also be driven directly from a 32.768kHz source.
2	X2	The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
3	V_{BAT}	This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin should be tied to ground if not used.
4	GND	Ground
5	SDA	Serial Data (SDA) is a bidirectional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs.
6	SCL	The Serial Clock (SCL) input is used to clock all serial data into and out of the device.
7	FT/OUT	512Hz Frequency Output or digital output pin. The function is set via the configuration register. This pin is open drain and requires an external pull-up resistor.
8	V_{DD}	Power supply

Absolute Maximum Ratings

Voltage on V_{DD}, V_{BAT}, SCL, SDA, and FT/OUT Pins
(Respect to GND). . . . . -0.5V to 6.5V
Voltage on X1 and X2 Pins
(Respect to GND)
V_{DD} Mode. . . . . -0.5V to V_{DD} + 0.5
V_{BAT} Mode . . . . . -0.5V to V_{BAT} + 0.5

Thermal Information

Thermal Resistance (Typical, Note 1) . . . . . θ_{JA} (°C/W)
8 Lead SOIC 115
Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

DC Operating Characteristics – RTC

Temperature = -40°C to +85°C. Recommended Operating Conditions, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 8)	TYP (Note 5)	MAX (Note 8)	UNITS	NOTES
V_{DD}	Main Power Supply		2.7		5.5	V	
V_{BAT}	Battery Supply Voltage		1.8		5.5	V	
I_{DD1}	Supply Current	V_{DD} = 5V		2.8	6	µA	2, 3
		V_{DD} = 3V		1.6	4	µA	
I_{DD2}	Supply Current With I²C Active	V_{DD} = 5V		40	120	µA	2, 3
I_{DD3}	Supply Current (Low Power Mode)	V_{DD} = 5V, LPMODE = 1		2.3	5	µA	2
I_{BAT}	Battery Supply Current	V_{BAT} = 3V, +25°C		800	950	nA	2
I_{LI}	Input Leakage Current on SCL		-1	0.1	+1	µA	
I_{LO}	I/O Leakage Current on SDA		-1	0.1	+1	µA	
V_{TRIP}	V_{BAT} Mode Threshold		2.3	2.6	2.9	V	
$V_{TRIPHYS}$	V_{TRIP} Hysteresis			36		mV	6
V_{BATHYS}	V_{BAT} Hysteresis			53		mV	6
FT/OUT							
V_{OL}	Output Low Voltage	V_{DD} = 5V I_{OL} = 3mA		0.02	0.4	V	
		V_{DD} = 2.7V I_{OL} = 1mA		0.02	0.4	V	

Power-Down Timing

Temperature = -40°C to +85°C. Recommended Operating Conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 8)	TYP (Note 5)	MAX (Note 8)	UNITS	NOTES
$V_{DD\ SR-}$	V_{DD} Negative Slewrate				5	V/ms	4

Serial Interface Specifications

Recommended Operating Conditions. Unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP (Note 5)	MAX (Note 8)	UNITS	NOTES
SERIAL INTERFACE SPECS							
V_{IL}	SDA and SCL Input Buffer LOW Voltage		-0.3		0.3 x V_{DD}	V	
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		0.7 x V_{DD}		V_{DD} + 0.3	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.05 x V_{DD}		V	6, 7
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA		0	0.02	0.4	V	
Cpin	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF	6, 7

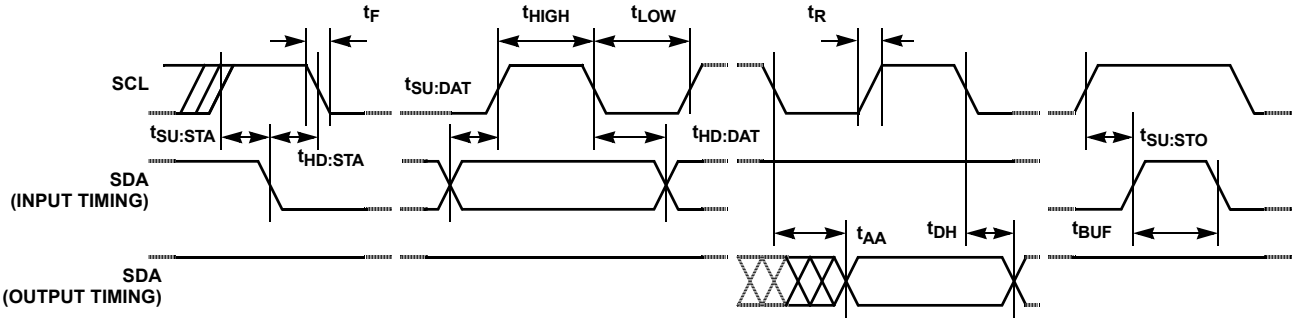
Serial Interface Specifications Recommended Operating Conditions. Unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP (Note 5)	MAX (Note 8)	UNITS	NOTES
f_{SCL}	SCL Frequency				400	kHz	
t_{IN}	Pulse width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns	
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.			900	ns	
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.	1300			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing.	1300			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing.	600			ns	
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}.	600			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}.	600			ns	
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}.	100			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.	20		900	ns	
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}.	600			ns	
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}.	600			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window.	0			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}	20 + 0.1 x Cb		300	ns	6, 7
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}	20 + 0.1 x Cb		300	ns	6, 7
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF	6, 7
Rpu	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ to~2.5kΩ. For Cb = 40pF, max is about 15kΩ to ~20kΩ.	1			kΩ	6, 7

NOTES:

2. FT/OUT inactive.
3. LPMODE = 0 (default).
4. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
5. Typical values are for T = +25°C and 3.3V supply voltage.
6. Limits should be considered typical and are not production tested.
7. These are I²C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SDA vs SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Typical Performance Curves

Temperature is +25°C, unless otherwise specified.

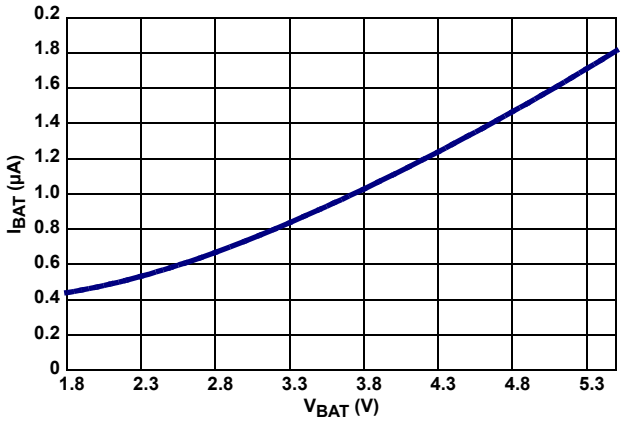


FIGURE 1. I_{BAT} vs V_{BAT}

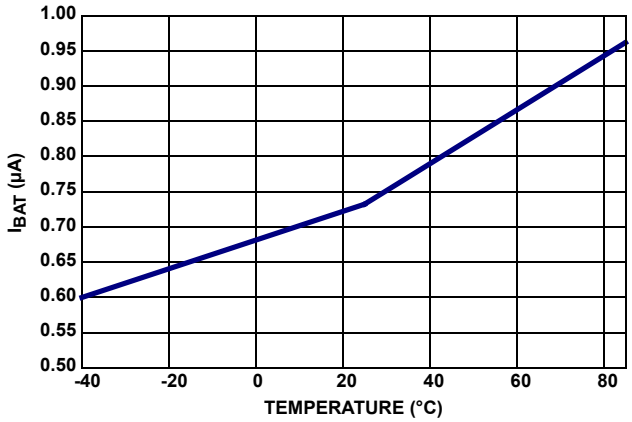


FIGURE 2. I_{BAT} vs TEMPERATURE AT V_{BAT} = 3V

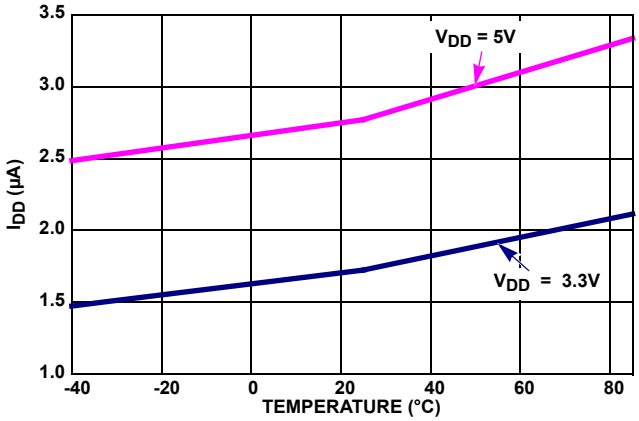


FIGURE 3. I_{DD1} vs TEMPERATURE

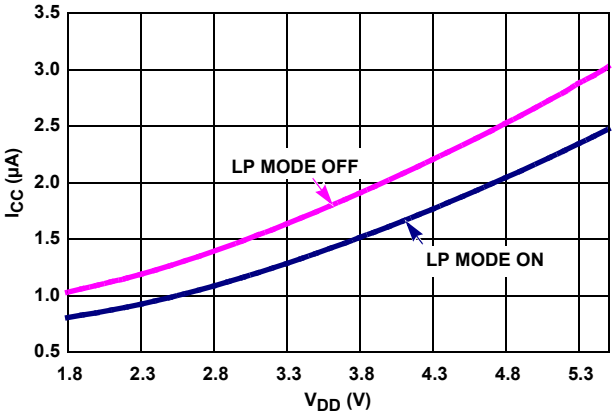


FIGURE 4. I_{DD1} vs V_{DD} WITH LPMODE ON AND OFF

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 5V

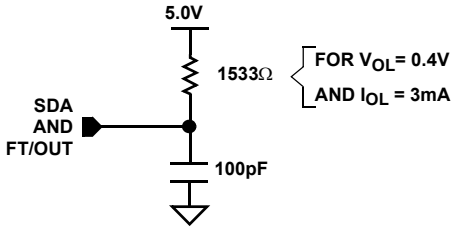


FIGURE 5. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 5.0V

General Description

The ISL12008 device is a low power real time clock with timing and crystal compensation, clock/calendar, power fail indicator, software alarm, and intelligent battery backup switching.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, seconds, and sub-seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

The ISL12008's powerful alarm can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register.

The device also offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or super capacitor with automatic switchover from V_{DD} to V_{BAT}. The entire ISL12008 device is fully operational from 2.7V to 5.5V and the clock/calendar portion of the device remains fully operational down to 1.8V in battery mode.

Pin Descriptions

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the ISL12008 to supply a timebase for the real time clock. Internal compensation circuitry provides high accuracy over the operating temperature range from -40°C to +85°C. This oscillator compensation network can be used to calibrate the crystal timing accuracy over-temperature either during

manufacturing or with an external temperature sensor and microcontroller for active compensation (see Figure 6).

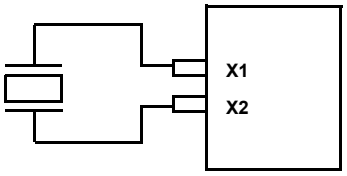


FIGURE 6. RECOMMENDED CRYSTAL CONNECTION

V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin can be connected to a battery, a super capacitor or tied to ground if not used.

FT/OUT (512Hz Frequency Output/Logic Output)

This dual function pin can be used as a 512Hz frequency output pin for on-chip crystal compensation or a simple digital output control via I²C. The FT/OUT mode is selected via the OUT and FT control bits of the control/status register (address 07h). This pin is an open drain output requires the use of a pull-up resistor.

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the V_{BAT} pin is activated to minimize power consumption.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I²C bus speeds. It is disabled when the backup power supply on the VBAT pin is activated.

V_{DD}, GND

Chip power supply and ground pins. The device will operate with a power supply from 2.7V to 5.5VDC. A 0.1µF decoupling capacitor is recommended on the V_{DD} pin to ground.

Functional Description

Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power the ISL12008 for up to 10 years. Another option is to use a super capacitor for applications where V_{DD} is interrupted for up to a month. See “Application Section” on page 16 for more information.

Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

Condition 1:

$V_{DD} < V_{BAT} - V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} < V_{TRIP}$
where $V_{TRIP} \approx 2.6V$

Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The ISL12008 device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

Condition 1:

$V_{DD} > V_{BAT} + V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} > V_{TRIP} + V_{TRIPHYS}$
where $V_{TRIPHYS} \approx 30mV$

These power control situations are illustrated in Figures 7 and 8.

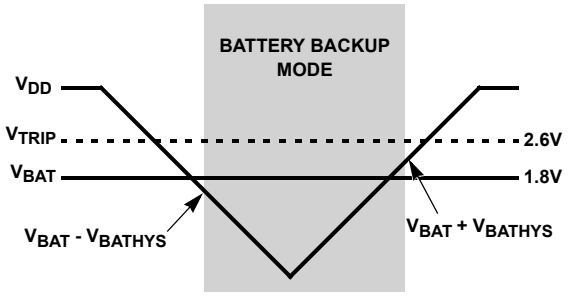


FIGURE 7. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$

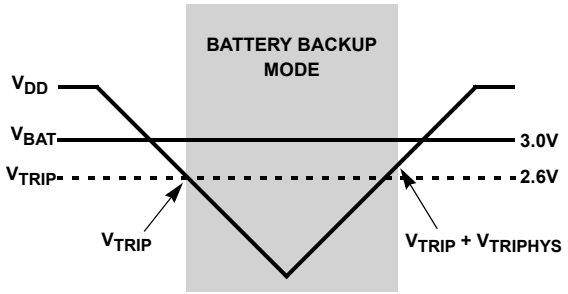


FIGURE 8. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$

The I2C bus is deactivated in battery backup mode to provide lower power. Aside from this, all RTC functions are operational during battery backup mode. Except for SCL and SDA, all the inputs and outputs of the ISL12008 are active during battery backup mode unless disabled via the control register.

Power Failure Detection

The ISL12008 provides a Real Time Clock Failure Bit (RTCF, address 0Bh) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both V_{DD} and V_{BAT}).

Low Power Mode

The normal power switching of the ISL12008 is designed to switch into battery backup mode only if the V_{DD} power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode. Another mode, called Low Power Mode, is available to allow direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below V_{TRIP}. Since the additional monitoring of V_{DD} vs V_{TRIP} is no longer needed, that circuitry is shut down and less power is used while operating from V_{DD}. Power savings are typically 600nA at V_{DD} = 5V. Low Power Mode is activated via the LPMODE bit (address 08h, bit 5) in the control and status registers.

Low Power Mode is useful in systems where V_{DD} is normally higher than V_{BAT} at all times. The device will switch from V_{DD} to V_{BAT} when V_{DD} drops below V_{BAT}, with about 50mV of hysteresis to prevent any switchback of V_{DD} after switchover. In a system with a V_{DD} = 5V and backup lithium battery of V_{BAT} = 3V, Low Power Mode can be used. However, it is not recommended to use Low Power Mode in a system with V_{DD} = 3.3V ±10%, $V_{BAT} \geq 3.0V$, and when there is a finite I-R voltage drop in the V_{DD} line.

InterSeal™ and ReSeal™ Battery Saver

The ISL12008 has the InterSeal Battery Saver, which prevents initial battery current drain before it is first used. For example, battery-backed RTCs are commonly packaged on a board with a battery connected. In order to preserve battery life, the ISL12008 will not draw any power from the battery source until after the device is first powered up from the V_{DD} source. Thereafter, the device will switchover to battery backup mode whenever V_{DD} power is lost.

The ISL12008 has the ReSeal function, which allows the device to enter into the InterSeal Battery Saver mode after manufacture testing for board functionality. To use the ReSeal function, simply set RESEAL bit to “1” (address 0Bh) after the testing is completed. It will enable the InterSeal Battery Saver mode and prevents battery current drain before it is first used.

Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of sub-second, second, minute, hour, day of week, date, month, and year. The RTC has leap-year correction, and corrects for months having fewer than 31 days. The RTC hours is in 24-hour format only. When the ISL12008 powers up after the loss of both V_{DD} and V_{BAT}, the RTC will not begin incrementing until at least one byte is written to the RTC registers. The sub-second register will increment after power up but it will not casue the other RTC registers to incremnent until at least one byte is written to the RTC registers.

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal’s nominal frequency. For example, a ~20ppm frequency deviation translates into an accuracy of ~1 minute per month. These parameters are available from the crystal manufacturer. The ISL12008 provides on-chip crystal compensation networks to adjust load capacitance to tune oscillator frequency from -97.0695ppm to +206.139ppm. For more detailed information. See “Application Section” on page 16.

I2C Serial Interface

The ISL12008 has an I2C serial bus interface that provides access to the control and status registers and the user SRAM. The I2C serial interface is compatible with other industry I2C serial bus protocols using a bidirectional data signal (SDA) and a clock signal (SCL).

Oscillator Compensation

The ISL12008 provides the option of timing correction due to temperature variation of the crystal oscillator for either manufacturing calibration or active calibration. The total possible compensation is typically -97.0695ppm to +206.139ppm. Two compensation mechanisms that are available are as follows:

1. An analog trimming (ATR) register that can be used to adjust individual on-chip digital capacitors for oscillator capacitance trimming. The individual digital capacitor is selectable from a range of 4.5pF to 20.25pF (based upon 32.758kHz). This translates to a calculated compensation of approximately -34ppm to +80ppm (see ATR description on page 16).
2. A digital trimming register (DTR) that can be used to adjust the timing counter by -63.0696ppm to +126.139ppm (see DTR description on page 16).

Also provided is the ability to adjust the crystal capacitance when the ISL12008 switches from V_{DD} to battery backup mode. See “Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})” on page 7.

Register Descriptions

The battery-backed registers are accessible following a slave byte of “1101000x” and reads or writes to addresses [00h:1Fh]. The defined addresses and default values are described in Table 1. Address 12h to 1Eh are not used. Reads or writes to 12h to 1Eh will not affect operation of the device but should be avoided.

REGISTER ACCESS

The contents of address 00h to 07h can be modified by performing a byte or a page write operation directly to any register address. In a page write operation to address 00h to 07h, the address will wrap around from 07h to 00h. All the other registers (Address 08h to 11h and 1Fh) can be modified by performing a byte write operation.

The registers are divided into 3 sections. These are:

1. Real Time Clock (8 bytes): Address 00h to 06h, and 1Fh. Address 1Fh is Sub-Second register and it is a read-only.
2. Control and Status (4 bytes): Address 07h to 0Bh.
3. Alarm (6 bytes): Address 0Ch to 11h.

There are no addresses above 1Fh.

Address 12h to 1Eh are not used. Reads or writes to 12h to 1Eh will not affect operation of the device but should be avoided.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read operation latches all clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register. In a sequential read, the address will warp around at address 07h to 00h; therefore, please use byte read operation to read the registers after address 07h.

Real Time Clock Registers

TABLE 1. REGISTER MEMORY MAP

ADDR.	SECTION	REG NAME	BIT								REG	
			7	6	5	4	3	2	1	0	RTC RANGE	DEFAULT
00h	RTC	SC	ST	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h		MN	OF	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0 to 59	80h
02h		HR	CEB	CB	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h		DW	0	0	0	0	0	DW12	DW11	DW10	1 to 7	00h
04h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	00h
05h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	00h
06h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
07h	Control	DTR	OUT	FT	DTR5	DTR4	DTR3	DTR2	DTR1	DTR0	N/A	80h
08h		INT	0	ALME	LPMODE	0	0	0	0	0	N/A	00h
09h		OF	OF	0	0	0	0	0	0	0	N/A	80h
0Ah		ATR	BMATR1	BMATR0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0	N/A	00h
0Bh	Status	SR	ARST	XSTOP	RESEAL	0	0	ALM	BAT	RTCF	N/A	03h
0Ch	Alarm0	SCA	ESCA	ASC22	ASC21	ASC20	ASC13	ASC12	ASC11	ASC10	00 to 59	00h
0Dh		MNA	EMNA	AMN22	AMN21	AMN20	AMN13	AMN12	AMN11	AMN10	00 to 59	00h
0Eh		HRA	EHRA	0	AHR21	AHR20	AHR13	AHR12	AHR11	AHR10	0 to 23	00h
0Fh		DTA	EDTA	0	ADT21	ADT20	ADT13	ADT12	ADT11	ADT10	1 to 31	00h
10h		MOA	EMOA	0	0	AMO20	AMO13	AMO12	AMO11	AMO10	1 to 12	00h
11h		DWA	EDWA	0	0	0	0	ADW12	ADW11	ADW10	1 to 7	00h
1Fh (Read-Only)	RTC	SS	SS23	SS22	SS21	SS20	SS13	SS12	SS11	SS10	0 to 99	00h

NOTE: 0 = must be set to‘0’

Addresses [00h to 06h, and 1Fh]

RTC REGISTERS (SC, MN, HR, DW, DT, MO, YR, SS)

These registers depict BCD representations of the time. As such, SC (Seconds, address 00h) and MN (Minutes, address 01h) range from 0 to 59, HR (Hour, address 02h) is in 24-hour mode with a range from 0 to 23, DW (Day of the Week, address 03h) is 1 to 7, DT (Date, address 04h) is 1 to 31, MO (Month, address 05h) is 1 to 12, YR (Year, address 06h) is 0 to 99, and SS (Sub-Seconds/Hundredths of Seconds, address 1Fh) is 0 to 99. The default for all the time keeping bits are set to “0” at power up.

Bit D7 of SC register contain the crystal enable/disable bit (ST). Setting ST to “1” will disable the crystal from oscillating and stop the counting in RTC register. When the ST bit is set to “1”, it will casue the OF bit to set to “1” due to no crystal oscillation on the X1 pin. The ST bit is set to “0” on power-up for normal operation.

Bit D7 of MN register contain the Oscillator Fail Indicator bit (OF). This bit is set to a “1” when the X1 pin has no oscillation. This bit can be reset when the X1 has crystal oscillation and a write to “0”. This bit can only be written as “0” and not as a “1”. The OF bit is set to “1” at power-up from a complete power down (V_{DD} and V_{BAT} are removed). Address 9, bit 7 is also used as the OF bit for DS1340 compatibility, and the two OF bits are interchangable.

Bits D6 and D7 of HR register (century/hours register) contain the century enable bit (CEB) and the century bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0', CB will not toggle.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 1-2-3-4-5-6-7-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The ISL12008 does not correct for the leap year in the year 2100.

Control and Status Registers

Addresses [07h to 0Bh]

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register, Analog Trimming and Digital Trimming Registers.

Status Register (SR) [Address 0Bh]

The Status Register is located in the memory map at address 0Bh. This is a volatile register that provides either control or status of RTC failure, battery mode, alarm trigger, crystal oscillator status, ReSeal™ and auto reset of status bits.

TABLE 2. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
0Bh	ARST	0	RESEAL	0	0	ALM	BAT	RTCF
Default	0	0	0	0	0	0	1	1

REAL TIME CLOCK FAIL BIT (RTCF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL12008 internally) when the device powers up after having lost all power to the device (both V_{DD} and V_{BAT} go to 0V). The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. On power-up after a total power failure, all registers are set to their default states and the clock will not increment until at least one byte is written to the clock register. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

BATTERY BIT (BAT)

This bit is set to a “1” when the device enters battery backup mode. This bit can be reset either manually by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

ALARM BIT (ALM)

These bits announce if the alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

NOTE: An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

ReSeal (RESEAL)

The ReSeal™ enables the device enter into the InterSeal™ Battery Saver mode after manufacture testing for board functionality. The factory default setting of this bit is “0”. The RESEAL must be set to “0” to enable the battery function during normal operation or full functional testing. To use the ReSeal function, simply set RESEAL bit to “1” after the testing is completed. It will enable the InterSeal™ Battery Saver mode and prevents battery current drain before it is first used.

AUTO RESET ENABLE BIT (ARST)

This bit enables/disables the automatic reset of the BAT, ALM and TMR status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the respective status register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the BAT and ALM bits.

Interrupt Control Register (INT) [Address 08h]

TABLE 3. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
08h	0	ALME	LPMODE	0	0	0	0	0
Default	0	0	0	0	0	0	0	0

LOW POWER MODE BIT (LPMODE)

This bit enables/disables low power mode. With LPMODE = “0”, the device will be in normal mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$ and $V_{DD} < V_{TRIP}$. With LPMODE = “1”, the device will be in low power mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$. There is a supply current saving of about 600nA when using LPMODE = “1” with V_{DD} = 5V. (See “Typical Performance Curves” on page 6: I_{DD} vs V_{CC} with LPMODE ON and OFF.)

ALARM ENABLE BIT (ALME)

This bit enables/disables the alarm function. When the ALME bit is set to “1”, the alarm function is enabled. When the ALME bit is cleared to “0”, the alarm function is disabled. ALME bit is set to “0” at power-up.

Oscillator Fail Register (OF) [Address 09h]

TABLE 4. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
09h	OF	0	0	0	0	0	0	0
Default	1	0	0	0	0	0	0	0

OSCILLATOR FAIL BIT (OF)

This bit is set to a “1” when the X1 pin has no oscillation. This bit can be reset when the X1 has crystal oscillation and a write to “0”. This bit can only be written as “0” and not as a “1”. The OF bit is set to “1” at power up from a complete power down (V_{DD} and V_{BAT} are removed). Address 1, bit 7 is also used as the OF bit for M41T00S compatibility, and the two OF bits are interchangable.

Analog Trimming Register (ATR) [Address 0Ah]

TABLE 5. ANALOG TRIMMING REGISTER (ATR)

ADDR	7	6	5	4	3	2	1	0
0Ah	BMATR1	BMATR0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Default	0	0	0	0	0	0	0	0

ANALOG TRIMMING REGISTER (ATR<5:0>)

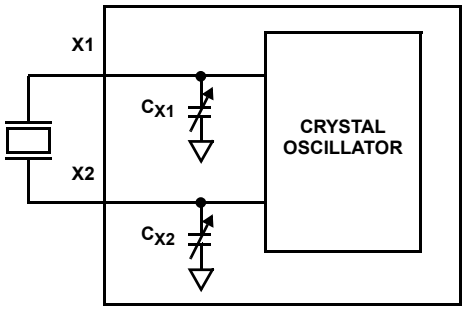


FIGURE 9. DIAGRAM OF ATR

Six analog trimming bits, **ATR0** to **ATR5**, are provided in order to adjust the on-chip load capacitance value for frequency compensation of the RTC. Each bit has a different weight for capacitance adjustment. For example, using a Citizen CFS-206 crystal with different ATR bit combinations provides an estimated ppm adjustment range from -34ppm to +80ppm to the nominal frequency compensation. The combination of analog and digital trimming can give up to -97.0695ppm to +206.139ppm of total adjustment.

The effective on-chip series load capacitance, C_{LOAD}, ranges from 9pF to 40.5pF with a mid-scale value of 12.5pF (default). C_{LOAD} is changed via two digitally controlled capacitors, C_{X1} and C_{X2}, connected from the X1 and X2 pins to ground (see Figure 9). The value of C_{X1} and C_{X2} are given in Equation 1:

$$C_X = (16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9)pF \quad \text{(EQ. 1)}$$

The effective series load capacitance is the combination of C_{X1} and C_{X2} in Equation 2:

$$C_{LOAD} = \frac{1}{\left(\frac{1}{C_{X1}} + \frac{1}{C_{X2}}\right)} \quad \text{(EQ. 2)}$$

$$C_{LOAD} = \left(\frac{16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9}{2}\right)pF$$

where b5 is ATR5 bit, b4 is ATR4 bit, b3 is ATR3 bit, b2 is ATR1 bit, and b0 is ATR0 bit.

For example, C_{LOAD}(ATR = 000000b [0d]) = 12.5pF, C_{LOAD} (ATR = 100000b [32d]) = 4.5pF and C_{LOAD} (ATR = 011111b [31d]) = 20.25pF. The entire range for the series combination of load capacitance goes from 4.5pF to 20.25pF in 0.25pF steps. Note that these are typical values.

BATTERY MODE ATR SELECTION (BMATR <1:0>)

Since the accuracy of the crystal oscillator is dependent on the V_{DD}/V_{BAT} operation, the ISL12008 provides the capability to adjust the capacitance between V_{DD} and V_{BAT} when the device switches between power sources.

BMATR1	BMATR0	DELTA CAPACITANCE (C_{BAT} TO C_{VDD})
0	0	0pF
0	1	-0.5pF (≈ +2ppm)
1	0	+0.5pF (≈ -2ppm)
1	1	+1pF (≈ -4ppm)

Digital Trimming Register (DTR) [Address 07h]

TABLE 6. DIGITAL TRIMMING REGISTER (DTR)

ADDR	7	6	5	4	3	2	1	0
07h	OUT	FT	DTR5	DTR4	DTR3	DTR2	DTR1	DTR0
Default	0	0	0	0	0	0	0	0

DIGITAL TRIMMING REGISTER (DTR<5:0>)

Six digital trimming bits, **DTR0** to **DTR5**, are provided to adjust the average number of counts per second and average the ppm error to achieve better accuracy.

- DTR5 is a sign bit. DTR5 = “0” means frequency compensation is < 0. DTR5 = “1” means frequency compensation is > 0.
- DTR<4:0> are scale bits. With DTR5 = “0”, DTR<4:0> gives -2.0345ppm adjustment per step. With DTR5 = “1”, DTR<4:0> gives +4.0690ppm adjustment per step.

A range from -63.0696ppm to +126.139ppm can be represented by using these 3 bits.

For example, with DTR = 11111, the digital adjustment is (1111b[15d]*4.0690) = +126.139ppm. With DTR = 01111, the digital adjustment is (-(1111b[15d]*2.0345)) = -63.0696ppm.

512HZ FREQUENCY OUTPUT ENABLE BIT (FT)

This bit enables/disables the 512Hz frequency output on the FT/OUT pin. When the FT is set to “1”, the FT/OUT pin outputs the 512Hz frequency, regardless of the Digital Output selection bit (OUT). The 512Hz frequency output is used for crystal compensation with ATR and DTR registers. When the FT is set to “0”, the 512Hz frequency is disabled and the function of FT/OUT pin is selected by the Digital Output selection bit (OUT). The FT bit is set to “0” on power-up. The FT/OUT pin is an open drain output requires the use of a pull-up resistor.

DIGITAL OUTPUT SELECTION BIT (OUT)

This bit selects the output status of the FT/OUT. 512Hz Frequency Output Enable bit (FT) must be set to “0” (disable) for OUT to take effect on FT/OUT pin. When the OUT is set to “1” and FT is set to “0”, the FT/OUT pin is set to logic level

high. The FT/OUT pin voltage level is controlled by the voltage of the pull-up resistor on FT/OUT pin. When the OUT is set to “0” and FT is set to “0”, the FT/OUT pin is set to logic level low. The voltage level of FT/OUT is set to VOL level. The OUT bit is set to “1” on power-up. The FT/OUT pin is an open drain output requires the use of a pull-up resistor.

Alarm Registers

Addresses [0Ch to 11h]

The Alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year and sub-second, and the register order for Alarm register is not a 100% matching to the RTC register so please take caution on programming the alarm function.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

To clear an alarm, the ALM status bit must be set to “0” with a write. Note that if the ARST bit is set to “1” (address 0Bh, bit 7), the ALM bit will automatically be cleared when the status register is read.

I2C Serial Interface

The ISL12008 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12008 operates as a slave device in all applications.

All communication over the I2C bus is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 10). On power-up of the ISL12008, the SDA pin is in the input mode.

All I2C bus operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12008 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 10). A START condition is ignored during the power-up sequence.

All I2C bus operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 10). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting 8 bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the 8 bits of data (see Figure 11).

The ISL12008 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL12008 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

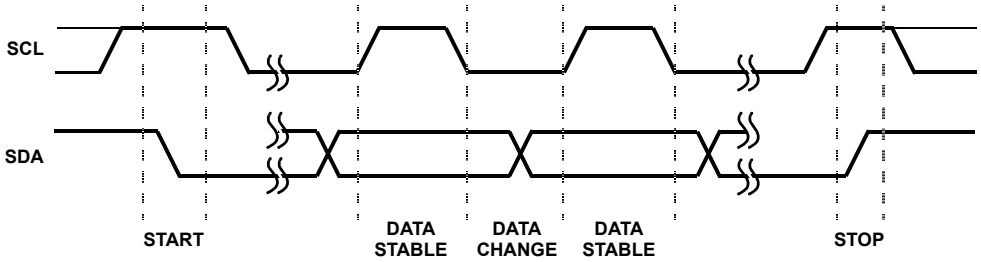


FIGURE 10. VALID DATA CHANGES, START, AND STOP CONDITIONS

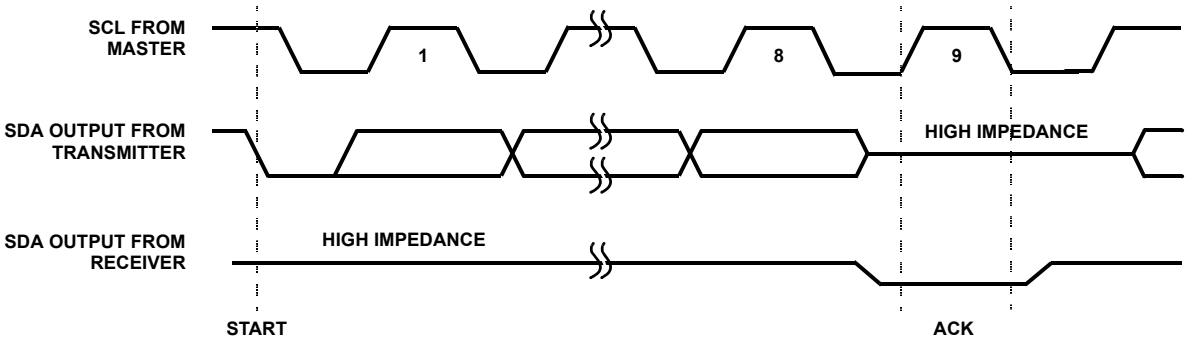


FIGURE 11. ACKNOWLEDGE RESPONSE FROM RECEIVER

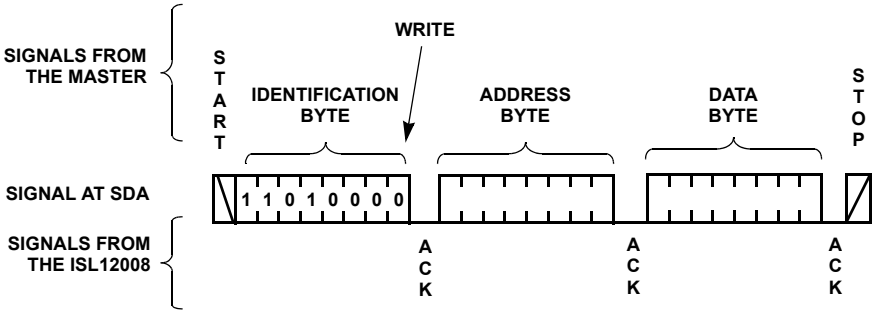


FIGURE 12. BYTE WRITE SEQUENCE

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifiers. These bits are “1101000”.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a “1”, then a read operation is selected (refer to Figure 16). When this R/$\overline{W}$ bit is a “0” , then a write operation (refer to Figure 12).

After loading the entire Slave Address Byte from the SDA bus, the ISL12008 compares the Slave bit and device select bits with “1101000”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 0h, so a current address read of the CCR array starts at address 0h. When required, as part of a random read, the master must supply the 1 Word Address Bytes, as shown in Figure 14.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Clock/Control Registers, the slave byte must be “1101000x” in both places.

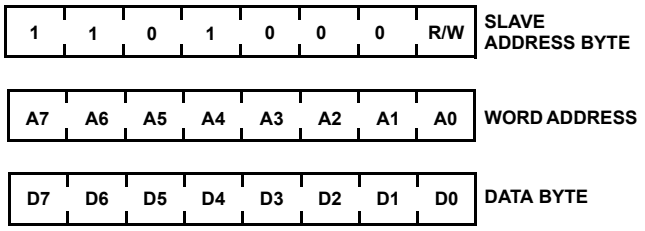


FIGURE 13. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12008 responds with an ACK. After received the STOP condition, the ISL12008 writes the data into the memory, then the I2C bus enters a standby state. After a Write operation, the internal address pointer will remain at the address for the last data byte written.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 14). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL12008 responds with an ACK. Then the ISL12008 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 14).

The Data Bytes are from the memory location indicated by an internal address pointer. This internal address pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte.

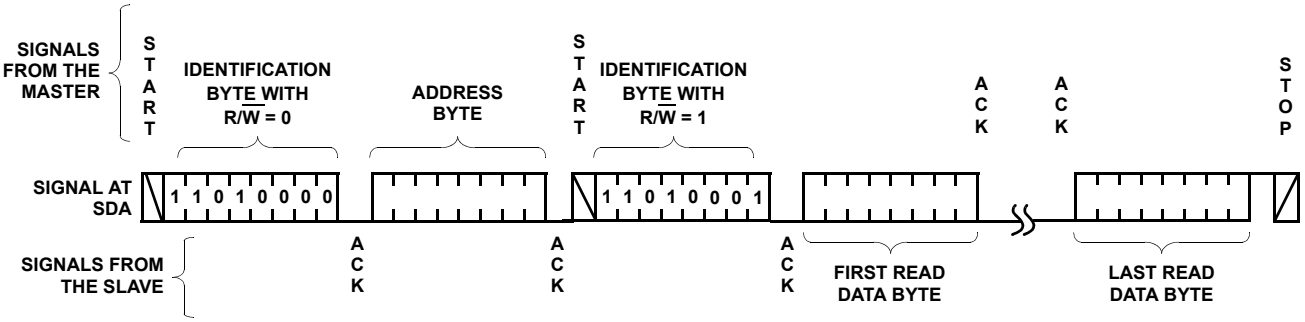


FIGURE 14. READ SEQUENCE

Application Section

Oscillator Crystal Requirements

The ISL12008 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 7 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL12008 if their specifications are very similar to the devices listed. The crystal should have a required parallel load capacitance of 12.5pF and an equivalent series resistance of less than 50k. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through-hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

TABLE 7. SUGGESTED SURFACE MOUNT CRYSTALS

MANUFACTURER	PART NUMBER
Citizen	CM200S
Epson	MC-405, MC-406
Raltron	RSM-200S
SaRonix	32S12
Ecliptek	ECPSM29T-32.768K
ECS	ECX-306
Fox	FSM-327

Crystal Oscillator Frequency Adjustment

The ISL12008 device contains circuitry for adjusting the frequency of the crystal oscillator. This circuitry can be used to trim oscillator initial accuracy as well as adjust the frequency to compensate for temperature changes.

The Analog Trimming Register (ATR) is used to adjust the load capacitance seen by the crystal. There are 6 bits of ATR control, with linear capacitance increments available for adjustment. Since the ATR adjustment is essentially "pulling" the frequency of the oscillator, the resulting frequency changes will not be linear with incremental capacitance changes. The equations (which govern pulling) show that lower capacitor values of ATR adjustment will provide larger increments. Also, the higher values of ATR adjustment will produce smaller incremental frequency changes. The range afforded by the ATR adjustment with a typical surface mount crystal is typically -34ppm to +80ppm around the ATR = 0 default setting because of this property. The user should note this when using the ATR for calibration. The temperature drift of the capacitance used in the ATR control is extremely low, so this feature can be used for temperature compensation with good accuracy.

In addition to the analog compensation afforded by the adjustable load capacitance, a digital compensation feature is available for the ISL12008. There are 6 bits known as the Digital Trimming Register (DTR). The range provided is -63.0695ppm to +126.139ppm. DTR operates by adding or skipping pulses in the clock counter. It is very useful for coarse adjustments of frequency drift over temperature or extending the adjustment range available with the ATR register.

Initial accuracy is best adjusted by enabling the 512Hz frequency output (using the FT bit, address 08h bit 6), and monitoring the FT/OUT pin with a calibrated frequency counter. The gating time should be set long enough to ensure accuracy to at least 1ppm. To calculate the ppm on the measured 512Hz, simply divide the measured 512Hz by 512, then subtract 1 from the result and mulitple by 1,000,000. Please see Equation 3 for the formula:

$$ppm = (FT/512 - 1)*1E6 \quad \text{(EQ. 3)}$$

The ATR should be set to the center position, or 00000b, to begin with. Once the initial measurement is made, then the ATR register can be changed to adjust the frequency. Note for a range of 0 to 31 for the ATR register will increased capacitance and lower the frequency with 31 for the maximum negative correction, and for a range of 32 to 63 for the ATR register will decreased capacitance and increase the frequency with 32 for the maximum positive correction. If the initial measurement shows the frequency is far off, it will be necessary to use the DTR register to do a coarse adjustment. Note that most all crystals will have tight enough initial accuracy at room temperature so that a small ATR register adjustment should be all that is needed.

Temperature Compensation

The ATR and DTR controls can be combined to provide crystal drift temperature compensation. The typical 32.768kHz crystal has a drift characteristic that is similar to that shown in Figure 15. There is a turnover temperature (T_0) where the drift is very near zero. The shape is parabolic as it varies with the square of the difference between the actual temperature and the turnover temperature.

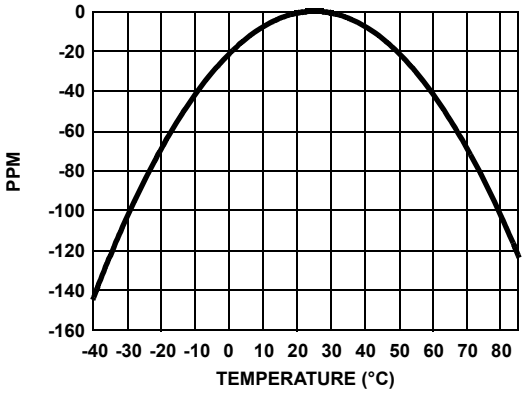


FIGURE 15. RTC CRYSTAL TEMPERATURE DRIFT

If full industrial temperature compensation is desired in an ISL12008 circuit, then both the DTR and ATR registers will

need to be utilized (total correction range = -97.0695ppm to +206.139ppm).

A system to implement temperature compensation would consist of the ISL12008, a temperature sensor, and a microcontroller. These devices may already be in the system so the function will just be a matter of implementing software and performing some calculations. Fairly accurate temperature compensation can be implemented just by using the crystal manufacturer's specifications for the turnover temperature T_0 and the drift coefficient (β). The formula for calculating the oscillator adjustment necessary is Equation 4:

$$\text{Adjustment(ppm)} = (T - T_0)^2 * \beta \quad \text{(EQ. 4)}$$

Once the temperature curve for a crystal is established, then the designer should decide at what discrete temperatures the compensation will change. Since drift is higher at extreme temperatures, the compensation may not be needed until the temperature is greater than +20°C from T_0.

A sample curve of the ATR setting vs Frequency Adjustment for the ISL12008 and a typical RTC crystal is given in Figure 16. This curve may vary with different crystals, so it is good practice to evaluate a given crystal in an ISL12008 circuit before establishing the adjustment values.

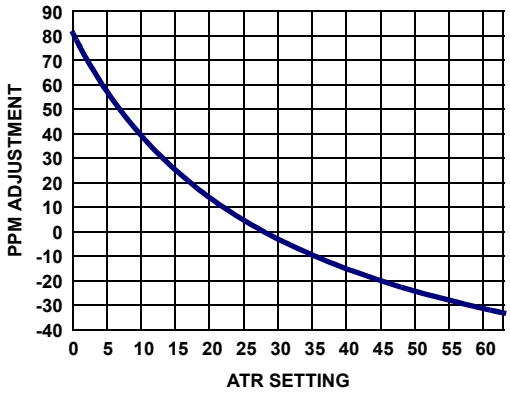


FIGURE 16. ATR SETTING vs OSCILLATOR FREQUENCY ADJUSTMENT

This curve is then used to figure what ATR and DTR settings are used for compensation. The results would be placed in a lookup table for the microcontroller to access.

Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies (such as 32.768kHz) are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 17 shows a suggested layout for the ISL12008 device using a surface mount crystal. Two main precautions should be followed:

1. Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.
2. Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

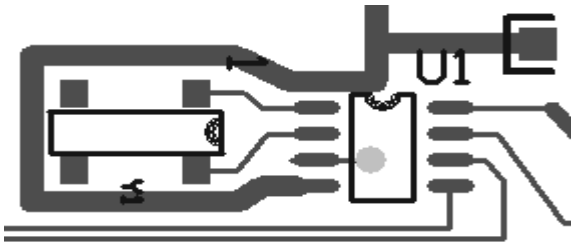


FIGURE 17. SUGGESTED LAYOUT FOR ISL12008 AND CRYSTAL

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the FT/OUT pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{BAT} and V_{CC} pins can be treated as a ground, and should be routed around the crystal.

Super Capacitor Backup

The ISL12008 device provides a VBAT pin which is used for a battery backup input. A super capacitor can be used as an alternative to a battery in cases where shorter backup times are required. Since the battery backup supply current required by the ISL12008 is extremely low, it is possible to get months of backup operation using a super capacitor. Typical capacitor values are a few µF to 1F or more, depending on the application.

If backup is only needed for a few minutes, then a small inexpensive electrolytic capacitor can be used. For extended periods, a low leakage, high capacity super capacitor is the best choice. These devices are available from such vendors as Panasonic and Murata. The main specifications include working voltage and leakage current. If the application is for charging the capacitor from a +5V ±5% supply with a signal diode, then the voltage on the capacitor can vary from ~4.5V to slightly over 5.0V. A capacitor with a rated WV of 5.0V may have a reduced lifetime if the supply voltage is slightly high. The leakage current should be as small as possible. For example, a super capacitor should be specified with leakage of well below 1µA. A standard electrolytic capacitor with DC leakage current in the microamps will have a severely shortened backup time.

Following are some examples with equations to assist with calculating backup times and required capacitance for the ISL12008 device. The backup supply current plays a major part in these equations, and a typical value was chosen for example purposes. For a robust design, a margin of 30% should be included to cover supply current and capacitance tolerances over the results of the calculations. Even more

margin should be included if periods of very warm temperature operation are expected.

EXAMPLE 1: CALCULATING BACKUP TIME GIVEN VOLTAGES AND CAPACITOR VALUE

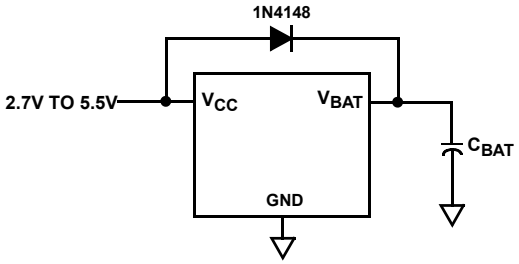


FIGURE 18. SUPERCAPACITOR CHARGING CIRCUIT

In Figure 18, use C_{BAT} = 0.47F and V_{CC} = 5V. With V_{CC} = 5V, the voltage at V_{BAT} will approach 4.7V as the diode turns off completely. The ISL12008 is specified to operate down to V_{BAT} = 1.8V. The capacitance charge/discharge in Equation 5 is used to estimate the total backup time as follows:

$$I = C_{BAT}*dV/dT \quad \text{(EQ. 5)}$$

Rearranging gives Equation 6:

$$dT = C_{BAT}*dV/I_{TOT} \text{ to solve for backup time.} \quad \text{(EQ. 6)}$$

C_{BAT} is the backup capacitance and dV is the change in voltage from fully charged to loss of operation. Note that I_{TOT} is the total of the supply current of the ISL12008 (I_{BAT}) plus the leakage current of the capacitor and the diode, I_{LKG}. In these calculations, I_{LKG} is assumed to be extremely small and will be ignored. If an application requires extended operation at temperatures over +50°C, these leakages will increase and hence reduce backup time.

Note that I_{BAT} changes with V_{BAT} almost linearly (see “Typical Performance Curves” on page 6). This allows us to make an approximation of I_{BAT}, using a value midway between the two endpoints. The typical linear equation for I_{BAT} vs V_{BAT} is shown in Equation 7:

$$I_{BAT} = 1.031E\text{-}7*(V_{BAT}) + 1.036E\text{-}7A \quad \text{(EQ. 7)}$$

Using Equation 7 to solve for the average current given 2 voltage points gives Equation 8:

$$I_{BATAVG} = 5.155E\text{-}8*(V_{BAT2} + V_{BAT1}) + 1.036E\text{-}7A \quad \text{(EQ. 8)}$$

Combining with Equation 6 gives the equation for backup time in Equation 9:

$$t_{BACKUP} = C_{BAT}*(V_{BAT2} - V_{BAT1}) / (I_{BATAVG} + I_{LKG}) \text{ seconds} \quad \text{(EQ. 9)}$$

where:

C_{BAT} = 0.47F

V_{BAT2} = 4.7V

V_{BAT1} = 1.8V

I_{LKG} = 0 (assumed minimal)

Solving Equation 8 for this example (I_{BATAVG} = 4.387E-7A) yields Equation 10:

$$t_{BACKUP} = 0.47 \bullet (2.9)/4.38E-7 = 3.107E6s \quad \text{(EQ. 10)}$$

Since there are 86,400 seconds in a day, this corresponds to 35.96 days. If the 30% tolerance is included for capacitor and supply current tolerances, then worst case backup time would be represented in Equation 11:

$$C_{BAT} = 0.70 \bullet 35.96 = 25.2 \text{ days} \quad \text{(EQ. 11)}$$

EXAMPLE 2: CALCULATING A CAPACITOR VALUE FOR A GIVEN BACKUP TIME

Referring to Figure 18 again, the capacitor value needs to be calculated to give 2 months (60 days) of backup time, given V_{CC} = 5.0V. As in Example 1, the V_{BAT} voltage will vary from 4.7V down to 1.8V. We will need to rearrange Equation 6 to solve for capacitance in Equation 12:

$$C_{BAT} = dT*I/dV \quad \text{(EQ. 12)}$$

Using the terms previously described, Equation 12 becomes Equation 13:

$$C_{BAT} = t_{BACKUP}*(I_{BATAVG} + I_{LKG})/(V_{BAT2} - V_{BAT1}) \quad \text{(EQ. 13)}$$

where:

t_{BACKUP} = 60 days*86,400 sec/day = 5.18 E6 seconds

I_{BATAVG} = 4.387 E-7A (same as Example 1)

I_{LKG} = 0 (assumed)

V_{BAT2} = 4.7V

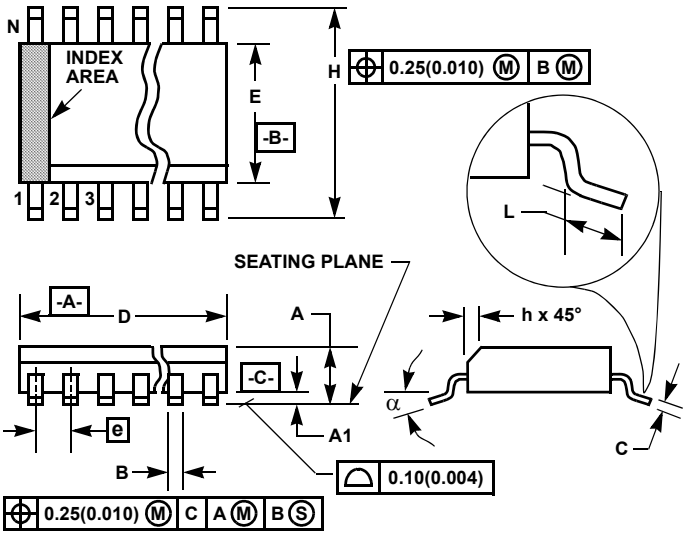
V_{BAT1} = 1.8VSolving gives

C_{BAT} = 5.18 E6*(4.387 E-7)/(2.9) = 0.784F

If the 30% tolerance is included for tolerances, then worst case capacitor value would be:

$$C_{BAT} = 1.3 \bullet 0.784 = 1.02F \quad \text{(EQ. 14)}$$

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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