Multichannel ISM Band FSK/GFSK/OOK/GOOK/ASK Transmitter

ADF7012

FEATURES

Single-chip, low power UHF transmitter
75 MHz to 1 GHz frequency operation
Multichannel operation using fractional-N PLL
2.3 V to 3.6 V operation
On-board regulator
Programmable output power
−16 dBm to +14 dBm, 0.4 dB steps
Data rates: dc to 179.2 kbps
Low current consumption
868 MHz, 10 dBm, 21 mA
433 MHz, 10 dBm, 17 mA
315 MHz, 0 dBm, 10 mA
Programmable low battery voltage indicator
24-lead TSSOP

APPLICATIONS

Low cost wireless data transfer
Security systems
RF remote controls
Wireless metering
Secure keyless entry

GENERAL DESCRIPTION

The ADF7012 is a low power FSK/GFSK/OOK/GOOK/ASK UHF transmitter designed for short-range devices (SRDs). The output power, output channels, deviation frequency, and modulation type are programmable by using four, 32-bit registers.

The fractional-N PLL and VCO with external inductor enable the user to select any frequency in the 75 MHz to 1 GHz band. The fast lock times of the fractional-N PLL make the ADF7012 suitable in fast frequency hopping systems. The fine frequency deviations available and PLL phase noise performance facilitates narrow-band operation.

There are five selectable modulation schemes: binary frequency shift keying (FSK), Gaussian frequency shift keying (GFSK), binary on-off keying (OOK), Gaussian on-off keying (GOOK), and amplitude shift keying (ASK). In the compensation register, the output can be moved in <1 ppm steps so that indirect compensation for frequency error in the crystal reference can be made.

A simple 3-wire interface controls the registers. In power-down, the part has a typical quiescent current of <0.1 μA.

FUNCTIONAL BLOCK DIAGRAM

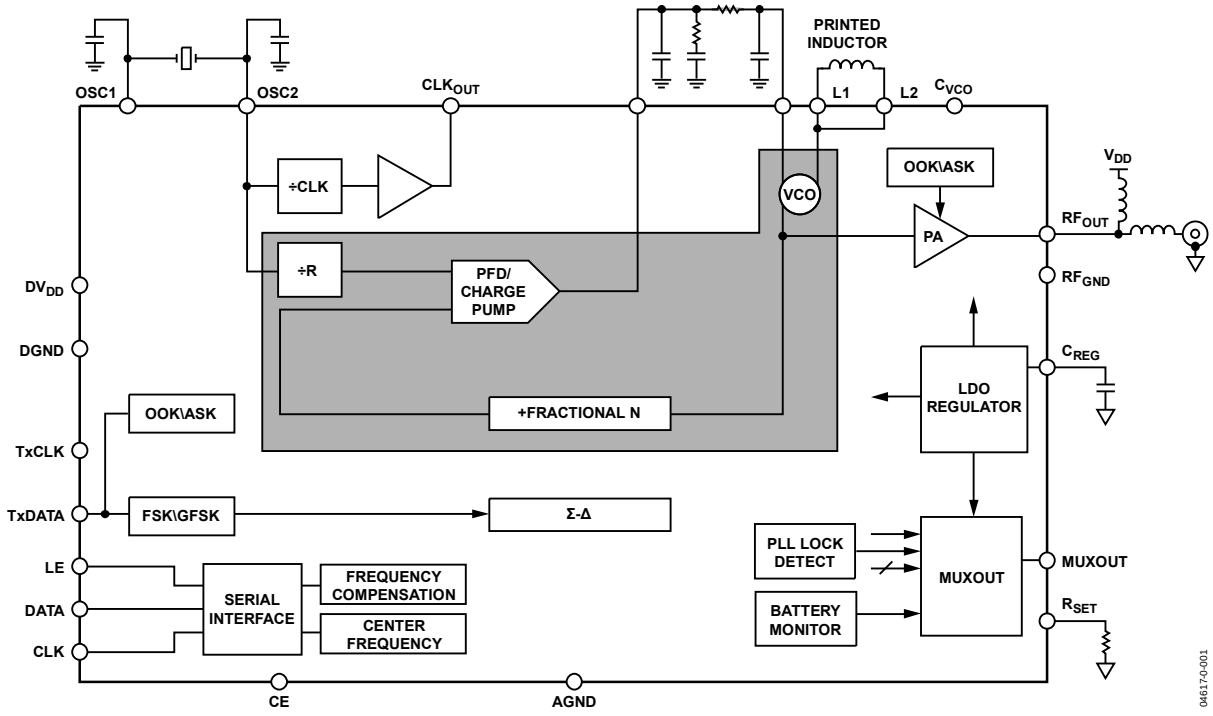

Figure 1.

Rev. A

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Timing Characteristics ... 5
Absolute Maximum Ratings ... 6
Transistor Count ... 6
ESD Caution ... 6
Pin Configuration and Function Descriptions ... 7
Typical Performance Characteristics ... 8
315 MHz ... 8
433 MHz ... 9
868 MHz ... 10
Circuit Description ... 12
PLL Operation ... 12
Crystal Oscillator ... 12
Crystal Compensation Register ... 12
Clock Out Circuit ... 12
Loop Filter ... 13
Voltage-Controlled Oscillator (VCO) ... 13
Voltage Regulators ... 13
FSK Modulation ... 13
GFSK Modulation ... 14
Power Amplifier ... 14
GOOK Modulation ... 15
Output Divider ... 16
MUXOUT Modes ... 16
Theory of Operation ... 17
Choosing the External Inductor Value ... 17
Choosing the Crystal/PFD Value ... 17
Tips on Designing the Loop Filter ... 18
PA Matching ... 18
Transmit Protocol and Coding Considerations ... 18
Application Examples ... 19
315 MHz Operation ... 20
433 MHz Operation ... 21
868 MHz Operation ... 22
915 MHz Operation ... 23
Register Descriptions ... 24
Register 0: R Register ... 24
Register 1: N-Counter Latch ... 25
Register 2: Modulation Register ... 26
Register 3: Function Register ... 27
Outline Dimensions ... 28
Ordering Guide ... 28

REVISION HISTORY

6/09—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Table 4 ... 7
Changes to Crystal Oscillator Section ... 12
Changes to Loop Filter Section ... 13
Changes to GFSK Modulation Section ... 14
Changes to Choosing the External Inductor Value Section ... 17
Changes to Component Values—Crystal: 3.6864 MHz ... 20
Changes to Component Values—Crystal: 4.9152 MHz ... 21
Changes to Component Values—Crystal: 4.9152 MHz ... 22
Changes to Component Values—Crystal: 10 MHz ... 23
Added Register Headings Throughout ... 24
Changes to Ordering Guide ... 28

10/04—Revision 0: Initial Version

SPECIFICATIONS

DV_{DD} = 2.3 V – 3.6 V; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Operating temperature range is −40°C to +85°C.

Table 1.

Parameter	B Version	Unit	Conditions/Comments
RF OUTPUT CHARACTERISTICS			
Operating Frequency	75/1000	MHz min/max	VCO range adjustable using external inductor; divide-by-2, -4, -8 options may be required
Phase Frequency Detector	$F_{RF}/128$	Hz min	
MODULATION PARAMETERS			
Data Rate FSK/GFSK	179.2	kbps	Using 1 MHz loop bandwidth
Data Rate ASK/OOK	64	Kbps	Based on US FCC 15.247 specifications for ACP; higher data rates are achievable depending on local regulations
Deviation FSK/GFSK	$PFD/2^{14}$	Hz min	For example, 10 MHz PFD – deviation min = ±610 Hz
	$511 \times PFD/2^{14}$	Hz max	For example, 10 MHz PFD – deviation max = ±311.7 kHz
GFSK BT	0.5	typ	
ASK Modulation Depth	25	dB max	
OOK Feedthrough (PA Off)	−40	dBm typ	$F_{RF} = F_{VCO}$
	−80	dBm typ	$F_{RF} = F_{VCO}/2$
POWER AMPLIFIER PARAMETERS			
Maximum Power Setting, DV_{DD} = 3.6 V	14	dBm	F_{RF} = 915 MHz, PA is matched into 50 Ω
Maximum Power Setting, DV_{DD} = 3.0 V	13.5	dBm	F_{RF} = 915 MHz, PA is matched into 50 Ω
Maximum Power Setting, DV_{DD} = 2.3 V	12.5	dBm	F_{RF} = 915 MHz, PA is matched into 50 Ω
Maximum Power Setting, DV_{DD} = 3.6 V	14.5	dBm	F_{RF} = 433 MHz, PA is matched into 50 Ω
Maximum Power Setting, DV_{DD} = 3.0 V	14	dBm	F_{RF} = 433 MHz, PA is matched into 50 Ω
Maximum Power Setting, DV_{DD} = 2.3 V	13	dBm	F_{RF} = 433 MHz, PA is matched into 50 Ω
PA Programmability	0.4	dB typ	PA output = −20 dBm to +13 dBm
POWER SUPPLIES			
DV_{DD}	2.3/3.6	V min/V max	
Current Consumption			
315 MHz, 0 dBm/5 dBm	8/14	mA typ	DV_{DD} = 3.0 V, PA is matched into 50 Ω, I_{VCO} = min
433 MHz, 0 dBm/10 dBm	10/18	mA typ	
868 MHz, 0 dBm/10 dBm/14 dBm	14/21/32	mA typ	
915 MHz, 0 dBm/10 dBm/14 dBm	16/24/35	mA typ	
VCO Current Consumption	1/8	mA min/max	VCO current consumption is programmable
Crystal Oscillator Current Consumption	190	µA typ	
Regulator Current Consumption	280	µA typ	
Power-Down Current	0.1/1	µA typ/max	
REFERENCE INPUT			
Crystal Reference Frequency	3.4/26	MHz min/max	
Single-Ended Reference Frequency	3.4/26	MHz min/max	
Crystal Power-On Time 3.4 MHz/26 MHz	1.8/2.2	ms typ	CE to clock enable valid
Single-Ended Input Level	CMOS levels		Refer to the LOGIC INPUTS parameter. Applied OSC 2, oscillator circuit disabled.

Parameter	B Version	Unit	Conditions/Comments
PHASE-LOCKED LOOP PARAMETERS			
VCO Gain			
315 MHz	22	MHz/V typ	VCO divide-by-2 active
433 MHz	24	MHz/V typ	VCO divide-by-2 active
868 MHz	80	MHz/V typ	
915 MHz	88	MHz/V typ	
VCO Tuning Range	0.3/2.0	V min/max	
Spurious (IVCO Min/Max)	−65/−70	dBc	I_{VCO} is programmable
Charge Pump Current			
Setting [00]	0.3	mA typ	Referring to DB[7:6] in Function Register
Setting [01]	0.9	mA typ	Referring to DB[7:6] in Function Register
Setting [10]	1.5	mA typ	Referring to DB[7:6] in Function Register
Setting [11]	2.1	mA typ	Referring to DB[7:6] in Function Register
Phase Noise (In band)[1]			
315 MHz	−85	dBc/Hz typ	PFD = 10 MHz, 5 kHz offset, I_{VCO} = 2 mA
433 MHz	−83	dBc/Hz typ	PFD = 10 MHz, 5 kHz offset, I_{VCO} = 2 mA
868 MHz	−80	dBc/Hz typ	PFD = 10 MHz, 5 kHz offset, I_{VCO} = 3 mA
915 MHz	−80	dBc/Hz typ	PFD = 10 MHz, 5 kHz offset, I_{VCO} = 3 mA
Phase Noise (Out of Band)[1]			
315 MHz	−103	dBc/Hz typ	PFD = 10 MHz, 1 MHz offset, I_{VCO} = 2 mA
433 MHz	−104	dBc/Hz typ	PFD = 10 MHz, 1 MHz offset, I_{VCO} = 2 mA
868 MHz	−115	dBc/Hz typ	PFD = 10 MHz, 1 MHz offset, I_{VCO} = 3 mA
915 MHz	−114	dBc/Hz typ	PFD = 10 MHz, 1 MHz offset, I_{VCO} = 3 mA
Harmonic Content (Second)[2]	−20	dBc typ	$F_{RF} = F_{VCO}$
Harmonic Content (Third)[2]	−30	dBc typ	
Harmonic Content (Others)[2]	−27	dBc typ	
Harmonic Content (Second)[2]	−24	dBc typ	$F_{RF} = F_{VCO}/N$ (where N = 2, 4, 8)
Harmonic Content (Third)[2]	−14	dBc typ	
Harmonic Content (Others)[2]	−19	dBc typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × DV_{DD}	V min	
Input Low Voltage, V_{INL}	0.2 × DV_{DD}	V max	
Input Current, I_{INH}/I_{INL}	±1	µA max	
Input Capacitance, C_{IN}	4.0	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	DV_{DD} − 0.4	V min	CMOS output chosen
Output High Current, I_{OH},	500	µA max	
Output Low Voltage, V_{OL}	0.4	V max	I_{OL} = 500 µA

[1] Measurements made with N_{FRAC} = 2048.
[2] Measurements made without harmonic filter.

TIMING CHARACTERISTICS

DV_{DD} = 3 V ± 10%; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	Data-to-clock setup time
t_3	10	ns min	Data-to-clock hold time
t_4	25	ns min	Clock high duration
t_5	25	ns min	Clock low duration
t_6	10	ns min	Clock-to-LE setup time
t_7	20	ns min	LE pulse width

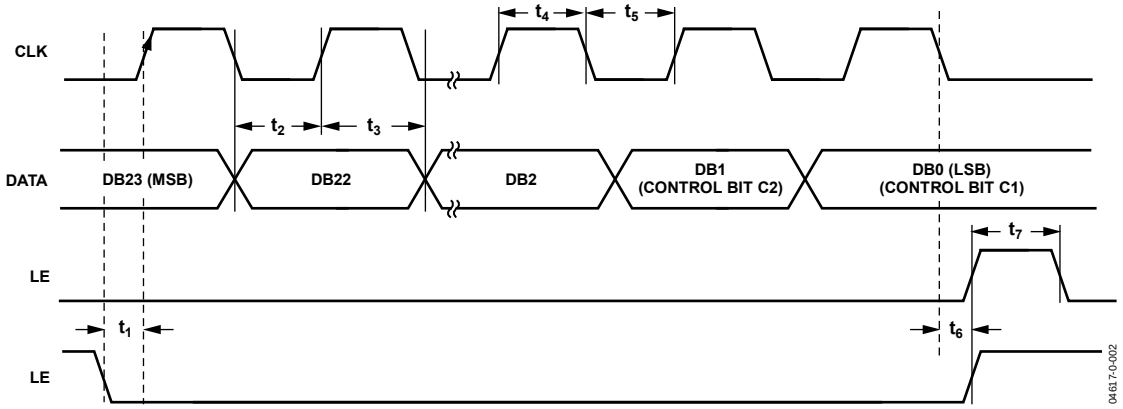


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
DV_{DD} to GND (GND = AGND = DGND = 0 V)	−0.3 V to +3.9 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	150.4°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of 1 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

TRANSISTOR COUNT

35819 (CMOS)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

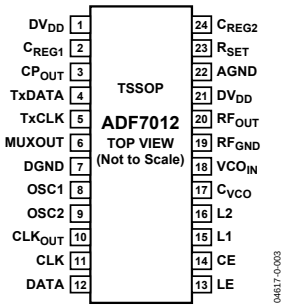


Figure 3. Pin Configuration

Table 4. Pin Functional Descriptions

Pin No.	Mnemonic	Description
1	DV_{DD}	Positive Supply for the Digital Circuitry. This must be between 2.3 V and 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin.
2	C_{REG1}	A 1 µF capacitor should be added at C_{REG} to reduce regulator noise and improve stability. A reduced capacitor improves regulator power-on time, but may cause higher spurious noise.
3	CP_{OUT}	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
4	TxDATA	Digital data to be transmitted is input on this pin.
5	TxCLK	GFSK and GOOK Only. This clock output is used to synchronize microcontroller data to the TxDATA pin of the ADF7012. The clock is provided at the same frequency as the data rate. The microcontroller updates TxDATA on the falling edge of TxCLK. The rising edge of TxCLK is used to sample TxDATA at the midpoint of each bit.
6	MUXOUT	Provides the Lock_Detect Signal. This signal is used to determine if the PLL is locked to the correct frequency. It also provides other signals, such as Regulator_Ready, which is an indicator of the status of the serial interface regulator, and a voltage monitor (see the MUXOUT Modes section for more information).
7	DGND	Ground for Digital Section.
8	OSC1	The reference crystal should be connected between this pin and OSC2.
9	OSC2	The reference crystal should be connected between this pin and OSC1. A TCXO reference may be used, by driving this pin with CMOS levels, and powering down the crystal oscillator bit in software.
10	CLK_{OUT}	A divided-down version of the crystal reference with output driver. The digital clock output may be used to drive several other CMOS inputs, such as a microcontroller clock. The output has a 50:50 mark-space ratio.
11	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This is a high impedance CMOS input.
13	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
14	CE	Chip Enable. Bringing CE low puts the ADF7012 into complete power-down, drawing < 1µA. Register values are lost when CE is low and the part must be reprogrammed once CE is brought high.
15	L1	Connected to external printed or discrete inductor. See Choosing the External Inductor Value for advice on the value of the inductor to be connected between L1 and L2.
16	L2	Connected to external printed or discrete inductor.
17	C_{VCO}	A 22 nF capacitor should be tied between the C_{VCO} and C_{REG2} pins. This line should run underneath the ADF7012. This capacitor is necessary to ensure stable VCO operation.
18	VCO_{IN}	The tuning voltage on this pin determines the output frequency of the voltage controlled oscillator (VCO). The higher the tuning voltage, the higher the output frequency.
19	RF_{GND}	Ground for Output Stage of Transmitter.
20	RF_{OUT}	The modulated signal is available at this pin. Output power levels are from –16 dBm to +12 dBm. The output should be impedance matched using suitable components to the desired load. See the PA Matching section.
21	DV_{DD}	Voltage supply for VCO and PA section. This should have the same supply as DV_{DD} (Pin 1), and should be between 2.3 V and 3.6 V. Place decoupling capacitors to the analog ground plane as close as possible to this pin.
22	AGND	Ground Pin for the RF Analog Circuitry.
23	R_{SET}	External Resistor to set charge pump current and some internal bias currents. Use 3.6 kΩ as default.
24	C_{REG2}	Add a 470 nF capacitor at C_{REG} to reduce regulator noise and improve stability. A reduced capacitor improves regulator power-on time and phase noise, but may have stability issues over the supply and temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

315 MHz

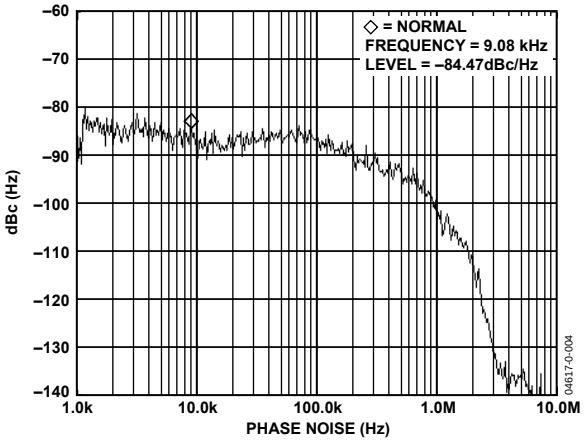


Figure 4. Phase Noise Response—DV_{DD} = 3.0 V, I_{CP} = 0.86 mA I_{VCO} = 2.0 mA, F_{OUT} = 315 MHz, PFD = 3.6864 MHz, PA Bias = 5.5 mA

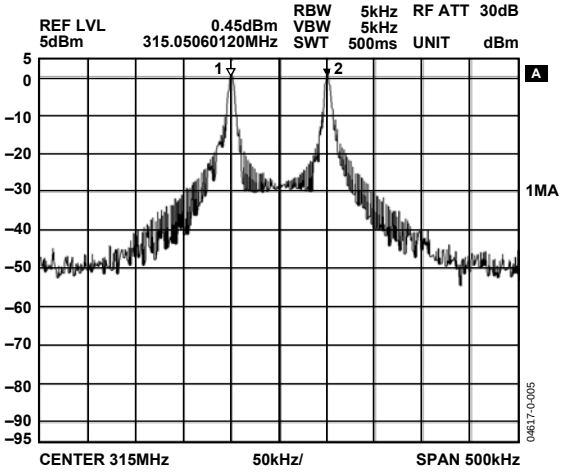


Figure 5. FSK Modulation, Power = 0 dBm, Data Rate = 1 kbps, $F_{DEVIATION}$ = ±50 kHz

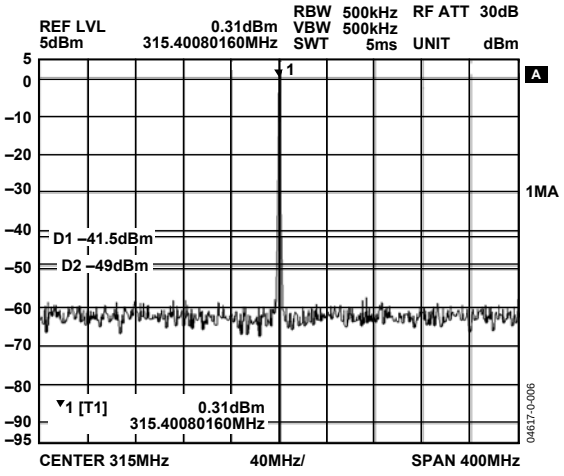


Figure 6. Spurious Components—Meets FCC Specs

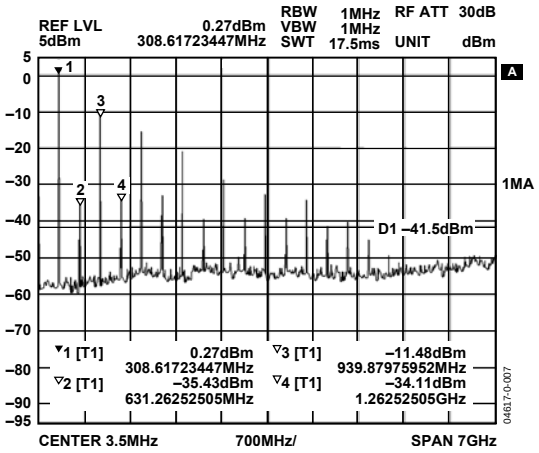


Figure 7. Harmonic Response, RF_{OUT} Matched to 50 Ω, No Filter

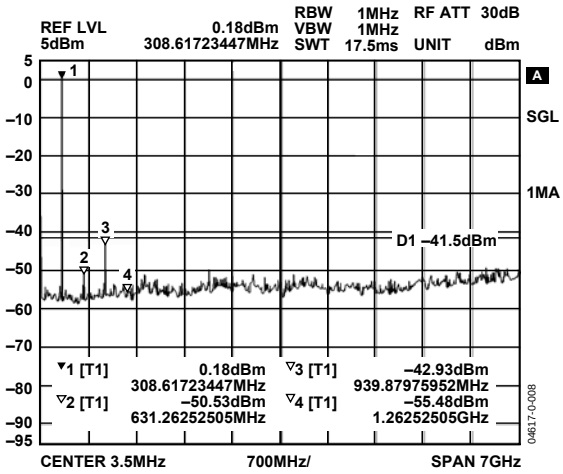


Figure 8. Harmonic Response, Fifth-Order Butterworth Filter

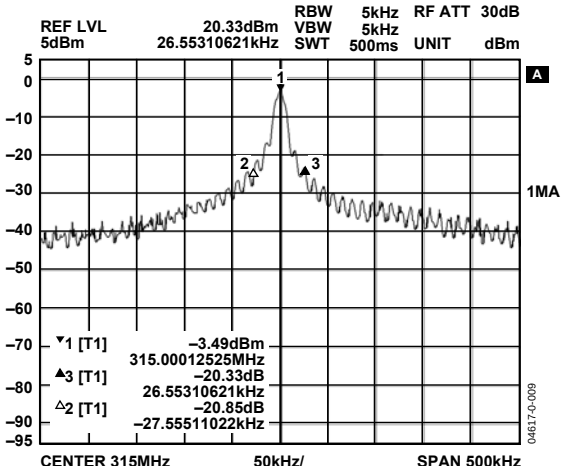


Figure 9. OOK Modulation, Power = 0 dBm, Data Rate = 10 kbps

433 MHz

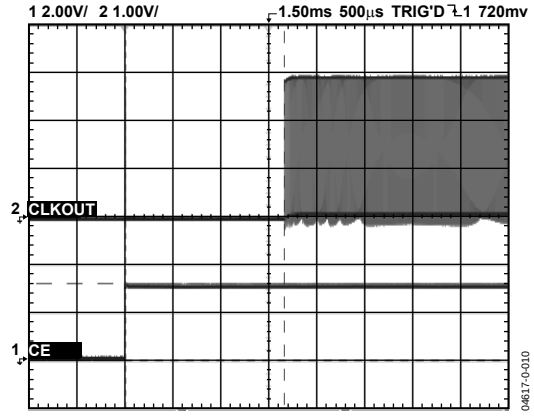


Figure 10. Crystal Power-On Time, 4 MHz, Time = 1.6 ms

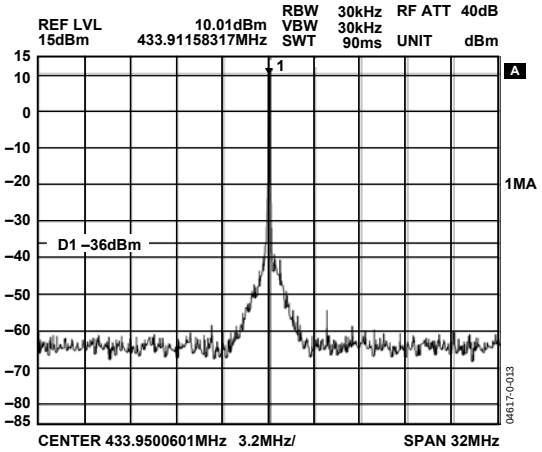


Figure 13. Spurious Components—Meets ETSI Specs

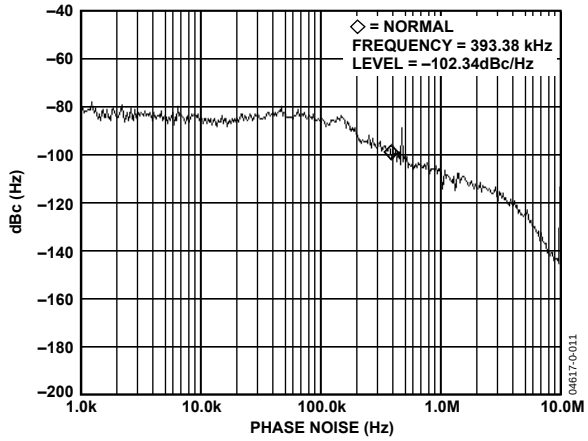


Figure 11. Phase Noise Response—I_{CP} = 2.0 mA, I_{VCO} = 2.0 mA, RF_{OUT} = 433.92 MHz, PFD = 4 MHz, PA Bias = 5.5 mA

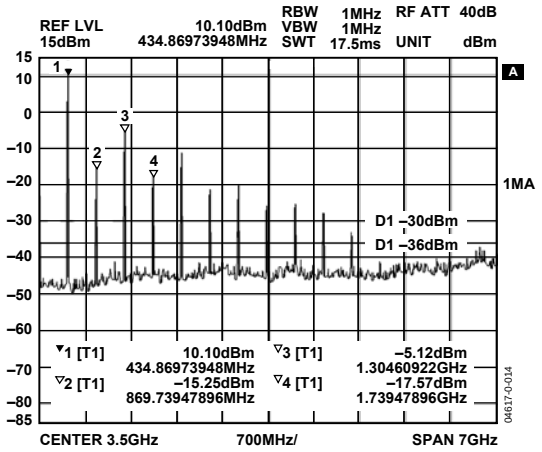


Figure 14. Harmonic Response, RF_{OUT} Matched to 50 Ω, No Filter

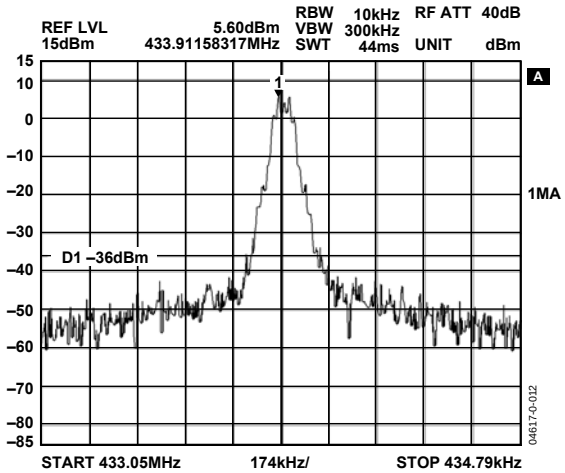


Figure 12. FSK Modulation, Power = 10 dBm, Data Rate = 38.4 kbps, $F_{DEVIATION}$ = ±19.28 kHz

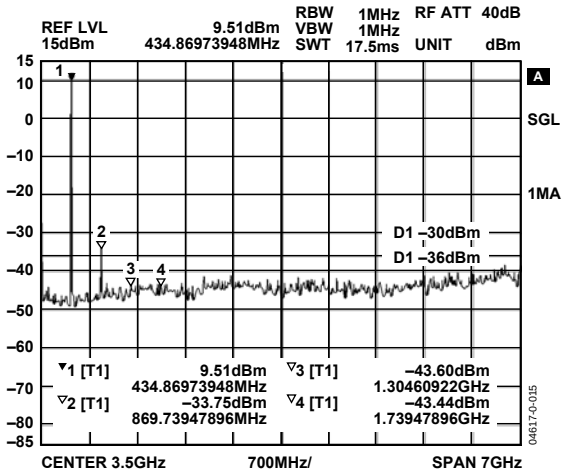


Figure 15. Harmonic Response, Fifth-Order Butterworth Filter

868 MHz

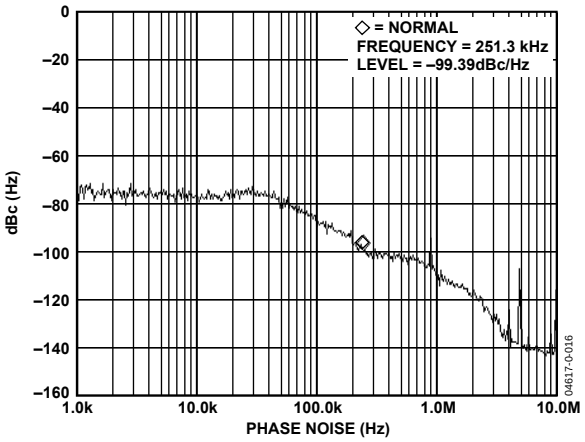


Figure 16. Phase Noise Response—I_{CP} = 2.5 mA, I_{VCO} = 1.44 mA, RF_{OUT} = 868.95 MHz, PFD = 4.9152 MHz, Power = 12.5 dBm, PA Bias = Max

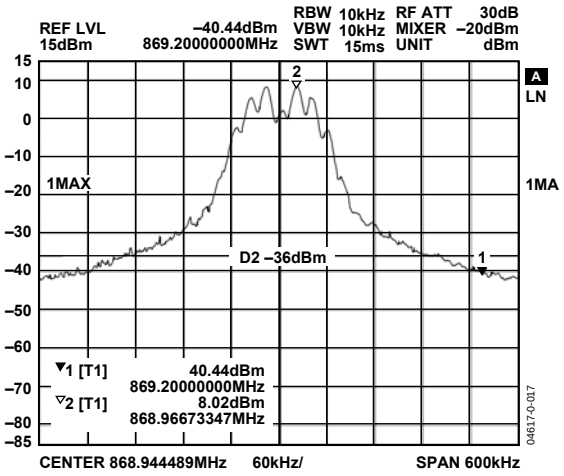


Figure 17. FSK Modulation, Power = 12.5 dBm, Data Rate = 38.4 kbps, $F_{DEVIATION}$ = ±19.2 kHz

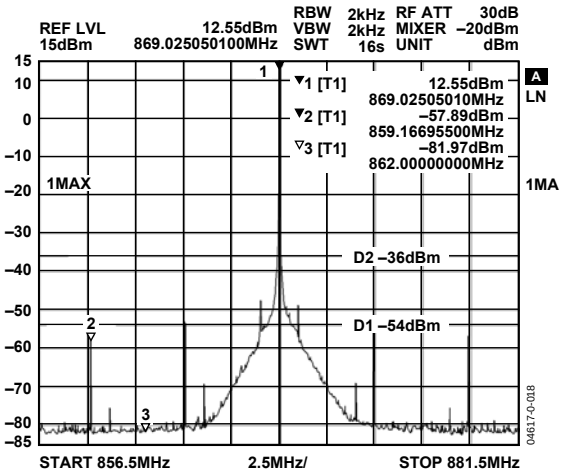


Figure 18. Spurious Components—Meets ETSI Specs

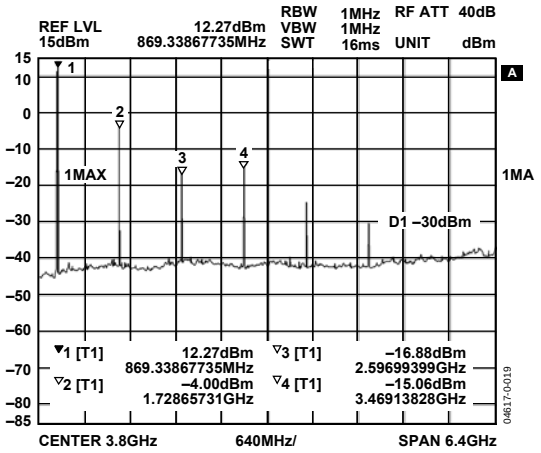


Figure 19. Harmonic Response, RF_{OUT} Matched to 50 Ω, No Filter

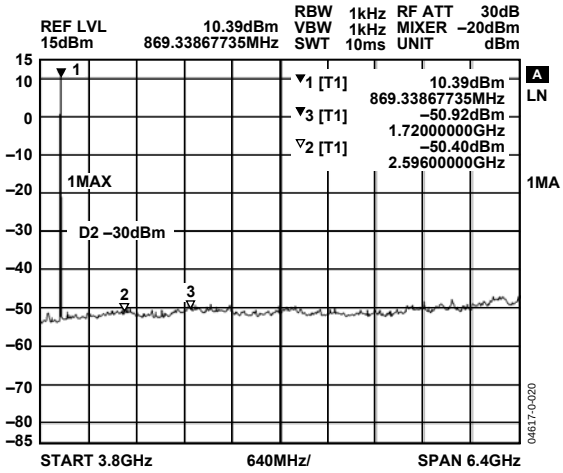


Figure 20. Harmonic Response, Fifth-Order Chebyshev Filter

915 MHz

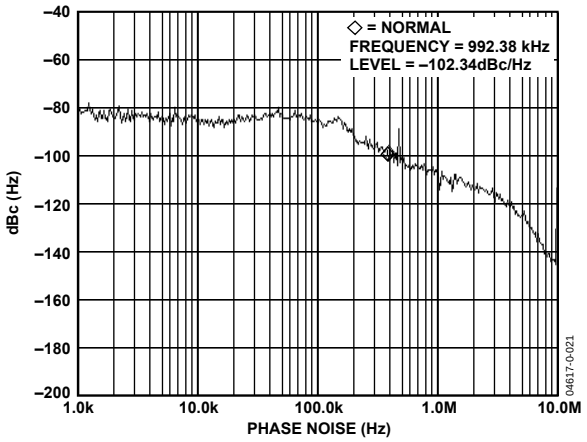


Figure 21. Phase Noise Response—I_{CP} = 1.44 mA, I_{VCO} = 3.0 mA, RF_{OUT} = 915.2 MHz, PFD =10 MHz, Power = 10 dBm, PA Bias = 5.5 mA

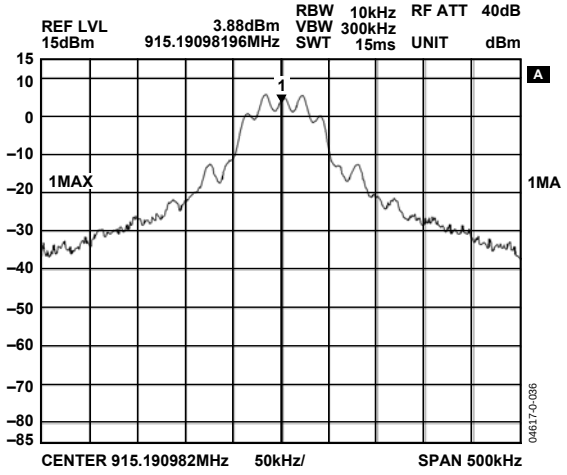


Figure 22. FSK Modulation, Power = 10 dBm, Data Rate = 38.4 kbps, $F_{DEVIATION}$ = ±19.2 kHz

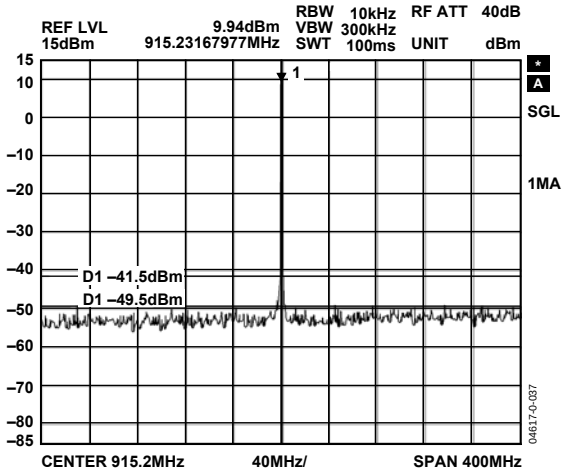


Figure 23. Spurious Components—Meets FCC Specs

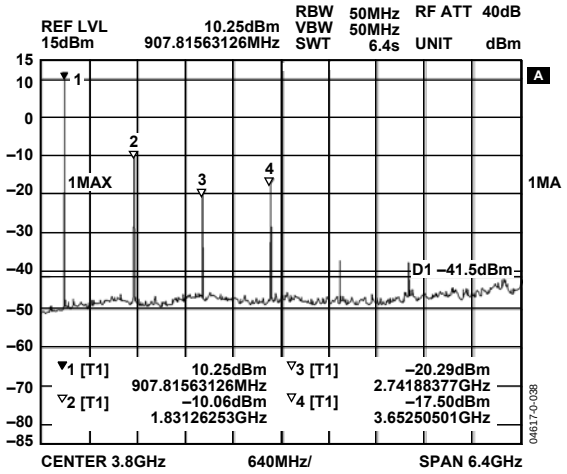


Figure 24. Harmonic Response, RF_{OUT} Matched to 50 Ω, No Filter

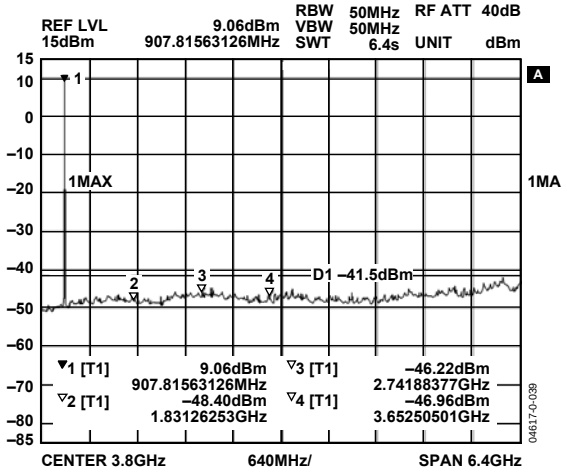


Figure 25. Harmonic Response, Fifth-Order Chebyshev Filter

CIRCUIT DESCRIPTION

PLL OPERATION

A fractional-N PLL allows multiple output frequencies to be generated from a single-reference oscillator (usually a crystal) simply by changing the programmable N value found in the N register. At the phase frequency detector (PFD), the reference is compared to a divided-down version of the output frequency (VCO/N). If VCO/N is too low a frequency, typically the output frequency is lower than desired, and the PFD and charge-pump combination sends additional current pulses to the loop filter. This increases the voltage applied to the input of the VCO. Because the VCO of the ADF7012 has a positive frequency vs. voltage characteristic, any increase in the V_{TUNE} voltage applied to the VCO input increases the output frequency at a rate of kilovolts, the tuning sensitivity of the VCO (MHz/V). At each interval of 1/PFD seconds, a comparison is made at the PFD until the PFD and charge pump eventually force a state of equilibrium in the PLL where PFD frequency = VCO/N. At this point, the PLL can be described as locked.

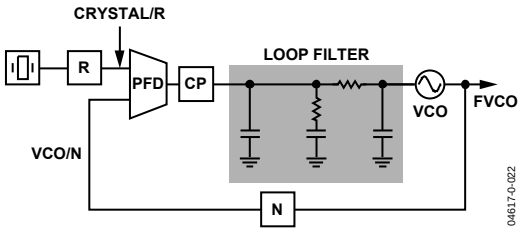


Figure 26. Fractional-N PLL

$$F_{OUT} = \frac{F_{CRYSTAL} \times N}{R} = F_{PFD} \times N \quad (1)$$

For a fractional-N PLL

$$F_{OUT} = F_{PFD} \times \left(N_{INT} + \frac{N_{FRAC}}{2^{12}} \right) \quad (2)$$

where N_{FRAC} can be Bits M1 to M12 in the fractional-N register.

CRYSTAL OSCILLATOR

The on-board crystal oscillator circuitry (Figure 27) allows an inexpensive quartz crystal to be used as the PLL reference. The oscillator circuit is enabled by setting XOEB low. It is enabled by default on power-up and is disabled by bringing CE low. Errors in the crystal can be corrected using the error correction register within the R register.

A single-ended reference may be used instead of a crystal, by applying a square wave to the OSC2 pin, with XOEB set high.

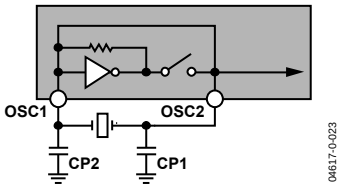


Figure 27. Oscillator Circuit on the ADF7012

Two parallel resonant capacitors are required for oscillation at the correct frequency—the value of these depend on the crystal specification. They should be chosen so that the series value of capacitance added to the PCB track capacitance adds to give the load capacitance of the crystal, usually 20 pF. Track capacitance values vary between 2 pF to 5 pF, depending on board layout.

Where possible, to ensure stable frequency operation over all conditions, capacitors should be chosen so that they have a very low temperature coefficient and/or opposite temperature coefficients

Typically, for a 10 MHz crystal with 20 pF load capacitance, the oscillator circuit can tolerate a crystal ESR value of ≤ 50 Ω. The ESR tolerance of the ADF7012 decreases as crystal frequency increases, but this can be offset by using a crystal with lower load capacitance.

CRYSTAL COMPENSATION REGISTER

The ADF7012 features a 15-bit fixed modulus, which allows the output frequency to be adjusted in steps of FPFD/15. This fine resolution can be used to easily compensate for initial error and temperature drift in the reference crystal.

$$F_{ADJUST} = F_{STEP} \times FEC \quad (3)$$

where:
F_{STEP} = FPFD/215
FEC = Bit F1 to Bit F11 in the R Register

Note that the notation is twos complement, so F11 represents the sign of the FEC number.

Example

F_{PFD} = 10 MHz
F_{ADJUST} = −11 kHz
F_{STEP} = 10 MHz/2^{15} = 305.176 Hz
FEC = −11 kHz/305.17 Hz = −36 = −(00000100100) = 11111011100 = 0x7DC

CLOCK OUT CIRCUIT

The clock out circuit takes the reference clock signal from the Crystal Oscillator section and supplies a divided-down 50:50 mark-space signal to the CLK_{OUT} pin. An even divide from 2 to 30 is available. This divide is set by the DB[19:22] in the R register. On power-up, the CLK_{OUT} defaults to divide by 16.

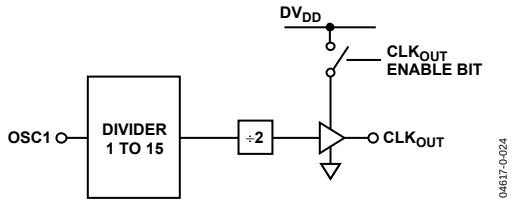


Figure 28. CLKOUT Stage

The output buffer to CLK_{OUT} is enabled by setting Bit DB4 in the function register high. On power-up, this bit is set high. The output buffer can drive up to a 20 pF load with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A small series resistor (50 Ω) can be used to slow the clock edges to reduce these spurs at F_{CLK}.

LOOP FILTER

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown in Figure 29.

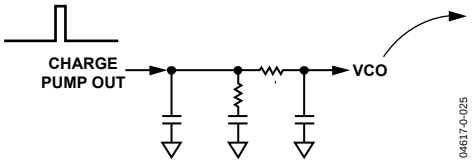


Figure 29. Typical Loop Filter

In FSK, it is recommended that the loop bandwidth be a minimum of two to three times the data rate. Widening the LBW excessively reduces the time spent jumping between frequencies, but results in reduced spurious attenuation. See the Tips on Designing the Loop Filter section.

For OOK/ASK systems, a wider loop bandwidth than for FSK systems is desirable. The sudden large transition between two power levels results in VCO pulling (VCO temporarily goes to incorrect frequency) and can cause a wider output spectrum. By widening the loop bandwidth a minimum of 10× the data rate, VCO pulling is minimized because the loop settles quickly back to the correct frequency. A free design tool, the *ADI SRD Design Studio*™, can be used to design loop filters for the Analog Devices family of transmitters.

VOLTAGE-CONTROLLED OSCILLATOR (VCO)

The ADF7012 features an on-chip VCO with an external tank inductor, which is used to set the frequency range. The center frequency of oscillation is governed by the internal varactor capacitance and that of the external inductor combined with the bond-wire inductance. An approximation for this is given in Equation 4. For a more accurate selection of the inductor, see the section Choosing the External Inductor Value.

$$F_{VCO} = \frac{1}{2\pi\sqrt{(L_{INT} + L_{EXT}) \times (C_{VAR} + C_{FIXED})}} \quad (4)$$

The varactor capacitance can be adjusted in software to increase the effective VCO range by writing to the VA1 and VA2 bits in the R register. Under typical conditions, setting VA1 and VA2 high increases the center frequency by reducing the varactor capacitance by approximately 1.3 pF.

Figure 37 shows the variation of VCO gain with frequency. VCO gain is important in determining the loop filter design—predictable changes in VCO gain resulting in a change in the loop filter bandwidth can be offset by changing the charge-pump current in software.

VCO Bias Current

VCO bias current may be adjusted using bits VB1 to VB4 in the function register. Additional bias current will reduce spurious levels, but increase overall current consumption in the part. A bias value of 0x5 should ensure oscillation at most frequencies and supplies. Settings 0x0, 0xE , and 0xF are not recommended. Setting 0x3 and Setting 0x4 are recommended under most conditions. Improved phase noise can be achieved for lower bias currents.

VOLTAGE REGULATORS

There are two band gap voltage regulators on the ADF7012 providing a stable 2.25 V internal supply: a 2.2 µF capacitor (X5R, NP0) to ground at C_{REG1} and a 470 nF capacitor at C_{REG2} should be used to ensure stability. The internal reference ensures consistent performance over all supplies and reduces the current consumption of each of the blocks.

The combination of regulators, band gap reference, and biasing typically consume 1.045 mA at 3.0 V and can be powered down by bringing the CE line low. The serial interface is supplied by Regulator 1, so powering down the CE line causes the contents of the registers to be lost. The CE line must be high and the regulators must be fully powered on to write to the serial interface. Regulator power-on time is typically 100 µs and should be taken into account when writing to the ADF7012 after power-up. Alternatively, regulator status may be monitored at the MUXOUT pin once CE has been asserted, because MUXOUT defaults to the regulator ready signal. Once Regulator_ready is high, the regulator is powered up and the serial interface is active.

FSK MODULATION

FSK modulation is performed internally in the PLL loop by switching the value of the N register based on the status of the TxDATA line. The TxDATA line is sampled at each cycle of the PFD block (every $1/F_{PFD}$ seconds). When TxDATA makes a low-to-high transition, an N value representing the deviation frequency is added to the N value representing the center frequency. Immediately the loop begins to lock to the new frequency of $F_{CENTER} + F_{DEVIATION}$. Conversely, when TxDATA makes a high-to-low transition, the N value representing the deviation is subtracted from the PLL N value representing the center frequency and the loop transitions to $F_{CENTER} - F_{DEVIATION}$.

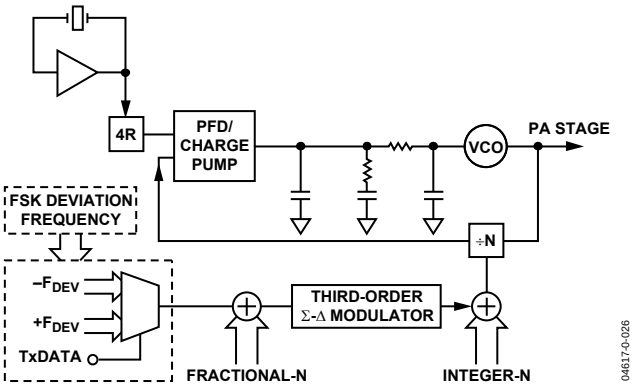


Figure 30. FSK Implementation

The deviation from the center frequency is set using the D1 to D9 bits in the modulation register. The frequency deviation may be set in steps of

$$F_{STEP}(Hz) = \frac{F_{PFD}}{2^{14}} \quad (5)$$

The deviation frequency is therefore

$$F_{DEVIATION}(Hz) = \frac{F_{PFD} \times ModulationNumber}{2^{14}} \quad (6)$$

where *ModulationNumber* is set by Bit D1 to Bit D9.

The maximum data rate is a function of the PLL lock time (and the requirement on FSK spectrum). Because the PLL lock time is reduced by increasing the loop-filter bandwidth, highest data rates can be achieved for the wider loop filter bandwidths. The absolute maximum limit on loop filter bandwidth to ensure stability for a fractional-N PLL is $F_{PFD}/7$. For a 20 MHz PFD frequency, the loop bandwidth could be as high as 2.85 MHz. FSK modulation is selected by setting the S1 and S2 bits in the modulation register low.

GFSK MODULATION

Gaussian frequency shift keying (GFSK) represents a filtered form of frequency shift keying. The data to be modulated to RF is prefiltered digitally using a finite impulse response filter (FIR). The filtered data is then used to modulate the sigma-delta fractional-N to generate spectrally-efficient FSK.

FSK consists of a series of sharp transitions in frequency as the data is switched from one level to another. The sharp switching generates higher frequency components at the output, resulting in a wider output spectrum.

With GFSK, the sharp transitions are replaced with up to 128 smaller steps. The result is a gradual change in frequency. As a result, the higher frequency components are reduced and the spectrum occupied is reduced significantly. GFSK does require some additional design work as the data is only sampled once per bit, and so the choice of crystal is important to ensure the correct sampling clock is generated.

For GFSK and GOOK, the incoming bit stream to be transmitted needs to be synchronized with an on-chip sampling clock which provides one sample per bit to the Gaussian FIR filter. To facilitate this, the sampling clock is routed to the TxCLK pin where data is fetched from the host microcontroller or microprocessor on the falling edge of TxCLK, and the data is sampled at the midpoint of each bit on TxCLK's rising edge. Inserting external RC LPFs on TxDATA and TxCLK lines creates smoother edge transitions and improves spurious performance. As an example, suitable components are a 1 kΩ resistor and a 10 nF capacitor for a data rate of 5 kbps.

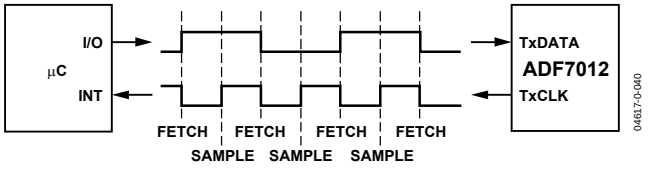


Figure 31. TxCLK/TxDATA Synchronization.

The number of steps between symbol 0 and symbol 1 is determined by the setting for the index counter.

The GFSK deviation is set up as

$$GFSK_{DEVIATION}(\text{Hz}) = \frac{F_{PFD} \times 2^{m}}{2^{12}} \quad (7)$$

where m is the mod control (Bit MC1 to Bit MC3 in the modulation register).

The GFSK sampling clock samples data at the data rate

$$DataRate\,(bps) = \frac{F_{PFD}}{DividerFactor \times IndexCounter} \quad (8)$$

where the *DividerFactor* is set by Bit D1 to Bit D7, and the *IndexCounter* is set by Bit IC1 and Bit IC2 in the modulation register.

POWER AMPLIFIER

The output stage is based on a Class E amplifier design, with an open-drain output switched by the VCO signal. The output control consists of six current mirrors operating as a programmable current source.

To achieve maximum voltage swing, the RF_{OUT} pin needs to be biased at DV_{DD}. A single pull-up inductor to DV_{DD} ensures a current supply to the output stage; PA is biased to DV_{DD} volts, and with the correct choice of value transforms the impedance.

The output power can be adjusted by changing the value of Bit P1 to Bit P6. Typically, this is P1 to P6 output −20dBm at 0x0, and 13 dBm at 0x7E at 868 MHz, with the optimum matching network.

The nonlinear characteristic of the output stage results in an output spectrum containing harmonics of the fundamental, especially the third and fifth. To meet local regulations, a low-pass filter usually is required to filter these harmonics.

The output stage can be powered down by setting Bit PD2 in the function register low.

GOOK MODULATION

Gaussian on-off keying (GOOK) represents a prefiltered form of OOK modulation. The usually sharp symbol transitions are replaced with smooth Gaussian-filtered transitions with the result being a reduction in frequency pulling of the VCO. Frequency pulling of the VCO in OOK mode can lead to a wider than desired bandwidth, especially if it is not possible to increase the loop filter bandwidth to > 300 kHz.

The GOOK sampling clock samples data at the data rate:

$$DataRate\,(bps) = \frac{F_{PFD}}{DividerFactor \times IndexCounter} \qquad (9)$$

Bit D1 to Bit D6 represent the output power for the system for a positive data bit. *Divider Factor* = 0x3F represents the maximum possible deviation from PA at minimum to PA at maximum output. Note that PA output level bits in Register 2 are defunct. An index counter setting of 128 is recommended.

Figure 32 shows the step response of the Gaussian FIR filter. An index counter of 16 is demonstrated for simplicity. While the pre-filter data would switch the PA directly from off to on with a low-to-high data transition, the filtered data gradually increases the PA output in discrete steps. This has the effect of making the output spectrum more compact.

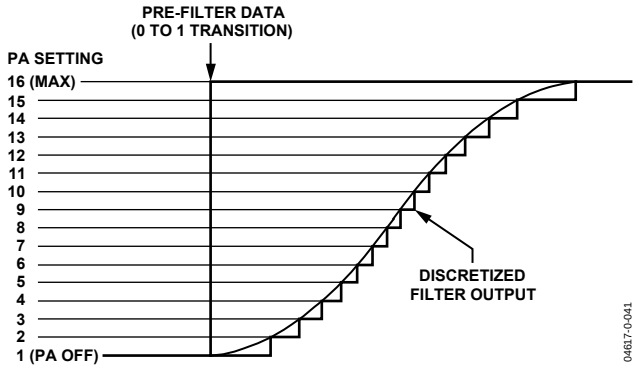


Figure 32. Varying PA Output for GOOK (Index Counter = 16).

As is the case with GFSK, GOOK requires the bit stream applied at TxDATA to be synchronized with the sampling clock, TxCLK (see the GFSK Modulation section).

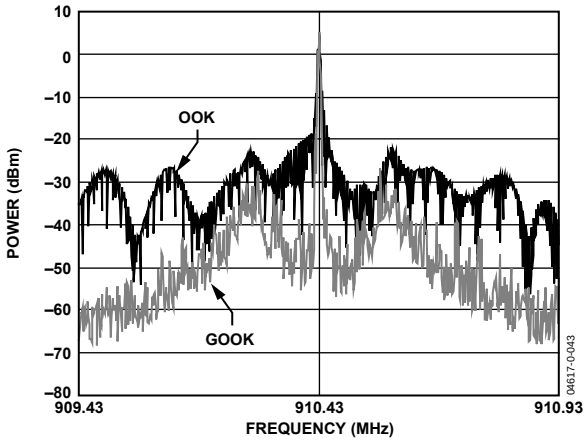


Figure 33. GOOK vs. OOK Frequency Spectra (Narrow-Band Measurement)

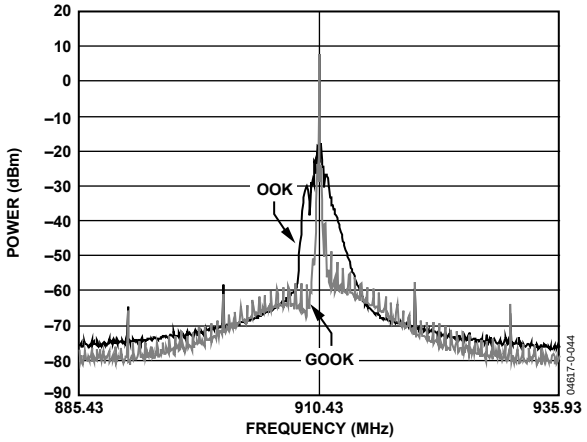


Figure 34. GOOK vs. OOK Frequency Spectra (Wideband Measurement)

OUTPUT DIVIDER

An output divider is a programmable divider following the VCO in the PLL loop. It is useful when using the ADF7012 to generate frequencies of < 500 MHz.

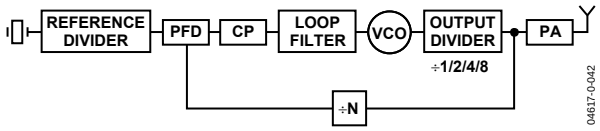


Figure 35. Output Divider Location in PLL

The output divider may be used to reduce feedthrough of the VCO by amplifying only the VCO/2 component, restricting the VCO feedthrough to leakage.

Because the divider is in loop, the N register values should be set up according to the usual formula. However, the VCO gain (K_V) should be scaled according to the divider setting, as shown in the following example:

F_{OUT} = 433 MHz
F_{VCO} = 866 MHz
K_V @ 868 MHz = 60 MHz/V

Therefore, K_V for loop filter design = 30 MHz/V.

The divider value is set in the R register.

Table 5.

OD1	OD2	Divider Status
0	0	Divider off
0	1	Divide by 2
1	0	Divide by 4
1	1	Divide by 8

MUXOUT MODES

The MUXOUT pin allows the user access to various internal signals in the transmitter, and provides information on the PLL lock status, the regulator, and the battery voltage. The MUXOUT is accessed by programming Bits M1 to M4 in the function register and observing the signal at the MUXOUT pin.

Battery Voltage Readback

By setting MUXOUT to 1010 to 1101, the battery voltage can be estimated. The battery measuring circuit features a voltage divider and a comparator where the divided-down supply voltage is compared to the regulator voltage.

Table 6.

MUXOUT	MUXOUT High	MUXOUT Low
1010	DV_{DD} < 2.35 V	DV_{DD} > 2.35 V
1011	DV_{DD} < 2.75 V	DV_{DD} > 2.75 V
1100	DV_{DD} < 3.0 V	DV_{DD} > 3.0 V
1101	DV_{DD} < 3.25 V	DV_{DD} > 3.25 V

The accuracy of the measurement is limited by the accuracy of the regulator voltage and the internal resistor tolerances.

Regulator Ready

The regulator has a power-up time, dependant on process and the external capacitor. The regulator ready signal indicates that the regulator is fully powered, and that the serial interface is active. This is the default setting on power-up at MUXOUT.

Digital Lock Detect

Digital lock detect indicates that the status of the PLL loop. The PLL loop takes time to settle on power-up and when the frequency of the loop is changed by changing the N value. When lock detect is high, the PFD has counted a number of consecutive cycles where the phase error is < 15 ns. The lock detect precision bit in the function register determines whether this is three cycles (LDP = 0), or five cycles (LDP = 1). It is recommended that LDP be set to 1. The lock detect is not completely accurate and goes high before the output has settled to exactly the correct frequency. In general, add 50% to the indicated lock time to obtain lock time to within 1 kHz. The lock detect signal can be used to decide when the power amplifier (PA) should be enabled.

R Divider

MUXOUT provides the output of the R divider. This is a narrow pulsed digital signal at frequency F_{PFD}. This signal may be used to check the operation of the crystal circuit and the R divider. R divider/2 is a buffered version of this signal at $F_{PFD}/2$.

THEORY OF OPERATION

CHOOSING THE EXTERNAL INDUCTOR VALUE

The ADF7012 allows operation at many different frequencies by choosing the external VCO inductor to give the correct output frequency. Figure 36 shows both the minimum and maximum frequency vs. the inductor value. These are measurements based on 0603 CS type inductors from Coilcraft, and are intended as guidelines in choosing the inductor because board layout and inductor type varies between applications.

The inductor value should be chosen so that the VCO is centered at the correct frequency. When locked, the VCO tuning voltage can be between 0.2 V and 2.1 V. This voltage can be measured at Pin 18 (VCO_{IN}). To ensure operation over temperature and from part to part, an inductor should be chosen so that the tuning voltage is ~1 V at the desired output frequency.

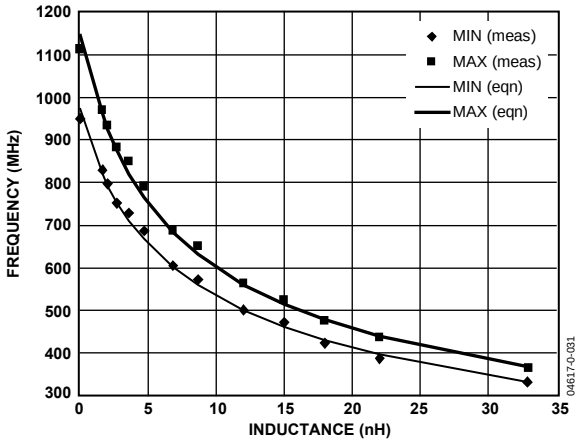


Figure 36. Output Frequency vs. External Inductor Value
I_{BIAS} = 2.0 mA.

For frequencies between 270 MHz and 550 MHz, it is recommended to operate the VCO at twice the desired output frequency and use the divide-by-2 option. This ensures reliable operation over temperature and supply.

For frequencies between 130 MHz and 270 MHz, it is recommended to operate the VCO at four times the desired output frequency and use the divide-by-4 option.

For frequencies below 130 MHz, it is best to use the divide-by-8 option. It is not necessary to use the VCO divider for frequencies above 550 MHz.

ADIsimSRD Design Studio is a design tool which can perform the frequency calculations for the ADF7012, and is available at www.analog.com.

CHOOSING THE CRYSTAL/PFD VALUE

The choice of crystal value is an important one. The PFD frequency must be the same as the crystal value or an integer division of it. The PFD determines the phase noise, spurious levels and location, deviation frequency, and the data rate in the case of GFSK. The following sections describe some factors to consider when choosing the crystal value.

Standard Crystal Values

Standard crystal values are 3.6864 MHz, 4 MHz, 4.096 MHz, 4.9152 MHz, 7.3728 MHz, 9.8304 MHz, 10 MHz, 11.0592 MHz, 12 MHz, and 14.4792 MHz. Crystals with these values are usually available in stock and cost less than crystals with nonstandard values.

Reference Spurious Levels

Reference spurious levels (spurs) occur at multiples of the PFD frequency. The reference spur closest to the carrier is usually highest with the spur further out being attenuated by the loop filter. The level of reference spur is lower for lower PFD frequencies. In designs with high output power where spurious levels are the main concern, a lower PFD frequency (<5 MHz) may be desirable.

Beat Note Spurs

Beat note spurs are spurs occurring for very small or very large values in the fractional register. These are quickly attenuated by the loop filter. Selection of the PFD therefore determines their location, and ensures that they have negligible effect on the transmitter spectrum.

Phase Noise

The phase noise of a frequency synthesizer improves by 3 dB for every doubling of the PFD frequency. Because ACP is related to the phase noise, the PFD may be increased to reduce the ACP in the system. PFD frequencies of < 5 MHz typically deliver sufficient phase noise performance for most systems.

Deviation Frequency

The deviation frequency is adjustable in steps of

$$F_{STEP}(Hz) = \frac{F_{PFD}}{2^{14}} \quad (10)$$

To get the exact deviation frequency required, ensure F_{STEP} is a factor of the desired deviation.

TIPS ON DESIGNING THE LOOP FILTER

The loop filter design is crucial in ensuring stable operation of the transmitter, meeting adjacent channel power (ACP) specifications, and meeting spurious requirements for the relevant regulations. ADIsimSRD Design Studio™ is a free tool available to aid the design of loop filters. The user enters the desired frequency range, the reference crystal and PFD values, and the desired loop bandwidth. ADIsimSRD Design Studio gives a good starting point for the filter, and the filter can be further optimized based on the criteria below.

Setting Tuning Sensitivity Value

The tuning sensitivity or kV, usually denoted in MHz/V, is required for the loop filter design. It refers to the amount that a change of a volt in the voltage applied to the VCO_{IN} pin, changes the output frequency. Typical data for the ADF7012 over a frequency range is shown.

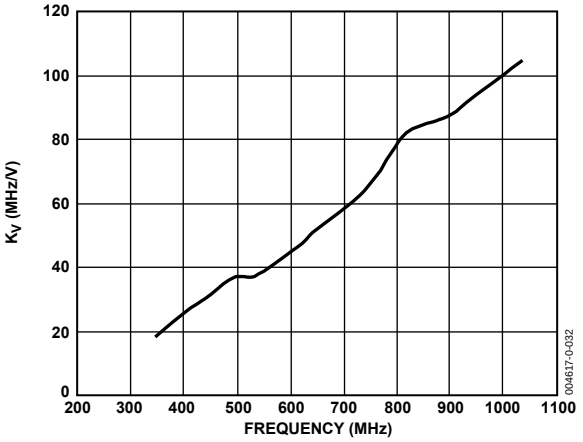


Figure 37. kV vs. VCO Frequency

Charge-Pump Current

The charge-pump current allows the loop filter bandwidth to be changed using the registers. The loop bandwidth reduces as the charge pump current is reduced and vice versa.

Selecting Loop Filter Bandwidth

Data Rate

The loop filter bandwidth should usually be at two to three times the data rate. This ensures that the PLL has ample time to jump between the mark and space frequencies.

ACP

In the case where the ACP specifications are difficult to meet, the loop filter bandwidth can be reduced further to reduce the phase noise at the adjacent channel. The filter rolls off at 20 dB per decade.

Spurious Levels

In the case where the output power is quite high, a reduced loop filter bandwidth reduces the spurious levels even further, and provides additional margin on the specification.

The following sections provide examples of loop filter designs for typical applications in specific frequencies.

PA MATCHING

The ADF7012 exhibits optimum performance in terms of transmit power and current consumption only if the RF output port is properly matched to the antenna impedance.

ZOPT_PA depends primarily on the required output power, and the frequency range. Selecting the optimum ZOPT_PA helps to minimize the current consumption. This data sheet contains a number of matching networks for common frequency bands. Under certain conditions it is recommended to obtain a suitable ZOPT_PA value by means of a load-pull measurement.

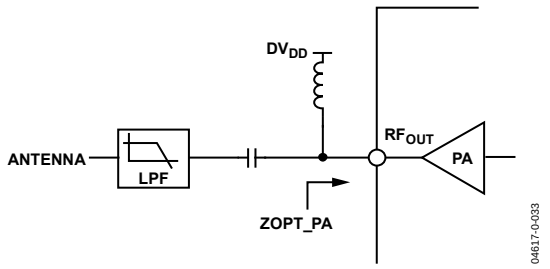


Figure 38. ADF7012 with Harmonic Filter

The impedance matching values provided in the next section are for 50 Ω environments. An additional matching network may be required after the harmonic filter to match to the antenna impedance. This can be incorporated into the filter design itself in order to reduce external components.

TRANSMIT PROTOCOL AND CODING CONSIDERATIONS

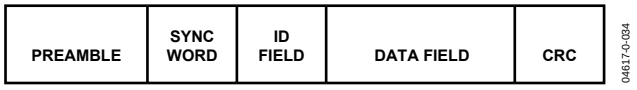


Figure 39. Typical Format of a Transmit Protocol

A dc-free preamble pattern such as 10101010… is recommended for FSK/ASK/OOK demodulation. Preamble patterns with longer run-length constraints such as 11001100…. can also be used. However, this can result in a longer synchronization time of the received bit stream in the chosen receiver.

APPLICATION EXAMPLES

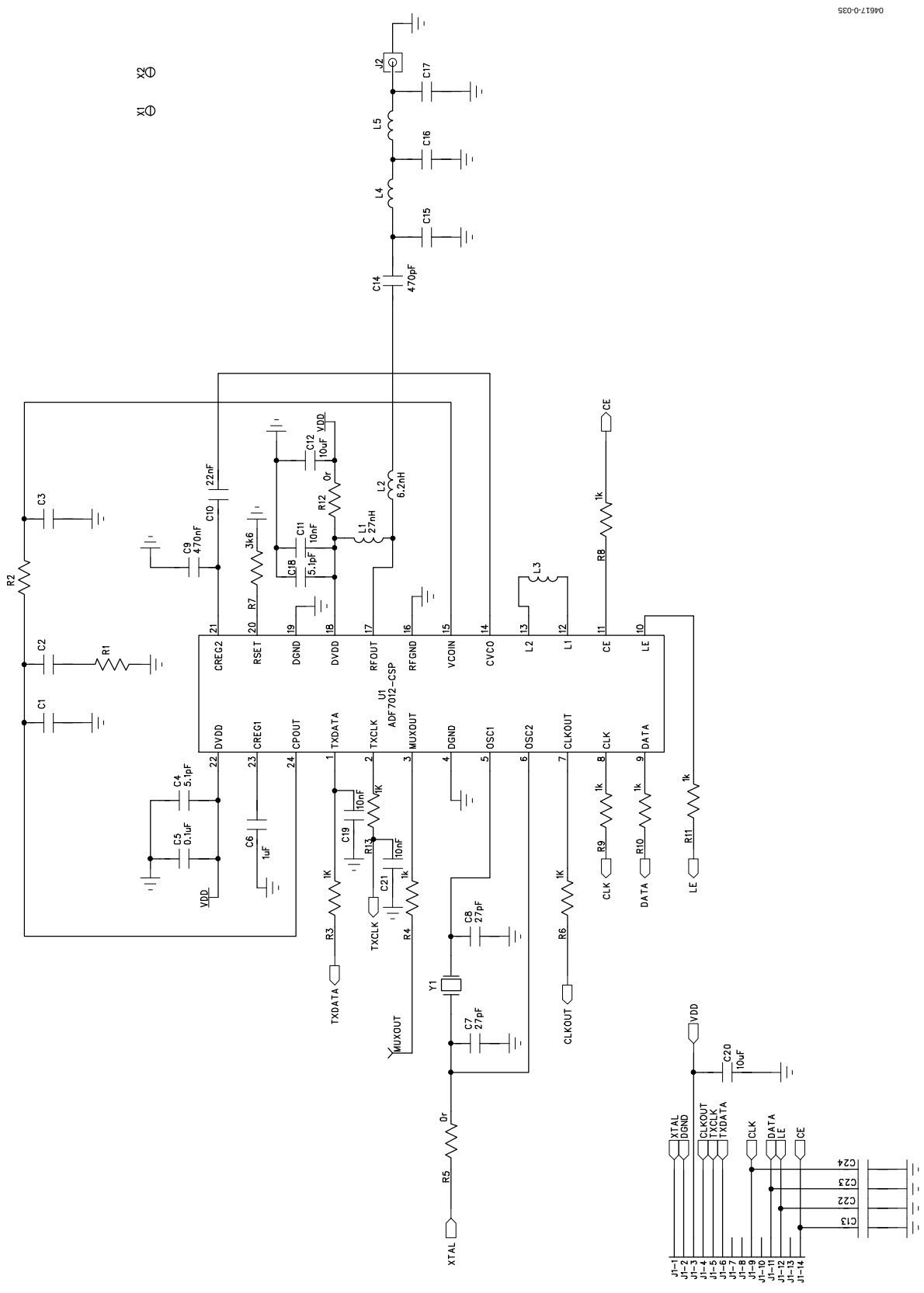


Figure 40. Applications Diagram with Harmonic Filter

315 MHz OPERATION

The recommendations presented here are guidelines only. The design should be subject to internal testing prior to FCC site testing. Matching components need to be adjusted for board layout.

The FCC standard 15.231 regulates operation in the band from 260 MHz to 470 MHz in the US. This is used generally in the transmission of RF control signals, such as in a satellite-decoder remote control, or remote keyless entry system. The band cannot be used to send any continuous signal. The maximum output power allowed is governed by the duty cycle of the system. A typical design example for a remote control is provided.

Design Criteria

315 MHz center frequency
FSK/OOK modulation
1 mW output power
House range
Meets FCC 15.231

The main requirements in the design of this remote are a long battery life and sufficient range. It is possible to adjust the output power of the ADF7012 to increase the range depending on the antenna performance.

The center frequency is 315 MHz. Because the ADF7012 VCO is not recommended for operation in fundamental mode for frequencies below 400 MHz, the VCO needs to operate at 630 MHz. Figure 36 implies an inductor value of, or close to, 7.6 nH. The chip inductor chosen = 7.5 nH (0402CS-7N5 from Coilcraft). Coil inductors are recommended to provide sufficient Q for oscillation.

Crystal and PFD

Phase noise requirements are not excessive as the adjacent channel power requirement is −20 dB. The PFD is chosen to minimize spurious levels (beat note and reference), and to ensure a quick crystal power-up time.

PFD = 3.6864 MHz − power-up time 1.6 ms.

Figure 10 shows a typical power-on time for a 4 MHz crystal.

N-Divider

The N-divider is determined as being

N_{INT} = 85
N_{FRAC} = (1850)/4096
VCO divide-by-2 is enabled

Deviation

The deviation is set to ± 50 kHz to accommodate simple receiver architecture.

The modulation steps available are in 3.6864 MHz/2^{14}:

Modulation steps = 225 Hz
Modulation number = 50 kHz/225 Hz = 222

Bias Current

Because low current is desired, a 2.0 mA VCO bias can be used. Additional bias current reduces any spur, but increases current consumption.

The PA bias can be set to 5.5 mA and can achieve 0 dBm.

Loop Filter Bandwidth

The loop filter is designed with the ADIsimSRD Design Studio. The loop bandwidth design is straightforward because the 20 dB bandwidth is generally of the order of >400 kHz (0.25% of center frequency). A loop bandwidth of close to 100 kHz strikes a good balance between lock time and spurious suppression. If it is found that pulling of the VCO is more than desired in OOK mode, the bandwidth could be increased.

Design of Harmonic Filter

The main requirement of the harmonic filter should ensure that the third harmonic level is < −41.5 dBm. A fifth-order Chebyshev filter is recommended to achieve this, and a suggested starting point is given next. The Pi format is chosen to minimize the more expensive inductors.

Component Values—Crystal: 3.6864 MHz

Loop Filter

I_{CP}	0.866 mA
LBW	100 kHz
C1	680 pF
C2	12 nF
C3	220 pF
R1	1.1 kΩ
R2	3 kΩ

Matching

L1	56 nH
L2	1 nF
C14	470 pF

Harmonic Filter

L4	22 nH
L5	22 nH
C15	3.3 pF
C16	8.2 pF
C17	3.3 pF

433 MHz OPERATION

The recommendations here are guidelines only. The design should be subject to internal testing prior to ETSI site testing. Matching components need to be adjusted for board layout.

The ETSI standard EN 300-220 governs operation in the 433.050 MHz to 434.790 MHz band. For many systems, 10% duty is sufficient for the transmitter to output 10 dBm.

Design Criteria

433.92 MHz center frequency
FSK modulation
10 mW output power
200 m range
Meets ETSI 300-220

The main requirement in the design of this remote is a long battery life and sufficient range. It is possible to adjust the output power of the ADF7012 to increase the range depending on the antenna performance.

The center frequency is 433.92 MHz. It is possible to operate the VCO at this frequency. Figure 36 shows the inductor value vs. center frequency. The inductor chosen is 22 nH. Coilcraft inductors such as 0603-CS-22NXJBU are recommended.

Crystal and PFD

The phase noise requirement is such to ensure the power at the edge of the band is < −36 dBm. The PFD is chosen to minimize spurious levels (beat note and reference), and to ensure a quick crystal power-up time.

PFD = 4.9152 MHz − Power-Up Time 1.6 ms. Figure 10 shows a typical power-up time for a 4 MHz crystal.

N-Divider

The N Divider is determined as being:

Nint = 88
Nfrac = (1152)/4096
VCO divide-by-2 is not enabled

Deviation

The deviation is set to ± 50 kHz to accommodate a simple receiver architecture.

The modulation steps available are in 4.9152 MHz/2^{14}:

Modulation steps = 300 Hz
Modulation number = 50 kHz/300Hz = 167

Bias Current

Because low current is desired, a 2.0 mA VCO bias can be used. Additional bias current reduces any spurious, but increases current consumption.

The PA bias can be set to 5.5 mA and achieve 10 dBm.

Loop Filter Bandwidth

The loop filter is designed with ADIsimSRD Design Studio. The loop bandwidth design requires that the channel power be < −36 dBm at ±870 kHz from the center. A loop bandwidth of close to 160 kHz strikes a good balance between lock time for data rates, including 32 kbps and spurious suppression. If it is found that pulling of the VCO is more than desired in OOK mode, the bandwidth could be increased.

Design of Harmonic Filter

The main requirement of the harmonic filter should ensure that the third harmonic level is < −30 dBm. A fifth-order Chebyshev filter is recommended to achieve this, and a suggested starting point is given next. The Pi format is chosen to minimize the more expensive inductors.

Component Values—Crystal: 4.9152 MHz

Loop Filter

Icp	2.0 mA
LBW	100 kHz
C1	680 pF
C2	12 nF
C3	270 pF
R1	910 Ω
R2	3.3 kΩ

Matching

L1	22 nH
L2	10 pF
C14	470 pF

Harmonic Filter

L4	22 nH
L5	22 nH
C15	3.3 pF
C16	8.2 pF
C17	3.3 pF

868 MHz OPERATION

The recommendations here are guidelines only. The design should be subject to internal testing prior to ETSI site testing. Matching components need to be adjusted for board layout.

The ETSI standard EN 300-220 governs operation in the 868 MHz to 870MHz band. The band is broken down into several subbands each having a different duty cycle and output power requirement. Narrowband operation is possible in the 50kHz channels, but both the output power and data rate are limited by the −36 dBm adjacent channel power specification. There are many different applications in this band, including remote controls for security, sensor interrogation, metering and home control.

Design Criteria

868.95 MHz center frequency (band 868.7MHz − 869.2 MHz)
FSK modulation
12 dBm output power
300 m range
Meets ETSI 300-220
38.4 kbps data rate

The design challenge is to enable the part to operate in this particular subband and meet the ACP requirement 250 kHz away from the center.

The center frequency is 868.95 MHz. It is possible to operate the VCO at this frequency. Figure 31 shows the inductor value vs. center frequency. The inductor chosen is 1.9 nH. Coilcraft inductors such as 0402-CS-1N9XJBU are recommended.

Crystal and PFD

The phase noise requirement is such to ensure the power at the edge of the band is < −36 dBm. This requires close to −100 dBc/Hz phase noise at the edge of the band.

The PFD is chosen to minimize spurious levels (beat note and reference), and to ensure a quick crystal power-up time. A PFD of < 6 MHz places the largest PFD spur at a frequency of greater than 862 MHz, and so reduces the requirement on the spur level to −36 dBm instead of −54 dBm.

PFD = 4.9152 MHz − Power Up-Time 1.6 ms. Figure 10 shows a typical power-on time for a 4MHz crystal.

N-Divider

The N divider is determined as being:

Nint = 176
Nfrac = (3229)/4096
VCO divide-by-2 is not enabled.

Deviation

The deviation is set to ±19.2 kHz to accommodate a simple receiver architecture and ensure that the modulation spectrum is narrow enough to meet the adjacent channel power (ACP) requirements.

The modulation steps available are in 4.9152 MHz/2^{14}:

Modulation steps = 300 Hz
Modulation number = 19.2 kHz/300 Hz = 64.

Bias Current

Because low current is desired, a 2.5 mA VCO bias can be used. Additional bias current reduces any spurious, but increases current consumption. A 2.5 mA bias current gives the best spurious vs. phase noise trade-off.

The PA bias should be set to 7.5 mA to achieve 12 dBm.

Loop Filter Bandwidth

The loop filter is designed with ADIsimSRD Design Studio. The loop bandwidth design requires that the channel power be < −36 dBm at ±250 kHz from the center. A loop bandwidth of close to <60 kHz is required to bring the phase noise at the edge of the band sufficiently low to meet the ACP specification. This represents a compromise between the data rate requirement and the phase noise requirement.

Design of Harmonic Filter

The main requirement of the harmonic filter should ensure that the second and third harmonic levels are < −30 dBm. A fifth-order Chebyshev filter is recommended to achieve this, and a suggested starting point is given next. The Pi format is chosen to minimize the more expensive inductors.

Component Values—Crystal: 4.9152 MHz

Loop Filter

Icp	1.44 mA
LBW	60 kHz
C1	1.5 nF
C2	22 nF
C3	560 pF
R1	390 Ω
R2	910 Ω

Matching

L1	27 nH
L2	6.2 nH
C14	470 pF

Harmonic Filter

L4	8.2 nH
L5	8.2 nH
C15	4.7 pF
C16	6.8 pF
C17	4.7 pF

915 MHz OPERATION

The recommendations here are guidelines only. The design should be subject to internal testing prior to FCC site testing. Matching components need to be adjusted for board layout.

FCC 15.247 and FCC 15.249 are the main regulations governing operation in the 902 MHz to 928 MHz Band. FCC 15.247 requires some form of spectral spreading. Typically, the ADF7012 would be used in conjunction with the frequency hopping spread spectrum (FHSS) or it may be used in conjunction with the digital modulation standard which requires large deviation frequencies. Output power of < 1 W is tolerated on certain spreading conditions.

Compliance with FCC 15.249 limits the output power to −1.5 dBm, but does not require spreading. There are many different applications in this band, including remote controls for security, sensor interrogation, metering, and home control.

Design Criteria

915.2MHz center frequency
FSK modulation
10 dBm output power
200 m range
Meets FCC 15.247
38.4 kbps data rate

The center frequency is 915.2 MHz. It is possible to operate the VCO at this frequency. Figure 36 shows the inductor value vs. center frequency. The inductor chosen is 1.6 nH. Coilcraft inductors such as 0603-CS-1N6XJBU are recommended. Additional hopping frequencies can easily be generated by changing the N value.

Crystal and PFD

The phase noise requirement is such to ensure that the 20 dB bandwidth requirements are met. These are dependent on the channel spacing chosen. A typical channel spacing would be 400 kHz, which would allow 50 channels in 20 MHz and enable the design to avoid the edges of the band.

The PFD is chosen to minimize spurious levels. There are beat note spurious levels at 910 MHz and 920 MHz, but the level is usually significantly less than the modulation power. They are also attenuated quickly by the loop filter to ensure a quick crystal power-up time.

PFD = 10 MHz – Power-Up Time 1.8 ms (approximately). Figure 10 shows a typical power-on time for a 4 MHz crystal.

N-Divider

The N divider is determined as being:

Nint = 91
Nfrac = (2130)/4096
VCO divide-by-2 is not enabled

Deviation

The deviation is set to ±19.2 kHz to accommodate a simple receiver architecture, and to ensure the available spectrum is used efficiently.

The modulation steps available are in 10 MHz/2^{14}:

Modulation steps = 610 Hz
Modulation number = 19.2 kHz/610 Hz = 31.

Bias Current

Because low current is desired, a 3 mA VCO bias can be used and still ensure oscillation at 928 MHz. Additional bias current reduces any spurious noise, but increases current consumption. A 3 mA bias current gives the best spurious vs. phase noise trade-off.

The PA bias should be set to 5.5 mA to achieve 10 dBm power.

Loop Filter Bandwidth

The loop filter is designed with the ADIsimSRD Design Studio. A data rate of 170 kHz is chosen, which allows for data rates of > 38.4 kbps. It also attenuates the beat note spurs quickly to ensure they have no effect on system performance.

Design of Harmonic Filter

The main requirement of the harmonic filter should ensure that the third harmonic level is < −41.5 dBm. A fifth-order Chebyshev filter is recommended to achieve this, and a suggested starting point is given next. The Pi format is chosen to minimize the number of inductors in the system.

Component Values—Crystal: 10 MHz

Loop Filter

Icp	1.44 mA
LBW	170 kHz
C1	470 pF
C2	12 nF
C3	120 pF
R1	470 Ω
R2	1.8 kΩ

Matching

L1	27 nH
L2	6.2 nH
C14	470 pF

Harmonic Filter

L4	8.2 nH
L5	8.2 nH
C15	4.7 pF
C16	6.8 pF
C17	4.7 pF

REGISTER DESCRIPTIONS

REGISTER 0: R REGISTER

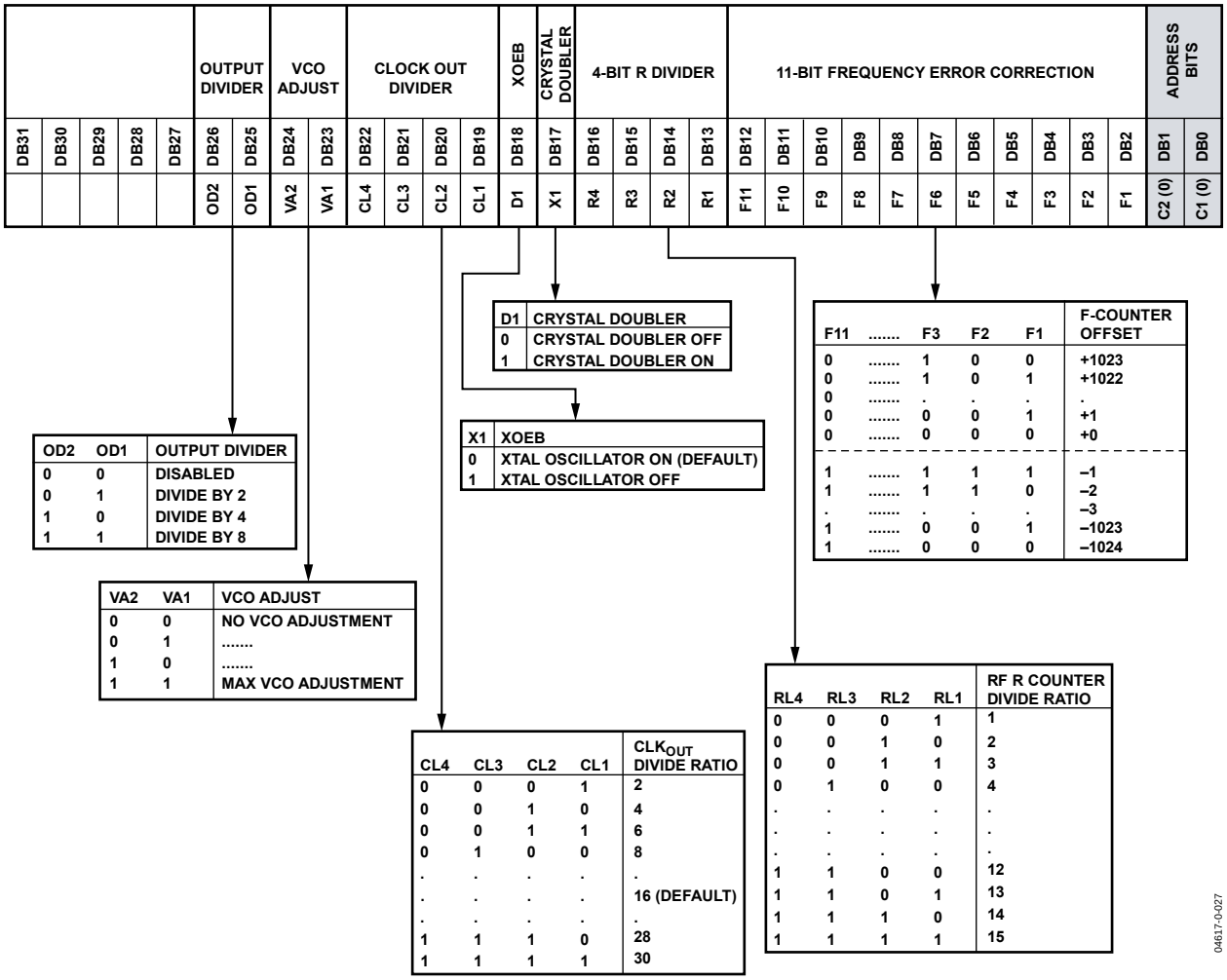


Figure 41. Register 0: R Register

REGISTER 1: N-COUNTER LATCH

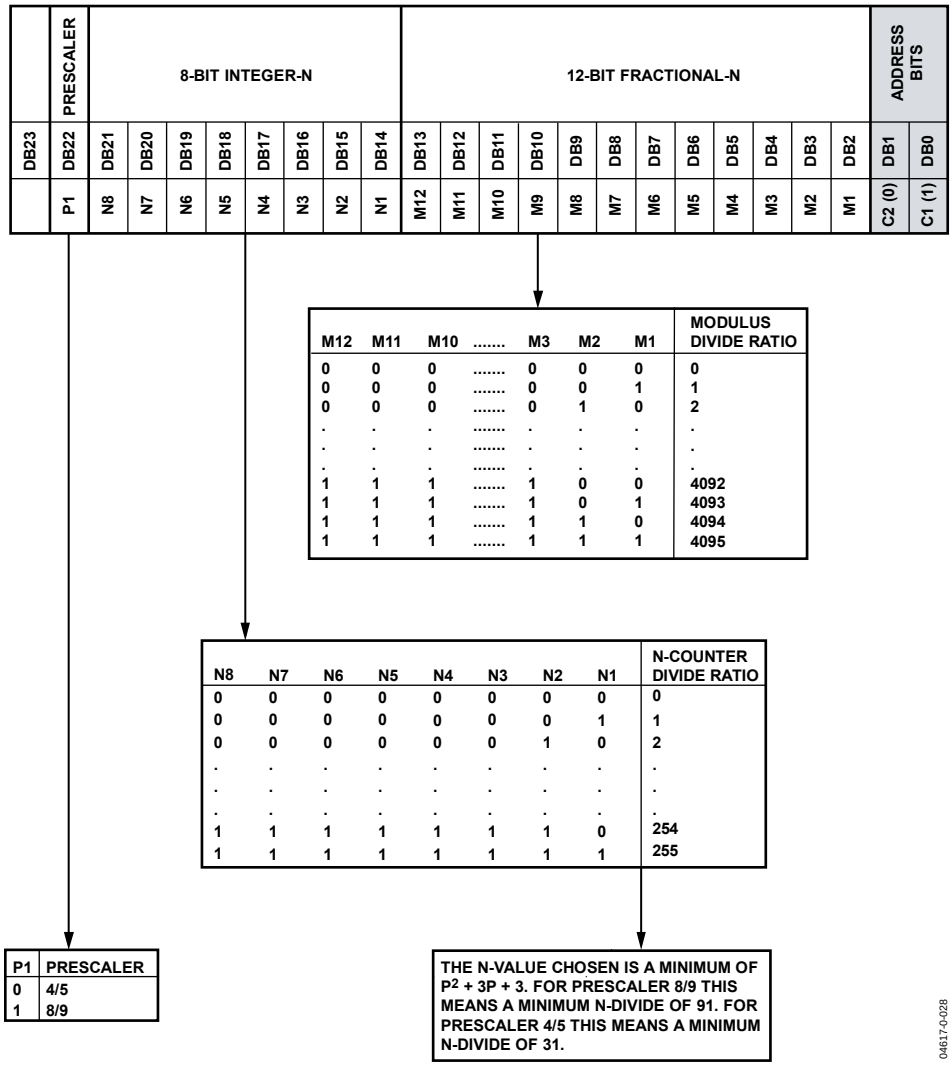


Figure 42. Register 1: N-Counter Latch

REGISTER 2: MODULATION REGISTER

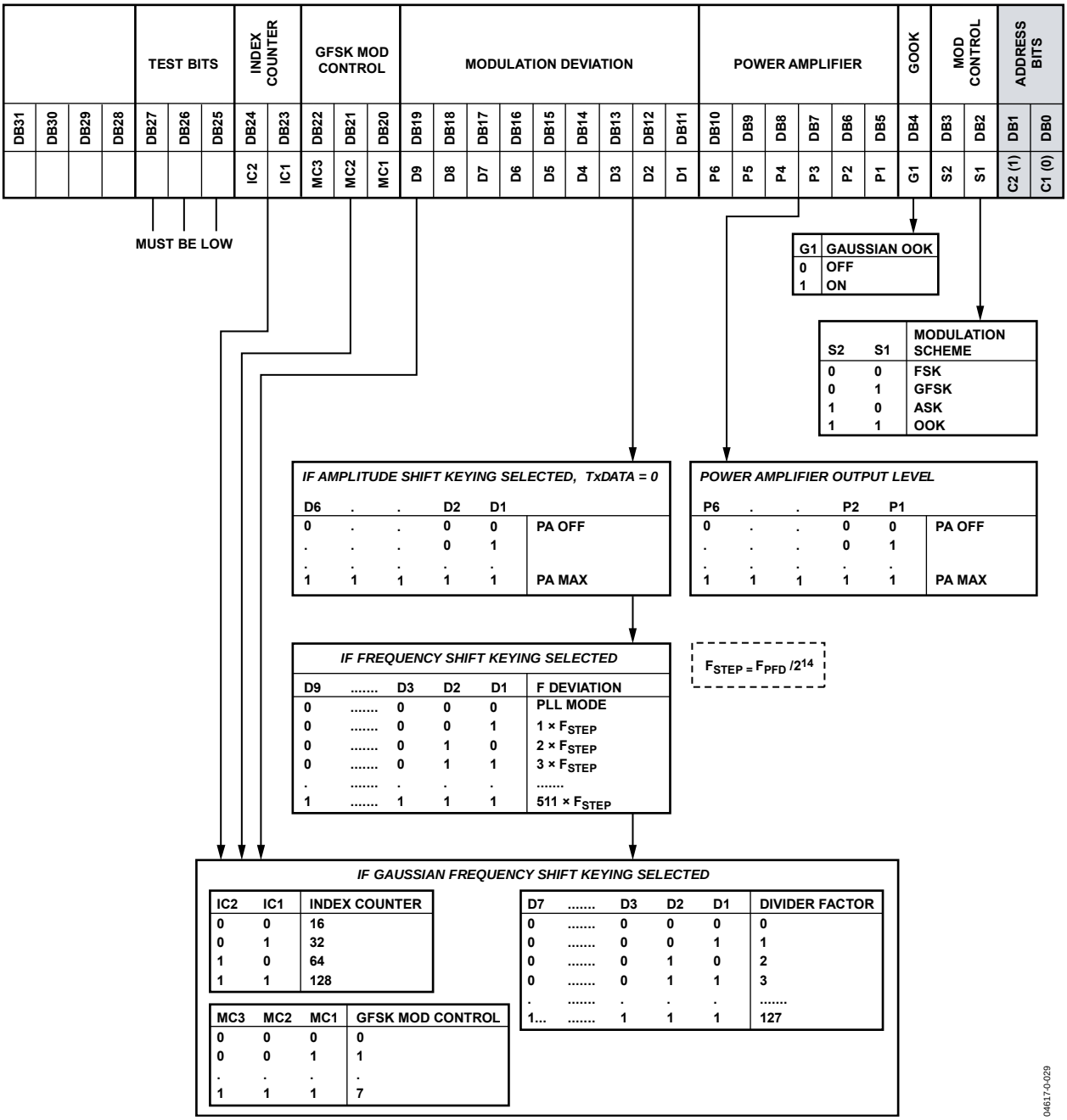
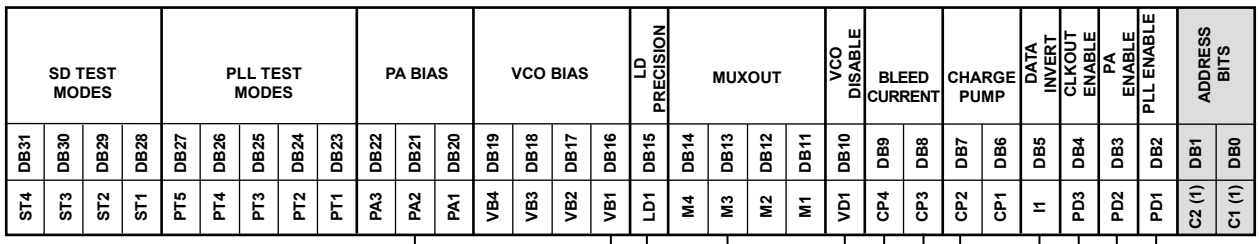


Figure 43. Register 2: Modulation Register

REGISTER 3: FUNCTION REGISTER



PA3	PA2	PA1	PA BIAS
0	0	0	5µA
0	0	1	6µA
0	1	0	7µA
.	.	.	.
.	.	.	.
1	1	1	12µA

CP4	BLEED DOWN
0	BLEED OFF (DEFAULT)
1	BLEED ON

I1	DATA INVERT
0	NORMAL
1	INVERTED

PD1	PLL ENABLE
0	PLL OFF
1	PLL ON

CP3	BLEED UP
0	BLEED OFF (DEFAULT)
1	BLEED ON

PD2	PA ENABLE
0	PA OFF
1	PA ON

VB4	VB3	VB2	VB1	VCO BIAS CURRENT
0	0	0	1	0.5mA
0	0	1	0	1mA
.	.	.	.	.
1	1	1	1	8mA

CP2	CP1	CHARGE PUMP CURRENT
0	0	0.3mA
0	1	0.9mA
1	0	1.5mA
1	1	2.1mA

LD1	LD PRECISION
0	3 CYCLES (DEFAULT)
1	5 CYCLES

VD1	VCO DISABLE
0	VCO ON
1	VCO OFF

PD3	CLK_{OUT}
0	CLK_{OUT} OFF
1	CLK_{OUT} ON

M4	M3	M2	M1	MUXOUT
0	0	0	0	LOGIC LOW
0	0	0	1	LOGIC HIGH
0	0	1	0	INVALID MODE – DO NOT USE
0	0	1	1	REGULATOR READY (DEFAULT)
0	1	0	0	DIGITAL LOCK DETECT
0	1	0	1	ANALOG LOCK DETECT
0	1	1	0	R DIVIDER/2 OUTPUT
0	1	1	1	N DIVIDER/2 OUTPUT
1	0	0	0	RF R DIVIDER OUTPUT
1	0	0	1	DATA RATE
1	0	1	0	BATTERY MEASURE IS < 2.35V
1	0	1	1	BATTERY MEASURE IS < 2.75V
1	1	0	0	BATTERY MEASURE IS < 3V
1	1	0	1	BATTERY MEASURE IS < 3.25V
1	1	1	0	NORMAL TEST MODES
1	1	1	1	Σ-Δ TEST MODES

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Figure 44. Register 3: Function Register

OUTLINE DIMENSIONS

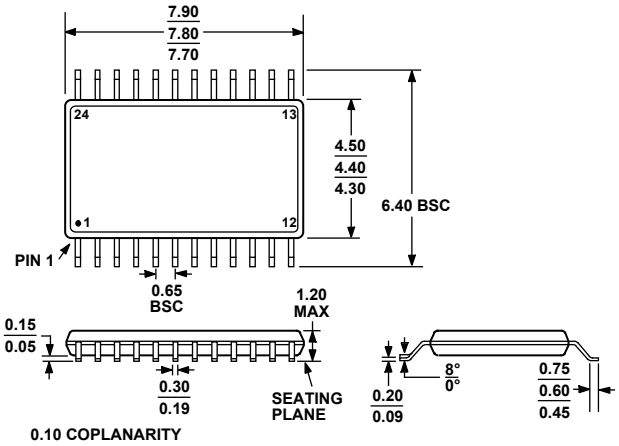

Figure 45. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Frequency Range
ADF7012BRU[1]	−40°C to +85°C	24-Lead TSSOP	RU-24	75 MHz to 1 GHz
ADF7012BRU-REEL[1]	−40°C to +85°C	24-Lead TSSOP, 13″ REEL	RU-24	75 MHz to 1 GHz
ADF7012BRU-REEL7[1]	−40°C to +85°C	24-Lead TSSOP, 7″ REEL	RU-24	75 MHz to 1 GHz
ADF7012BRUZ[1]	−40°C to +85°C	24-Lead TSSOP	RU-24	75 MHz to 1 GHz
ADF7012BRUZ-RL[1]	−40°C to +85°C	24-Lead TSSOP, 13″ REEL	RU-24	75 MHz to 1 GHz
ADF7012BRUZ-RL7[1]	−40°C to +85°C	24-Lead TSSOP, 7″ REEL	RU-24	75 MHz to 1 GHz
EVAL-ADF7012DBZ1[1]		Evaluation Board		902 MHz to 928 MHz
EVAL-ADF7012DBZ2[1]		Evaluation Board		860 MHz to 880 MHz
EVAL-ADF7012DBZ3[1]		Evaluation Board		418 MHz to 435 MHz
EVAL-ADF7012DBZ4[1]		Evaluation Board		310 MHz to 330 MHz
EVAL-ADF7012DBZ5[1]		Evaluation Board		75 MHz to 1 GHz

[1] Z = RoHS Compliant Part.

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D04617-0-6/09(A)

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