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December 2013

FCP190N60_GF102

N-Channel SuperFET® II MOSFET

600 V, 20.2 A, 199 mΩ

Features

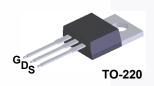
- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 170 m Ω
- Ultra Low Gate Charge (Typ. Q_q = 57 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 160 pF)
- · 100% Avalanche Tested
- RoHS Compliant

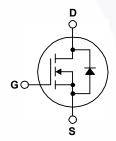
Application

- · LCD / LED / PDP TV Lighting
- · Solar Inverter
- · AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter	FCP190N60_GF102	Unit	
V _{DSS}	Drain to Source Voltage		600	V	
V _{GSS}	Cata ta Sauraa Valtaga	- DC	±20	V	
	Gate to Source Voltage	- AC (f > 1 Hz	±30	V	
	Drain Current	- Continuous (T _C = 25°C)	20.2	Α	
D	Drain Current	- Continuous (T _C = 100°C)	12.7	A	
I _{DM}	Drain Current	- Pulsed (Note 1	60.6	Α	
E _{AS}	Single Pulsed Avalanche Energ	y (Note 2	400	mJ	
I _{AR}	Avalanche Current	(Note 1	4.0	Α	
E _{AR}	Repetitive Avalanche Energy	(Note 1	2.1	mJ	
	MOSFET dv/dt		100	V/ns	
dv/dt	Peak Diode Recovery dv/dt	(Note 3	20	V/IIS	
П	Dower Discipation	$(T_C = 25^{\circ}C)$	208	W	
P_{D}	Power Dissipation - Derate Above 25°C		1.67	W/°C	
T _J , T _{STG}	Operating and Storage Temperation	-55 to +150	οС		
T _L	Maximum Lead Temperature fo	r Soldering, 1/8" from Case for 5 Seconds	300	οС	

Thermal Characteristics

Symbol	Parameter	FCP190N60_GF102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	*C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP190N60_GF102	FCP190N60 GF102	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
D\/	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	600	-	-	V
BV _{DSS}		$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	650	-	-	
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
BV _{DS}	Drain to Source Avalanche Breakdown Voltage	V _{GS} = 0 V, I _D = 20 A	-	700	-	V
1	Zero Gate Voltage Drain Current	V _{DS} = 480 V, V _{GS} = 0 V	-	-	1	^
I _{DSS}	Zero Gate voltage Drain Current	$V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	10	μΑ
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.5	-	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	0.17	0.199	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 10 \text{ A}$	-	21	-	S

Dynamic Characteristics

•						
C _{iss}	Input Capacitance	V 05.V V 0.V	-	2220	2950	pF
C _{oss}	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	-	1630	2165	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	-	85	128	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	-	42	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	-	160	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 10 A,	-	57	74	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	9	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	21	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	1	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	20	50	ns
t _r		$V_{DD} = 380 \text{ V}, I_D = 10 \text{ A},$	_	10	30	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_g = 4.7 \Omega$	-	64	138	ns
t _f	Turn-Off Fall Time	(Note 4)	-	5	20	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Di	Maximum Continuous Drain to Source Diode Forward Current			20.2	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current			-	60.6	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 10 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 10 A,	-	280	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	3.8	-	μС

Notes:

- ${\it 1. Repetitive\ rating: pulse-width\ limited\ by\ maximum\ junction\ temperature.}$
- 2. I_{AS} = 4 A, V_{DD} = 50 V, R_G = 25 Ω , starting T_J = 25°C.
- 3. I_{SD} \leq 10 A, di/dt \leq 200 A/µs, V_DD \leq BV_DSS, starting T_J = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

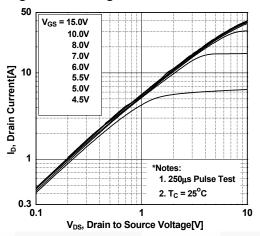


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

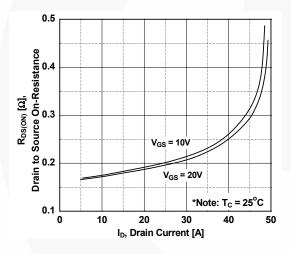


Figure 5. Capacitance Characteristics

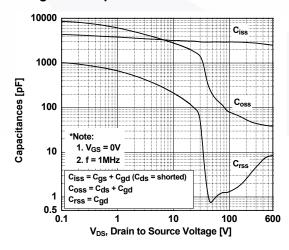


Figure 2. Transfer Characteristics

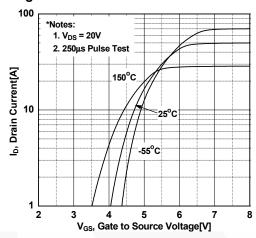


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

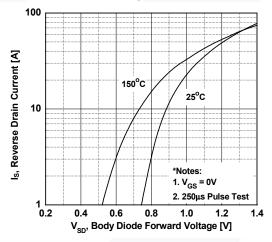
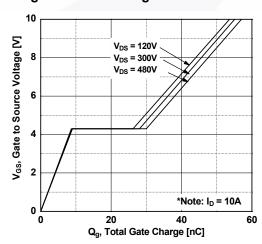


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

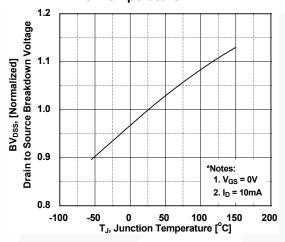


Figure 9. Maximum Safe Operating Area

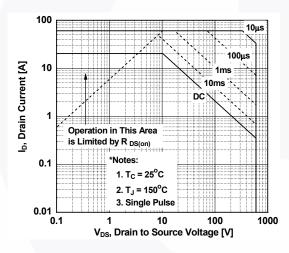


Figure 11. Eoss vs. Drain to Source Voltage

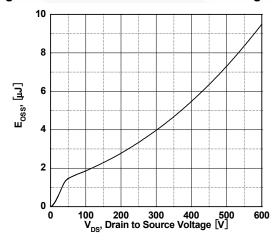


Figure 8. On-Resistance Variation vs. Temperature

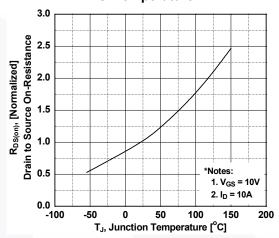
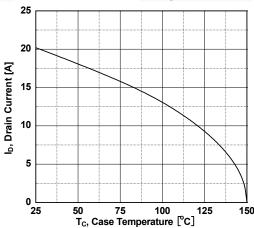
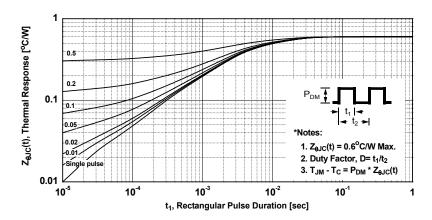


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



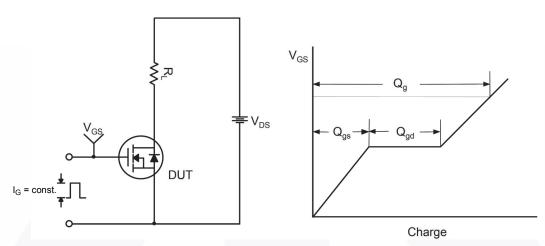


Figure 13. Gate Charge Test Circuit & Waveform

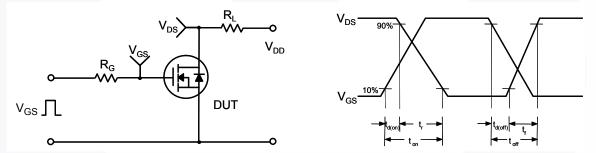


Figure 14. Resistive Switching Test Circuit & Waveforms

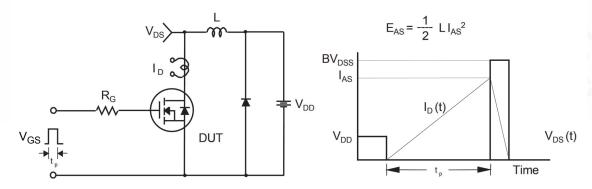


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

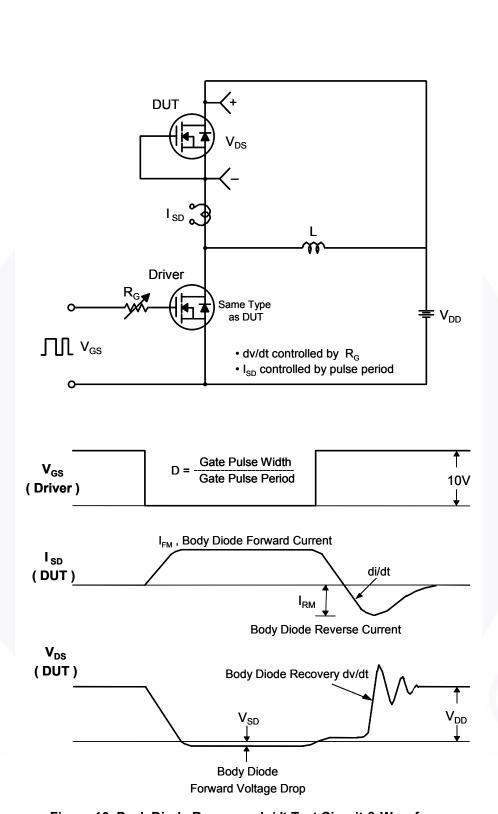
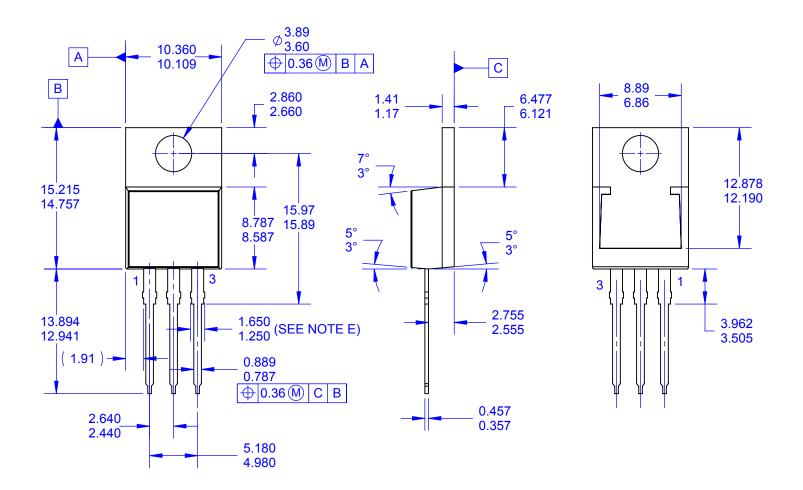
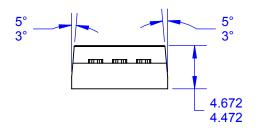


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms





NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 **VARIATION AB**
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. MAX WIDTH FOR F102 DEVICE = 1.35mm. F. DRAWING FILE NAME: TO220T03REV4.
- G. FAIRCHILD SEMICONDUCTOR.

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Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9