



FDY6342L

Integrated Load Switch

November 2014



Features

- Max $r_{DS(on)}$ = 0.5 Ω at V_{GS} = 4.5 V, I_D = -0.83 A
- Max $r_{DS(on)}$ = 0.7 Ω at V_{GS} = 2.5 V, I_D = -0.70 A
- Max $r_{DS(on)}$ = 1.2 Ω at V_{GS} = 1.8 V, I_D = -0.43 A
- Max $r_{DS(on)}$ = 1.8 Ω at V_{GS} = 1.5 V, I_D = -0.36 A
- Control MOSFET (Q1) includes Zener protection for ESD ruggedness (>4 kV Human body model)
- High performance trench technology for extremely low $r_{DS(on)}$
- Compact industry standard SC89-6 surface mount package
- RoHS Compliant

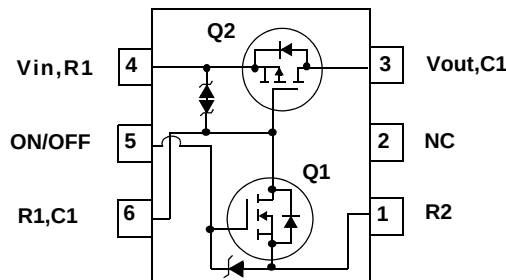
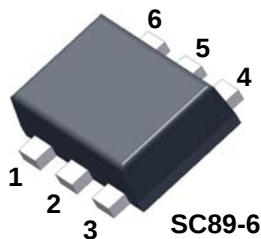


General Description

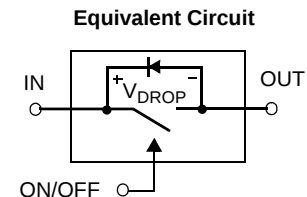
This device is particularly suited for compact power management in portable electronic equipment where 2.5 V to 8 V input and 0.83 A output current capability are needed. This load switch integrates a small N-Channel power MOSFET (Q1) that drives a large P-Channel power MOSFET (Q2) in one tiny SC89-6 package.

Applications

- Power management
- Load switch



See Application Circuit



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{IN}	Gate to Source Voltage (Q2)	± 8	V
$V_{ON/OFF}$	Gate to Source Voltage (Q1)	-0.5 to 8	V
I_{Load}	Load Current -Continuous	0.83	A
	-Pulsed	1.0	
P_D	Power Dissipation	0.625	W
	Power Dissipation	0.446	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	200	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	280	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
H	FDY6342L	SC89-6	7"	8 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{IN}	V_{IN} Breakdown Voltage	$I_D = -250\ \mu\text{A}$, $V_{ON/OFF} = 0\ \text{V}$	8			V
I_{Load}	Zero Gate Voltage Drain Current	$V_{IN} = -6.4\ \text{V}$, $V_{ON/OFF} = 0\ \text{V}$			-1	μA
I_{FL}	Leakage Current, Forward	$V_{IN} = 8\ \text{V}$, $V_{ON/OFF} = 0\ \text{V}$			10	μA
I_{RL}	Leakage Current, Reverse	$V_{IN} = -8\ \text{V}$, $V_{ON/OFF} = 0\ \text{V}$			-10	μA

On Characteristics (note 2)

$V_{ON/OFF(th)}$	Gate Threshold Voltage	$V_{IN} = V_{ON/OFF}$, $I_D = -250\ \mu\text{A}$	0.65	0.85	1.5	V
$r_{DS(on)}$	Static Drain to Source On Resistance (Q2)	$V_{IN} = 4.5\ \text{V}$, $I_D = -0.83\ \text{A}$		0.28	0.5	Ω
		$V_{IN} = 2.5\ \text{V}$, $I_D = -0.70\ \text{A}$		0.35	0.7	
		$V_{IN} = 1.8\ \text{V}$, $I_D = -0.43\ \text{A}$		0.45	1.2	
		$V_{IN} = 1.5\ \text{V}$, $I_D = -0.36\ \text{A}$		0.57	1.8	
		$V_{IN} = 4.5\ \text{V}$, $I_D = 0.4\ \text{A}$		2.9	4.0	
	Static Drain to Source On Resistance (Q1)	$V_{IN} = 2.7\ \text{V}$, $I_D = 0.2\ \text{A}$		3.5	5.0	Ω

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current				-0.25	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{ON/OFF} = 0\ \text{V}$, $I_S = -0.25\ \text{A}$ (Note 2)		-0.8	-1.2	V

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

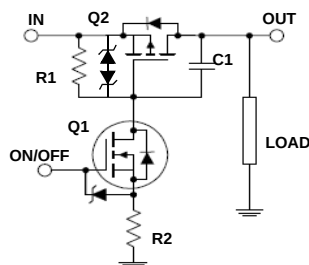


a) 200 °C/W when mounted on a 1 in² pad of 2 oz copper.



b) 280 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

FDY6342L Load Switch Application circuit**External Component Recommendation:**

For additional in-rush current control, R2 and C1 can be added. For more information, see application note AN1030

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

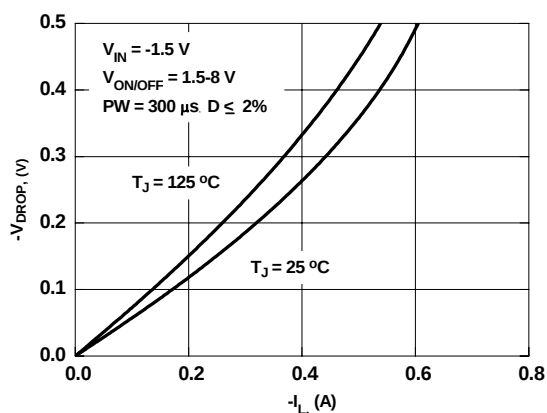


Figure 1. Conduction Voltage Drop Variation with Load Current

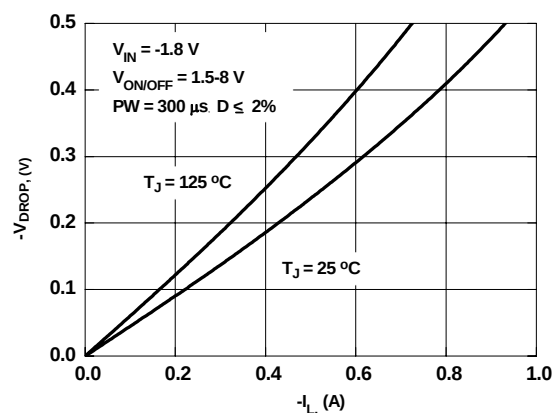


Figure 2. Conduction Voltage Drop Variation with Load Current

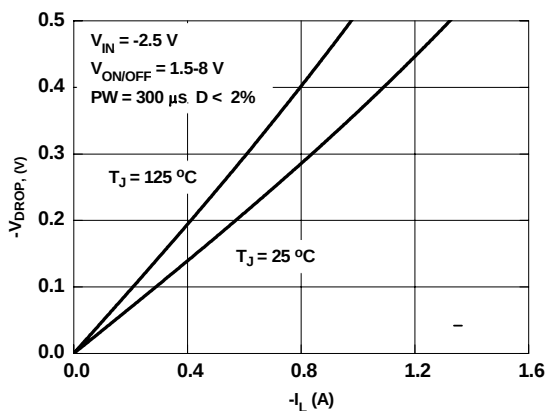


Figure 3. Conduction Voltage Drop Variation with Load Current

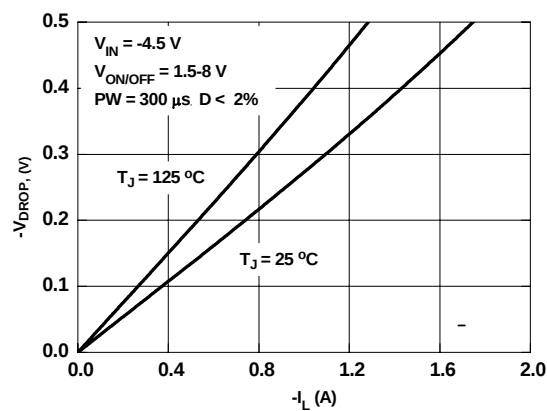


Figure 4. Conduction Voltage Drop Variation with Load Current

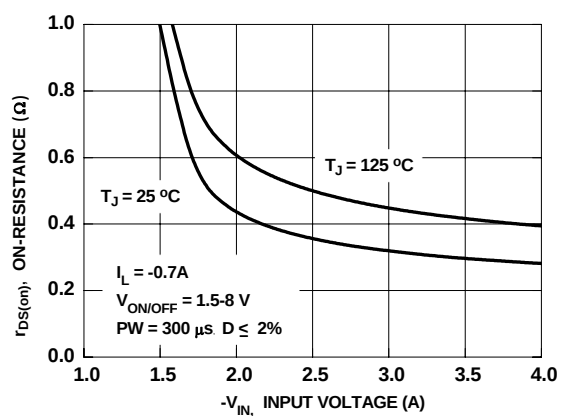


Figure 5. On-Resistance Variation with Input Current

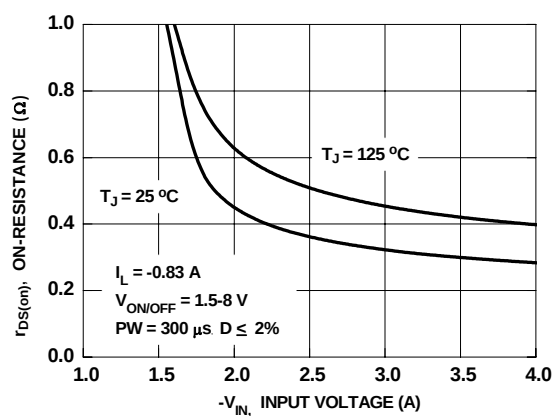
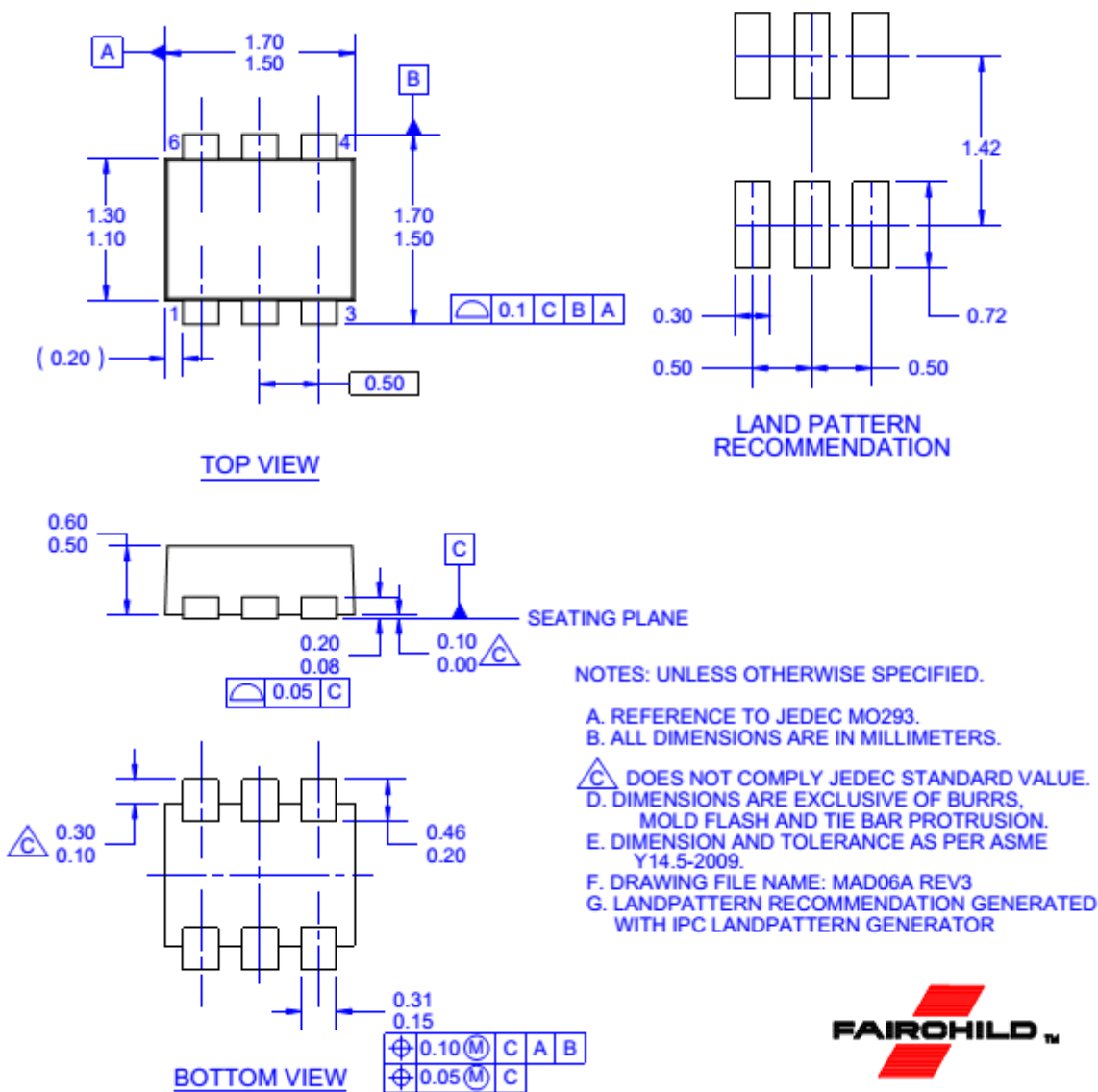


Figure 6. On-Resistance Variation with Input Current

Dimensional Outline and Pad Layout



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